8.2.2 Detailed Design Procedure

8.2.2.1 Input Bulk Capacitance and Minimum Bulk Voltage

In an offline application, the input bulk capacitor (C_{BULK}) should be sized for the minimum input AC line voltage ($V_{IN(MIN)}$) and minimum voltage of the input bulk capacitor ($V_{BULK(MIN)}$). Due to the transition-mode operation, too low of $V_{BULK(MIN)}$ selection results in higher RMS current at $V_{IN(MIN)}$ and affects the full load efficiency, while too high of $V_{BULK(MIN)}$ enlarges the volume of the bulk capacitor. This equation does not account for the hold-up time requirement over line drop-outs.

$$C_{BULK(MIN)} = \frac{\frac{P_O}{\eta} \times [0.5 + \frac{1}{\pi} \times \arcsin(\frac{V_{BULK(MIN)}}{\sqrt{2} \times V_{IN(MIN)}})]}{(2 \times {V_{IN(MIN)}}^2 - {V_{BULK(MIN)}}^2) \times f_{LINE}} \quad (18)$$

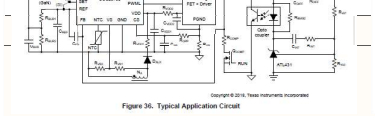
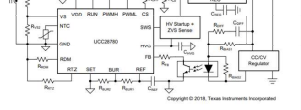
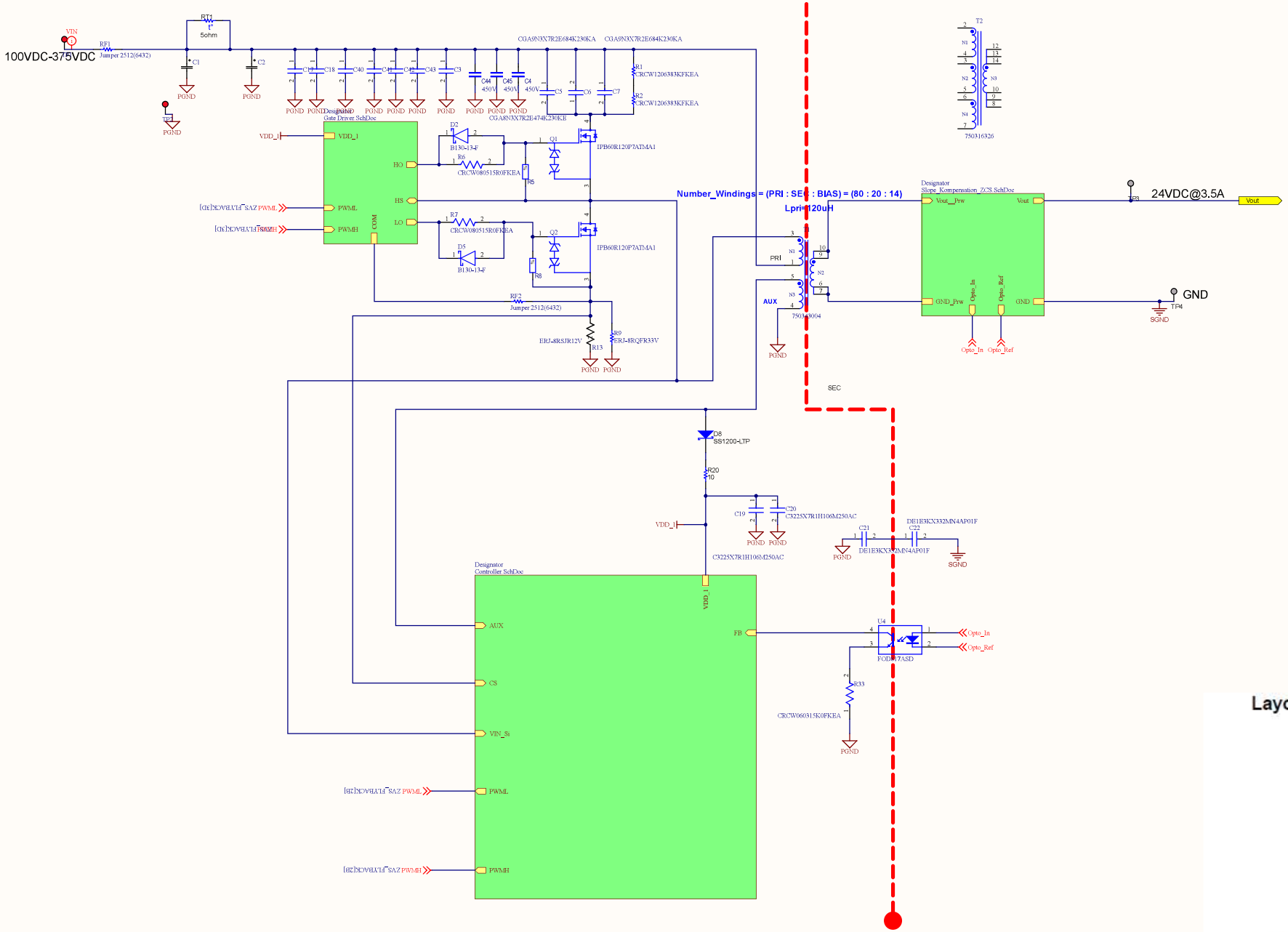
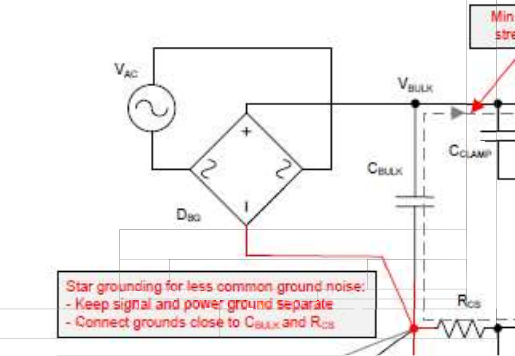


Figure 36. Typical Application Circuit





Layout Guidelines (continued)



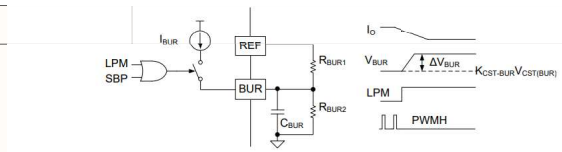
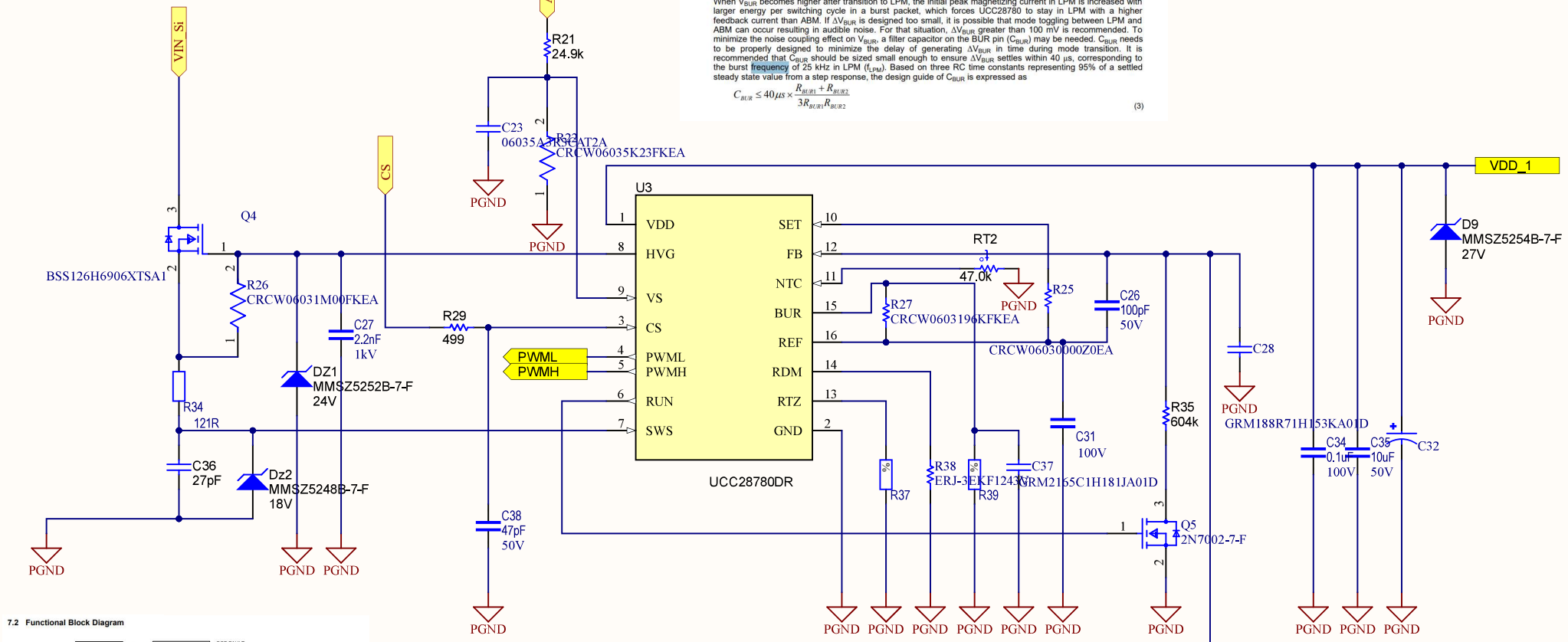


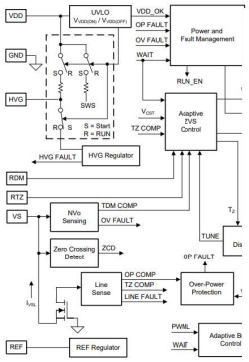
Figure 12. Hysteresis Voltage Generation on BUR Pin

When V_{BUR} becomes higher after transition to LPM, the initial peak magnetizing current in LPM is increased with larger energy per switching cycle in a burst packet, which forces UCC28780 to stay in LPM with a higher feedback current than ABM. If ΔV_{BUR} is designed too small, it is possible that mode toggling between LPM and ABM can occur resulting in audible noise. For that situation, ΔV_{BUR} greater than 100 mV is recommended. To minimize the noise coupling effect on V_{BUR}, a filter capacitor on the BUR pin (C_{BUR}) may be needed. C_{BUR} needs to be properly designed to minimize the delay of generating ΔV_{BUR} in time during mode transition. It is recommended that C_{BUR} should be sized small enough to ensure ΔV_{BUR} settles within 40 µs, corresponding to the burst frequency of 25 kHz in LPM (f_{LPM}). Based on three RC time constants representing 95% of a settled steady state value from a step response, the design guide of C_{BUR} is expressed as

$$C_{BUR} \le 40\mu s \times \frac{R_{BUR1} + R_{BUR2}}{3R_{BUR1}R_{BUR2}} \quad (3)$$



7.2 Functional Block Diagram



7.4.3 Control Law across Entire Load Range

UCC28780 contains four modes of operation summarized in Table 1. Starting from heavier load, the AAM mode forces PWML and PWMH into complementary switching with ZVS tuning enabled. ABM mode generates a group of PWML and PWMH pulses as a burst packet, and adjusts the burst off-time to regulate the output voltage. At the same time, the burst frequency variation is confined above 20kHz by adjusting the number of PWML and PWMH pulses per packet to mitigate audible noise and reduce burst output ripple. In LPM and SBP modes, PWMH and the ZVS tuning loop are disabled, so the converter operates in valley-switching.

Table 1. Functional Modes

	MODE	OPERATION	PWMH	ZVS
AAM	Adaptive Amplitude Modulation	ACF operation with PWML and PWMH in complementary switching	Enabled	Yes
ABM	Adaptive Burst Mode	Variable f_{BUR} > 20 kHz, ACF operation in complementary switching	Enabled	Yes
LPM	Low Power Mode	Fix f_{BUR} ≈ 25 kHz, valley-switching	Disabled	No
SBP	StandBy Power	Variable f_{BUR} < 25 kHz, valley-switching	Disabled	No

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8.2 Typical Application

The circuit in Figure 44 shows a reference design example with UCC27712 driving a typical half-bridge configuration which could be used in several common power converter topologies such as synchronous buck, synchronous boost, half-bridge/full bridge isolated topologies, and motor drive applications.

For more information, please refer to Figure 44.

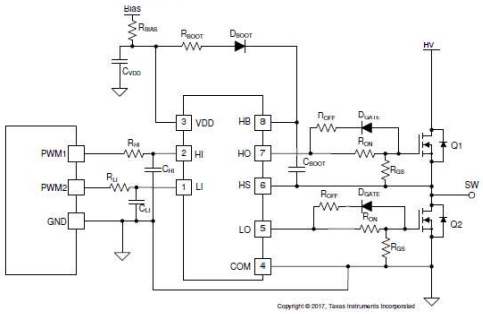


Figure 44. Typical Application Schematic

Diode Voltage Drop:	0.05	V
Inductor Current Ripple:	50	%
Maximum Duty Cycle:	70	%
Magnetization Current:	40	%

Recommended Values

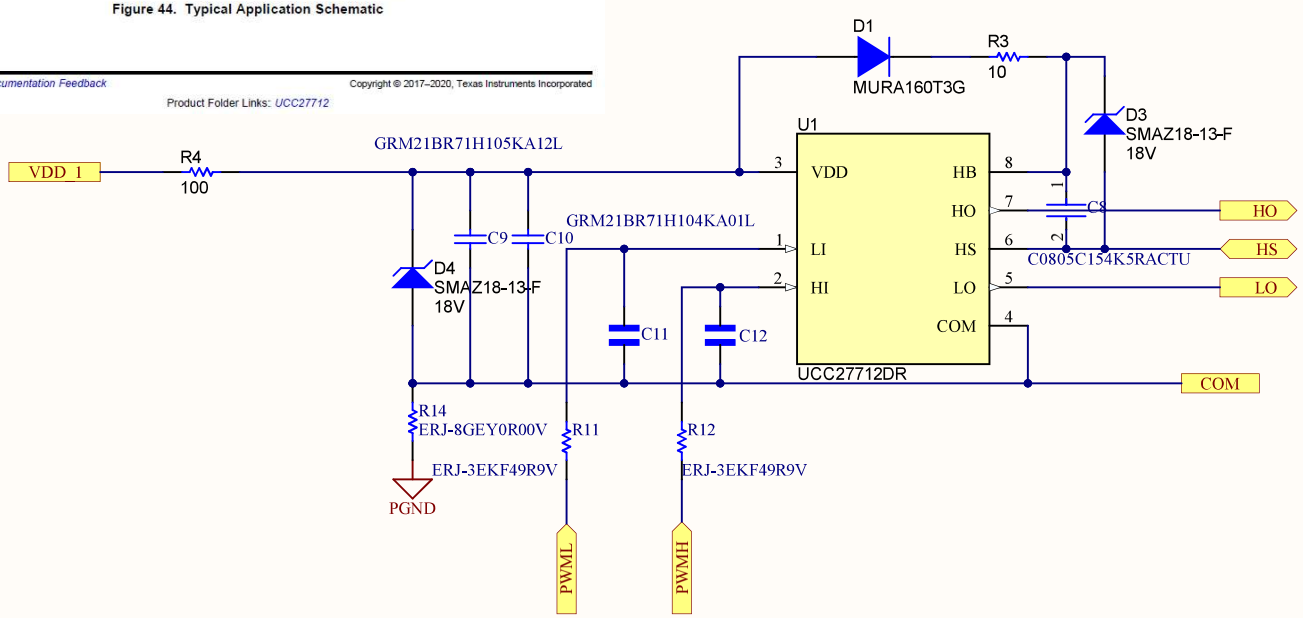
Turns Ratio:	2.91	: 1
Transformer Inductance:	145.53	µH
Inductance:	11.34	µH

Calculated Values at Input Voltage:

Period:	1.00	µs
Duty Cycle:	48.10	%
On-Ti...	0.48	µs
Off-Time:	0.52	µs
Zero-Ti...	0.00	µs
Input Power:		
Output Pow...		
Rectifier Diode		
Freewheeling		

Choose Values

Turns Ratio:	2	: 1
Transformer Inductance:	100	µH
Inductance:	12.2	µH



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r components C3 and R3 to get the best performance when using the

knowledge of the Flyback transformer secondary leakage inductance
nant ring frequency (fr) in circuit. It is recommended that the SR is not
ocess. It is also recommended to do this test at partial load to avoid
diode because the conduction loss is much higher. TP3 should be
o ensure FET Q1 is turned off while setting up the snubber.

then needs to be calculated based on the following equation. Please
nding leakage inductance of 3.8 µH and a ring frequency of 2 MHz, the
example.

$$\frac{1}{(2MHz)^2 \times 3.8\mu H} = 1.7nF \quad (3)$$

the snubber resistor R3 can be set to critically dampen the ringing on
Q of the circuit equal to 1.

Ω (4)

e snubber resistor is applied to the aux winding during the switching
ober capacitor C3 with the following equation based on the Flyback
a Flyback converter switching at 85 kHz in the example would require a

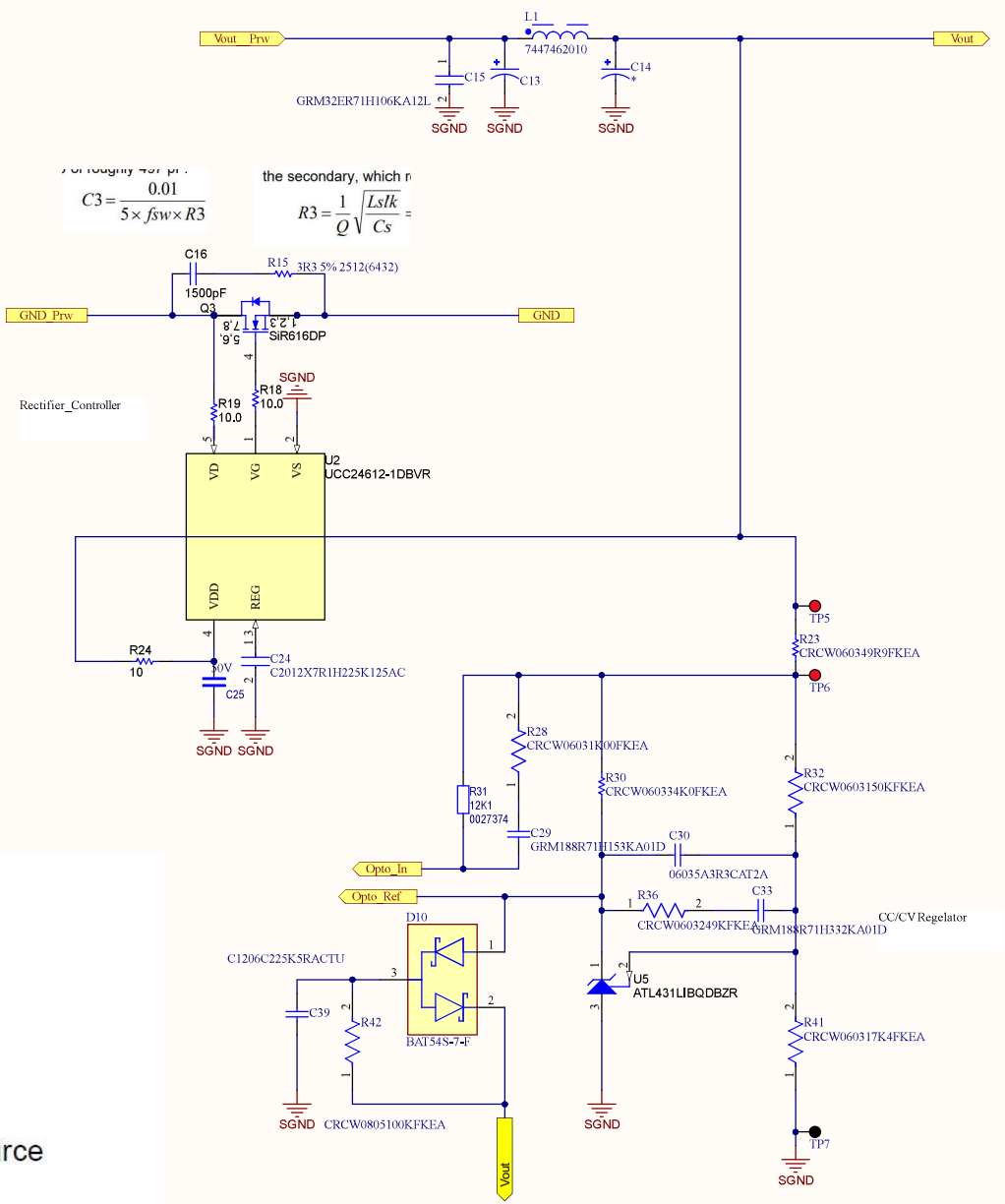
$\Omega \approx 497\,pF$ (5)

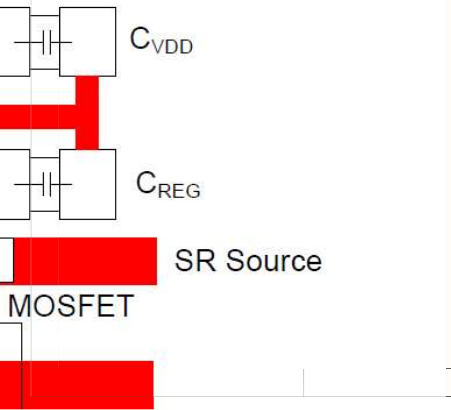
and C3 are just starting points and should be adjusted based on
ficiency requirements. More snubber design information can be found
pplication".

$$C3 = \frac{0.01}{5 \times fsw \times R3}$$

the secondary, which r

$$R3 = \frac{1}{Q}\sqrt{\frac{Lslk}{Cs}} =$$





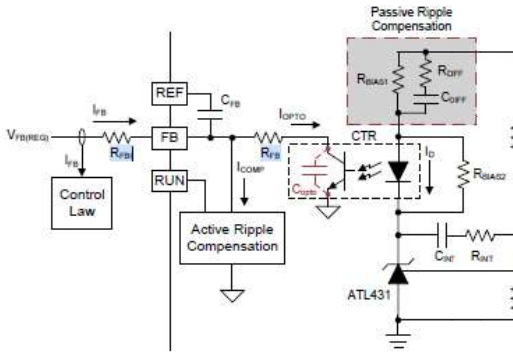


Figure 40. Compensation Network, $H_v(s)$

In order to minimize the phase-delay of I_{FB}, the transfer function from I_{FB} to V_O guides
the secondary-side passive ripple compensation network in Figure 40. In the primar
poles at ω_{FB} and ω_{OPTO} introduce phase-delay on I_{FB}. ω_{FB} pole is formed by the exter
the parallel resistance of the internal R_{FBI} and the external current-limiting resistor (R_F
the parasitic capacitance of the optocoupler output (C_{OPTO}) and the series resistance
100 pF, R_{FBI} = 8 KΩ, and R_{FB} = 20 KΩ, the delay effect of ω_{FB} pole located at 278 k
ω_{OPTO} pole is located less than 10 kHz, and introduces large phase delay in the inte
since C_{OPTO} is in a few nF range contributed by the Miller effect of the collector-to-base
the optocoupler output. Therefore, an RC network (R_{DIFF} and C_{DIFF}) in parallel with R_B
the phase-delay of the optocoupler, which introduces an extra pole/zero pair located a
The basic design guide is to place the ω_{Z1} zero close to the ω_{OPTO} pole, and to place
f_{BUR}.

$$\frac{I_{FB}(s)}{V_O(s)} = \frac{CTR}{R_{BIAS1}} \frac{1+(s/\omega_{Z0})}{(s/\omega_{Z0})} \frac{1}{1+(s/\omega_{P1})} \frac{1+(s/\omega_{Z1})}{1+(s/\omega_{OPTO})} \frac{1}{1+(s/\omega_{FB})}$$

$$\omega_{Z0} = \frac{1}{(R_{Vo1} + R_{INT})C_{INT}}$$

$$\omega_{Z1} = \frac{1}{(R_{DIFF} + R_{BIAS1})C_{DIFF}}$$

$$\omega_{P1} = \frac{1}{R_{DIFF}C_{DIFF}}$$

$$\omega_{OPTO} = \frac{1}{(R_{FB} + R_{FBI})C_{OPTO}}$$

$$\omega_{FB} = \frac{1}{(R_{FBI} // R_{FB})C_{FB}}$$

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