106-2 Digital System Design Homework 2

b04901099 電機三 吳書帆

1.(3)

首先我們先將testbench裡的x假設為1，y假設為255，並開始做運算，得到以下結果：

a. RT-Level

```
PASS --- 0000 boolean add
PASS --- 0001 boolean sub
PASS --- 0010 boolean and
PASS --- 0011 boolean or
PASS --- 0100 boolean not
PASS --- 0101 boolean xor
PASS --- 0110 boolean nor
PASS --- 0111 boolean Shift left logical variable
PASS --- 1000 boolean Shift right logical variable
PASS --- 1001 boolean Shift right arithmetic
PASS --- 1010 boolean Rotate left
PASS --- 1011 boolean Rotate right
PASS --- 1100 boolean Equal
==========================================

=======  Congratulation! You Pass!  ========

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Simulation complete via $finish(1) at time 32 NS + 0
./alu_rtl_tb2.v:145      $finish;
```

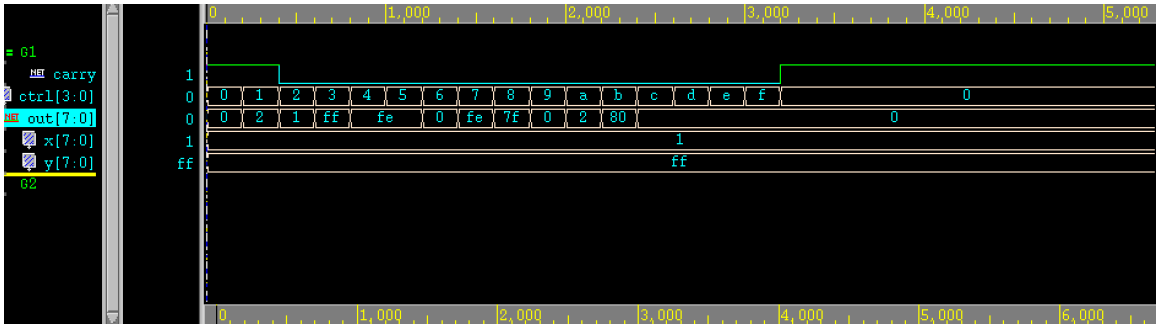

從測資的結果及波形圖可看出利用RT-Level設計的ALU是正常運作的。

b. Behavior-Level

```
PASS --- 0000 boolean add
PASS --- 0001 boolean sub
PASS --- 0010 boolean and
PASS --- 0011 boolean or
PASS --- 0100 boolean not
PASS --- 0101 boolean xor
PASS --- 0110 boolean nor
PASS --- 0111 boolean Shift left logical variable
PASS --- 1000 boolean Shift right logical variable
PASS --- 1001 boolean Shift right arithmetic
PASS --- 1010 boolean Rotate left
PASS --- 1011 boolean Rotate right
PASS --- 1100 boolean Equal
========================================

======  Congratulation! You Pass!  =======

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Simulation complete via $finish(1) at time 32 NS + 0
./alu_tb2.v:145     $finish;
```

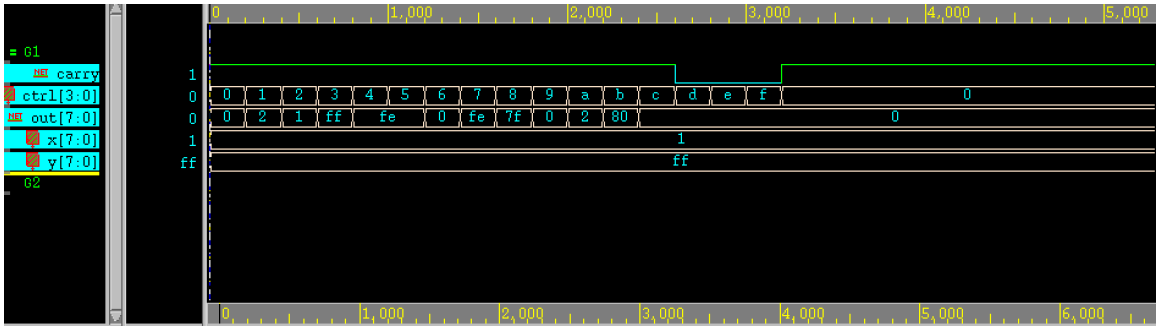

從測資及波形圖來看可得到與前面 RT-Level 一致的結果，唯一有差別的地方是 carry 的部分，由於在設計 RT-Level 時的設定為 carry 只有在進行加或減時會受到 ALU 影響，其餘預設值皆為 0，但在 Behavior-level 時第三筆到第十二筆的 carry 會受到第二筆的 carry 影響，直到最後第十三筆進來才會掉回預設值 0，但這都不影響我們要的結果，因為除了第一筆及第二筆其餘的 carry 皆為 don't care。