2020 Digital IC Design Homework 5: Sobel

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Simulation Result

Functional simulation	A	Gate-level simulation	A	Gate-level simulation time	27525308645 ps 27525308.645 ns

(your pre-sim result)

```
# --------------------- S U M M A R Y -----------------
#
# Congratulations! Sobel X data have been generated successfully! The result is PASS!!
#
# Congratulations! Sobel Y data have been generated successfully! The result is PASS!!
#
# Congratulations! Sobel combine data have been generated successfully! The result is PASS!!
#
# -------------------------------------------------------
#
# ** Note: $finish    : C:/Users/frank/Desktop/university/IC/hw5/testfixture.v(198)
#    Time: 27525300 ns  Iteration: 0  Instance: /testfixture
```

(your post-sim result)

```
# --------------------- S U M M A R Y -----------------
#
# Congratulations! Sobel X data have been generated successfully! The result is PASS!!
#
# Congratulations! Sobel Y data have been generated successfully! The result is PASS!!
#
# Congratulations! Sobel combine data have been generated successfully! The result is PASS!!
#
# -------------------------------------------------------
#
# ** Note: $finish    : C:/Users/frank/Desktop/university/IC/hw5/testfixture.v(198)
#    Time: 27525308645 ps  Iteration: 0  Instance: /testfixture
```

Synthesis Result

Total logic elements	883 / 68,416 (1 %)
Total memory bit	0 / 1,152,000 (0 %)
Embedded multiplier 9-bit element	0 / 300 (0 %)

(your flow summary)

Flow Status	Successful - Thu Jun 04 20:11:30 2020
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	SOBEL
Top-level Entity Name	SOBEL
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	N/A
Total logic elements	883 / 68,416 (1 %)
Total combinational functions	879 / 68,416 (1 %)
Dedicated logic registers	189 / 68,416 (< 1 %)
Total registers	189
Total pins	81 / 622 (13 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design
我延續 HW4 的 coding 方式，使用多個 state 來控制程式的流程。 我並沒有儲存 img 的 data 在 SOBEL 裡，而是讀入一個 pixel 和其周邊的八個 pixel 後就直接計算並存入 testbench 的 mem 中 四捨五入我使用 (n+1)/2 的方法實現 這是我使用的 cycle `define CYCLE 30.0 `define End_CYCLE 100000000 這次作業的 post-sim 真的有點久

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*