2020 Digital IC Design Homework 2: Divider

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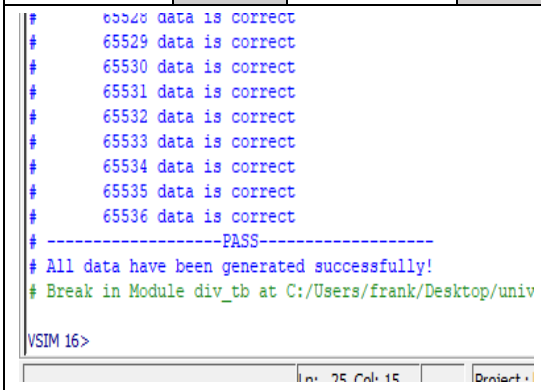
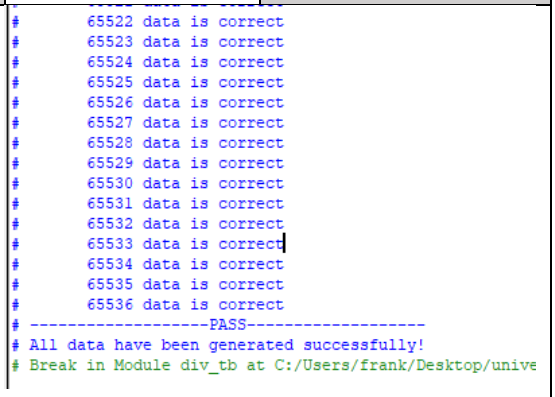
Simulation Result

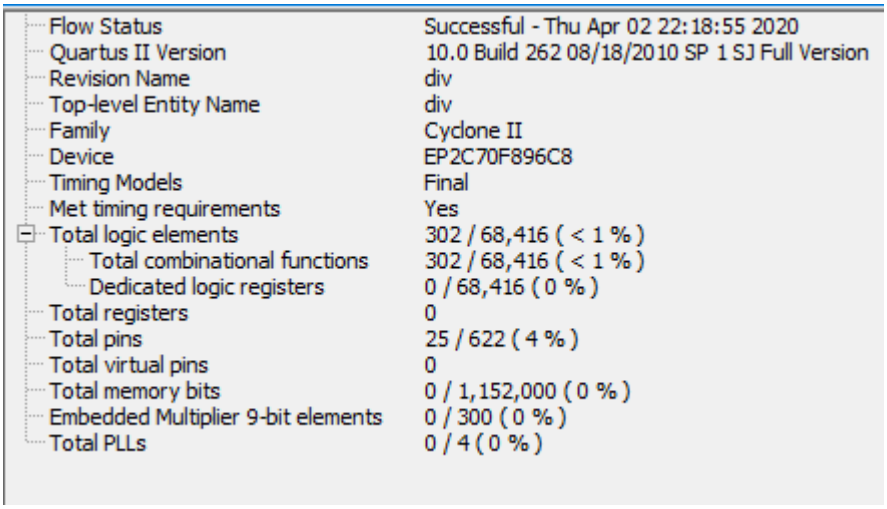
Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	6553610ns





Synthesis Result

Total logic elements	302 / 68,416 (< 1 %)
Total memory bit	0 / 1,152,000 (0 %)
Embedded multiplier 9-bit element	0 / 300 (0 %)



Description of your design

我將被除數前面加八個零，除數後面加八個零，每個 loop 判斷被除數是否比除數大，如果是，將被除數減掉除數，out[0]+1，並且將除數右移，out[0]左移，依此方式 loop 結束後，便可以得到正確的 out 解答。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*