2020 Digital IC Design Homework 3: Approximate Average

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	240480

```
# ----------------------------------------------
#
# ----------------------------------------------
#
# All data have been generated successfully!
#
# -------------------PASS-------------------
#
# ----------------------------------------------
#
# ** Note: $finish    : C:/Users/frank/Desktop/univer
#    Time: 100200 ns  Iteration: 2  Instance: /test
```

```
# ----------------------------------------------
#
# ----------------------------------------------
#
# All data have been generated successfully!
#
# -------------------PASS-------------------
#
# ----------------------------------------------
#
# ** Note: $finish    : C:/Users/frank/Desktop/unive
#    Time: 240480 ns  Iteration: 2  Instance: /test
```

Synthesis Result

Total logic elements	2,246 / 68,416 (3 %)
Total memory bit	0 / 1,152,000 (0 %)
Embedded multiplier 9-bit element	0 / 300 (0 %)

Flow Summary

Flow Status	Successful - Thu Apr 23 20:02:31 2020
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	CS
Top-level Entity Name	CS
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	Yes
Total logic elements	2,246 / 68,416 (3 %)
Total combinational functions	2,246 / 68,416 (3 %)
Dedicated logic registers	79 / 68,416 (< 1 %)
Total registers	79
Total pins	20 / 622 (3 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

我使用 reg 儲存之前八次的輸入 X，加上本次輸入的 X，計算出 Y 值，Y 值的計算我放在 combination 的部分，另外存每筆輸入 X 與平均的差值。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*