2020 Digital IC Design Homework 4: RC4 Encrypt

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Simulation Result

Functional simulation	Pass Pass	Gate-level simulation	Pass Pass	Gate-level simulation time	371032547 ps 190104047 ps

(your pre-sim result)

```
# ---------------------------------------------------
#
#  ---------------- Cipher is correct ! ----------------
#  ----------------- Plain is correct ! -----------------
# ---------------------------------------------------------
#
# --------------------- T B 1 - S U M M A R Y -----------------
#
# Congratulations! Cipher data have been generated successfully! The result is PASS!!
#
# Congratulations! Plain data have been generated successfully! The result is PASS!!
#
# ** Note: $finish    : C:/Users/frank/Desktop/university/IC/HW4/testfixture.v(244)
#    Time: 371023500 ps  Iteration: 2  Instance: /testfixture

# ---------------------------------------------------
#
#  ---------------- Cipher is correct ! ----------------
#  ----------------- Plain is correct ! -----------------
# ---------------------------------------------------------
#
# --------------------- T B 2 - S U M M A R Y -----------------
#
# Congratulations! Cipher data have been generated successfully! The result is PASS!!
#
# Congratulations! Plain data have been generated successfully! The result is PASS!!
#
# ** Note: $finish    : C:/Users/frank/Desktop/university/IC/HW4/testfixture2.v(244)
#    Time: 190095 ns  Iteration: 2  Instance: /testfixture2
```

(your post-sim result)

```
# ------------------------------------------------------
#
#  ---------------- Cipher is correct ! ----------------
#  ----------------- Plain is correct ! -----------------
# ------------------------------------------------------------
#
# --------------------- T B 1 - S U M M A R Y -----------------
#
# Congratulations! Cipher data have been generated successfully! The result is PASS!
#
# Congratulations! Plain data have been generated successfully! The result is PASS!!
#
# ** Note: $finish    : C:/Users/frank/Desktop/university/IC/HW4/testfixture.v(244)
#    Time: 371032547 ps  Iteration: 0  Instance: /testfixture
# 1

# ------------------------------------------------------
#
#  ---------------- Cipher is correct ! ----------------
#  ----------------- Plain is correct ! -----------------
# ------------------------------------------------------------
#
# --------------------- T B 2 - S U M M A R Y -----------------
#
# Congratulations! Cipher data have been generated successfully! The result is PASS!
#
# Congratulations! Plain data have been generated successfully! The result is PASS!!
#
# ** Note: $finish    : C:/Users/frank/Desktop/university/IC/HW4/testfixture2.v(244)
#    Time: 190104047 ps  Iteration: 0  Instance: /testfixture2
```

Synthesis Result

Total logic elements	3,214 / 68,416 (5 %)
Total memory bit	192 / 1,152,000 (< 1 %)
Embedded multiplier 9-bit element	0 / 300 (0 %)

Flow Status	Successful - Sun May 17 22:07:10 2020
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	RC4
Top-level Entity Name	RC4
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	Yes
Total logic elements	3,214 / 68,416 (5 %)
Total combinational functions	3,204 / 68,416 (5 %)
Dedicated logic registers	679 / 68,416 (< 1 %)
Total registers	679
Total pins	50 / 622 (8 %)
Total virtual pins	0
Total memory bits	192 / 1,152,000 (< 1 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

我在讀入 plain_in 和 cipher_in 時，沒有將全部的明文(密文)一次讀入
而是在每接到一個輸入時就加密(解密)它，並將它輸出之後才接收下一個輸入。
附上我 testbench 使用的參數
Testfixture1

```
`define CYCLE      31.0
`define End_CYCLE  100000
```

Testfixture2

```
`define CYCLE      30.0
`define End_CYCLE  100000
```

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*