2020 Digital IC Design Homework 1: 4-bit binary adder-subtractor

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	25700ns

```
#        495 data is correct
#        496 data is correct
#        497 data is correct
#        498 data is correct
#        499 data is correct
#        500 data is correct
#        501 data is correct
#        502 data is correct
#        503 data is correct
#        504 data is correct
#        505 data is correct
#        506 data is correct
#        507 data is correct
#        508 data is correct
#        509 data is correct
#        510 data is correct
#        511 data is correct
#        512 data is correct
# ------------------PASS--------------------
# All data have been generated successfully!
# ** Note: $finish    : C:/Users/frank/Desktop/university/IC/HW1/AS_tb.v(63)
#    Time: 25700 ns  Iteration: 0  Instance: /AS_tb
# 1
# Break in Module AS_tb at C:/Users/frank/Desktop/university/IC/HW1/AS_tb.v line 6
```

```
#        502 data is correct
#        503 data is correct
#        504 data is correct
#        505 data is correct
#        506 data is correct
#        507 data is correct
#        508 data is correct
#        509 data is correct
#        510 data is correct
#        511 data is correct
#        512 data is correct
# ------------------PASS--------------------
# All data have been generated successfully!
# ** Note: $finish    : C:/Users/frank/Desktop/university/IC/HW1/AS_tb.v(63)
#    Time: 25700 ns  Iteration: 0  Instance: /AS_tb
# 1
# Break in Module AS_tb at C:/Users/frank/Desktop/university/IC/HW1/AS_tb.v line 63
```

Synthesis Result

Total logic elements	8 / 68,416 (< 1 %)
Total memory bit	0 / 1,152,000 (0 %)
Embedded multiplier 9-bit element	0 / 300 (0 %)

Flow Summary

Flow Status	Successful - Thu Apr 02 15:52:25 2020
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	AS
Top-level Entity Name	AS
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	Yes
Total logic elements	8 / 68,416 (< 1 %)
Total combinational functions	8 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	14 / 622 (2 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

這次作業中，我將 full adder 獨立出來成一個 module，名叫 AS，在測試 4-bit binary adder-subtractor 時就可以直接呼叫，這可以讓 code 可讀性高些，其餘的部分就是照著作業上 block 的圖加上對應的邏輯閘。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*