

2020 Digital IC Design Homework 2: Divider

NAME	方嘉祥				
Student ID	F74056166				
Simulation Result					
Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	6553610ns
<pre># 65528 data is correct # 65529 data is correct # 65530 data is correct # 65531 data is correct # 65532 data is correct # 65533 data is correct # 65534 data is correct # 65535 data is correct # 65536 data is correct # -----PASS----- # All data have been generated successfully! # Break in Module div_tb at C:/Users/frank/Desktop/univ VSIM 16></pre>			<pre>65522 data is correct 65523 data is correct 65524 data is correct 65525 data is correct 65526 data is correct 65527 data is correct 65528 data is correct 65529 data is correct 65530 data is correct 65531 data is correct 65532 data is correct 65533 data is correct 65534 data is correct 65535 data is correct 65536 data is correct # -----PASS----- # All data have been generated successfully! # Break in Module div_tb at C:/Users/frank/Desktop/univ</pre>		
Synthesis Result					
Total logic elements			302 / 68,416 (< 1 %)		
Total memory bit			0 / 1,152,000 (0 %)		
Embedded multiplier 9-bit element			0 / 300 (0 %)		
<div><div><div>Flow Status</div><div>Quartus II Version</div><div>Revision Name</div><div>Top-level Entity Name</div><div>Family</div><div>Device</div><div>Timing Models</div><div>Met timing requirements</div><div><div>Total logic elements</div><div>Total combinational functions</div><div>Dedicated logic registers</div></div><div>Total registers</div><div>Total pins</div><div>Total virtual pins</div><div>Total memory bits</div><div>Embedded Multiplier 9-bit elements</div><div>Total PLLs</div></div><div>Successful - Thu Apr 02 22:18:55 2020 10.0 Build 262 08/18/2010 SP 1 SJ Full Version div div Cyclone II EP2C70F896C8 Final Yes 302 / 68,416 (< 1 %) 302 / 68,416 (< 1 %) 0 / 68,416 (0 %) 0 25 / 622 (4 %) 0 0 / 1,152,000 (0 %) 0 / 300 (0 %) 0 / 4 (0 %)</div></div>					
Description of your design					
我將被除數前面加八個零，除數後面加八個零，每個 loop 判斷被除數是否比除數大，如果是，將被除數減掉除數，out[0]+1，並且將除數右移，out[0]左移，依此方式 loop 結束後，便可以得到正確的 out 解答。					

$$\text{Scoring} = (\text{Total logic elements} + \text{total memory bit} + 9 * \text{embedded multiplier 9-bit element}) \times (\text{gate-level simulation time in } \underline{\text{ns}})$$