```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 04/25/2021 09:01:51 PM
// Design Name:
// Module Name: countUD16L
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module counterUD16L(
    input clk,
    input Up,
    input Dw,
    input [15:0] D,
    output [15:0] Q,
    output UTC,
    output DTC,
    input LD
    );
    wire UTC0, UTC1, UTC2, UTC3;
    wire DTC0, DTC1, DTC2, DTC3;
    //wire [15:0] R;

    //m2_1x4 sel4(.in0(Q[3:0]), .in1(D[3:0]), .sel(LD), .o(R[3:0]));
    //m2_1x4 sel8(.in0(Q[7:4]), .in1(D[7:4]), .sel(LD), .o(R[7:4]));
    //m2_1x4 sel12(.in0(Q[11:8]), .in1(D[11:8]), .sel(LD), .o(R[11:8]));
    //m2_1x4 sel16(.in0(Q[15:12]), .in1(D[15:12]), .sel(LD), .o(R[15:12]));

    countUD4L count4(.clk(clk), .Up(Up & ~Dw), .Dw(Dw & ~Up), .LD(LD), .Din(D[3:0]),
.Q(Q[3:0]), .UTC(UTC0), .DTC(DTC0));
    countUD4L count8(.clk(clk), .Up(Up & ~Dw & UTC0), .Dw(Dw & ~Up & DTC0), .LD(LD),
.Din(D[7:4]), .Q(Q[7:4]), .UTC(UTC1), .DTC(DTC1));
    countUD4L count12(.clk(clk), .Up(Up & ~Dw & UTC1 & UTC0), .Dw(Dw & ~Up & DTC1 &
```

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DTC0), .LD(LD), .Din(D[11:8]), .Q(Q[11:8]), .UTC(UTC2), .DTC(DTC2));
    countUD4L count16(.clk(clk), .Up(Up & ~Dw & UTC2 & UTC1 & UTC0), .Dw(Dw & ~Up &
DTC2 & DTC1 & DTC0), .LD(LD), .Din(D[15:12]), .Q(Q[15:12]), .UTC(UTC3), .DTC(DTC3));

    assign UTC = UTC0 & UTC1 & UTC2 & UTC3;
    assign DTC = DTC0 & DTC1 & DTC2 & DTC3;

endmodule
```