```
`timescale 1ns / 1ps
// Company:
// Engineer:
// Create Date: 05/09/2021 11:55:16 PM
// Design Name:
// Module Name: lab5 state machine
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
module lab5 state machine(
   input btnU,
   input TimeUp,
   input Anow,
   input Bnow,
   input clk,
   output LoadTime,
   output RunTime,
   output IncA,
   output IncB,
   output ShowScore
   );
   wire [3:0] Q;
   wire [3:0] D;
   //assign D[0] = (Q[0] & ~btnU) | (Q[2] & (Anow | Bnow)) | (Q[3] & (Anow | Bnow));
   //assign D[1] = (Q[0] \& btnU) | (Q[1] \& btnU);
   //assign D[2] = (Q[1] & ~btnU) | (Q[2] & ~TimeUp) | (Q[2] & (~Anow & ~Bnow));
   //assign D[3] = (Q[2] & TimeUp) | (Q[3] & (~Anow & ~Bnow));
   lab5 one hot one hot encoding (.Q(Q[3:0]), .A(Anow), .B(Bnow), .Up(btnU),
.Time(TimeUp), .D(D[3:0]));
   FDRE #(.INIT(1'b1) ) Q0 (.C(clk), .CE(1'b1), .D(D[0]), .Q(Q[0]));
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FDRE #(.INIT(1'b0)) Q1 (.C(clk), .CE(1'b1), .D(D[1]), .Q(Q[1]));
    FDRE #(.INIT(1'b0)) Q2 (.C(clk), .CE(1'b1), .D(D[2]), .Q(Q[2]));
    FDRE #(.INIT(1'b0)) Q3 (.C(clk), .CE(1'b1), .D(D[3]), .Q(Q[3]));
    //FDRE #(.INIT(1'b0) ) Load (.C(clk), .CE(1'b1), .D(Q[1] & ~Q[0] & ~Q[2] &
~Q[3]), .Q(LoadTime));
    //FDRE #(.INIT(1'b0) ) Run (.C(clk), .CE(1'b1), .D(Q[2] & ~Q[0] & ~Q[1] &
\simQ[3]), .Q(RunTime));
    //FDRE #(.INIT(1'b0) ) incA (.C(clk), .CE(1'b1), .D((Q[2] & ~Q[3] & Bnow &
\sim \text{Anow}) | (Q[3] & \sim \text{Q}[2] & Anow)), .Q(IncA));
    //FDRE #(.INIT(1'b0) ) incB (.C(clk), .CE(1'b1), .D((Q[2] & ~Q[3] & Anow &
\sim Bnow) \mid (Q[3] \& \sim Q[2] \& Bnow)), .Q(IncB));
    //FDRE \#(.INIT(1'b0) ) score (.C(clk), .CE(1'b1), .D(Q[0] & ~Q[1] & ~Q[2] &
\simQ[3]), .Q(ShowScore));
    assign LoadTime = Q[1] & \sim Q[0] & \sim Q[2] & \sim Q[3];
    assign RunTime = Q[2] \& \sim Q[0] \& \sim Q[1] \& \sim Q[3];
    assign IncA = (Q[2] \& \neg Q[3] \& Bnow \& \neg Anow) | (Q[3] \& \neg Q[2] \& Anow);
    assign IncB = (Q[2] \& \neg Q[3] \& Anow \& \neg Bnow) | (Q[3] \& \neg Q[2] \& Bnow);
    assign ShowScore = Q[0] \& \sim Q[1] \& \sim Q[2] \& \sim Q[3];
```

endmodule