```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 04/26/2021 10:10:45 PM
// Design Name:
// Module Name: lab4_top
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module lab4_top(
    input clkin,
    input btnR,
    input btnU,
    input btnD,
    input btnC,
    input btnL,
    input [15:0] sw,
    output [6:0] seg,
    output dp,
    output [3:0] an,
    output [15:0] led
    );
    wire Up, Dw, LD, UTC, DTC, digsel, clk;
    wire [15:0] Q;
    wire [3:0] sel;
    wire [3:0] H;
    wire UpQ, UpEdge;
    wire [3:0] an_dummy;

    lab4_clks slowit (.clkin(clkin), .greset(btnR), .clk(clk), .digsel(digsel));
```

```
    edge_detector UpDetector (.clk(clk), .in(btnU), .out(UpEdge));
    //continuous_blocker UpBlocker (.clk(clk), .C(btnC), .Q(Q), .Up(UpQ));
    //assign UpQ = btnC & clk & (~(&Q[15:2] & ((Q[1] & Q[0]) | (Q[1] & ~Q[0]) |
(~Q[1] & Q[0]) | (~Q[1] & ~Q[0]))));
    //continuous_blocker ContinuousDetector (.clk(clk), .C(btnC), .in(clk & (~(&Q[15:
    //& ~((~Q[2] & ~Q[1] & ~Q[0]) | (~Q[2] & ~Q[1] & Q[0]) | (~Q[2] & Q[1] &
~Q[0])))))), .out(UpQ));
    assign Up = UpEdge | (btnC & ~&Q[15:2]);

    edge_detector Down (.clk(clk), .in(btnD), .out(Dw));


    counterUD16L count16 (.clk(clk), .Up(Up), .Dw(Dw), .D(sw), .Q(Q), .UTC(UTC),
.DTC(DTC), .LD(btnL));


    ring_counter ring (.clk(clk), .adv(digsel), .sel(sel));
    ring_counter segments(.clk(clk), .adv(digsel), .sel(an_dummy));
    Selector selectdisp (.N(Q), .sel(sel), .H(H));
    hex7seg seven_seg_disp (.n(H), .e(1'b1), .seg(seg));


    assign dp = 1'b1;
    assign an[0] = ~an_dummy[0];
    assign an[1] = ~an_dummy[1];
    assign an[2] = ~an_dummy[2];
    assign an[3] = ~an_dummy[3];
    //Flip these if they function normally.
    assign led[0] = UTC;
    assign led[15] = DTC;
    assign led[14:1] = 1'b0;

endmodule
```