```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 04/26/2021 08:02:32 PM
// Design Name:
// Module Name: ring_counter
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module ring_counter(
    input clk,
    input adv,
    output [3:0] sel
    );
    //wire [3:0] A;

    //assign A[0] = (adv & ~sel[1] & ~sel[2] & ~sel[3]);
    //assign A[1] = (adv & ~sel[0] & ~sel[2] & ~sel[3]);
    //assign A[2] = (adv & ~sel[1] & ~sel[0] & ~sel[3]);
    //assign A[3] = (adv & ~sel[1] & ~sel[2] & ~sel[0]);

    FDRE #(.INIT(1'b1) ) sel0 (.C(clk), .R(1'b0), .CE(adv), .D(sel[3]), .Q(sel[0]));
    FDRE #(.INIT(1'b0) ) sel1 (.C(clk), .CE(adv), .D(sel[0]), .Q(sel[1]));
    FDRE #(.INIT(1'b0) ) sel2 (.C(clk), .CE(adv), .D(sel[1]), .Q(sel[2]));
    FDRE #(.INIT(1'b0) ) sel3 (.C(clk), .CE(adv), .D(sel[2]), .Q(sel[3]));
endmodule
```