```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 04/20/2021 01:36:19 PM
// Design Name:
// Module Name: lab3_top
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module lab3_top(
    input [15:0] sw,
    input btnU,
    input btnR,
    input clkin,
    output [6:0] seg,
    output dp,
    output [3:0] an
    );
    wire [7:0] summation;
    wire [6:0] C_display;
    wire [6:0] B_display;
    //wire B_enable = 1'b1;
    //wire C_enable = 1'b1;
    wire dummy;
    wire overflow_dummy;
    wire dig_sel;
    //wire [7:0] segbus;

    lab3_digsel digsel (.clkin(clkin), .greset(btnR), .digsel(dig_sel));

    AddSub8 topAdder (.A(sw[15:8]), .B(sw[7:0]), .sub(btnU), .S(summation),
.ovfl(overflow_dummy));
    hex7seg highDisp (.n(summation[7:4]), .e(1'b1), .seg(B_display));
```

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    hex7seg lowDisp (.n(summation[3:0]), .e(1'b1), .seg(C_display));
    m2_1x8 combination (.in0({1'b0, B_display}), .in1({1'b0, C_display}),
.sel(dig_sel), .o({dummy, seg}));

    //assign seg = ~segbus[6:0];
    assign an[0] = ~dig_sel;
    assign an[1] = dig_sel;
    assign an[2] = 1;
    assign an[3] = 1;
    assign dp = ~overflow_dummy;
endmodule
```