```
module m4_1e_testbench();
   reg input3;
   reg [3:0] input_bus;
   reg [1:0] input_bus2;
   wire output1;
   //wire [3:0] output_bus1;

   m4_1e   UUT   ( .in(input_bus), .sel(input_bus2), .e(input3),
                     .o(output1));

// below is the "stimuli," the values for the inputs
// be sure to select a range of inputs that will fully exercise your design

    initial
    begin

        //-------------  Current Time:  0ns
        //input1=1'b0;
        //input2=1'b0;
        input3=1'b1;
        input_bus = 4'b0000;
        input_bus2 = 2'b00;
        #100;  //This advances time by 100 units (ns in this case)
        // -------------  Current Time:  100ns
        input_bus = 4'b1100;
        input_bus2 = 2'b00;
        #100; // -------------  Current Time:  200ns
        input_bus2 = 2'b01;
        #100; // -------------  Current Time:  300ns
        input_bus2 = 2'b10;
        #100; // -------------  Current Time:  400ns
        input_bus2 = 2'b11;
        #100; // -------------  Current Time:  500ns
        input_bus = 4'b1111;
        input_bus2 = 2'b00;
        #100; // -------------  Current Time:  600ns
        input_bus2 = 2'b01;
        #100; // -------------  Current Time:  700ns
        input_bus2 = 2'b10;
        #100; // -------------  Current Time:  800ns
        input_bus2 = 2'b11;
        #100; // -------------  Current Time:  900ns
        input3=1'b0;
    end
endmodule
```