```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 05/10/2021 12:14:27 AM
// Design Name:
// Module Name: lab5_one_hot
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module lab5_one_hot(
    input [3:0] Q,
    input A,
    input B,
    input Up,
    input Time,
    output [3:0] D
    );

    assign D[0] = (Q[0] & ~Up) | (Q[2] & (A | B)) | (Q[3] & (A | B)) | (Q[0] & Up &
(A | B)) | (Q[1] & Up & (A | B));
    assign D[1] = (Q[0] & Up & ~A & ~B) | (Q[1] & Up & ~A & ~B);
    assign D[2] = (Q[1] & ~Up) | (Q[2] & ~Q[0] & (~A & ~B) & ~Time);
    assign D[3] = (Q[2] & Time) | (Q[3] & (~A & ~B));
endmodule
```