```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 05/10/2021 01:00:52 PM
// Design Name:
// Module Name: LFSR
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module LFSR(
    input clk,
    output [7:0] Q
    );
    wire [7:0] rnd;
    wire rndXor;
    assign rndXor = rnd[0] ^ rnd[5] ^ rnd[6] ^ rnd[7];

    FDRE #(.INIT(1'b1) ) rnd0 (.C(clk), .CE(1'b1), .D(rndXor), .Q(rnd[0]));
    FDRE #(.INIT(1'b0) ) rnd1 (.C(clk), .CE(1'b1), .D(rnd[0]), .Q(rnd[1]));
    FDRE #(.INIT(1'b0) ) rnd2 (.C(clk), .CE(1'b1), .D(rnd[1]), .Q(rnd[2]));
    FDRE #(.INIT(1'b0) ) rnd3 (.C(clk), .CE(1'b1), .D(rnd[2]), .Q(rnd[3]));
    FDRE #(.INIT(1'b0) ) rnd4 (.C(clk), .CE(1'b1), .D(rnd[3]), .Q(rnd[4]));
    FDRE #(.INIT(1'b0) ) rnd5 (.C(clk), .CE(1'b1), .D(rnd[4]), .Q(rnd[5]));
    FDRE #(.INIT(1'b0) ) rnd6 (.C(clk), .CE(1'b1), .D(rnd[5]), .Q(rnd[6]));
    FDRE #(.INIT(1'b0) ) rnd7 (.C(clk), .CE(1'b1), .D(rnd[6]), .Q(rnd[7]));

    assign Q[0] = rnd[0];
    assign Q[1] = rnd[1];
    assign Q[2] = rnd[2];
    assign Q[3] = rnd[3];
    assign Q[4] = rnd[4];
    assign Q[5] = rnd[5];
    assign Q[6] = 1'b0;
```

```
    assign Q[7] = 1'b0;
endmodule
```