```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer: Frank Isidore Gomez
//
// Create Date: 04/11/2021 02:52:58 PM
// Design Name:
// Module Name: Full_Adder
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module Full_Adder(
    input c_in,
    input a0,
    input a1,
    input a2,
    input b0,
    input b1,
    input b2,
    output s0,
    output s1,
    output s2,
    output s3
    );
    wire t0, t1;
    mini_adder p1 (.a(a0), .b(b0), .c(c_in), .s(s0), .c_out(t0)) ;
    mini_adder p2 (.a(a1), .b(b1), .c(t0), .s(s1), .c_out(t1)) ;
    mini_adder p3 (.a(a2), .b(b2), .c(t1), .s(s2), .c_out(s3)) ;
    //seven_segment sx (.n3(s3), .n2(s2), .n1(s1), .n0(s0));
endmodule
```