```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 04/18/2021 06:09:49 PM
// Design Name:
// Module Name: AddSub8
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module AddSub8(
    input [7:0] A,
    input [7:0] B,
    input sub,
    output [7:0] S,
    output ovfl
    );
    wire c0, c1, c2, c3, c4, c5, c6, c7;
    Full_Adder ones (.A(A[0]), .B(sub ^ B[0]), .c_in(sub), .s(S[0]), .c_out(c0));
    Full_Adder twos (.A(A[1]), .B(sub ^ B[1]), .c_in(c0), .s(S[1]), .c_out(c1));
    Full_Adder fours (.A(A[2]), .B(sub ^ B[2]), .c_in(c1), .s(S[2]), .c_out(c2));
    Full_Adder eights (.A(A[3]), .B(sub ^ B[3]), .c_in(c2), .s(S[3]), .c_out(c3));
    Full_Adder sixteens (.A(A[4]), .B(sub ^ B[4]), .c_in(c3), .s(S[4]), .c_out(c4));
    Full_Adder threetwos (.A(A[5]), .B(sub ^ B[5]), .c_in(c4), .s(S[5]), .c_out(c5));
    Full_Adder sixfours (.A(A[6]), .B(sub ^ B[6]), .c_in(c5), .s(S[6]), .c_out(c6));
    Full_Adder onetwoeights (.A(A[7]), .B(sub ^ B[7]), .c_in(c6), .s(S[7]),
.c_out(c7));
    assign ovfl = (c6 & ~A[7] & ~B[7] & ~c7) | (~c6 & A[7] & B[7]) | (~A[7] & A[6] &
B[7] & ~B[6]) | (~A[7] & B[7] & c6 & sub) | (A[7] & ~B[7] & ~c6 & sub);
    //The third case is to handle >=64 - (<-65).
    //Fourth case is for 64 - (-64).
    //Fifth case is for -128 - 8.
endmodule
```