```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 04/26/2021 11:54:00 AM
// Design Name:
// Module Name: countUD4L_testbench
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module countUD4L_testbench();
    reg Up = 1'b0;
    reg Dw = 1'b0;
    reg LD = 1'b0;
    wire [3:0] D = 4'b0000;
    //wire [3:0] C = 4'b0101;
    wire [3:0] Q;
    wire UTC;
    wire DTC;
    reg clkin;
    countUD4L UUT (.clk(clkin), .Up(Up), .Dw(Dw), .LD(LD), .Din(D), .Q(Q),
.UTC(UTC), .DTC(DTC));

    parameter PERIOD = 10;
    parameter real DUTY_CYCLE = 0.5;
    parameter OFFSET = 2;

    initial    // Clock process for clkin
    begin
        #OFFSET
          clkin = 1'b1;
        forever
        begin
            #(PERIOD-(PERIOD*DUTY_CYCLE)) clkin = ~clkin;
```

```
    end
end
initial
begin
 // add your stimuli here
 // to set signal foo to value 0 use
 // foo = 1'b0;
 // to set signal foo to value 1 use
 // foo = 1'b1;
 //always advance time my multiples of 100ns
 // to advance time by 100ns use the following line
  #1000;
  LD = 1'b1;
  #100;
  LD = 1'b0;
  #100;

  Up = 1'b1; //1
  #100;
  Up = 1'b1;
  #100;
  #100;
  #100;
  #100;
  #100;
  #100;
  #100;
  #100;
  #100;
  #100;
  #100;
  #100;
  #100;
  #100;
  #100;
  #100;
  #100;
  #100;
  #100;
  Up = 1'd0;
  #100;
  LD = 1'b1;
  #100; //0
  LD = 1'b0;
  Up = 1'b0;
  #100; //0
  Dw = 1'b1;
  #100;
  #100;
```

```
      #100;
      #100;
      #100;
      #100;
      #100;
      #100;
      Up = 1'b1;
      #100;
      #100;
      LD = 1'b1;
      #100;
      #100;
      Up = 1'b0;
      Dw = 1'b0;
    end
endmodule
```