```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer: Frank Gomez
//
// Create Date: 04/11/2021 06:16:41 PM
// Design Name:
// Module Name: lab2_top
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module lab2_top(
    input sw0,
    input sw1,
    input sw2,
    input sw3,
    input sw4,
    input sw5,
    input sw6,
    output CA,
    output CB,
    output CC,
    output CD,
    output CE,
    output CF,
    output CG,
    output AN0,
    output AN1,
    output AN2,
    output AN3,
    output DP
    );
    wire x0, x1, x2, x3;
    Full_Adder adder (.c_in(sw0), .a0(sw1), .a1(sw2), .a2(sw3), .b0(sw4), .b1(sw5),
.b2(sw6), .s0(x0), .s1(x1), .s2(x2), .s3(x3));
```

```
    seven_segment converter (.n3(x3), .n2(x2), .n1(x1), .n0(x0), .a(CA), .b(CB),
.c(CC), .d(CD), .e(CE), .f(CF), .g(CG));
    assign AN0 = 0;
    assign AN1 = 1;
    assign AN2 = 1;
    assign AN3 = 1;
    assign DP = 1;
endmodule
```