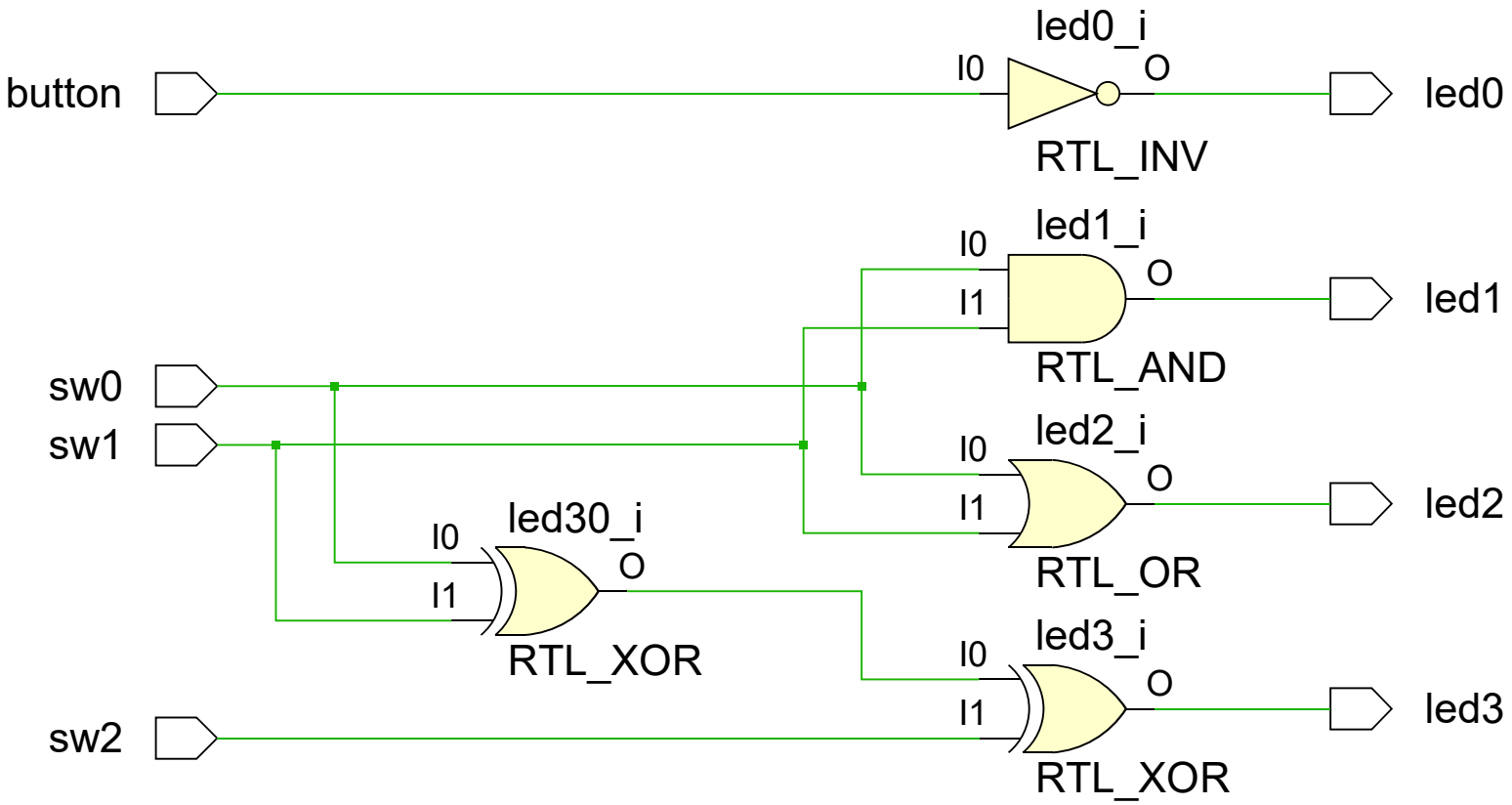
```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer: Frank Isidore Gomez
//
// Create Date: 04/02/2021 06:15:31 PM
// Design Name:
// Module Name: lab1
// Project Name: lab1
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module lab1(
    input sw0,
    input sw1,
    input sw2,
    input button,
    output led0,
    output led1,
    output led2,
    output led3
    );
    assign led0 = ~button ;
    assign led1 = sw0 & sw1 ;
    assign led2 = sw0 | sw1 ;
    assign led3 = sw0 ^ sw1 ^ sw2 ;
endmodule
```


led0_i
button
I0
O
led0
RTL_INV
led1_i
I0
I1
O
led1
RTL_AND
sw0
sw1
led2_i
I0
I1
O
led2
RTL_OR
led30_i
I0
I1
O
RTL_XOR
led3_i
I0
I1
O
led3
sw2
RTL_XOR