Coen 921c Final Exam Review Guide

The exam is comprehensive and 2 hours in length: 5pm-7pm. The following topics, while not exclusive or definitive, are some of the things that may likely be represented by questions on the upcoming final exam. These topics are not in any particular order or priority. During the exam, you may use

- a calculator (dedicated, ie. no cell phone apps)
- one notebook size sheet of handwritten notes if needed, but nothing else.
- Internet access is NOT allowed

You are required to show all work for problems. Even a correct answer, without showing how you arrived at it, may be marked off. Please attempt to make your solution legible and logical. If I cannot read or follow your solution, you will lose credit on the problem.

The exam will be done via a Zoom meeting, like both midterms. Please leave your zoom cameras ON during the 2 hrs of the final exam. When time is called, stop working, scan your answers into a pdf file, and email it to me. Please rename the scanned file you email me as: **YourLastname_YourFurstname_Final.pdf**

Related chapters from text: 1-3.10, 4-4.6, 5-5.5, 6-6.4, 7-7.4
Slides: up through the end of unit 8

Topics (again, not all inclusive)

1. You should be knowledgeable in the material from the early part of the course
    a. Number systems, arithmetic, conversions, 2's complement
    b. Boolean algebra and theorums
    c. Common gates and functioning (AND, OR, NOT, NAND, NOR, XOR, XNOR
    d. Cannonical Form: Minterms vs. Maxterms;.
2. Switching and Electrical Characteristics
    a. Propagation delay, electrical loading, open collector, Tri-state
3. VHDL: Entity and Architectural descriptions
4. Minimization: K-map and Quine McCluskey
    a. SOP, POS, implicants, Implicates
    b. How to use 5 or 6 variable K-maps
    c. XOR/XNOR Bridging
5. Designing with MSI devices
    a. Decoders, Multiplexors, etc.
        i. Implementing arbitrary Boolean functions with Decoders and/or MUXes.
6. LSI Programmable devices
    a. ROMs (etc.); PLAs & PALs in particular
7. Sequential logic
    a. Difference between Combinational and Sequential
    b. State diagrams, State tables; Mealy and Moore FSSMs; Sequence recognizers
        i. Sequence recognizers
        ii. Construct stat diagrams and tables, especially for Moore machines

c. Latches and Flip Flops, clocked and un-clocked circuits
    i. Setup and hold times; Clocking the various devices
    ii. Async vs Sync inputs such as preset and clear
d. Registers, Counters, Shift Registers.
    i. Configuring varying count moduli with MSI counters