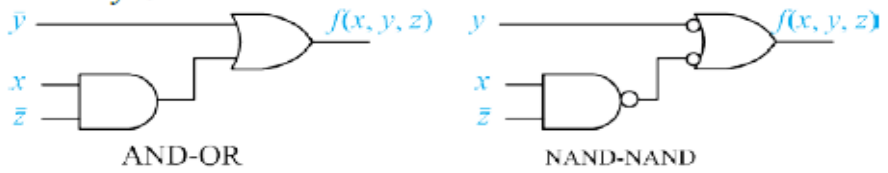
Coen/Elen 921c
Homework 3 Solution

Chapter 3

Textbook: 3.1, 3.2, 3.20

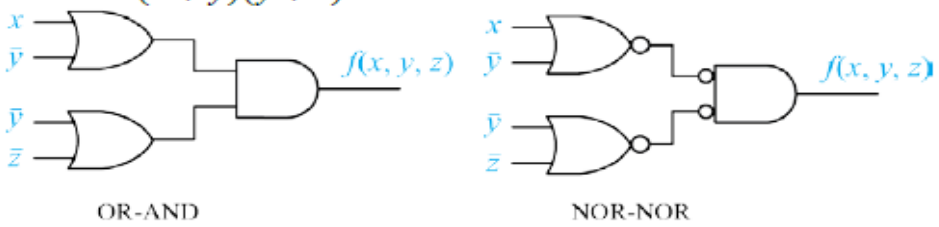
3.1 Design minimal 2-level AND-OR and NAND-NAND realizations of the following logic function. Draw circuit diagrams of your realizations.

$$f(x,y,z) = \Sigma m(0,1,4,5,6)$$
$$= \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + x\bar{y}\bar{z} + x\bar{y}z + xy\bar{z}$$
$$= \bar{y} + x\bar{z}$$

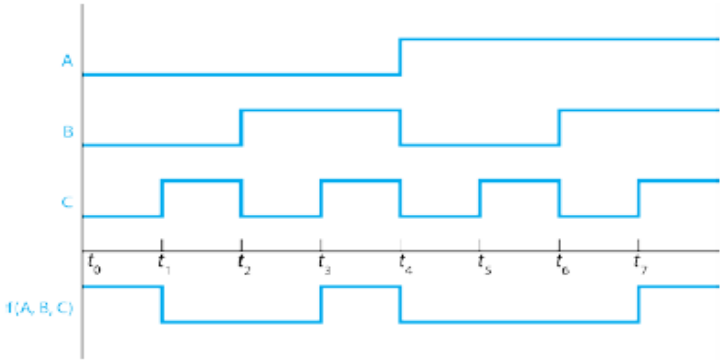


3.2 Design minimal 2-level OR-AND and NOR-NOR realizations of the function defined in problem 3.1. Draw circuit diagrams.

$$f(x,y,z) = \Pi M(2,3,7)$$
$$= (x + \bar{y} + z)(x + \bar{y} + \bar{z})(\bar{x} + \bar{y} + \bar{z})$$
$$= (x + \bar{y})(\bar{y} + \bar{z})$$



3.20 Given the timing diagram below, find the simplest Boolean expression for $f(A,B,C)$.



Time	a b c	f(A,B.C)
t_0	0 0 0	1
t_1	0 0 1	0
t_2	0 1 0	0
t_3	0 1 1	1
t_4	1 0 0	0
t_5	1 0 1	0
t_6	1 1 0	0
t_7	1 1 1	1

$$f(A,B,C) = \Sigma m(0,3,7)$$
$$= \bar{A}\bar{B}\bar{C} + \bar{A}BC + ABC$$
$$= \bar{A}\bar{B}\bar{C} + BC$$

Prob 1

Again, use the circuit diagram shown. Answer the following:

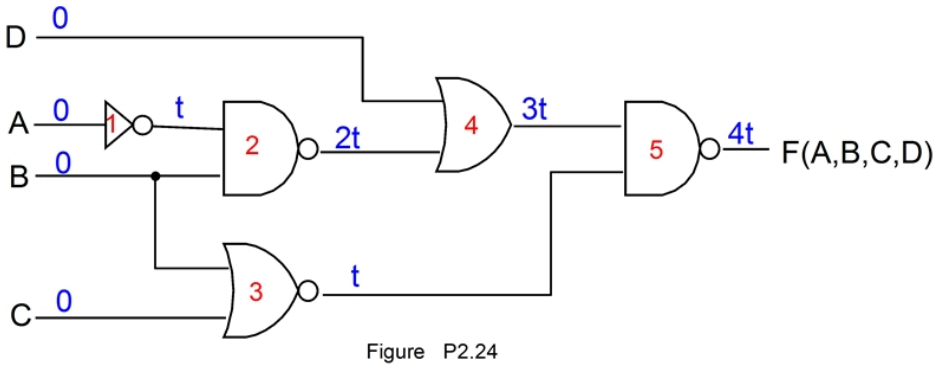


Figure P2.24

a) Assuming the propagation delay through all the gates is identical and equal to "t". What is the propagation delay through this circuit?

Using $\max(t_1, t_2, .., t_n) + t_{pd}$ for the delay at each gate output results in the delay at NAND gate 5 is 4t.

b) Assuming the propagation delay through the gates is not equal, it is:

INVERTER = 5 ns NAND = 10 ns NOR = 12 ns OR = 8 NS

What is the propagation delay through this circuit (in ns)?

The path from input A through INV 1, NAND 2, OR 4, and NAND 5 is the delay of the circuit. Since the delay is NOT uniform 't', we must add up the individual delays

5 ns + 10 ns + 8 ns + 10 ns = 33 ns So, the delay through the circuit is **33 ns.**

c) What is the worst case (slowest) signal path through this circuit, ie. starting at which input, through which gates, getting to the output?

It is from: Input A through INV 1, NAND 2, OR 4, and NAND 5

Prob 2

Given the following set of electrical and switching specs for the 3 gates show:

	NAND 74xx	NAND 74LSxx	AND 74xx	Units
Voh	2.4	2.7	2.4	V
Vol	0.4	0.5	0.4	V
Vih	2.0	2.0	2.0	V
Vil	0.8	0.8	0.8	V
Iih	40	**20**	40	uA
Iil	1.6	**0.4**	1.6	mA
Ioh	0.4	0.4	**0.8**	mA
Iol	16	8	**16**	mA
Icch	8	1.6	**12**	mA
Iccl	22	4.4	**33**	mA
t_{PHL}	14	21	17	ns
t_{PLH}	7	8	9	ns

a. What is the maximum fan-out for a 74xx AND gate driving 74LSxx NAND gates?

Ioh / Iih = 0.8 ma / 20 ua = 40

Iol / Iil = 16 ma / 0.4 ma = 40

Must choose the smaller of the two (ie. the worst case). Since both are the same, it doesn't matter and the fan out is 40.

Fan Out = 40

b. What is the average power consumption of the 74xx AND gate package?

$$P = (I_{cch} + I_{ccl}) / 2 * V_{CC} = (12 \text{ ma} + 33 \text{ ma})/2 * 5\text{v} = 112.5 \text{ mW}$$

c. What is the propagation delay of the circuit shown. Calculate average propagation delay for each gate if the NANDs are 74LSxx, and use those to determine delay of complete circuit.

Delay through NAND gates are (21+8)/2 ns = 14.5 ns
Delay through AND gate is (17+9)/2 ns = 13 ns

Total delay Path A-F = 14.5 + 14.5 = 29 ns
Total delay Path B-F = 13 + 14.5 = 27.5 ns

So, worst cast delay is path A-F = 29 ns