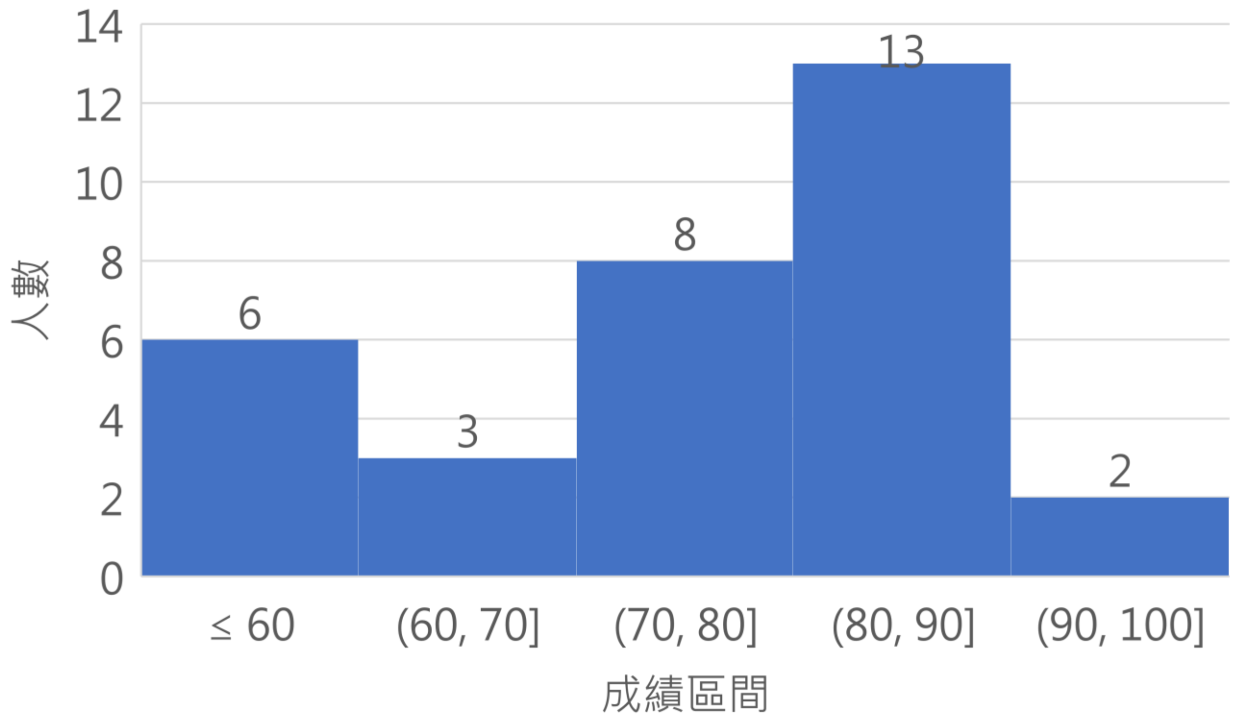
PDA 期末考解答

2022.01.14

成績分佈

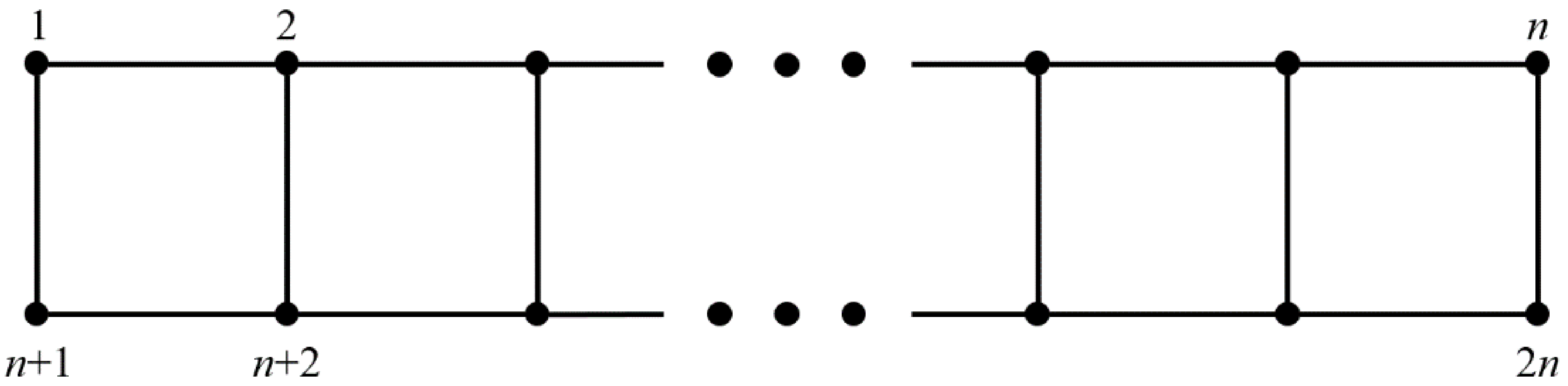
(已排除缺考同學成績)

最高：92
最低：39
平均：72.8



1. Question

Consider the following ladder graph with $2n$ vertices, and an initial bipartition $A = \{1,2,\dots,n\}$ and $B = \{n+1, n+2, \dots, 2n\}$.



1(a) Question + Solution (5%)

Prove that the given initial bipartition is a local minimum if only one step (i.e., exchanging one pair of vertices) of the KL algorithm is applied.

Ans:

All gains are smaller than or equal to 0.

So the initial bipartition is a local minimum.

1(b) Question + Solution (5%)

What is the resulting bipartition if one pass of the KL algorithm is applied?

Ans: (寫與initial相同得2分、有分奇偶討論得2分、有討論不同n的範圍得1分)

- If n is smaller than or equal to 3, the result is the same as the initial bipartition.
- If n is odd and greater than 3, it can obtain a 3-cut partitioning result after $\frac{n-1}{2}$ swaps.

  Swap$(n, n+1)$, Swap$(n-1, n+2)$, … , Swap$(n-\frac{n-1}{2}+1, n+\frac{n-1}{2})$

  $A = \left\{1,2, \dots, \frac{n+1}{2}, n+1, n+2, \dots, n+\frac{n-1}{2}\right\}, B = \{the\ remaining\ vertices\}$ (答案不唯一且AB可交換)
- If n is even and greater than 3, it can obtain a 2-cut partitioning result after $\frac{n}{2}$ swaps.

  Swap$(n, n+1)$, Swap$(n-1, n+2)$, … , Swap$(n-\frac{n}{2}+1, n+\frac{n}{2})$

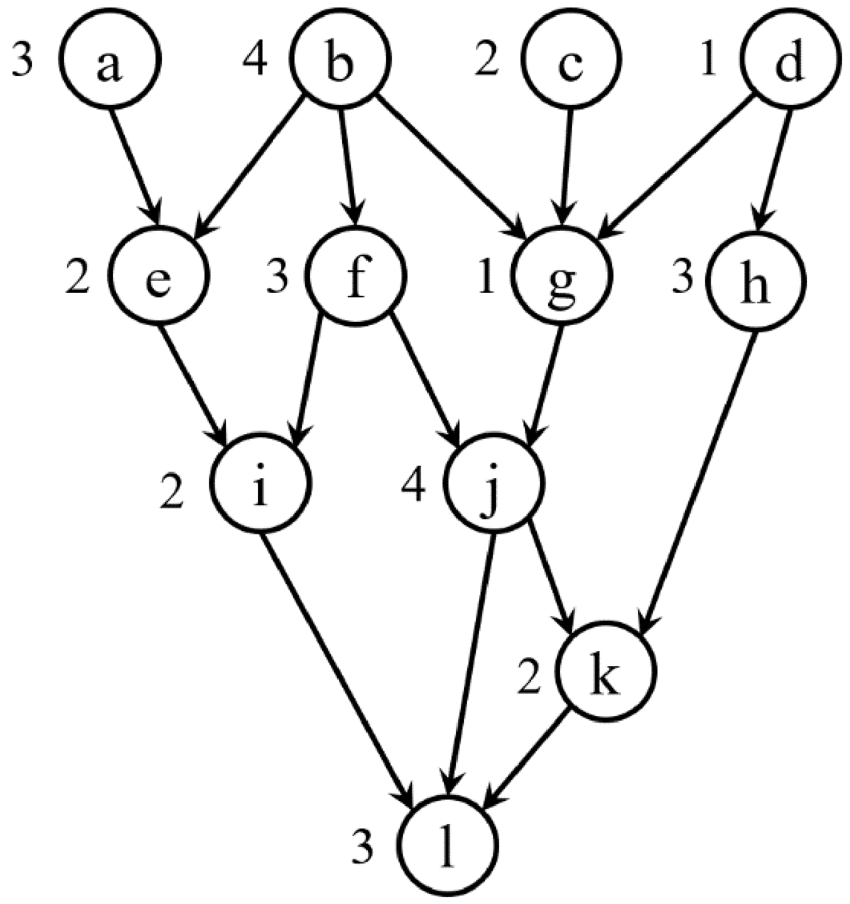
  $A = \left\{1,2, \dots, \frac{n}{2}, n+1, n+2, \dots, n+\frac{n}{2}\right\}, B = \{the\ remaining\ vertices\}$ (AB可交換)

2. Question

Consider the circuit shown below.

Assume the area of each gate is 1 unit, the area constraint of each cluster is 4 units, and the interconnection delay between two clusters is 5 units. The gate delay is given next to each gate.

Show your work by applying the clustering algorithm discussed in class to find *l*(i), *l*(j), *l*(k), *l*(l), *cluster*(i), *cluster*(j), *cluster*(k), and *cluster*(l).



2. Solution (15%)

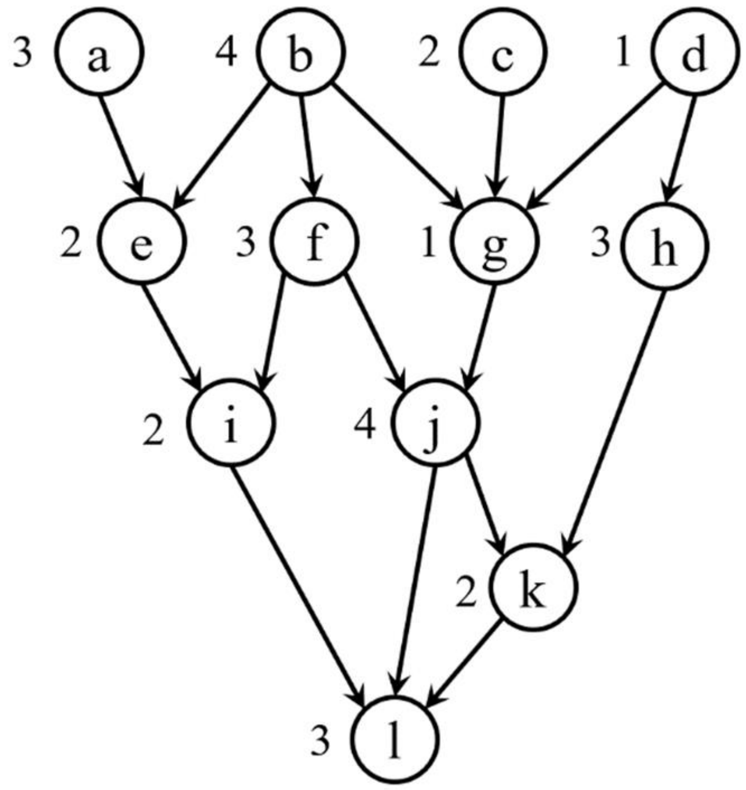
(每個l 2分、$cluster$ 2分，若公式正確但計算錯誤，受影響的答案每個扣2分)

$l(i) = 12, cluster(i) = \{b, e, f, i\}$

$l(j) = 12, cluster(j) = \{b, f, g, j\}$

$l(k) = 16, cluster(k) = \{b, f, j, k\}$

$l(l) = 21, cluster(l) = \{f, j, k, l\}$



3(a) Question

Consider a set of hard modules in the following table. Assume that each module cannot be rotated.

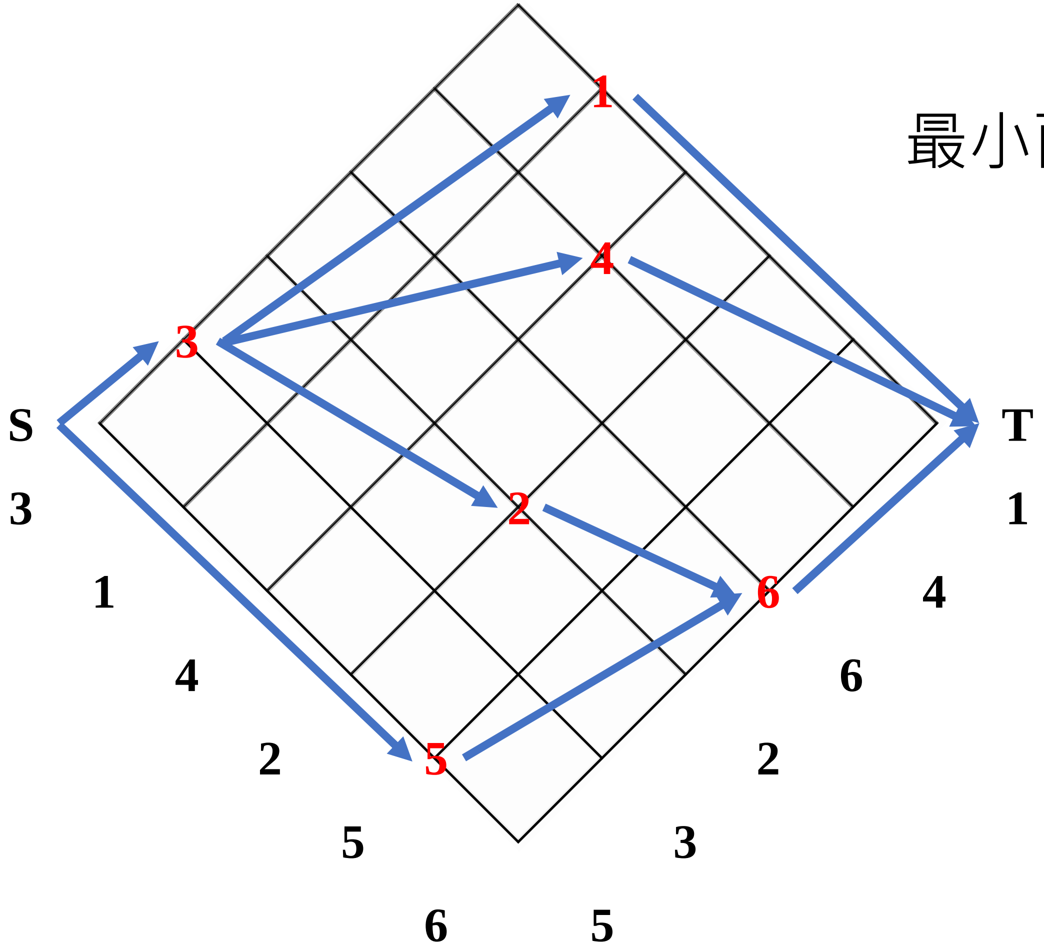
Show your work for finding a minimum-area placement for the sequence-pair (314256, 532641) and show the placement result.

Module	**Width**	**Height**
1	4	2
2	3	2
3	2	1
4	1	4
5	4	2
6	2	3

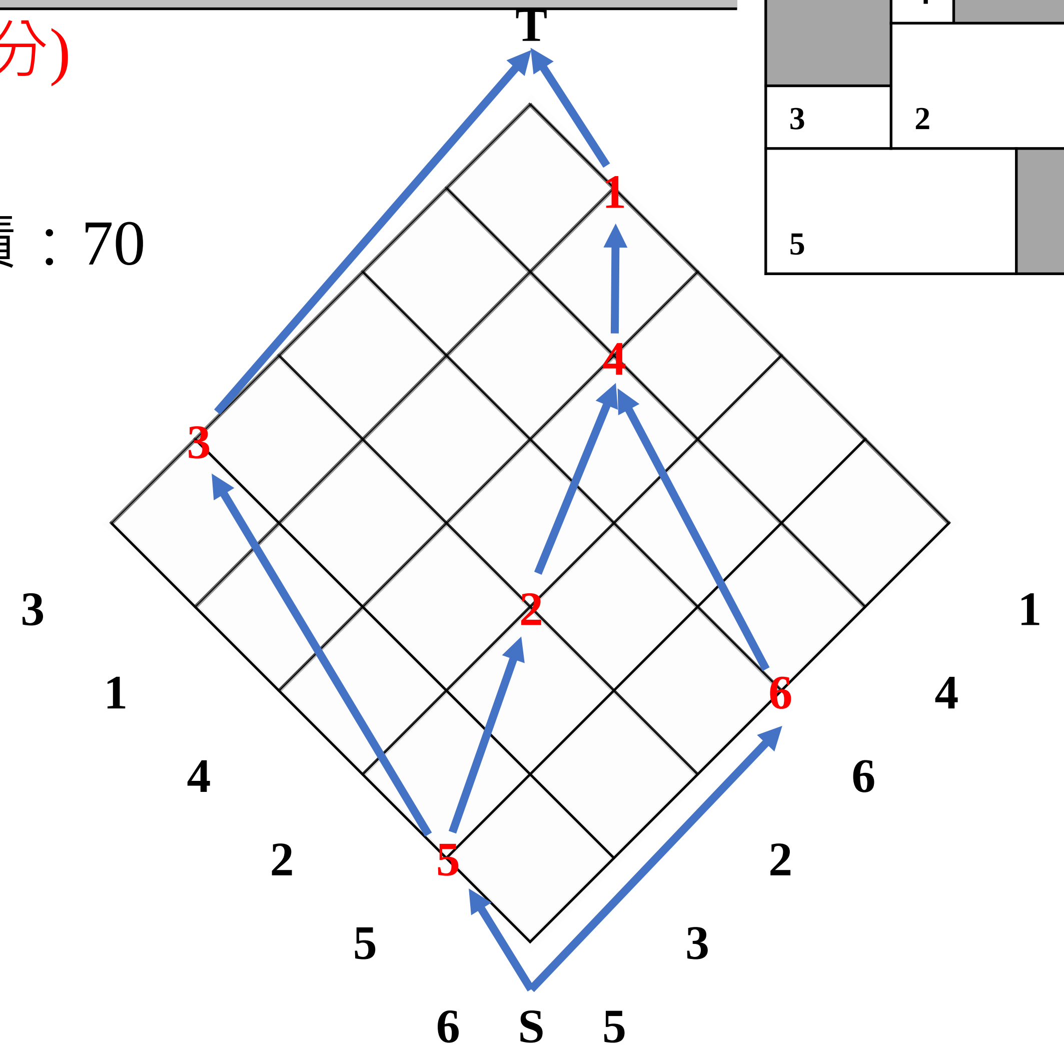
3(a) Solution (7%)

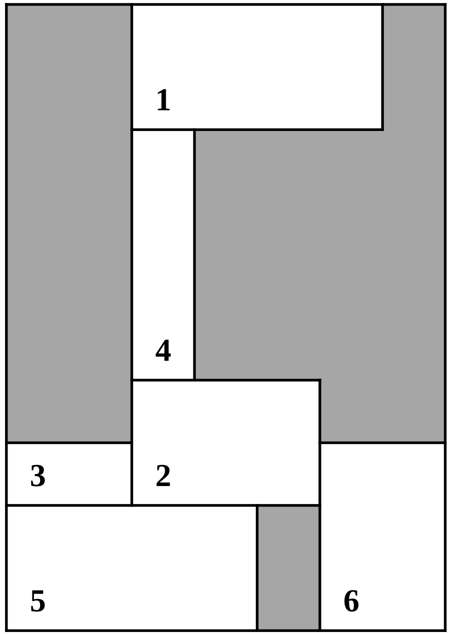
Module	Width	Height
1	4	2
2	3	2
3	2	1
4	1	4
5	4	2
6	2	3

(左右、上下關係各2分，畫placement圖3分)



最小面積：70

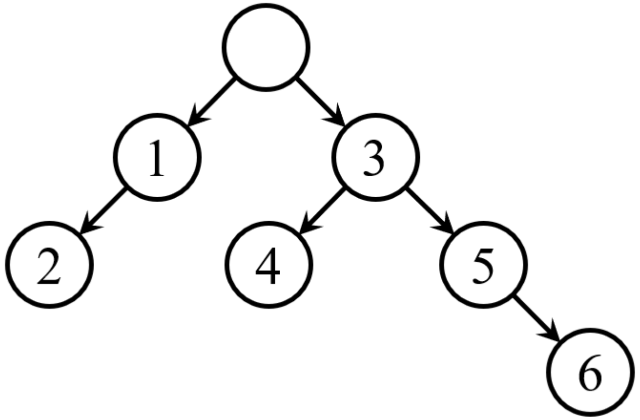


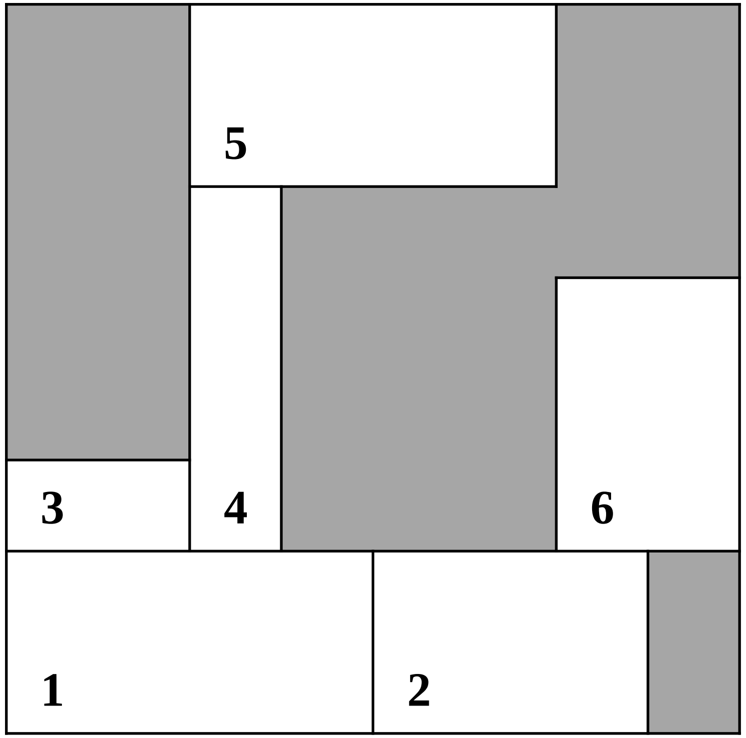


3(b) Question + Solution (4%)

Module	Width	Height
1	4	2
2	3	2
3	2	1
4	1	4
5	4	2
6	2	3

Assume that each module cannot be rotated. Show the placement for the following horizontal O-tree.

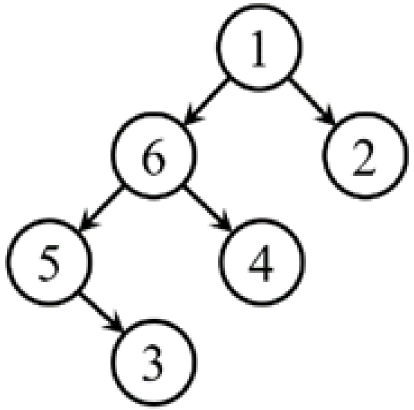


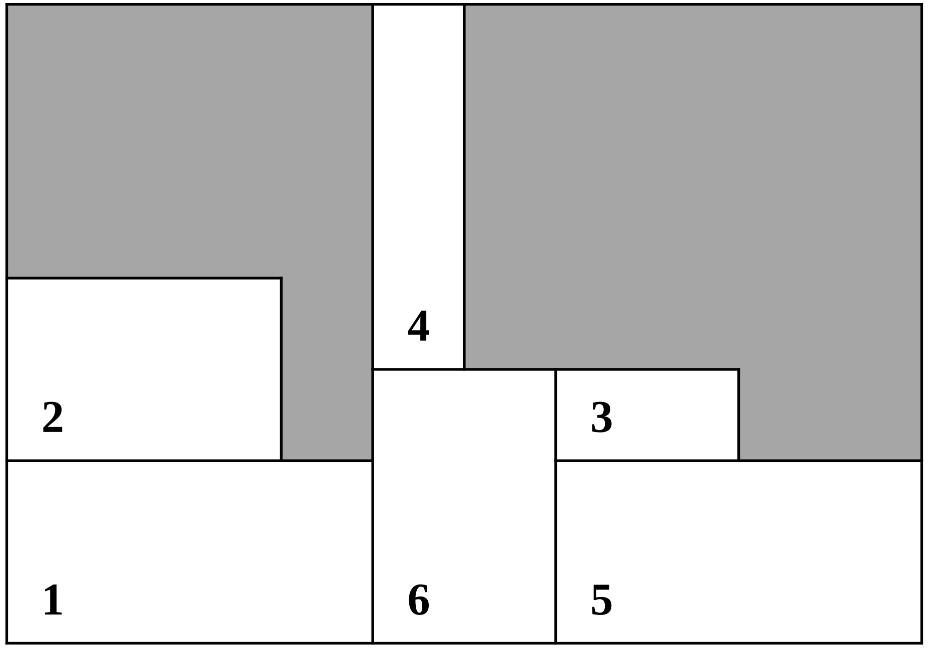


3(c) Question + Solution (4%)

Module	Width	Height
1	4	2
2	3	2
3	2	1
4	1	4
5	4	2
6	2	3

Assume that each module cannot be rotated. Show the placement for the following B*-tree.





4. Question

Given a slicing floorplan tree for n rectangular hard modules, where each module can be rotated but the cut direction of each internal node is undecided yet, describe how to extend Stockmeyer’s algorithm to simultaneously determine a cut direction for each internal node and a shape for each module such that the total area of the floorplan is minimized.

You should also analyze the time complexity of your method. Note that the time complexity of your method could be exponential, but it should be as low as possible.

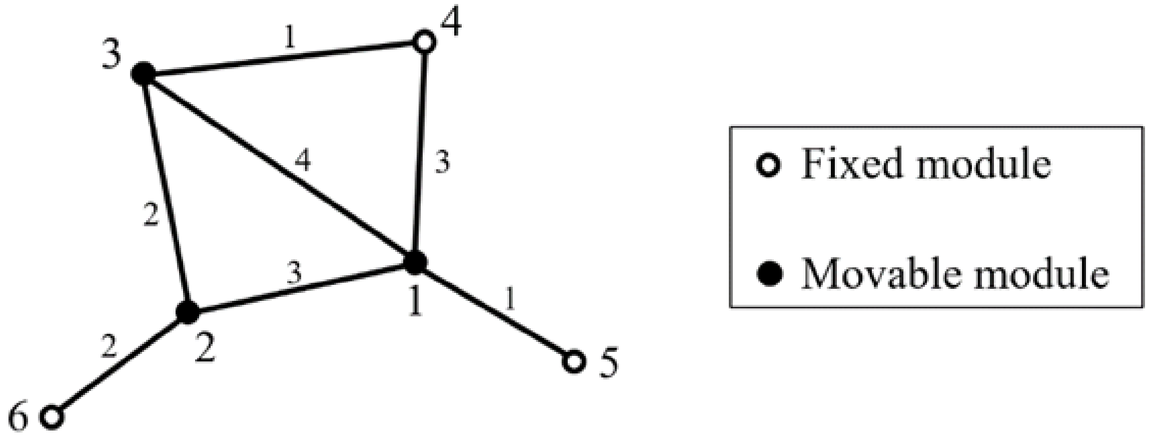
4. Solution (10%)

Bottom-up to apply Stockmeyer's algorithm to calculate the combinations of the horizontal cut and the vertical cut for each internal node. Record the combination information. Then, merge the combinations into one list. (6分)

Top-down to determine the cut of each internal node and determine whether the module is rotated or not. (2分)

Complexity:$O(n2^d)$, where n is # modules, d is the depth of tree. (2分)

5. Question



Consider a circuit with movable and fixed modules as represented by the following graph.

In the graph, each vertex denotes a module, while each edge denotes a two-pin net and is associated with a weight next to it.

For the three fixed modules, module 4 is at (8, 11), module 5 is at (10, 6), and module 6 is at (3, 5).

Determine Q, d_x, and d_y such that the cost function of quadratic placement for this circuit can be written as follows:

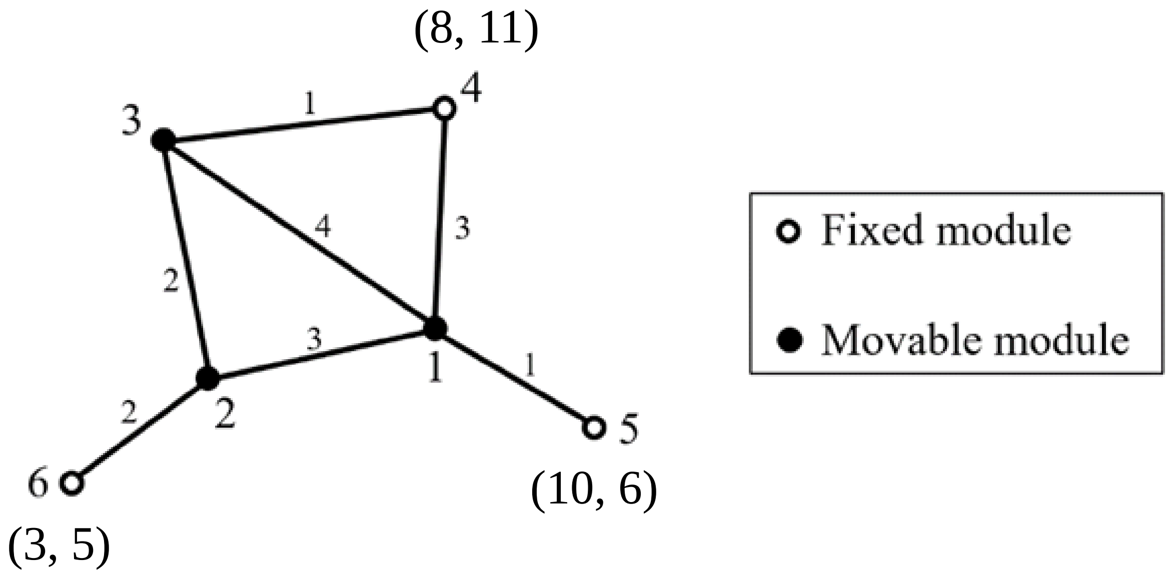
$$\frac{1}{2}x^T Q x + d_x^T x + \frac{1}{2}y^T Q y + d_y^T y + \text{const}$$

5. Solution (10%)

(Q矩陣4分，d_x矩陣與d_y矩陣各3分，計算錯誤一個地方扣1分)

$$Q = \begin{bmatrix} 11 & -3 & -4 \\ -3 & 7 & -2 \\ -4 & -2 & 7 \end{bmatrix}$$

$$d_x = \begin{bmatrix} -34 \\ -6 \\ -8 \end{bmatrix},\ d_y = \begin{bmatrix} -39 \\ -10 \\ -11 \end{bmatrix}$$



6. Question + Solution (6%)

Given a net with four pins a, b, c, d which are located at (9, 3), (6, 2), (1, 6), (5, 12), estimate its wire lengths by using the half-perimeter wire length method and the minimum spanning-tree method, respectively.

Ans:

HPWL: 18 (3分)

MST: 23 (3分)

7. Question + Solution (4%)

You are asked to place a cell on a chip. The cell connects to four other cells located at (2,8), (4, 2), (3, 5), and (8, 2) with the weights 1, 2, 2, and 1, respectively. Find an appropriate position to place the cell by using the force-directed method.

Ans:

(4, 4)

8. Question

An analytical placement approach usually models a k-pin net connecting modules 1, 2, …, k as one or more 2-pin nets, depending on the value of k.

Let N denote such a k-pin net. Suppose the weights of each 2-pin net (which originates from N) in the clique and star models are respectively set to c and $k\times c$. Let s denote the star module in the star model and F_s denote the total force on s.

Prove that if $F_s=0$, then for each i ($1\leq i \leq k$), the total force on module i by the 2-pin nets (which originate from N) in the clique model is equal to the force on module i by the 2-pin net connecting to s (which originates from N) in the star model. You only need to do the proof for the x direction.

8. Solution (5%)

The total force on module i by the 2-pin nets in the clique is given by: $F_i^{clique} = c \times \sum_{j=1}^{k}(x_j - x_i)$

The total force on the star node is given by: $F_s = \sum_{j=1}^{k} k \times c \times (x_j - x_s)$

By setting $F_s = 0$, the force-equilibrium position for the star node is: $x_s = \frac{1}{k}\sum_{j=1}^{k} x_j$

The force on module i by the 2-pin net connecting to the star is given by:

$$\begin{aligned}
F_i^{star} &= k \times c \times (x_s - x_i) \\
&= k \times c \times (\tfrac{1}{k}\textstyle\sum_{j=1}^{k} x_j - x_i) \\
&= c \times (\textstyle\sum_{j=1}^{k} x_j - k \times x_i) \\
&= c \times \textstyle\sum_{j=1}^{k}(x_j - x_i) = F_i^{clique}
\end{aligned}$$

9(a) Question + Solution (8%)

Show your work for finding a shortest path between S and T using the Lee algorithm.

(若未填寫完整扣4分(27以下要全標，至少標到27，最多標到27)，

沒有traceback扣4分，紅色數字為最短路徑(答案不唯一))

6	7	8	9	10	11	12	13	14	15	16	17	18
5						13	14				18	19
4						14	15					20
3	2			13	14	15	16	17				21
2	1			**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**
1	**S**			**11**	12	13	14				20	**21**
2	**1**			**10**	11	12						**22**
3	**2**			**9**	10	11					24	**23**
4	**3**			**8**		12			27	26	25	**24**
5	**4**	**5**	**6**	**7**		13				T **27**	**26**	**25**
	5	6	7	8		14					27	26
	6	7	8	9		13	14					27
				10	11	12	13					

9(b) Question + Solution (7%)

Show your work for finding a shortest path between *S* and *T* using the Hadlock's detour algorithm.

(若未填寫完整扣4分(7以下要全標，至少標到7，最多標到8)，

沒有traceback扣3分，紅色數字為最短路徑(答案不唯一))

6	6	6	6	6	6	6	6	6	6	6	7	8
5						6	6				7	8
4						6/7	6/7					
3	2			6	6	6	6	6				8
2	1			**5**	**5**	**5**	**5**	**5**	**5**	**5**	**6**	**7**
1	**S**			**4**	4	4	4				6	**7**
1	**0**			**3**	3	3						**7**
1	**0**			**2**	2	2					7	**7**
1	**0**			**1**		2			8	7	7	**7**
1	**0**	**0**	**0**	**0**		2				**T**	**7**	**7**
	1	1	1	1		3					8	8
	2	2	2	2		3	3					
				3	3	3	3					

10. Question

Consider a two-pin net with length l and a buffer inserted as shown in Figure (a) below. Assume that the driver and the buffer both have the same output resistance R, the buffer input capacitance is the same as the sink load capacitance C_L, the buffer intrinsic delay is t_b, the wire resistance per unit length is r, and the wire capacitance per unit length is c. The corresponding RC circuit for this buffered net is shown in Figure (b) below.

Find an optimal position of the buffer (i.e., the value of x in terms of given parameters) such that the driver-sink delay (i.e., the buffered net delay) based on the Elmore delay model is minimum.

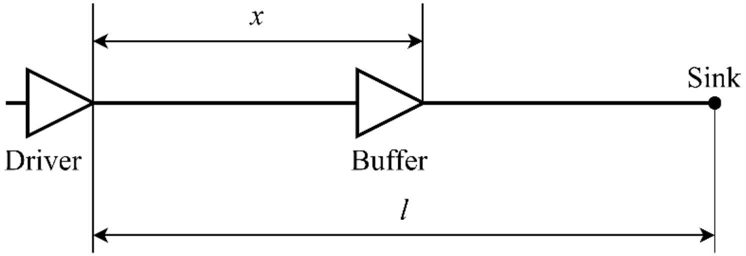


Figure (a)

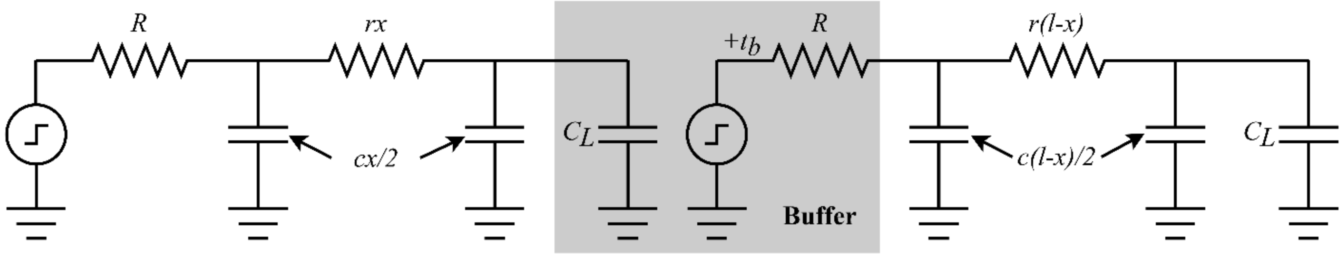


Figure (b)

10. Solution (10%)

(方程式對5分，答案對5分)

The driven-sink delay can be expressed as:

$$t = R\left(\frac{cx}{2} \times 2 + C_L\right) + rx\left(\frac{cx}{2} + C_L\right) + t_b + R\left(\frac{c(l-x)}{2} \times 2 + C_L\right) + r(l-x)\left(\frac{c(l-x)}{2} + C_L\right)$$

$$= \frac{1}{2}rcx^2 + \frac{1}{2}rc(l-x)^2 + A$$

$$= rc(x^2 - lx) + B$$

where A and B are constants. Evidently, $t = f(x)$ is a convex function and its minimum value can be obtained by letting $\frac{dt}{dx} = 0$. Hence the source-sink delay t reached the minimum when $x = \frac{l}{2}$.