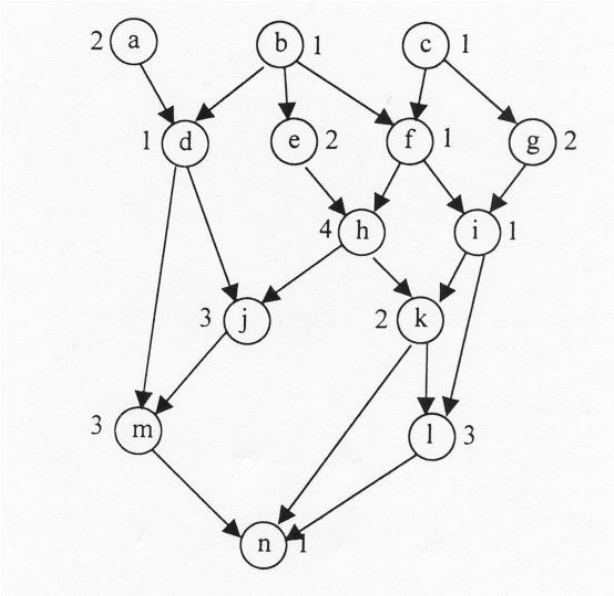
CS 6135 VLSI Physical Design Automation

Final Exam: 10:10 a.m. - 13:10 p.m., January 5, 2021

1. (15 points) Consider the circuit shown below. Assume the area of each gate is 1 unit, the area constraint of each cluster is 3 units, and the interconnection delay between two clusters is 4 units. The gate delay is given next to each gate. Show your work by applying the clustering algorithm discussed in class to find *l*(h), *l*(i), *l*(k), *cluster*(h), *cluster*(i), and *cluster*(k).



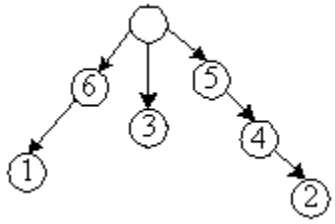
2. (10 points) Given a circuit *C*, a weighted graph *G* is obtained from *C* by modeling each *k*-pin net of *C* as a clique (i.e., a complete graph) on the *k* vertices and assigning a weight of 1/(*k*-1) to each edge. The cut size of a two-way partitioning of *G* (*C*, respectively) is defined to be the sum of the weights of all cut edges (the number of all cut nets, respectively). Prove that if each net in *C* has at most 3 pins, an optimal balanced two-way partitioning of *G* corresponds to an optimal balanced two-way partitioning of *C*.

3. Consider a set of modules in the following table.

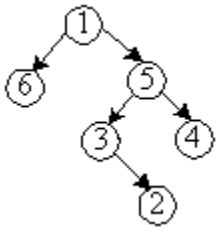
Module	Width	Height
1	1	3
2	4	1
3	1	2
4	3	2
5	2	3
6	2	4

   (a) (10 points) Assume that each module can be rotated by 90-degree. Perform the Stockmeyer algorithm to find a minimum-area floorplan for the Polish expression 123V4H56VHV.
   (b) (7 points) Assume that each module cannot be rotated. Show your work for finding a minimum-area placement for the sequence-pair (132546, 546321).

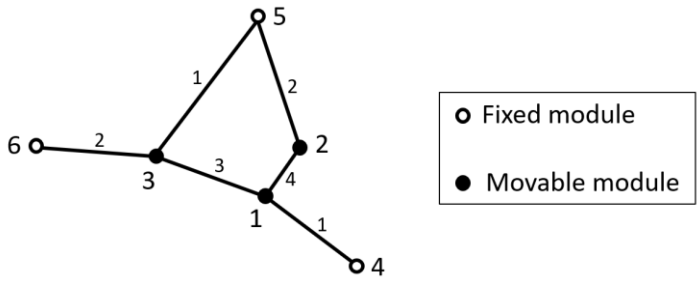
(c) (4 points) Assume that each module cannot be rotated. Show the placement for the following horizontal O-tree.



(d) (4 points) Assume that each module cannot be rotated. Show the placement for the following B*-tree.



4. (10 points) Consider a circuit with movable and fixed modules as represented by the following graph. In the graph, each vertex denotes a module, while each edge denotes a two-pin net and is associated with a weight next to it.



For the three fixed modules, module 4 is at (15, 2), module 5 is at (9, 11), and module 6 is at (1, 7). Determine Q, d_x, and d_y such that the cost function of quadratic placement for this circuit can be written as follows:

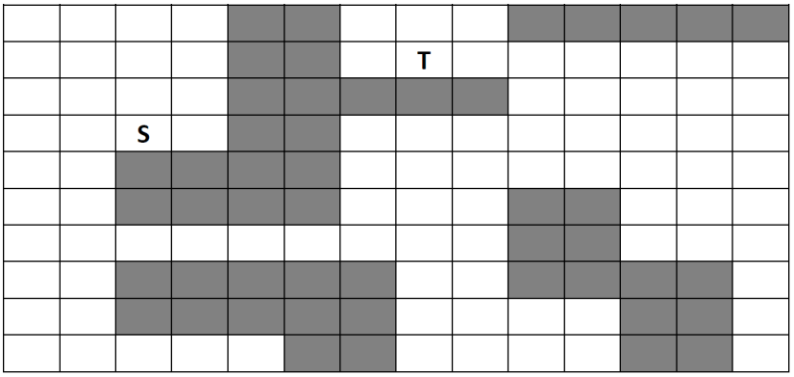
$$\frac{1}{2}x^T Qx + d_x^T x + \frac{1}{2}y^T Qy + d_y^T y + \text{const}$$

5. (5 points) Prove that half-perimeter wirelength (HPWL) is a lower bound of rectilinear Steiner minimal tree (RSMT) wirelength.

6. An analytical placement approach usually models a k-pin net as one or more 2-pin nets, depending on the value of k. For each of the following net models, give the number of 2-pin nets and the number of extra x and y variables introduced for a k-pin net.
   (a) (2 points) Clique
   (b) (2 points) Star

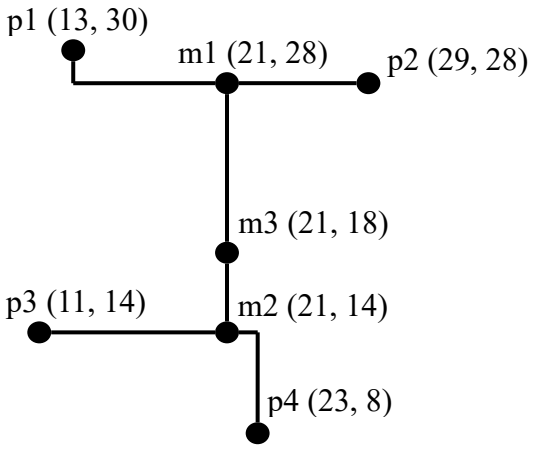
(c) (4 points) Hybrid
(d) (2 points) BoundingBox

7. Consider the following routing instance with shaded blockages.



(a) (8 points) Show your work for finding a shortest path between S and T using the Lee algorithm.
(b) (7 points) Show your work for finding a shortest path between *S* and *T* using the Hadlock's detour algorithm.

8. A routing tree for four clock pins p1, p2, p3, and p4 is given below. Suppose m1 is the tapping point for (p1, p2), m2 is the tapping point for (p3, p4), and m3 is the tapping point for (m1, m2). (Note that it is possible that a tapping point may not achieve zero skew in this problem.) The coordinates of p1, p2, p3, p4, m1, m2, and m3 are also shown below. The loading capacitances of p1, p2, p3, and p4 are 4*F*, 2*F*, 2*F* and 1*F*, respectively. The per unit values of resistance and capacitance of a wire segment are $\alpha = 0.2\Omega$ and $\beta = 0.1F$, respectively. The point m3 is the final clock entry point. Assume the π-model is used for wires, and the Elmore delay model (i.e., the RC delay model discussed in class) is used for calculating delays.



(a) (6 points) What are the delay and skew of the routing tree?
(b) (4 points) Assume the switch-resistor model discussed in class is used for buffers, and the intrinsic delay of each buffer is negligible. If two identical buffers with resistance $r_b = 0.1\Omega$ and capacitance $c_b = 0.2F$ are inserted at m1 and m2, respectively, what are the resultant delay and skew of the routing tree?