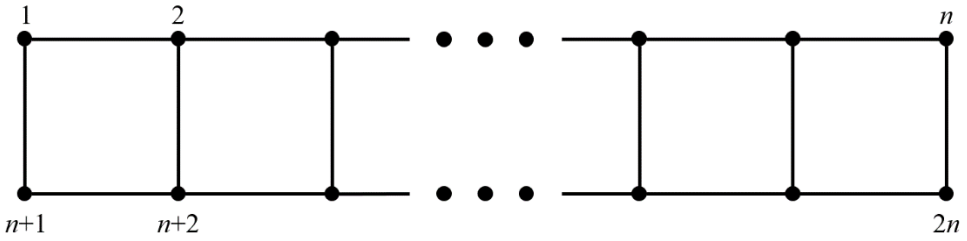
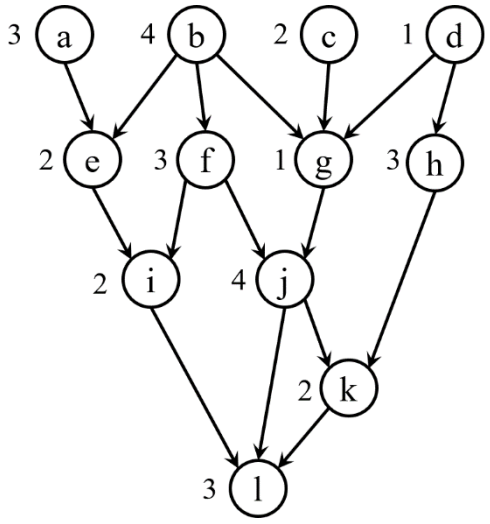
CS 6135 VLSI Physical Design Automation
Final Exam: 10:10 a.m. – 13:10 p.m., December 28, 2021

1. Consider the following ladder graph with $2n$ vertices, and an initial bipartition $A=\{1, 2,\ldots, n\}$ and $B=\{n+1, n+2,\ldots, 2n\}$.



   (a) (5 points) Prove that the given initial bipartition is a local minimum if only one step (i.e., exchanging one pair of vertices) of the KL algorithm is applied.
   (b) (5 points) What is the resulting bipartition if one pass of the KL algorithm is applied?

2. (15 points) Consider the circuit shown below. Assume the area of each gate is 1 unit, the area constraint of each cluster is 4 units, and the interconnection delay between two clusters is 5 units. The gate delay is given next to each gate. Show your work by applying the clustering algorithm discussed in class to find l(i), l(j), l(k), l(l), *cluster*(i), *cluster*(j), *cluster*(k), and *cluster*(l).

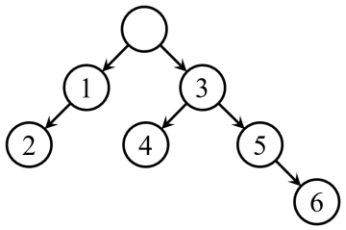


3. Consider a set of hard modules in the following table. Assume that each module cannot be rotated.

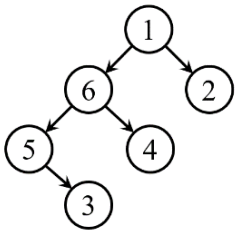
Module	Width	Height
1	4	2
2	3	2
3	2	1
4	1	4
5	4	2
6	2	3

(a) (7 points) Show your work for finding a minimum-area placement for the sequence-pair (314256, 532641) and show the placement result.

(b) (4 points) Show the placement for the following horizontal O-tree.

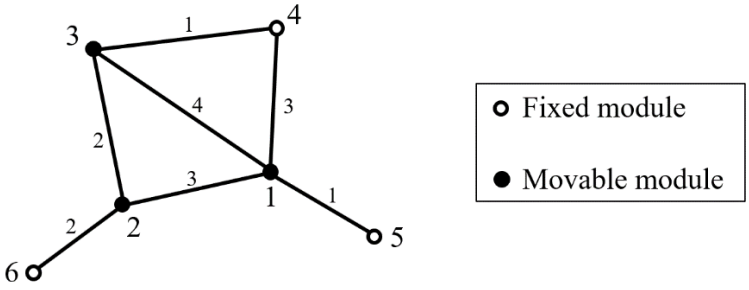


(c) (4 points) Show the placement for the following B*-tree.



4. (10 points) Given a slicing floorplan tree for *n* rectangular hard modules, where each module can be rotated but the cut direction of each internal node is undecided yet, describe how to extend Stockmeyer's algorithm to simultaneously determine a cut direction for each internal node and a shape for each module such that the total area of the floorplan is minimized. You should also analyze the time complexity of your method. Note that the time complexity of your method could be exponential, but it should be as low as possible.

5. (10 points) Consider a circuit with movable and fixed modules as represented by the following graph. In the graph, each vertex denotes a module, while each edge denotes a two-pin net and is associated with a weight next to it.



For the three fixed modules, module 4 is at (8, 11), module 5 is at (10, 6), and module 6 is at (3, 5). Determine Q, d_x, and d_y such that the cost function of quadratic placement for this circuit can be written as follows:

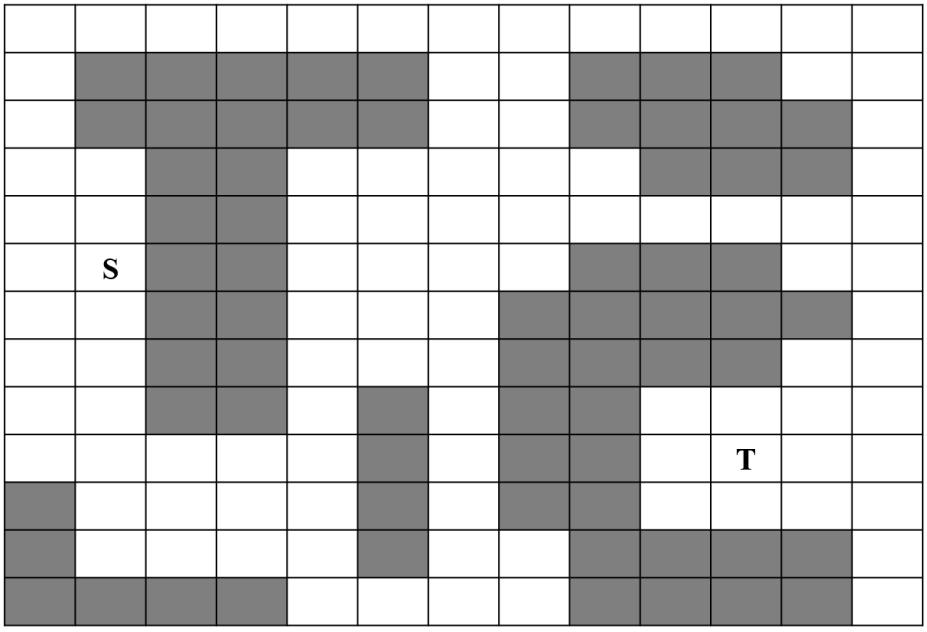
$$\frac{1}{2}x^T Q x + d_x^T x + \frac{1}{2}y^T Q y + d_y^T y + \text{const}$$

6. (6 points) Given a net with four pins *a*, *b*, *c*, *d* which are located at (9, 3), (6, 2), (1, 6), (5, 12), estimate its wire lengths by using the half-perimeter wire length method and the minimum spanning-tree method, respectively.

7. (4 points) You are asked to place a cell on a chip. The cell connects to four other cells located at (2,8), (4, 2), (3, 5), and (8, 2) with the weights 1, 2, 2, and 1, respectively. Find an appropriate position to place the cell by using the force-directed method.

8. (5 points) An analytical placement approach usually models a *k*-pin net connecting modules 1, 2, …, *k* as one or more 2-pin nets, depending on the value of *k*. Let *N* denote such a *k*-pin net. Suppose the weights of each 2-pin net (which originates from *N*) in the clique and star models are respectively set to *c* and $k \times c$. Let *s* denote the star module in the star model and F_s denote the total force on *s*. Prove that if $F_s=0$, then for each *i* ($1 \leq i \leq k$), the total force on module *i* by the 2-pin nets (which originate from *N*) in the clique model is equal to the force on module *i* by the 2-pin net connecting to *s* (which originates from *N*) in the star model. You only need to do the proof for the *x* direction.

9. Consider the following routing instance with shaded blockages.



(a) (8 points) Show your work for finding a shortest path between *S* and *T* using the Lee algorithm.
(b) (7 points) Show your work for finding a shortest path between *S* and *T* using the Hadlock's detour algorithm.

10. (10 points) Consider a two-pin net with length *l* and a buffer inserted as shown in Figure (a) below. Assume that the driver and the buffer both have the same output resistance *R*, the buffer input capacitance is the same as the sink load capacitance C_L, the buffer intrinsic delay is t_b, the wire resistance per unit length is *r*, and the wire capacitance per unit length is *c*. The corresponding RC circuit for this buffered net is shown in Figure (b) below. Find an optimal position of the buffer (i.e., the value of *x* in terms of given parameters) such that the driver-sink delay (i.e., the buffered net delay) based on the Elmore delay model is minimum.

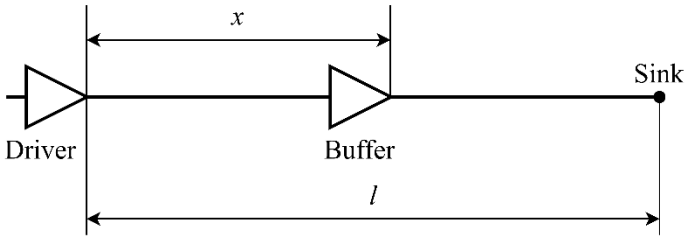


Figure (a)

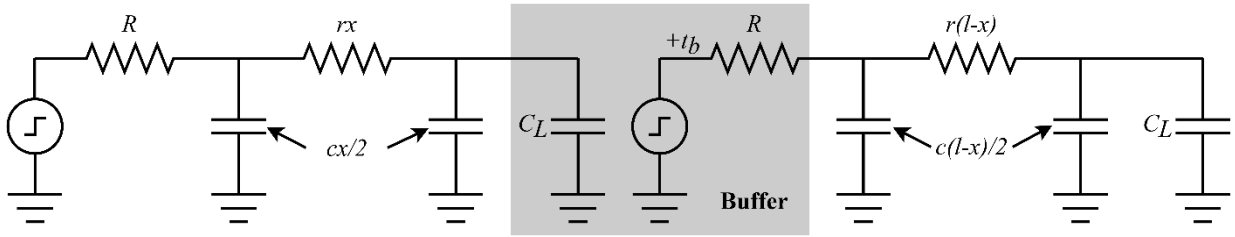


Figure (b)