Final Report 6.334 Buck Converter Design

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Summary of Design

- Switching Frequency: 150kHz
- Power Dissipated by Mosfet: 5.34 Watts
- Efficiency: 96.56%
- Inductor (Power Stage): 25uH, RM14-950um gap, N=10, 11 AWG
- Capacitor (Power Stage): 2.2mF U767D25VH222M19X41LL 25 Volts 58 mOhms ESR
- Input Filter:
    - Inductor: 81uH, RM14-950um gap, N=18, 14 AWG
    - Capacitor 2.2mF LXG50VN222M22X35T2 50 Volts .141 Ohms ESR
    - Resistor: 0.1 Ohms
- MOSFET: NTMFS5844 Power Mosfet
- Diode: PMEG045V100EPD Diode
- Heat Sink: 1 deg C /W. #22 AAVID Extruded Heat Sink 1.4066 mm.
- Compensator Transfer Function. Hc(s) = Kp + Kd*s + Ki*(1/s). Kp = .002, Kd = 1, Ki = 1

	Specifications	Results
Output Voltage (static req.)	14.55 - 15.45 V	14.95-15.05 V
Output Voltage (trans. req.)	12 - 18 V	14 - 16 V
Max o/p Voltage ripple (p-p)	75 mV	45 mV
Max i/p Current Ripple (p-p)	60 mA	1.23 uA
Min. Efficiency	90 %	96.46%
Ambient Temperature Range	-20 to 50 deg C	-30-90 deg C

Output Voltage Ripple

The output voltage is calculated with the following equation. Based on the equations we can see that generally, having a larger capacitor, inductor, and switching frequency allows us to reduce the voltage ripple. There is a drawback to increasing switching frequency because a larger switching frequency leads to increased switching losses which hurts the efficiency of the circuit.

$$V_{out\ pp} = \frac{V_{out} * (1-D)}{8 * L_{buck} * C_{buck} * f_s^2} + ESR * I_{L_{buck} pp}$$

Inductor Design

I tried to maximize the size of the inductor based on the cores provided. The inductor design is limited by the saturation of the core, current density, wire geometry and the provided cores. I did a parameter search with different cores, gap sizes, and coils to choose an inductor with the largest inductance that still meets the other requirements. The inductor I chose was a RM-14 with 950um gap with 10 turns. L = 25 uH.

1. Core doesn't reach saturation

   The saturation flux density is .3 Teslas, minimum area of the core A_core = 168mm2 and a max current of 20 Amps was considered.

   $$N * B_{sat} * A_{core} > L\, i_{max}$$

   $$5.0389 * 10^{-4} > 5 * 10^{-4}$$

   Saturation limit condition is satisfied

2. Inductance Calculation

   The inductance factor is 250 nH per turn

   $$L = A_L * N^2 = 25\, uH$$

3. Inductor Gap for Energy Storage

   The energy stored in the inductor has to be less than the amount of energy that can be stored in the inductor. The effective area of the core is 198 mm2 and effective length is 70 mm.

   $$\frac{B^2 A_c l_c}{2 u_c u_0} + \frac{B^2 A_c l_g}{2 u_0} > \frac{1}{2} L\, i_{max}^2$$

   $$247 > .005$$

   Energy storage condition satisfied

4. Winding Sizing

   We want to choose a wire size that allows 10 turns to fit inside the coil former and at the same time have a current density of less than 500 A/cm2. AWG 11 wire, which has a diameter of 2.31 mm and an area of 4.17 mm2 was chosen. The RM-14 has a coiler former with an area of 111 mm2 and winding width of 18 mm. The coil former can fit 10 turns in one layer.

   1. Current Density

      The current density has to be less than the max current density

      $$J < J_{max}$$

      $$I_{peak}/(N * A_{wire}) < 5 * 10^{6}\ Amps/m2$$

      $$A_{wire} > .4\ mm^{2}$$

      4.17 mm2 > .4 mm2

   2. Geometry

      The diameter of AWG 11 is 2.31 mm and the coil former is 18 mm by 6.1667 mm. We can fit 7 turns in the innermost layer and 3 turns to form the second layer. The coil former is larger enough to accomodate 10 turns of wire.

Switching Frequency

Let's consider the inductor current ripple given in the equation below

$$I_{pp} = \frac{(V_{out} - V_{in})\ D}{f_s * L_{buck}}$$

Although the switching frequency can help greatly reduce the ripple, we don't want to rely too heavily on it because then our switching losses would be too large. A switching frequency of 150KHz was chosen. We want to keep our inductor ripple ratio low because high ripple could cause current loading on the input side and cause voltage ripple. We also don't want the converter to enter discontinuous conduction mode, so we need to make sure the ripple ratio is not greater than 1. With a 25uH inductor and a switching frequency of 150kHz, the ripple ratio is below 1. The bottom chart shows the calculations for different operating conditions.

Power Out	V-in	R-load	AvgI_L	$I_{L\,pp}$	Ripple Ratio
150 W o/p	40 V	1.5 Ohms	10 Amps	2.5 Amps	.125
50 W o/p	40 V	4.5 Ohms	3.3 Amps	2.5 Amps	.378
150 W o/p	27 V	1.5 Ohms	18 Amps	1.78 Amps	.0495
50 W o/p	27 V	4.5 Ohms	6 Amps	1.78 Amps	.1978

Capacitor Design

This capacitor was chosen to be the power stage capacitor: 2.2mF U767D25VH222M19X41LL 25 Volts 58 mOhms ESR. When choosing the capacitor, the output voltage ripple was considered. We want to keep the output ripple small in order to meet the design constraints of 3% from the desired output voltage during steady state operation.
We must also make sure that the capacitor meets the maximum ripple current requirement. The maximum ripple current is 2.5 Amps considering all possible operating conditions (see chart above). The chosen capacitor has a maximum ripple current Arms of 4.86 at 120 Hz and 7.44 at 20 kHz. The Arms of the triangle wave ripple is less than that maximum.

$$Arms_{triangle\ wave} = 0.2885 * I_{pp} = .7212 < Max_{Arms}\ where\ 4.86 < Max_{Arms} < 7.44$$

$$V_{out\ pp} = \frac{V_{out}*(1-D)}{8*L_{buck}*C_{buck}*f_s^{\,2}} + ESR * I_{L_{buck}pp}$$

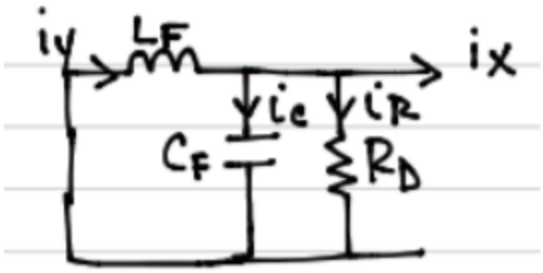
$$V_{out\ pp} = \frac{V_{out}*(1-D)}{8*L_{buck}*C_{buck}*f_s^{\,2}} + ESR * \frac{(V_{in}-V_{out})*D}{f_s*L_{buck}}$$

V-in	V-out pp	% from 15 V
40 V	35.1 m V	0.49%
27 V	17.9 mV	0.35%

The voltage ripple percentage from 15V is less than 3% and has a ripple of less than 75 mV. This satisfies the output voltage ripple requirement. This capacitor has a voltage rating of 25 V which is almost twice the size of the desired output voltage.

Input Current Ripple

The input current can be approximated by this circuit diagram. The magnitude of the transfer function is also given below. We want to create a low pass filter that removes the AC component of the input current ix.



$$\left|\frac{i_y}{i_x}\right| = \left|\frac{1}{1+\frac{sL_F}{\frac{1}{sC_F}+ESR+sESL}+s\frac{L_F}{R_D}}\right|$$

The input ix can be approximated as a square wave represented by its fourier series. We can make further approximations and only consider the fundamental because the harmonics will be much more attenuated by the low pass filter.

$$i_{x1} = \frac{4*I_L}{\pi} sin(w_0 t)$$

The current I_L can be chosen to be the peak inductor current of 20 Amps in order to give us a safety margin. We want the peak current to be attenuated so that the output current is less than the 60mA peak to peak requirement. The gain at the switching frequency has to be less than 1.2*10^(-3).

$$\left|\frac{i_y}{i_x}\right| < \pi * 30mA/(4 * I_L) = 1.2 * 10^{-3}$$

Converting gain to db, we get the following

$$x\,dB < 10\,log(i_y/i_x) = -67.44\,dB$$

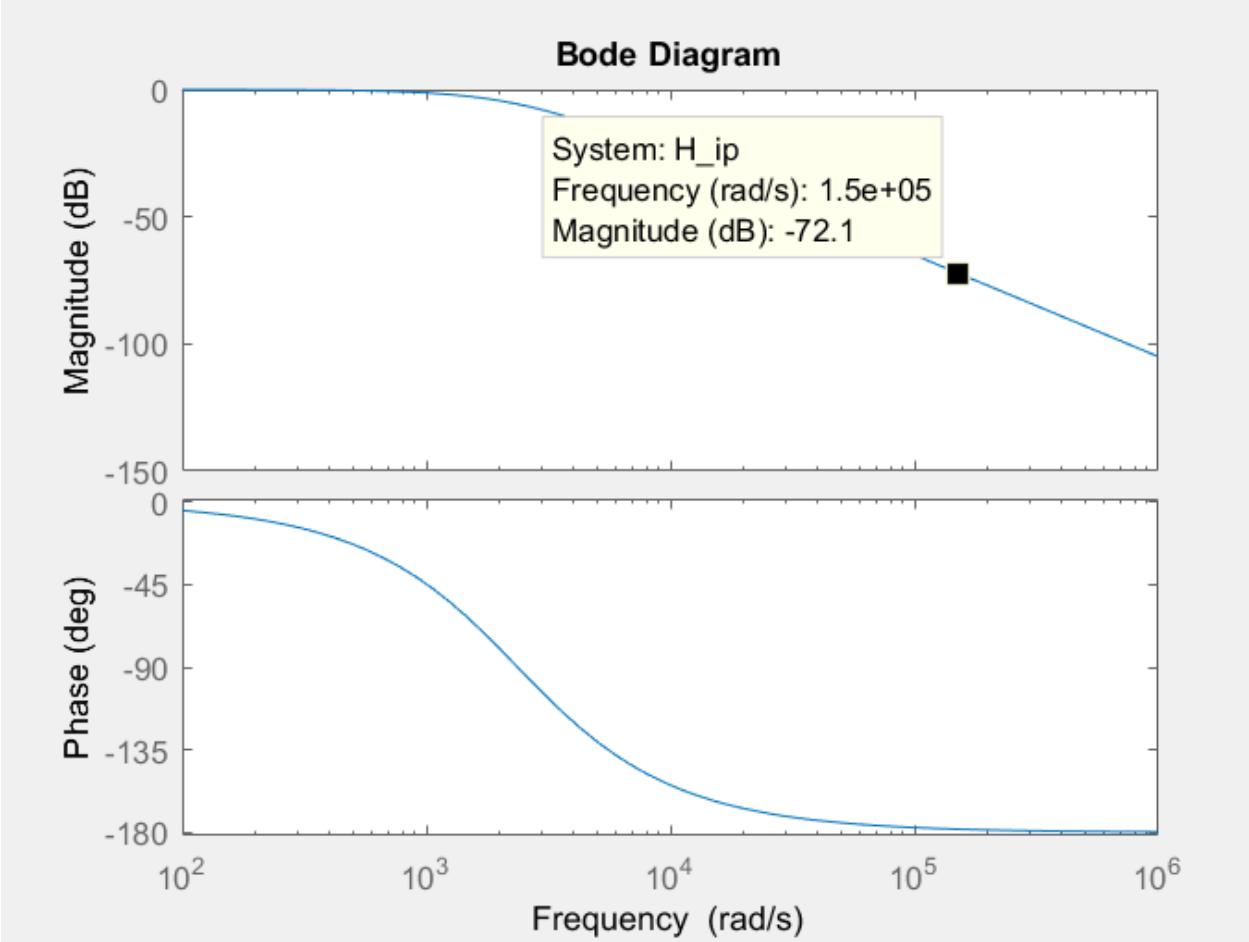
We also have to damp the filter so that we don't have a large gain at resonance. We can minimize the gain by choosing a damping resistance. The equation for gain at resonance is given by:

$$\left|\frac{i_y}{i_x}\right| = R_D\sqrt{\frac{C_f}{L_f}}$$

The damping capacitor C_d is in series with R_d, which we did not include in the circuit diagram above because it is large enough that we can assume it only blocks DC. The capacitor has to meet these requirements

$$C_D >> \frac{\sqrt{C_f L_f}}{R_D} \text{ and } C_D >> C_f$$

Choosing a value of L_f = 81uH, C_f = 2.2 mF, C_d = 10mF and R_d = .1 Ohms, we get a Gain of -72.1 dB at the switching frequency and a small peaking at the resonant frequency of the filter. C_d is around 5 times the size of C_f and meets its other requirements as well. With these values we can guarantee that the input current ripple is small enough to meet the design requirements.



The gain of -72.1 dB translates to a peak to peak current given below

$$i_y = i_x * 10^{(-72.1/10)} = 1.23\ uA$$

This satisfies the input current ripple requirement.

Input Inductor Design

Assuming we have a efficiency of 90%, we can calculate the input current. We can also approximate the peak input current by considering the maximum allowable input ripple.

V-in	P-out	P-in	I-in	I-in-peak
40	50	55.56	1.389	1.419

40	150	166.67	4.1667	4.197
27	50	55.56	2.0578	2.088
27	150	166.67	6.1730	6.103

The inductor chosen for the input filter is the RM-14 950um gap inductor with N = 18 turns. Like the power stage inductor, this inductor should satisfy all the previous constraints. Let's use a max current of 7 Amps in our calculations.

1. Core doesn't reach saturation

   The saturation flux density is .3 Teslas, minimum area of the core A_core = 168mm2 and a max current of 7 Amps was considered.

   $$N * B_{sat} * A_{core} > L\, i_{max}$$

   $$9.07 * 10^{-4} > 5.67 * 10^{-4}$$

   Saturation limit condition is satisfied

2. Inductance Calculation

   The inductance factor is 250 nH per turn

   $$L = A_L * N^2 = 81\, uH$$

3. Inductor Gap for Energy Storage

   The energy stored in the inductor has to be less than the amount of energy that can be stored in the inductor. The effective area of the core is 198 mm2 and effective length is 70 mm.

   $$\frac{B^2 A_c l_c}{2u_c u_0} + \frac{B^2 A_c l_g}{2u_0} > \frac{1}{2} L\, i_{max}^2$$

   $$247 > .002$$

   Energy storage condition satisfied

4. Winding Sizing

   We want to choose a wire size that allows 18 turns to fit inside the coil former and at the same time have a current density of less than 500 A/cm2. AWG 14 wire, which has a diameter of 1.628 mm and an area of .122 mm2 was chosen. The RM-14 has a coiler former with an area of 111 mm2 and winding width of 18 mm. The coil former can fit 18 turns.

   3. Current Density

      The current density has to be less than the max current density

      $$J < J_{max}$$

      $$I_{peak}/(N * A_{wire}) < 5 * 10^6\, Amps/m2$$

      $$A_{wire} > .0778\, mm^2$$

      .122 mm2 > .0778 mm2

4. Geometry
   The diameter of AWG 14 is 1.628 mm and the coil former is 18 mm by 6.1667 mm. We can fit 11 turns in the innermost layer and 7 turns to form the second layer. The coil former is larger enough to accomodate 10 turns of wire.

Input Capacitors Design

The inductors chosen for the circuit should have the required voltage rating. Here we choose the mentioned capacitors with a 50 V rating.
C_f is 2.2mF LXG50VN222M22X35T2 50 Volts .141 Ohms ESR
C_d is 10mF LXG50VN103M35X50T2 50 Volts .033 Ohms ESR
The capacitors must also satisfy the ripple current ratings. The ripple current at the input is a square wave going from 0 to the peak current. We will consider a peak current value of 20 Amps peak to peak.

$$Arms_{sq\ wave} = (1/2) * I_{pp} = 10 < Max_{Arms}$$

$$Max_{Arms} = 3.57\ @120Hz\ for\ C_d$$

$$Max_{Arms} = 1.33\ @120\ Hz\ for\ C_f$$

The datasheet doesn't give maximum ripple current at 150kHz. Provided capacitors don't satisfy all the requirements. Further searching needs to be done to find capacitors that meet all the design requirements.

Active Switch Design

The mosfet choice is important because it can have huge impacts on efficiency. The mosfet can burn energy through conduction losses, switching losses and parasitics losses. For now we will only consider the switching and conduction losses

$$P_{sw} = (1/2) * V_{dc} * I_{dc}(t_r + t_f)$$

$$P_{cond} = I_{dc}^{\ 2} * R_{DS(on)} * D$$

Power Out	V-in	AvgI_L	$I_{L\,peak}$	P_{sw}	P_{cond} @ 25^oC $R_{DS} = 12m$	P_{cond} @ $100C$ $R_{DS} = 20m$	Efficiency
150 W o/p	40 V	10 Amps	11.25 Amps	1.18 W	.5695 W	.9492 W	98.99%
50 W o/p	40 V	3.3 Amps	4.55 Amps	.4778 W	.0932 W	.1553 W	98.73%

150 W o/p	27 V	18 Amps	18.89 Amps	1.339 W	2.379 W	3.9648 W	96.46%
50 W o/p	27 V	6 Amps	6.89 Amps	.4882 W	.3165 W	.5275 W	97.97%

Temperature Considerations

We want to keep the junction temperature to be below 100 deg C. If the temperature is too high, then there would be more losses during switching and the mosfet can't operate at above 175 deg C.

The power dissipated the mosfet is 6.3448 Watts maximum over all considered operating conditions. The exposed pad on the mosfet is 4.057 by 4.56 mm which gives us an area of 18.5 mm2.

The thermal resistance from junction to ambient is given by the following equation

$\Theta_{j-a} \leq \frac{T_j - T_a}{P_{diss}} = \frac{100-50}{5.3438} = 9.4272^oC/W$

$\Theta_{j-a} \geq \Theta_{j-mb} + \Theta_{hs-a} = 1.4 + \Theta_{hs-a}$ where $\Theta_{j-mb} = \Theta_{j-c} + \Theta_{j-hs}$

If we choose a heat sink #22 from the AAVID Extruded heat sinks, then we get that

$\Theta_{hs-a} = \frac{0.7^oC}{W * 3\ in} * \frac{0.03927\ in}{1\ mm} * 4\ mm = 0.0367^oC/W$

$\Theta_{j-a} = 9.4272 \geq \Theta_{j-mb} + \Theta_{hs-a} = 1.4367$ Satisfies

Heat sink: 4 mm of #22 extruded heat sink from AAVID. $0.0367^oC/W$

Mounting Board: As specified in the datasheet. Surface Mounted FR4 board using 650mm2 2oz Cu pad

The calculation of junction temperature at different operating conditions is shown below. This was calculated using this equation. Since the junction temperature will be lower if ambient temperature is lower, we are only considering the condition where the ambient temperature is at the maximum value of 50 deg C.

$T_j = T_a + \Theta_{j-a} * P_{loss}$

Power Out	V-in	AvgI_L	$I_{L\,peak}$	P_{sw}	P_{cond}@ $100C$ $R_{DS} = 20m$	P_{loss}	Junction Temp Celsius
150 W o/p	40 V	10 Amps	11.25 Amps	1.18 W	.9492 W	2.13 W	53.062
50 W o/p	40 V	3.3 Amps	4.55 Amps	.4778 W	.1553 W	0.63 W	50.9051

150 W o/p	27 V	18 Amps	18.89 Amps	1.339 W	3.9648 W	5.30 W	57.6145
50 W o/p	27 V	6 Amps	6.89 Amps	.4882 W	.5275 W	1.10 W	51.5804

We wanted to keep the junction temperature below 100 deg C to be within the safe operating condition of the mosfet and so that our approximation of the drain source resistance is correct. The above calculations show that the mosfet does operate below 100 deg C during all considered operating conditions.

Maximum operating temperature of the converter can be calculated considering that the junction temp of the mosfet ranges between -55 to 175 deg C. We can cap the temp at 100 deg C.
Maximum operating temp: $T_a - \Theta_{j-a} * P_{loss} with\, T_a being\, 100$ =92.38 deg C
Minimum operating temp: $T_a - \Theta_{j-a} * P_{loss} with\, T_a being\, -30 = -27.61 > -55\, deg\, C$
The converter is safe to operate between -30 and 90 deg C.

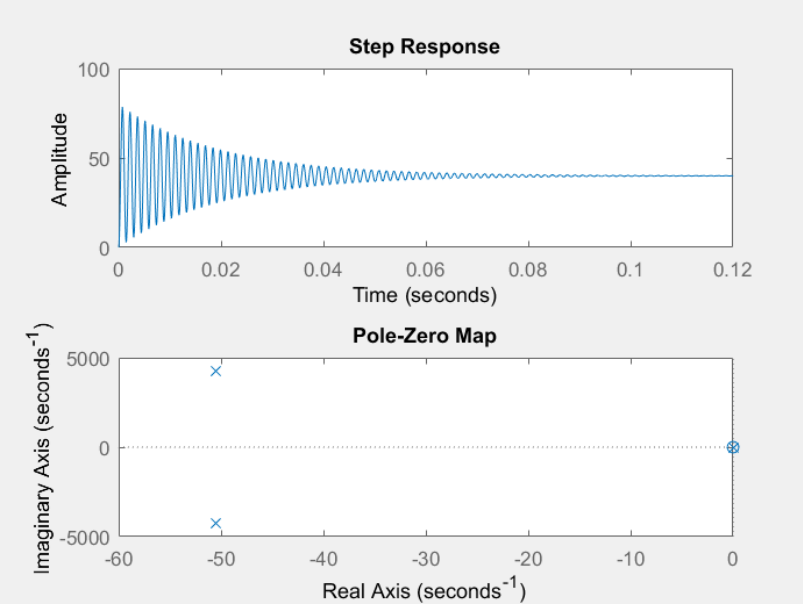
Control Design

The small signal averaged duty cycle to Vout transfer function is given below, along with the poles of the system.

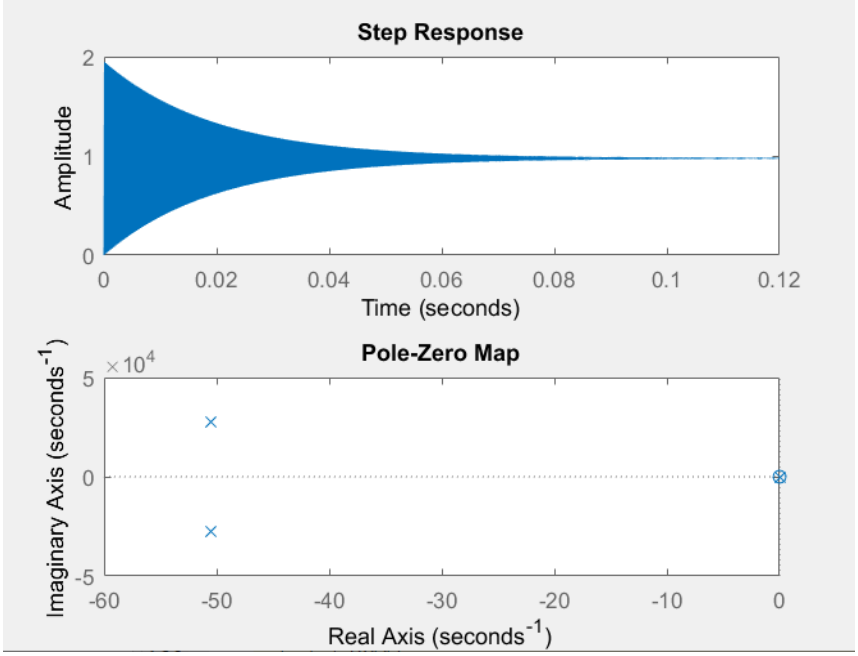
$$\frac{\widehat{V_{out}}}{\widehat{d}} = \left(\frac{V_{in}}{LC}\right) * 1/\left(s^2 + s\left(\frac{1}{RC}\right) + \frac{1}{LC}\right)$$

$$p_{1,2} = (1/2) * \left((-1/RC) \pm \sqrt{(1/(RC))^2 - 4/(LC)} \right)$$

The open loop response of the system along with its pole zero map is shown below. We can see that the open loop response is stable but has a lot of oscillations. Also the output settles at 40 times the desired steady state. The imaginary part of the poles are too large, which causes the large oscillations.

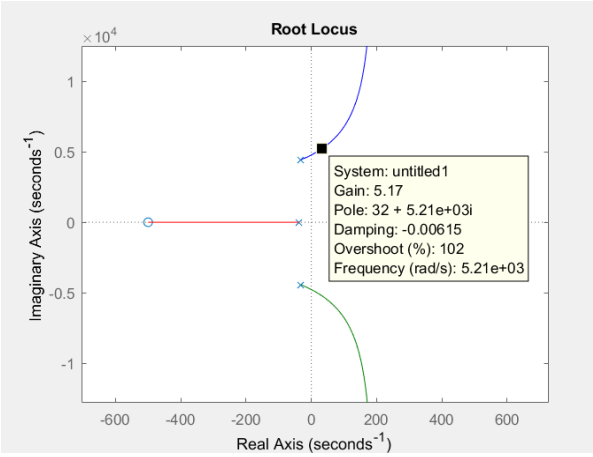


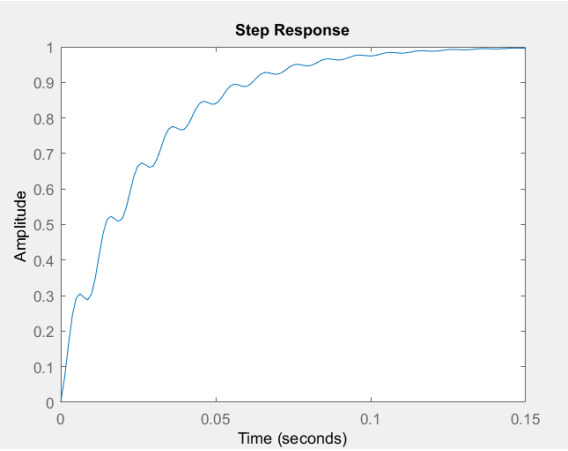
The controller design will involve using the output voltage as feedback to control the duty cycle. The step response and pole zero map of the system in feedback with a unity compensator is shown.



PI Control

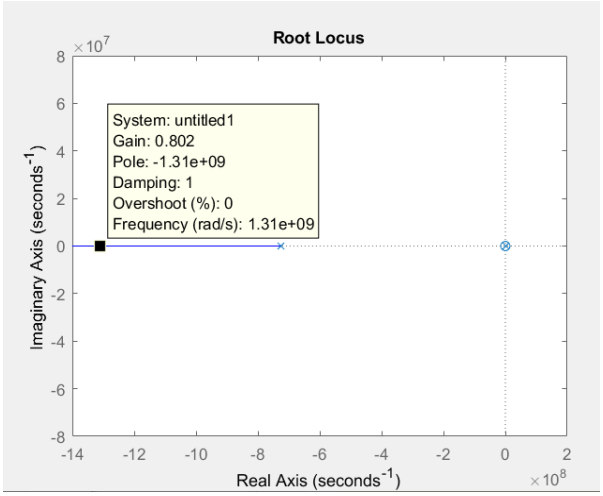
A PI controller was first used to control the system. The root locus plot shows that with the right values for the gains, the poles of the system do exist in the left half plane. However, large enough gains will cause the system to be unstable. Compared to unity feedback and open loop response, the imaginary part of the poles are much smaller, causing there to be much less oscillations. However, there is still some oscillation and overshoot.
PI Control: Kp = 0.002 Ki = 1

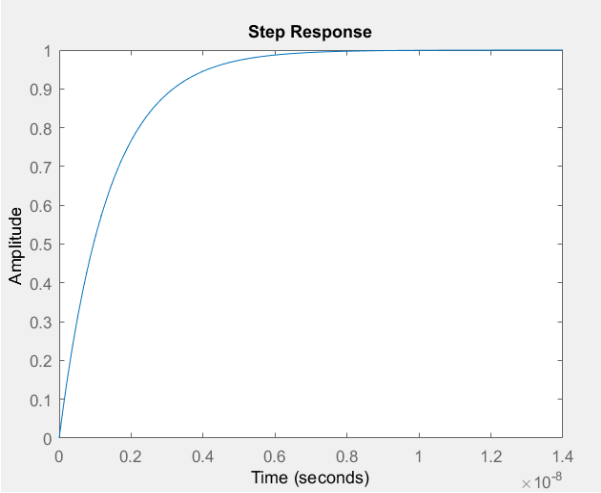




PID Control

Next I tried using a PID controller and the same plots are shown below. The poles lie on the real axis, meaning that there are no oscillations. The overshoot is 0% and the system reaches steady state in around 10 nanoseconds, which is fast, much smaller than our switching frequency. This means that the controller can reach the desired output voltage due to steps in output loading in very few switching cycles, making our controller fast and robust.
PID Controller: Kp = 0.002 Ki = 1 Kd = 1





The results show that the PID controller works as a reasonable compensator for the system. The output returns 0% overshoot, meaning that the output voltage of the buck converter is reliably centered at 15 V based on this simplified model. With a 0% overshoot, the transient response easily falls between 1 Volt of the desired output. We can rate this to produce an output voltage 14-15 V.