Logic Usage Cost

 ${\bf Dan~Gisselquist,~Ph.D.}$ 

 $\mathrm{June}\ 18,\ 2022$ 

	iCE40	Xilinx 7
ZipBones	4-LUTs	6-LUTs
ASM	1114	581
Trap	1655	962
Minimum	2691	1456
Pipelined	3578	1983
Cached	5407	3217
Low power	5381	3167

	iCE40	Xilinx 7
ZipSystem	4-LUTs	6-LUTs
ASM	3358	1652
Trap	4037	2209
Minimum	5157	2678
Pipelined	6348	3431
Cached	8089	4507
Low power	8126	4539

	iCE40	Xilinx 7
ZipAXI-Lite	4-LUTs	6-LUTs
ASM	1477	876
Trap	2124	1161
Minimum	3166	1669
Pipelined	4193	2322

	iCE40	Xilinx 7
ZipAXI	4-LUTs	6-LUTs
ASM	1471	878
Trap	2042	1228
Minimum	3116	1702
Pipelined	4181	2250
Cached	5225	2908
Low power	5362	3060

Bus, 6-Luts	Wishbone	AXI4-Lite	AXI4
Minimum	1456	1669	1701
Pipelined	1983	2322	2250
4kB Caches, I+D	3217		2908
Low power option	3167		3060