Digital Integrated Circuit Design
HW-5: Modified Booth's Radix-4 Multiplier

Problem:

Design a modified Booth's radix-4 multiplier that is composed of booth encoder and CSA tree. The multiplication performs the 8×8 operation $W=X\times Y$. All of W, X and Y are 8-bit 2's complement. The block diagram of the modified Booth's radix-4 multiplier is illustrated as follows,

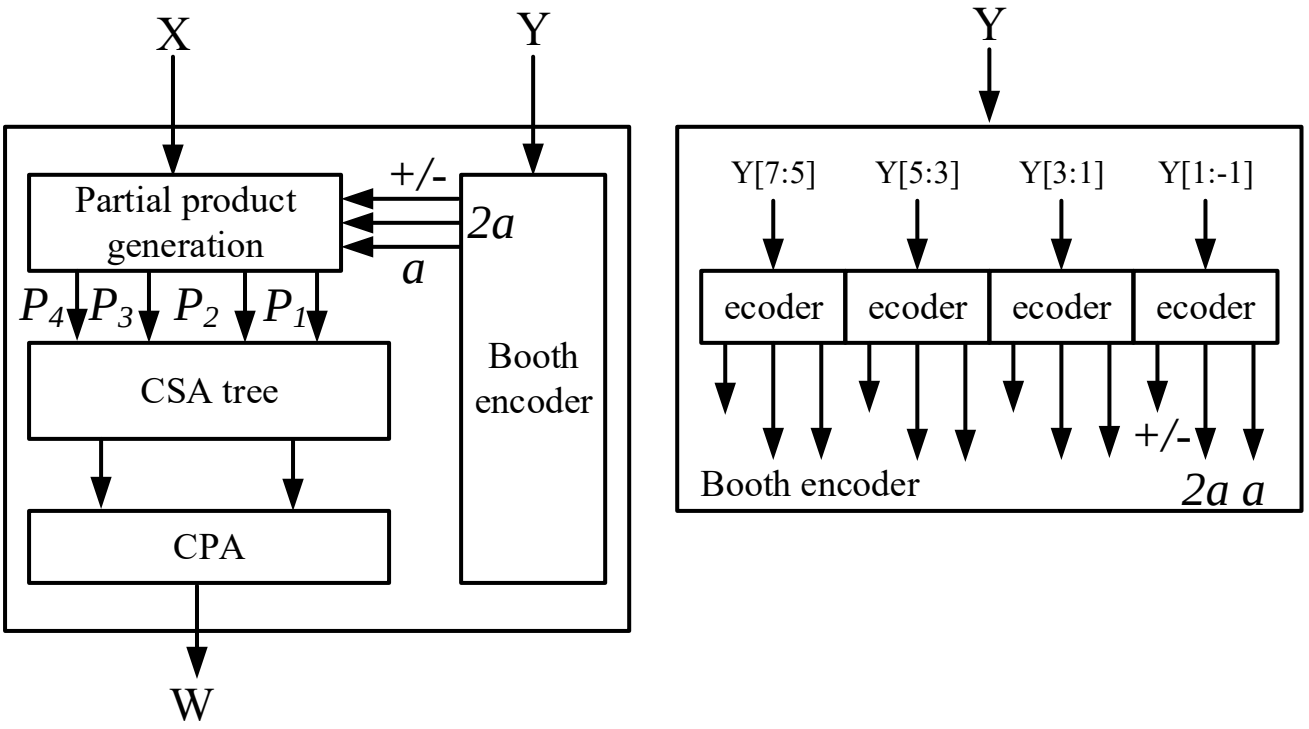

Fig. Block diagram of Booth's radix-4 multiplier

Both HA- and FA-RTL codes will be uploaded to E-learning for constructing your CSA tree and CPA. All of **data-flow** constructions have **delay time** of 1-ns, which is demonstrated as follows,

```
`timescale 1 ns/1 ps
`define DLY 1
:
assign `DLY Ax = …;
:
```

Submission

1. Please submit the following files to E-learning.
   - **(a) B123456_HW5_BoothMUL_rtl.v**: It is your 8x8 Booth multiplier, which may include **CSA**, **CPA**, **BoothEncoder**, etc.
   - **(b) B123456_HW5_BoothEncoder_rtl.v**: 3-bit Booth encoder.
   - **(c) B123456_HW5_BoothMUL_rtb.v**: A testbench for you top-module design
   - **(d) Report timing, area, power and reference**
   - **(e) Post-sim (gate-level simulation) using .sdf**
2. Please deliver the simulation results and the circuit diagrams of your design (.docx) in class.

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(a) For the simulation results, please attach the related photos (.jpg or pdf) in .docx.

(b) For the circuit diagrams, please sketch it using VISIO (.vsdx) or pen and then scan it (.jpg or .pdf). After that, please paste the circuit diagram in .docx.