Logic Synthesis with Design Compiler

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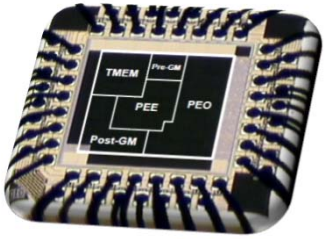
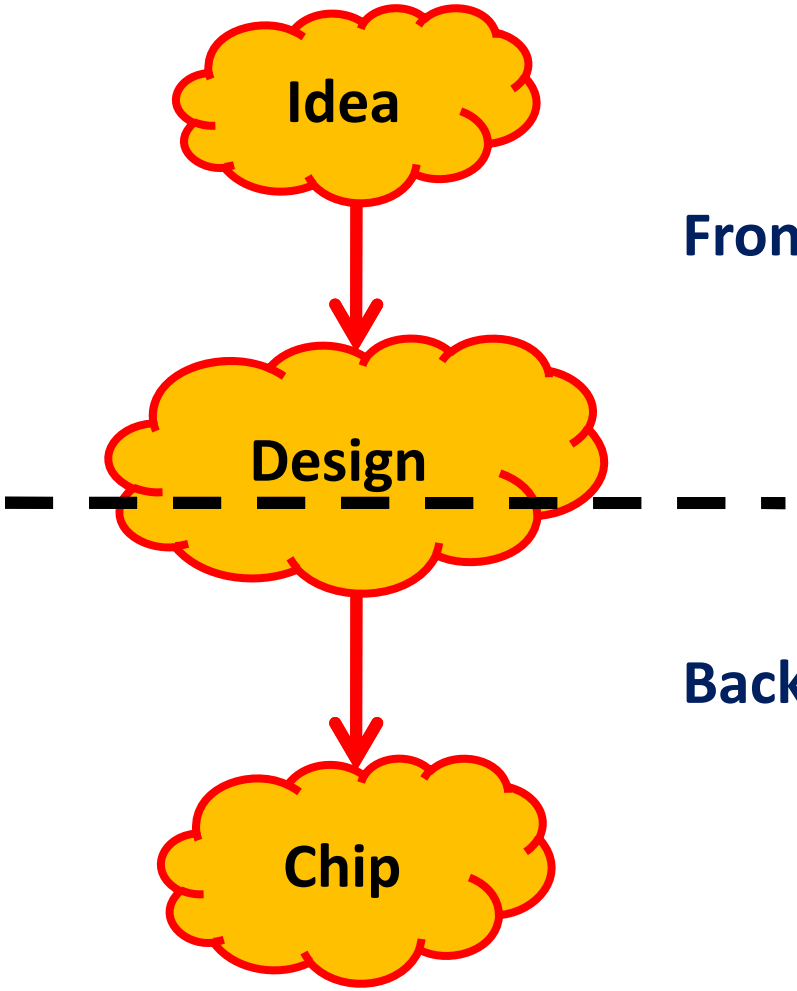


Cell-based Design Flow



Front-end

- **Front-end**
  - System partitioning
  - Design entry: HDL/Schematic
  - Logic synthesis
  - Pre-layout simulation

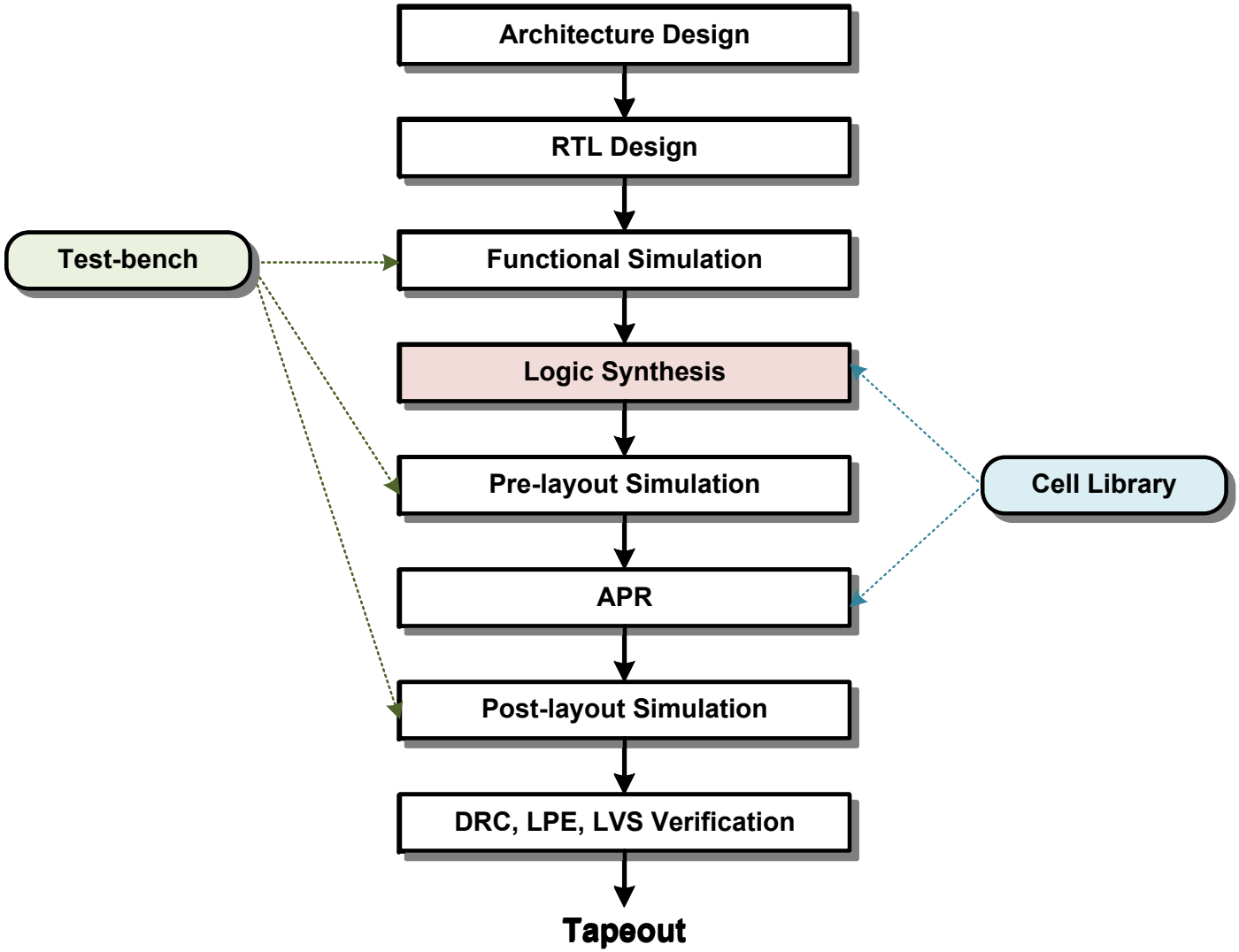
Back-end

- **Back-end**
  - Floor plan
  - Placement
  - Routing
  - Extraction
  - Post-layout simulation

References

- ***Logic Synthesis with Design Compiler***, **CIC Training Manual.**
- ***Handout of Introduction to Integrated Circuits Design***, **T.-Y. Chang, EE, NTHU.**
- ***Larc Synthesis Course***, **EE, NTHU.**

Cell-based Design Flow

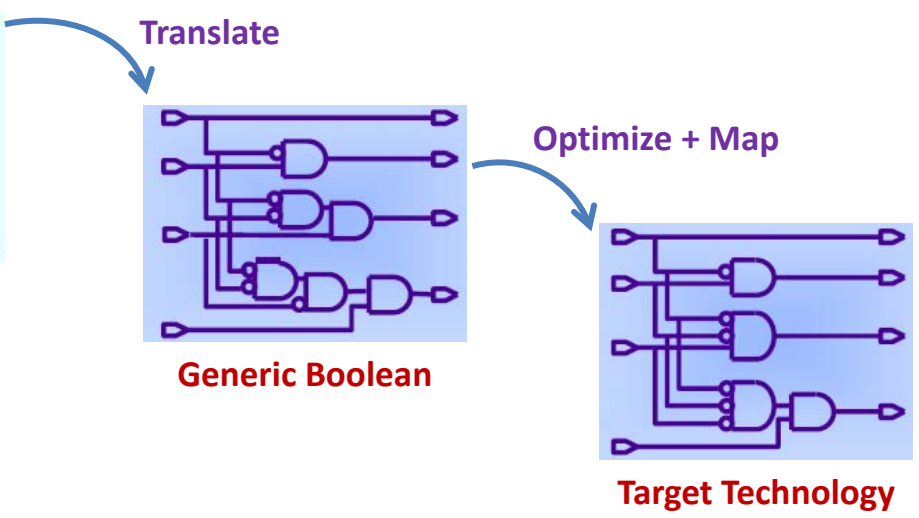


Synthesis

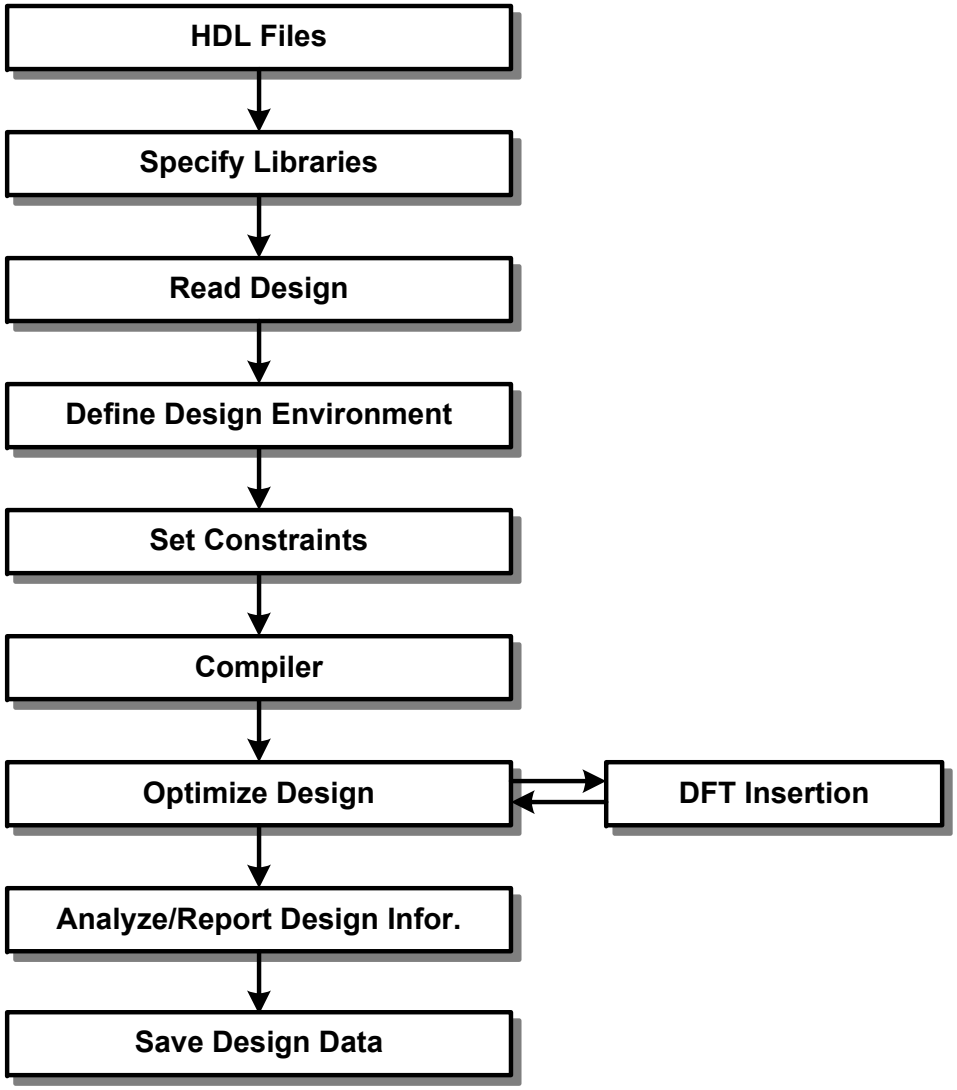
- **Convert a high-level RTL into an optimized gate-level netlist.**
  - Standard cell library *Provide from Fab., such TSMC or UMC*
  - Constraints
  - Translation + Optimization + Mapping

```
residue = 16'h0000;
if (high_bits == 2'b10)
      residue = state_table[index];
else  state_table[index] = 16'h0000;
```

RTL code



Basic Synthesis Flow



Getting Start

- **Setup file**
  - Put .synopsys_dc.setup in your local home directory
  - $HOME/.synopsys_dc.setup

- **Start design compiler**
  - **dv**
  - **design_vision-xg**
  - **dc_shell-xg-t** (script mode)

.synopsys_dc.setup File

```
set designer  "Yuan-Ho Chen"
set company " ICLab. ELE. CGU."

set search_path “~/../tech/Synth/ $search_path"
set link_library "* slow.db fast.db dw_foundation.sldb"
set target_library "slow.db fast.db"
set symbol_library "generic.sdb"
set synthetic_library "dw_foundation.sldb"

set verilogout_no_tri true
set sh_enable_line_editing true
set sh_line_editing_mode emacs
history keep 100
alias h history
```

Design Objects

```
module Top(a, b, c, clk, dout);
   input    a, b, c, clk;
   output   dout;

    wire    din;

    ADDER  U1(.Ain(a), .Bin(b), .Cin(c), .S(din));
    DFF    U2(.clk(clk), .D(din), .Q(dout));

endmodule
```

design

clock

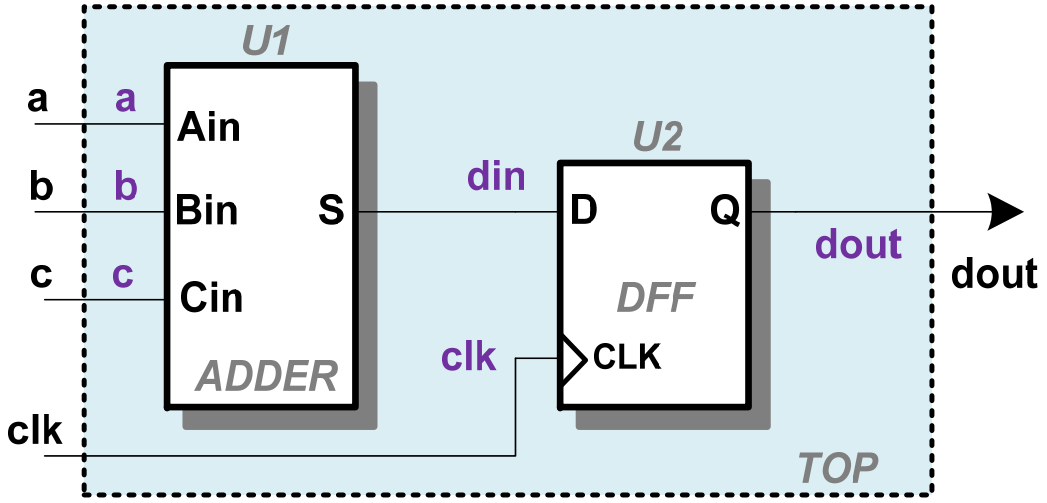
port

net

pin

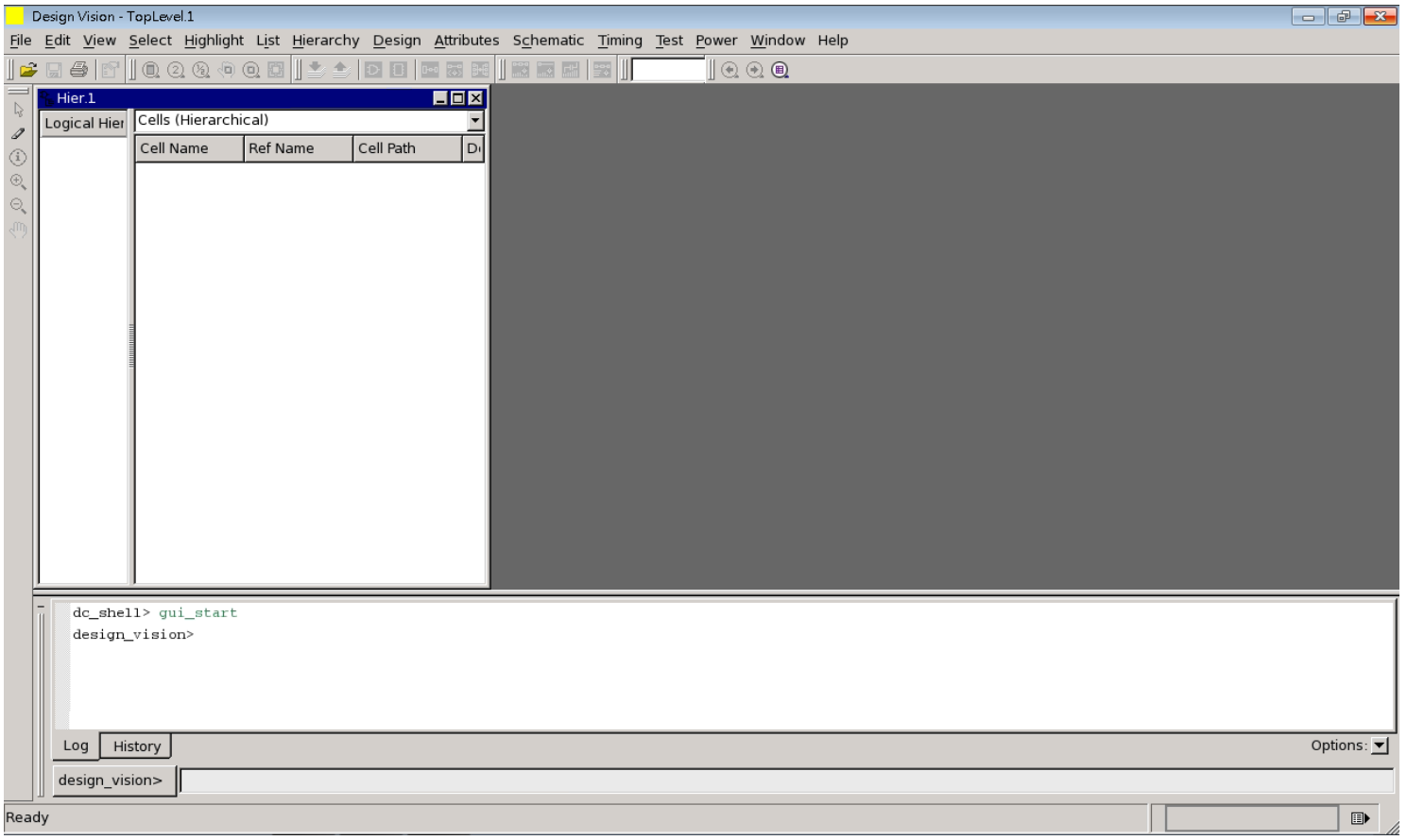
cell

reference

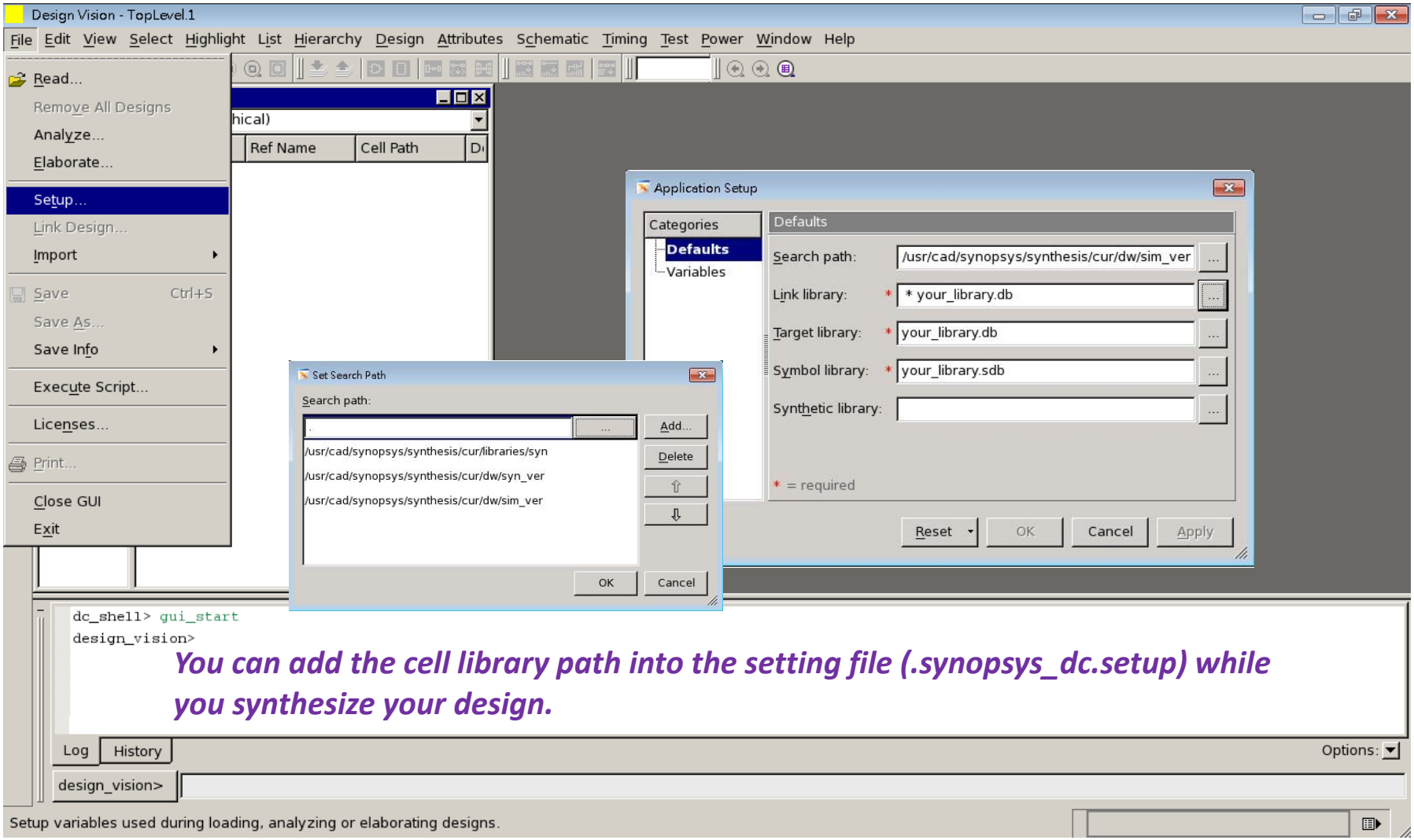


Invoke Design Compiler

- **%> design_vision-xg**
- **%> dv**

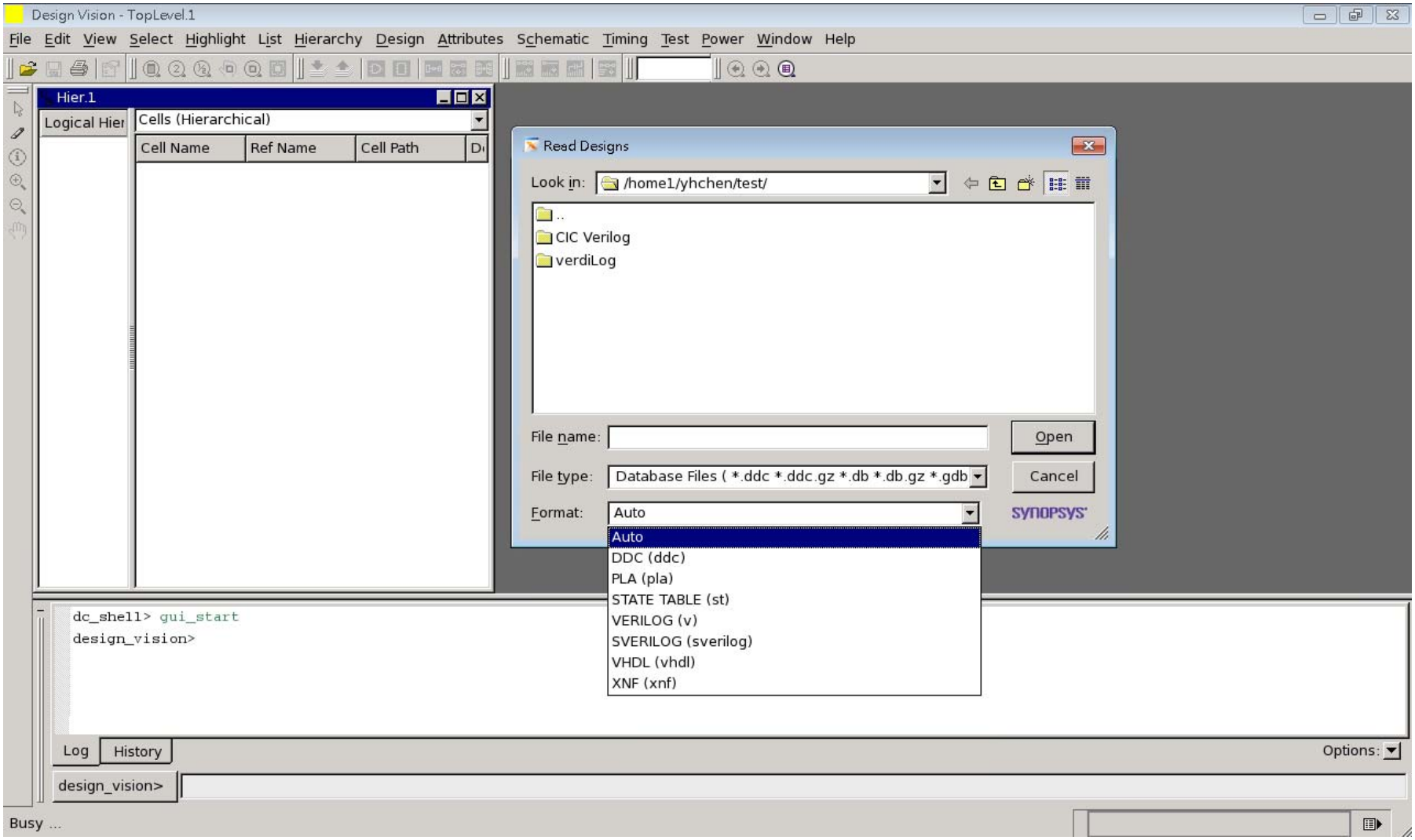


Add Cell Library Path

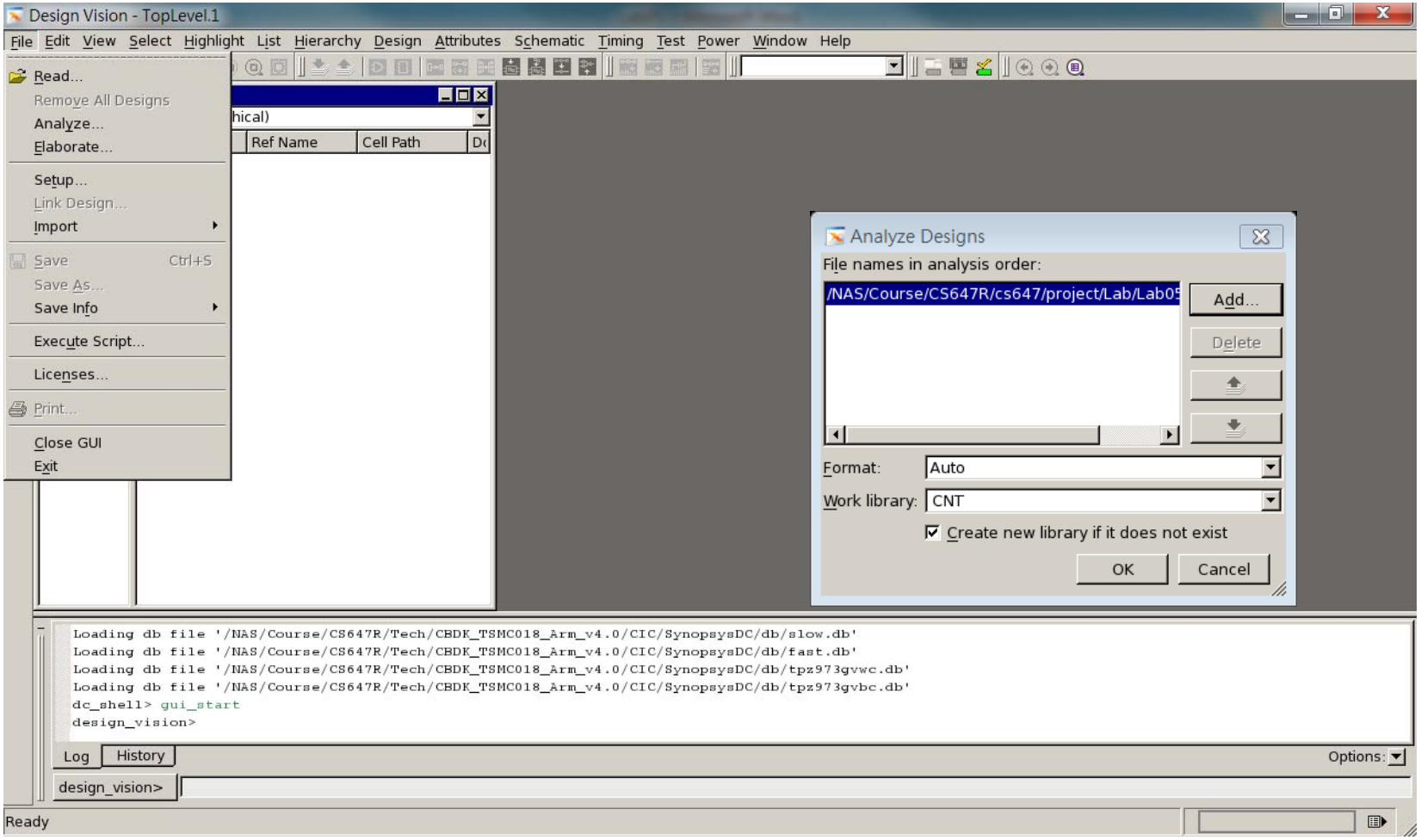


You can add the cell library path into the setting file (.synopsys_dc.setup) while you synthesize your design.

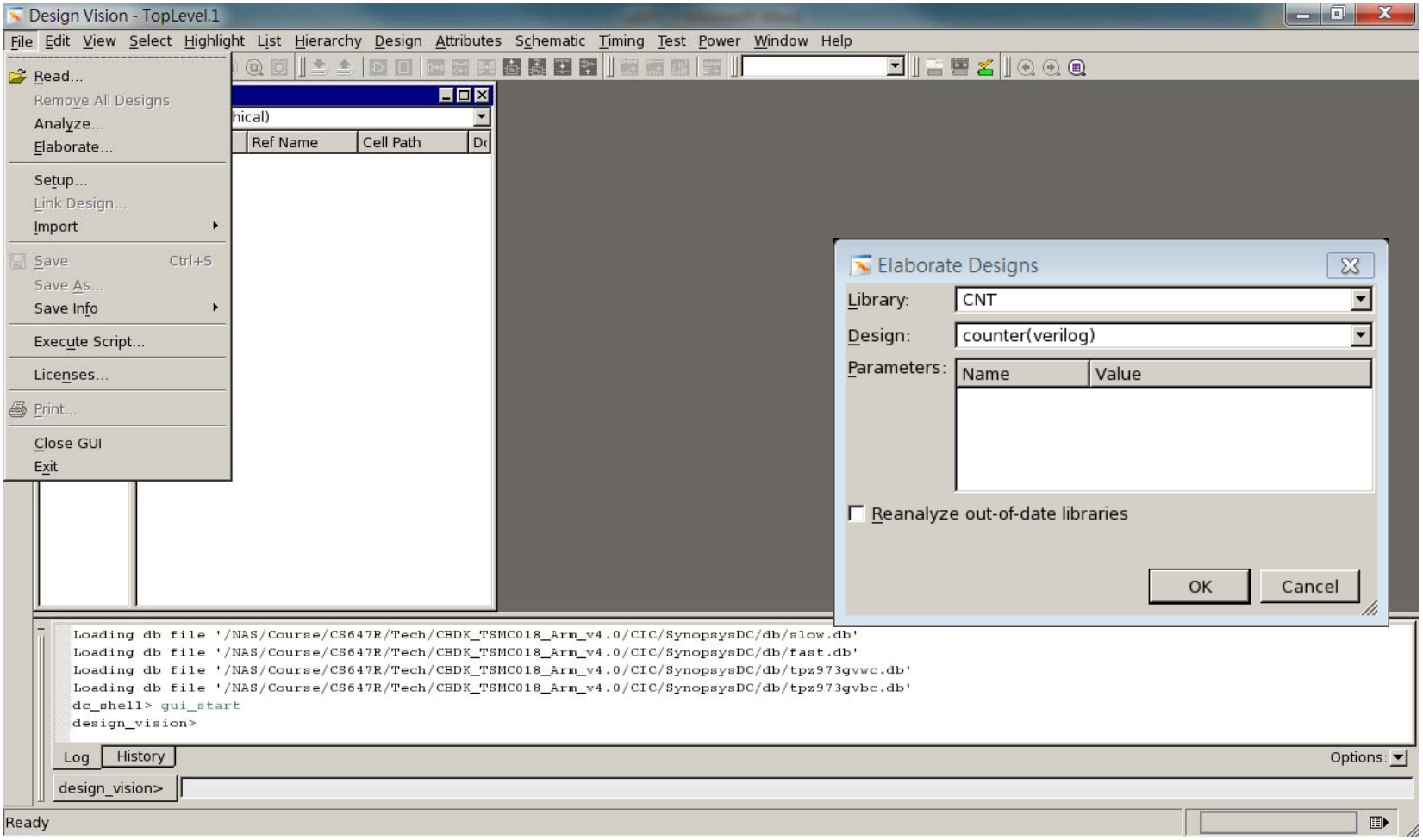
Read Design – Method 1: Read File



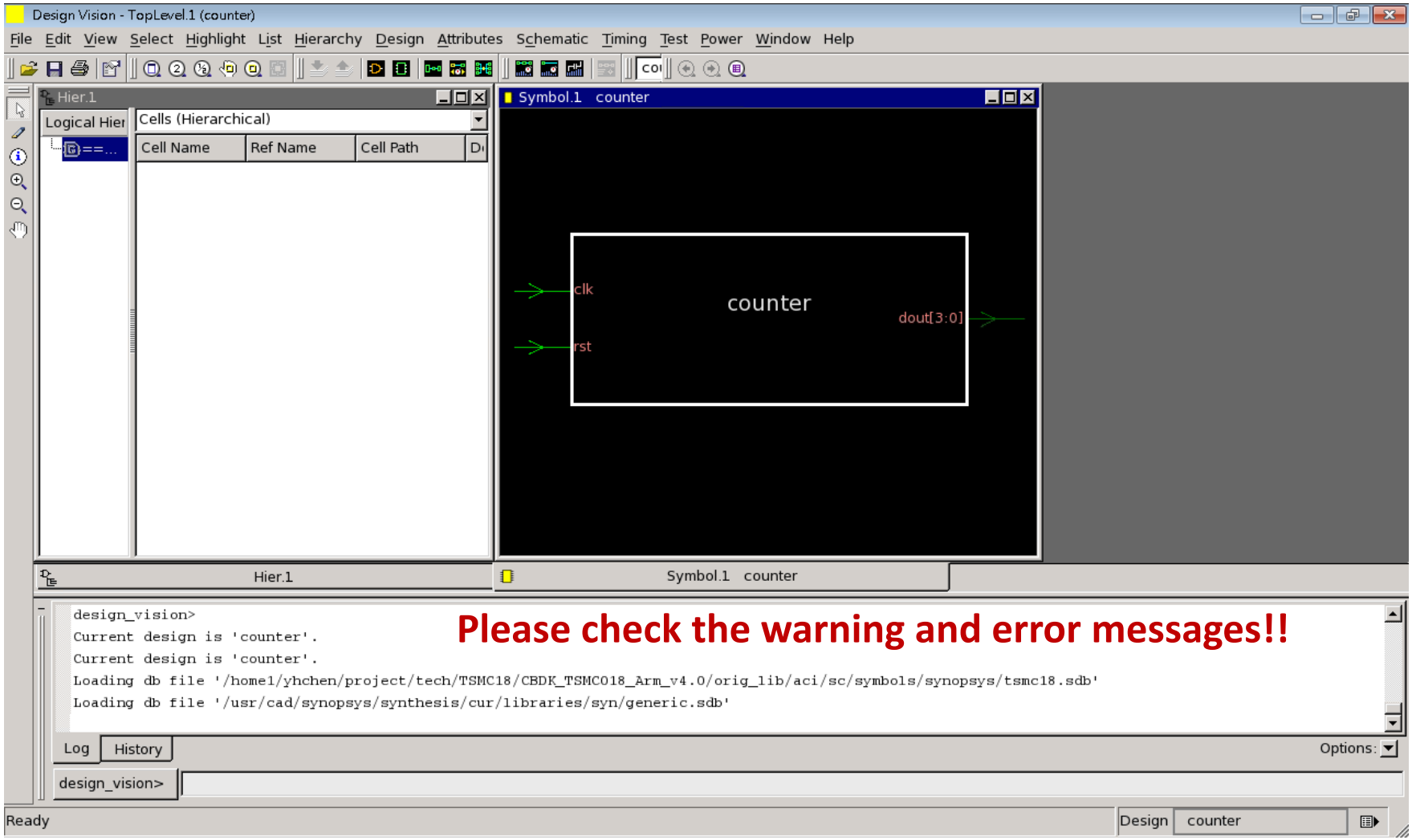
Read Design – Method 2: Analyze



Read Design – Method 2: Elaborate



Read Design

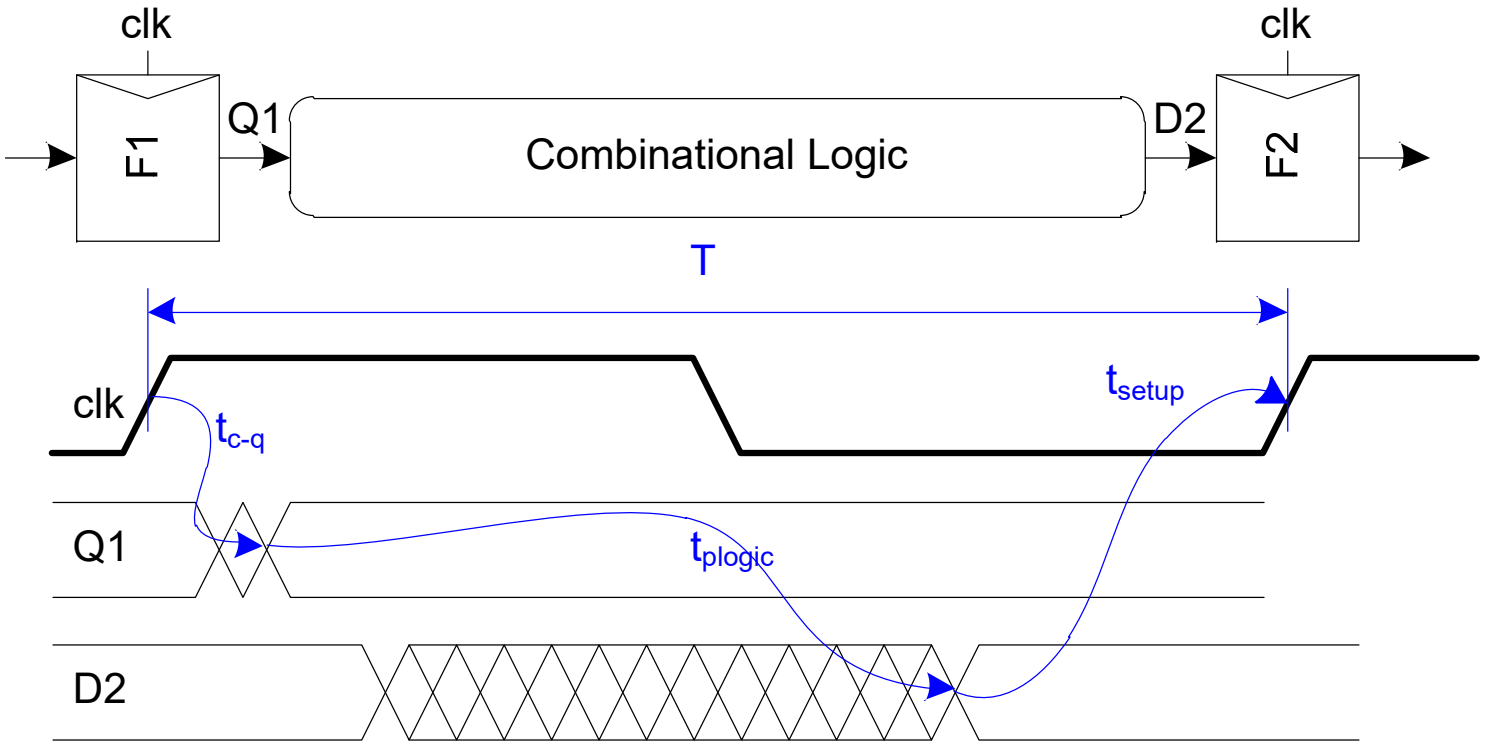

Design Vision - TopLevel.1 (counter)
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help
Hier.1
Logical Hier
Cells (Hierarchical)
Cell Name
Ref Name
Cell Path
Symbol.1 counter
clk
rst
counter
dout[3:0]
Hier.1
Symbol.1 counter
design_vision>
Current design is 'counter'.
Current design is 'counter'.
Loading db file '/home1/yhchen/project/tech/TSMC18/CBDK_TSMC018_Arm_v4.0/orig_lib/aci/sc/symbols/synopsys/tsmc18.sdb'
Loading db file '/usr/cad/synopsys/synthesis/cur/libraries/syn/generic.sdb'
Please check the warning and error messages!!
Log
History
Options:
design_vision>
Ready
Design
counter

Setting Design Environment

- **Operation condition**
- **Input driving strength**
- **Output loading**
- **Input/output delay**
- **Wire load model**

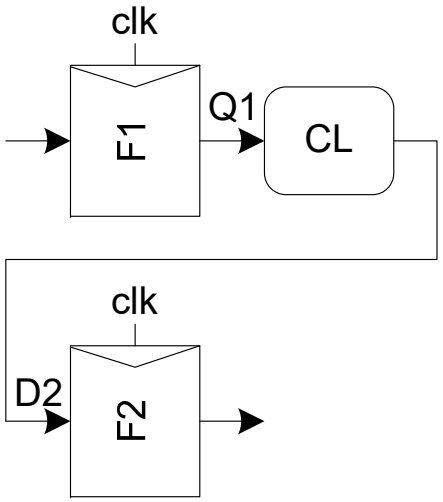
Setup Time → Max. Delay

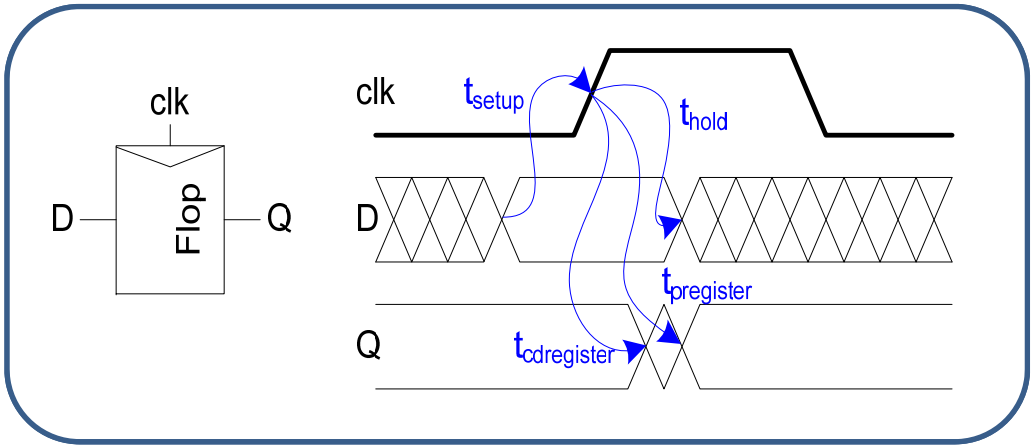
$$t_{plogic} \le T - \underbrace{\left(t_{\text{setup}} + t_{c-q}\right)}_{\text{sequencing overhead}}$$

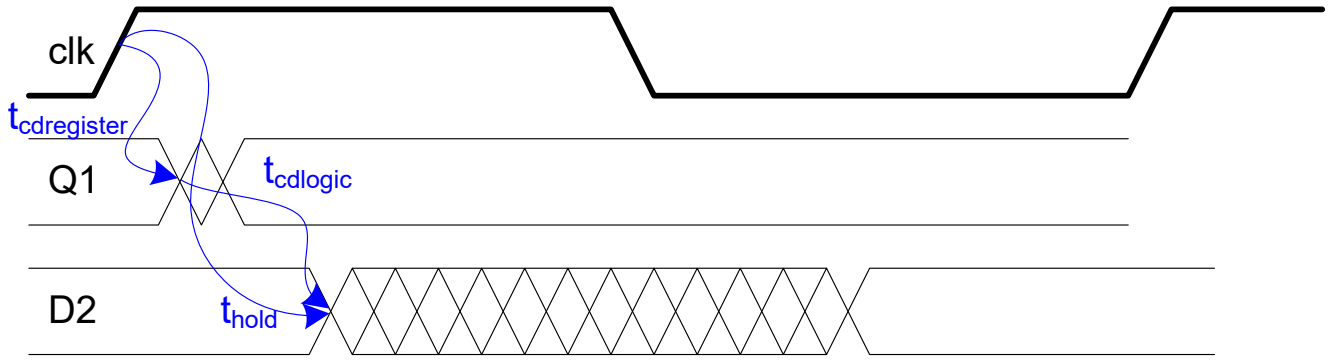


Hold Time → Min. Delay

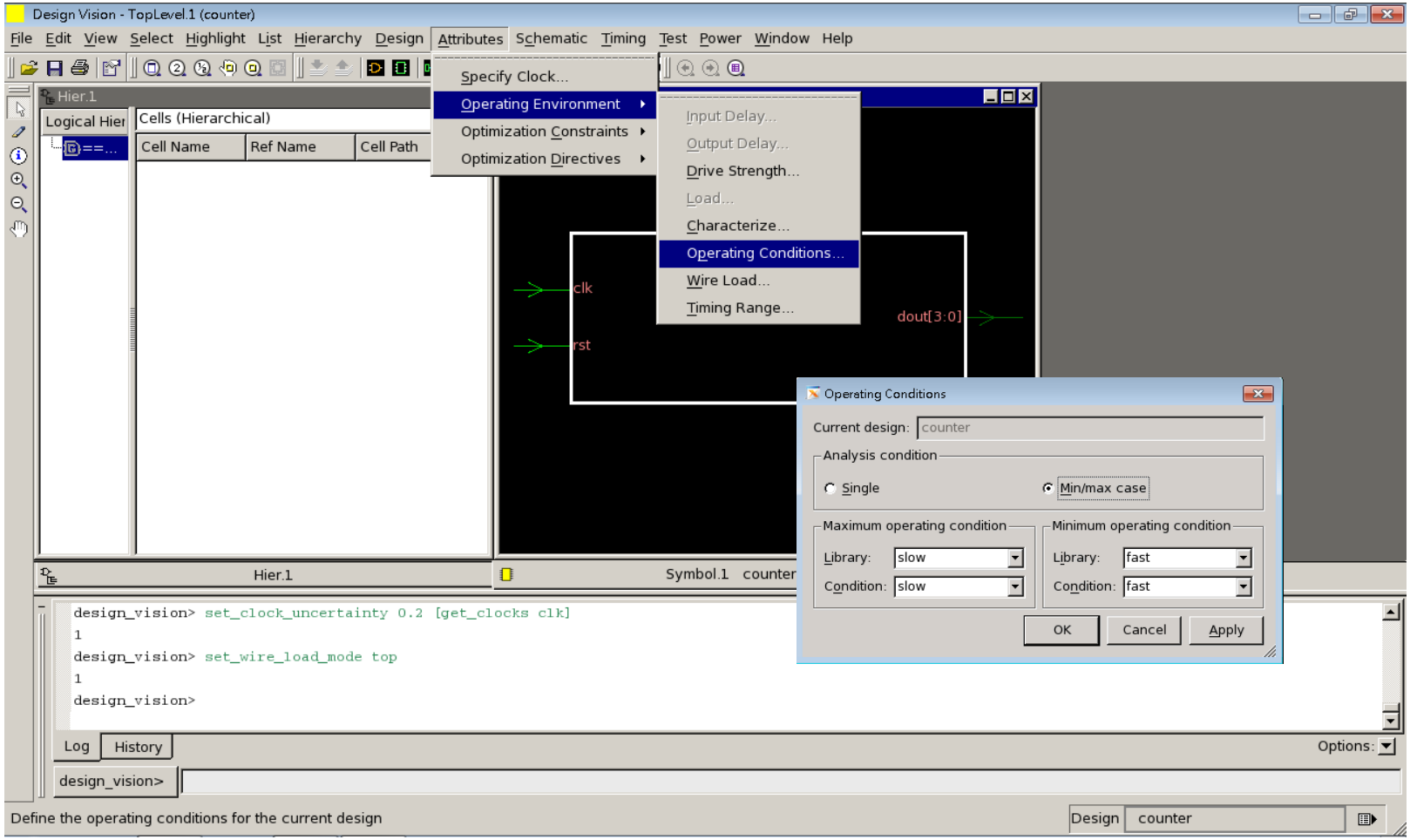
$$t_{cd\,\log ic} \geq t_{\text{hold}} - t_{cdregister}$$







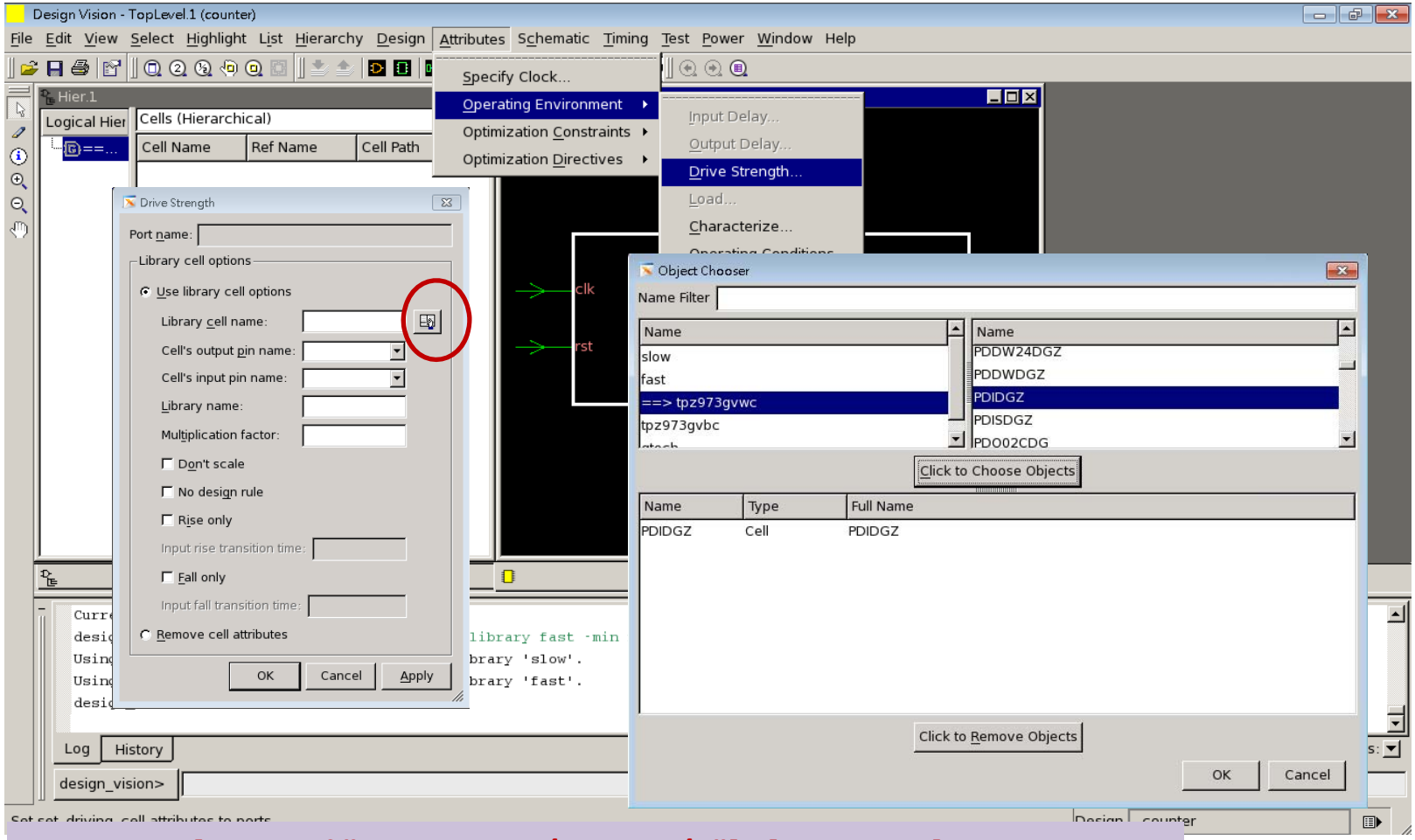
Operation Condition



Max. → setup time check

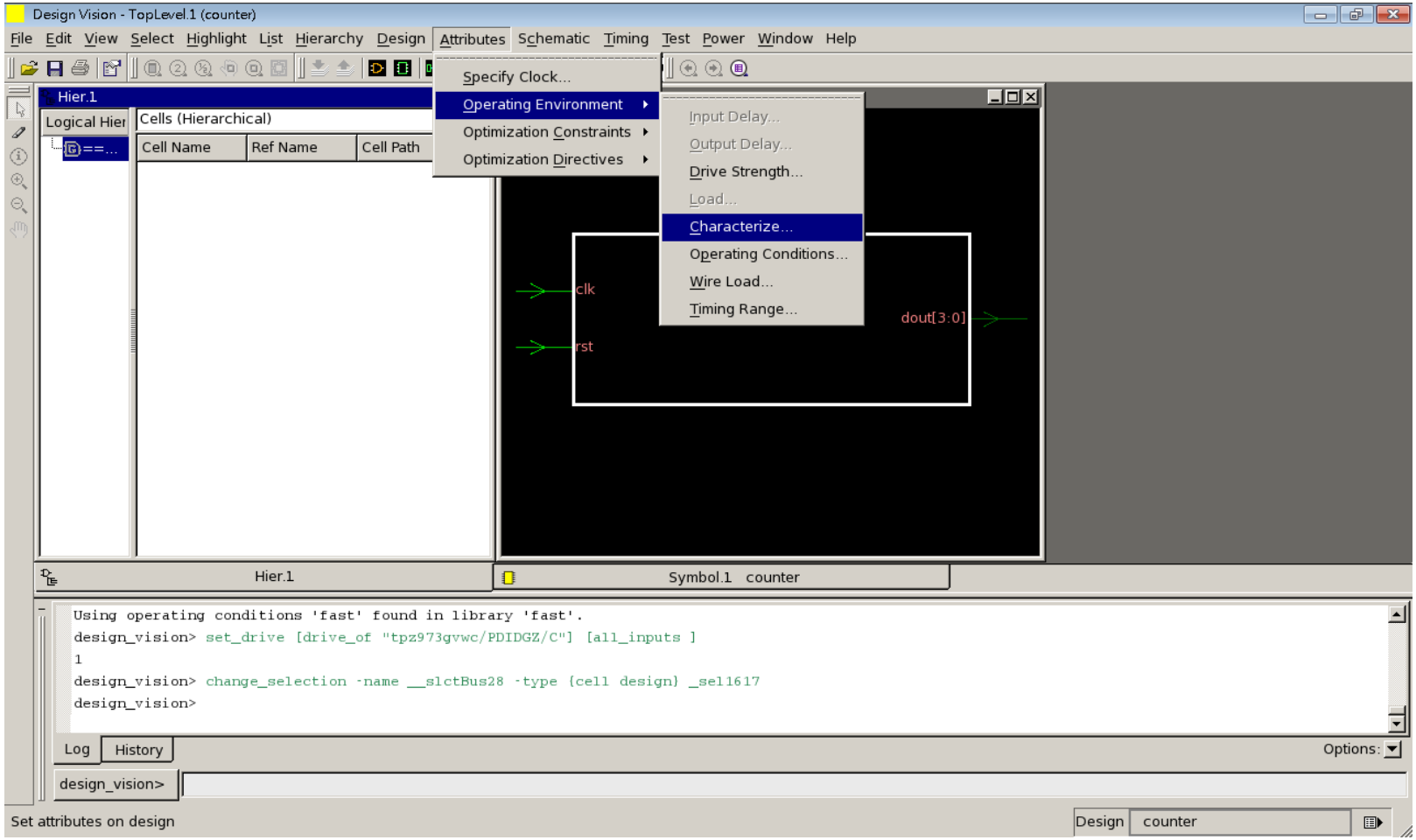
Min. → hold time check

Input Driving Strength



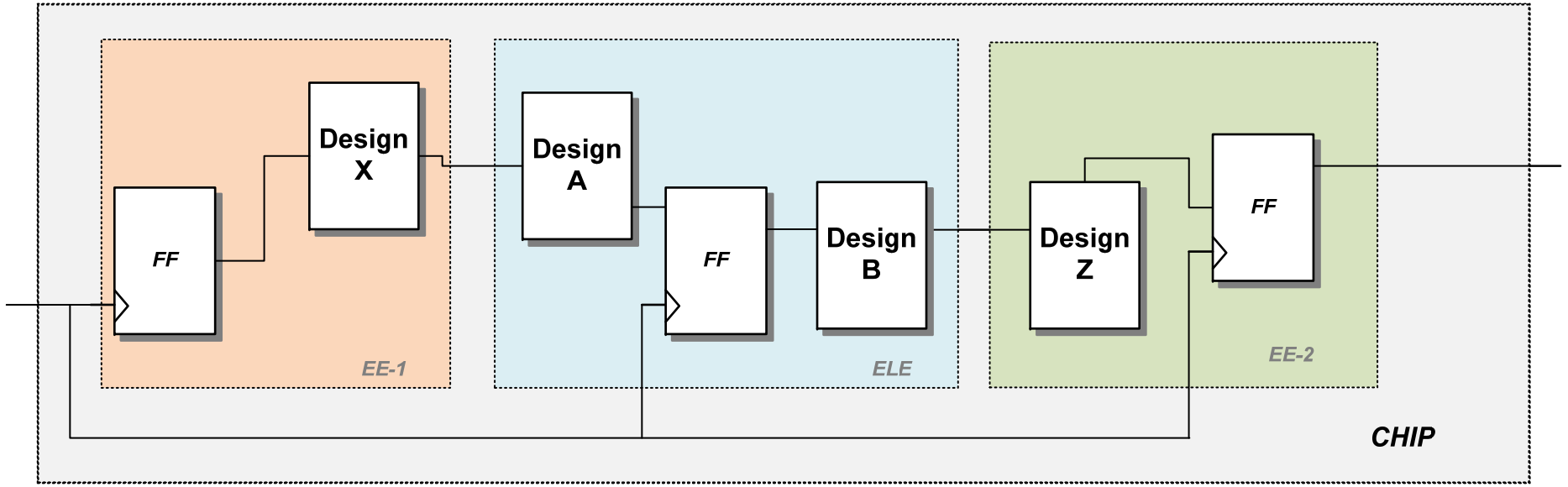

```
set_drive   [drive_of "tpz973gvwc/PDIDGZ/C"]   [all_inputs]
set_driving_cell -library tpz973gvwc -lib_cell PDIDGZ -pin {C} [all_inputs ]
```

Output Loading



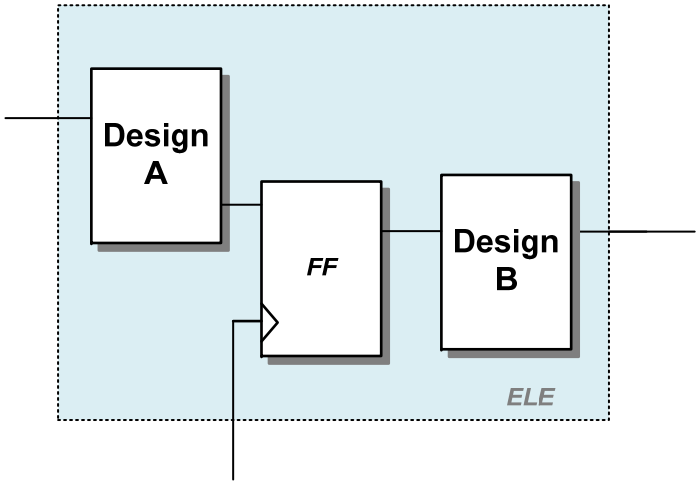

```
set_load [load_of "tpz973gvwc/PDO08CDG/I"] [all_outputs ]
```

Input/output Delay



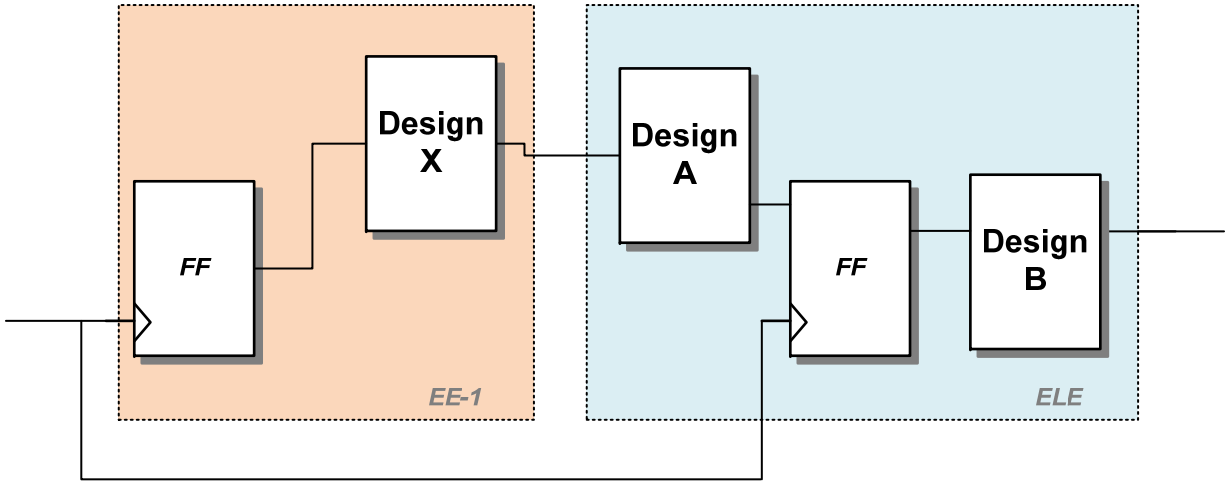
Clock Frequency

- $T = \max(T_A + T_{ff\text{-}w}, T_{ff\text{-}r} + T_B)$



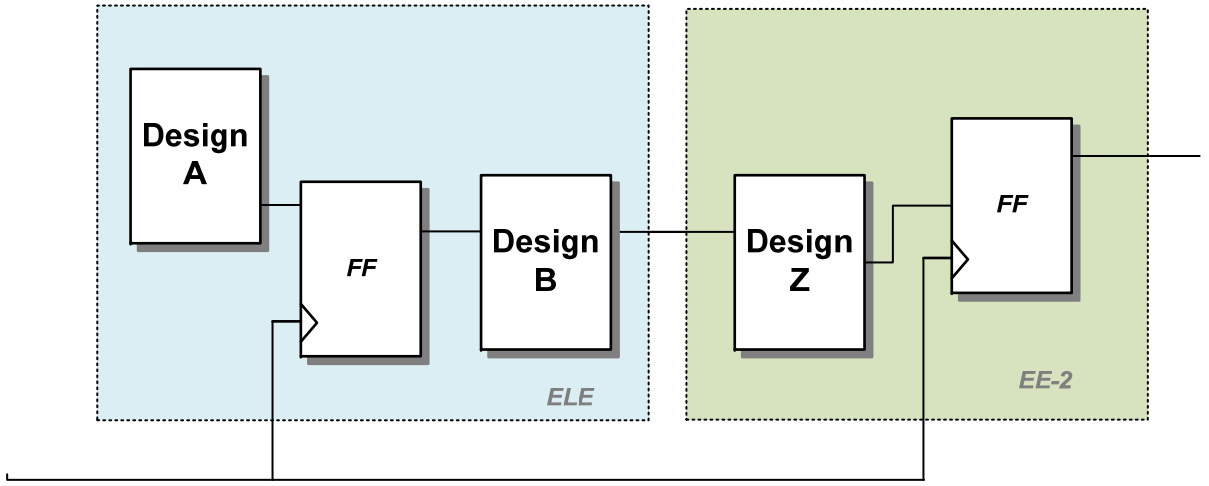
Input Delay

- EE-1: $T_{ff\text{-}r} + T_X$
- $T = T_{ff\text{-}r} + T_X + T_A + T_{ff\text{-}w}$
- **Input Delay = $T_{ff\text{-}r} + T_X$**

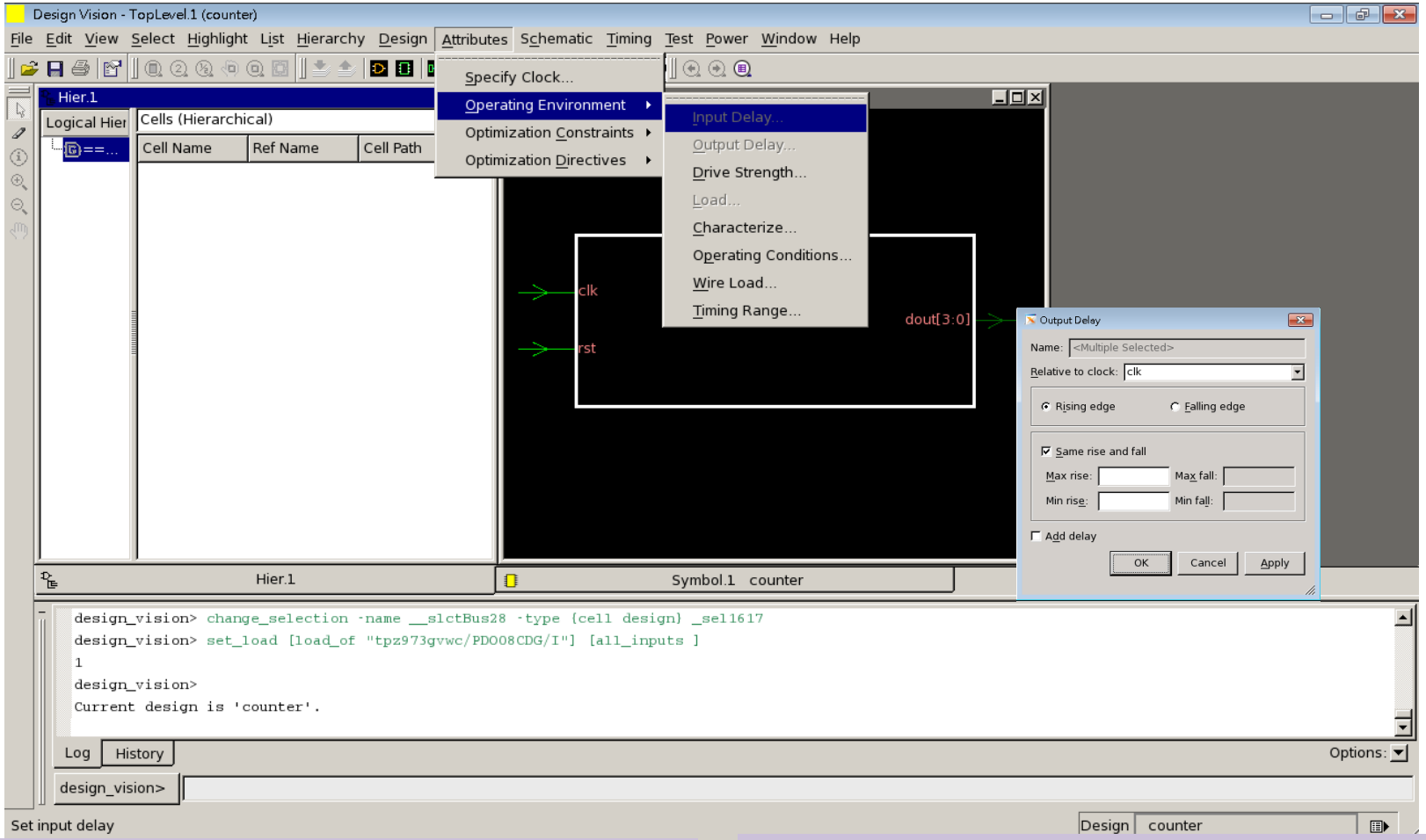


Output Delay

- EE-2: $T_Z + T_{ff\text{-}w}$
- $T = T_{ff\text{-}r} + T_B + T_Z + T_{ff\text{-}w}$
- **Output Delay = $T_Z + T_{ff\text{-}w}$**



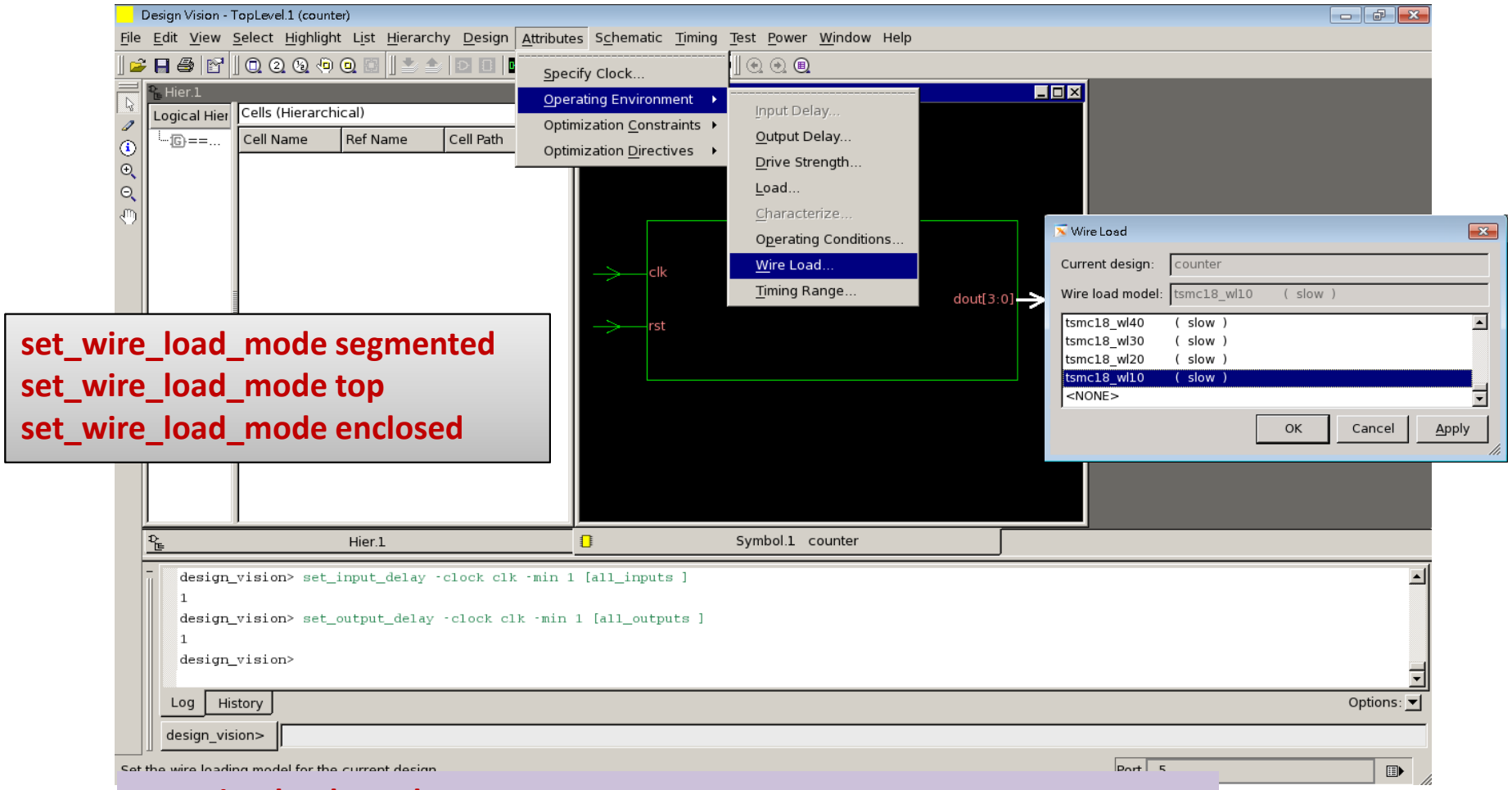
Input/output Delay




```
set_input_delay -clock clk -max 2 [all_inputs]
set_input_delay -clock clk  -min 1 [all_inputs]
```

```
set_output_delay -clock clk -max 2 [all_outputs]
set_output_delay -clock clk  -min 1 [all_outputs]
```

Wire Load Model



set_wire_load_mode segmented
set_wire_load_mode top
set_wire_load_mode enclosed

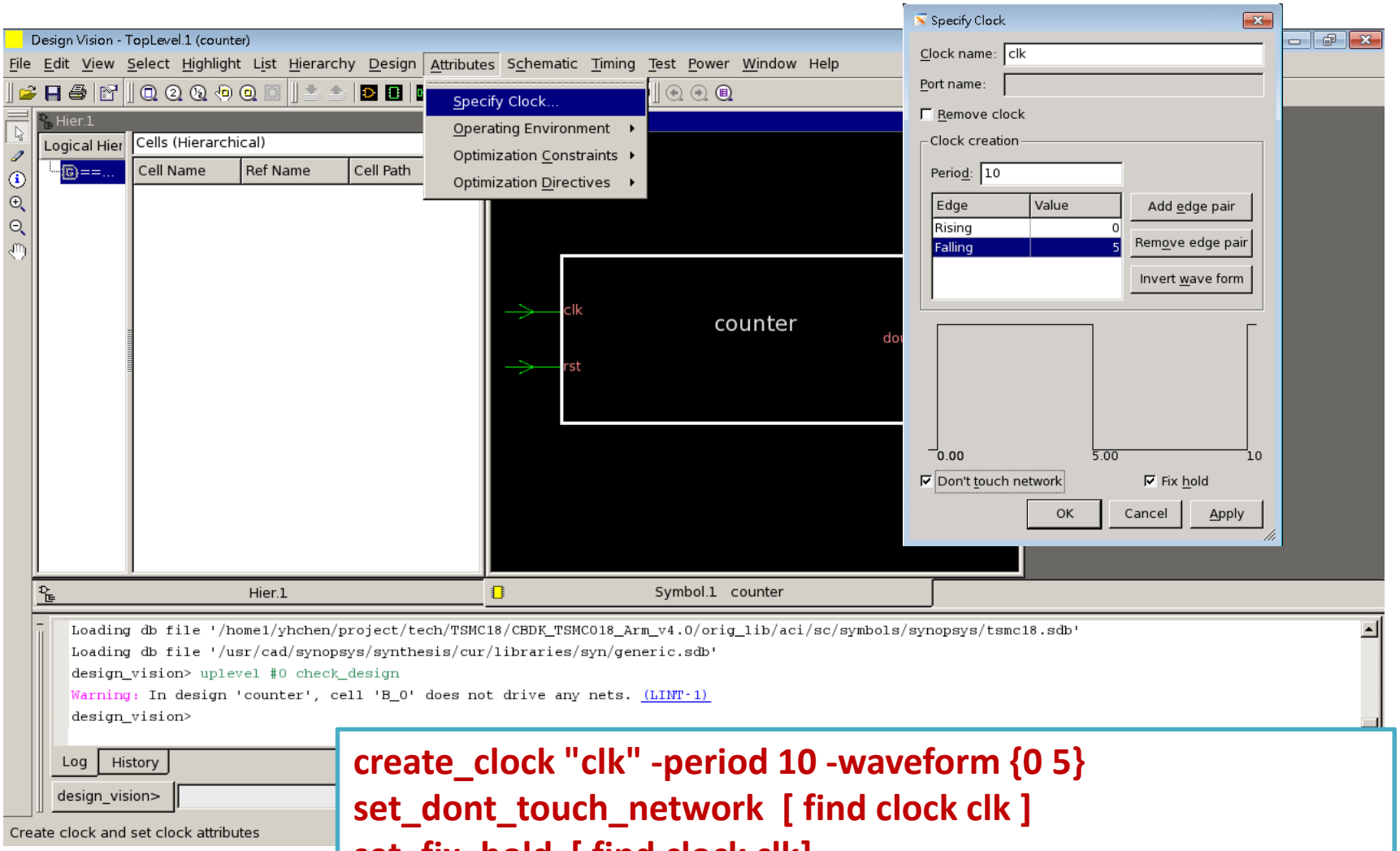
set_wire_load_mode top

set_wire_load_model -name tsmc18_wl10 -library slow

Setting Design Constraints

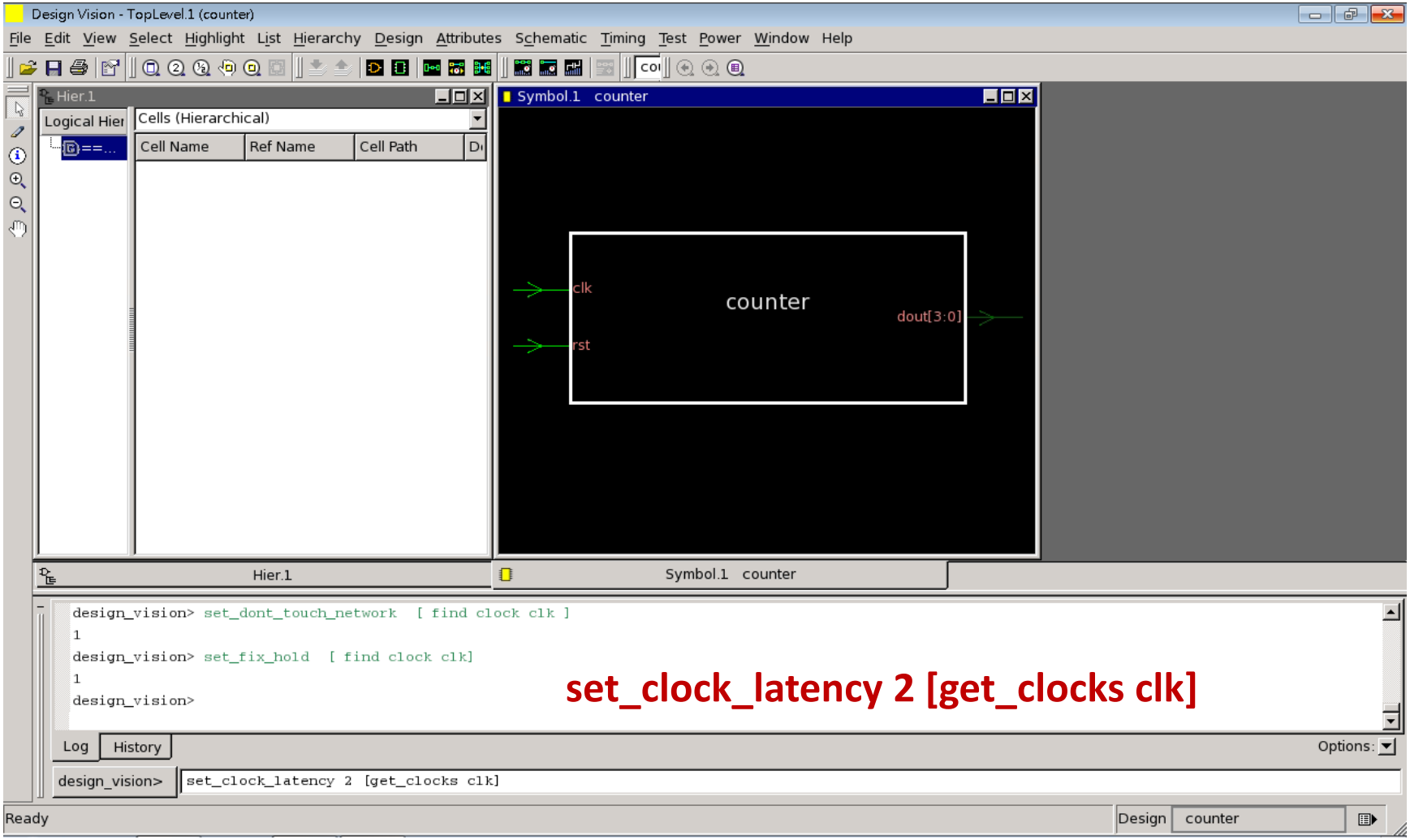
- **Optimization**
  - Specify clock
    - Period, waveform
    - Clock latency
    - Clock uncertainty
  - Power and area
- **Final check design**

Specify Clock



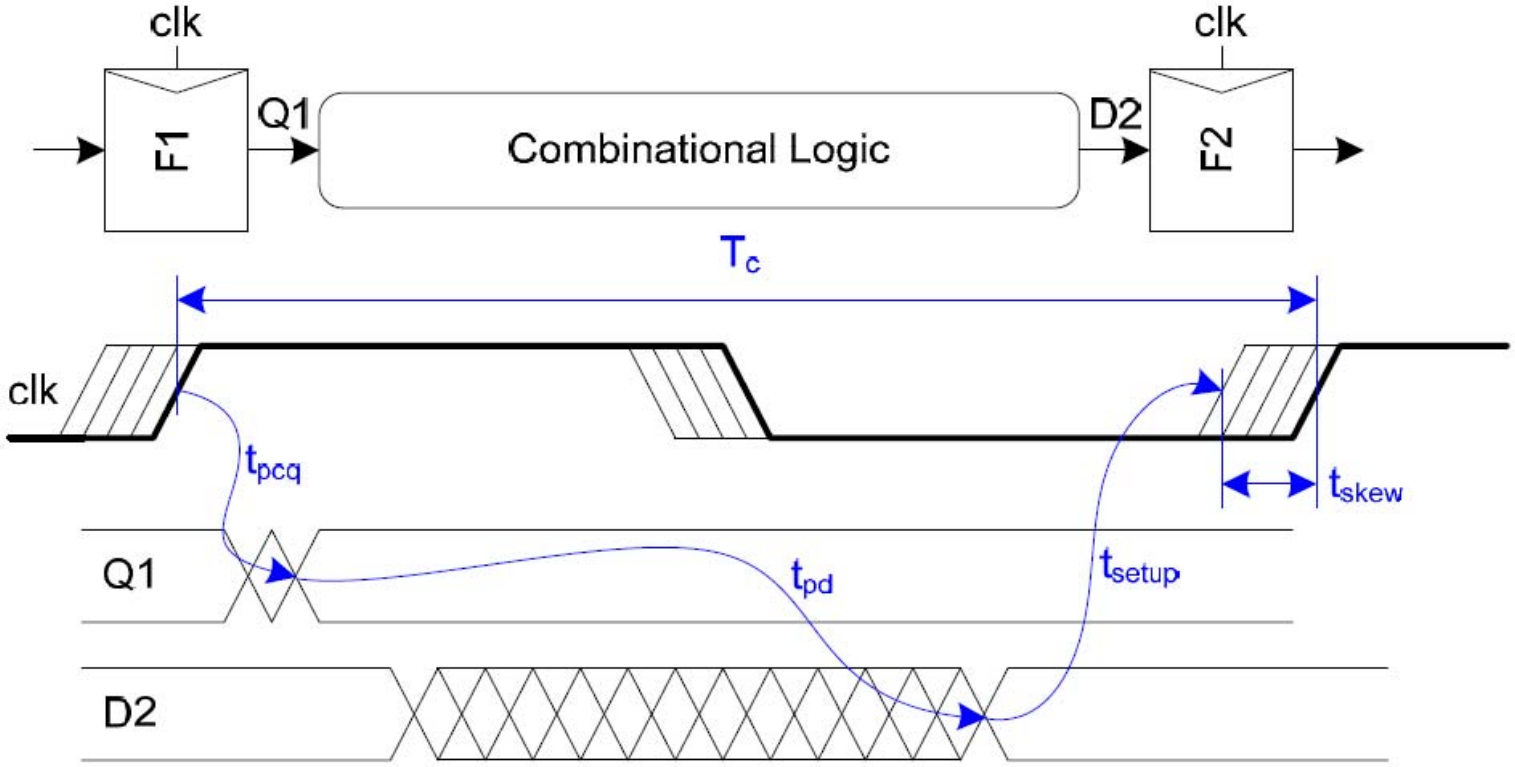

```
create_clock "clk" -period 10 -waveform {0 5}
set_dont_touch_network  [ find clock clk ]
set_fix_hold  [ find clock clk]
```

Clock Latency

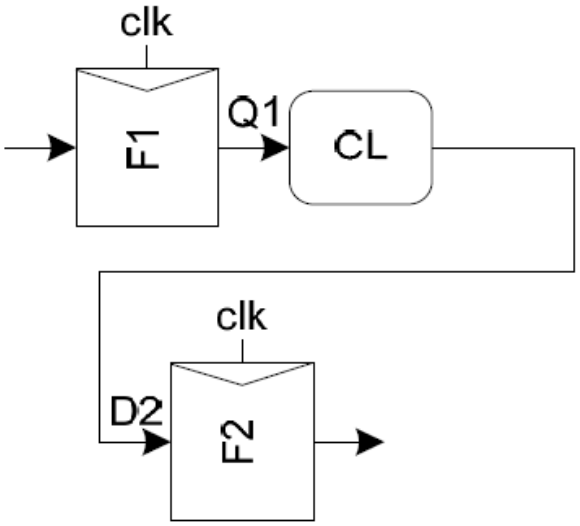


Clock Skew : Setup Time → Max. Delay

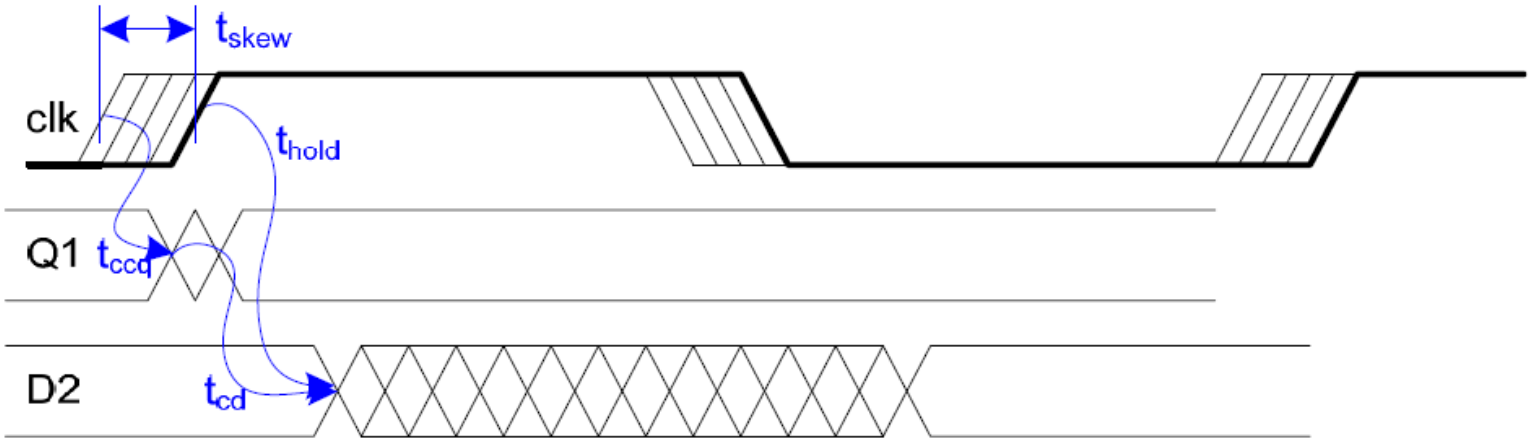
$$t_{pd} \le T_c - \underbrace{\left(t_{pcq} + t_{\text{setup}} + t_{\text{skew}}\right)}_{\text{sequencing overhead}}$$



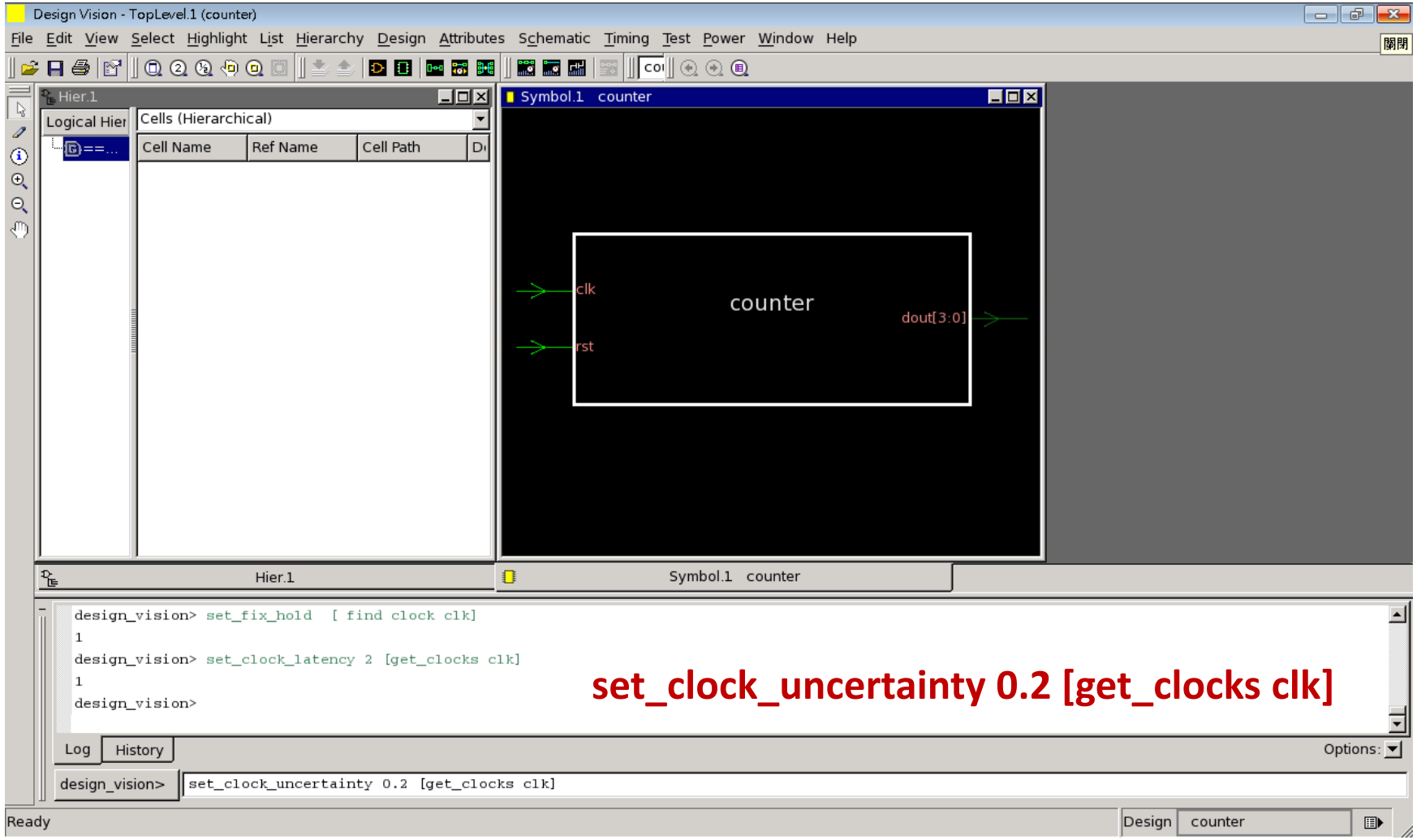
Clock Skew : Hold Time → Min. Delay



$$t_{cd} \geq t_{\text{hold}} - t_{ccq} + t_{\text{skew}}$$



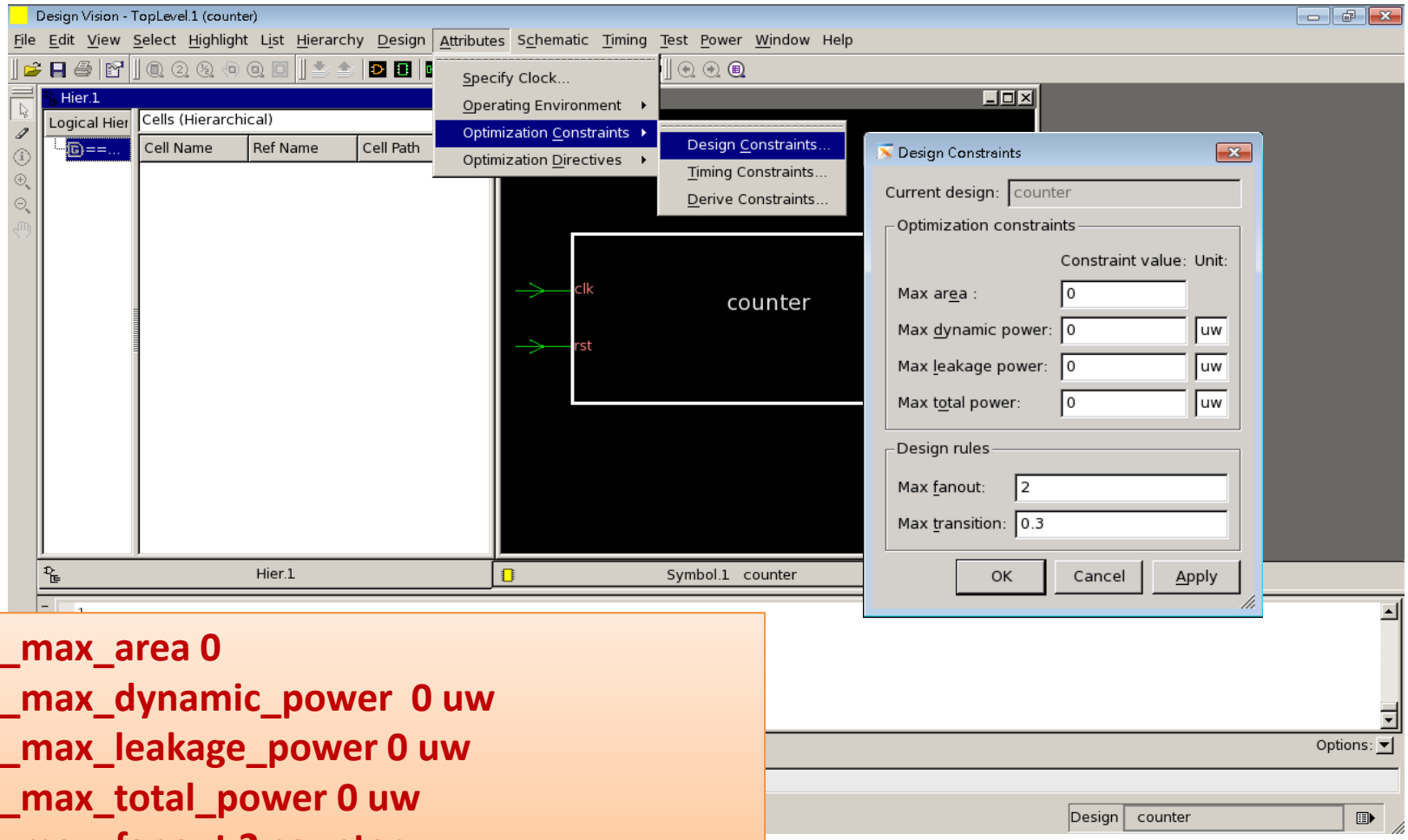
Clock Uncertainty (Skew)



Setting Design Constraints

- **Optimization**
  - Specify clock
    - Period, waveform
    - Clock latency
    - Clock uncertainty
  - Power and area
- **Final check design**

Power and Area

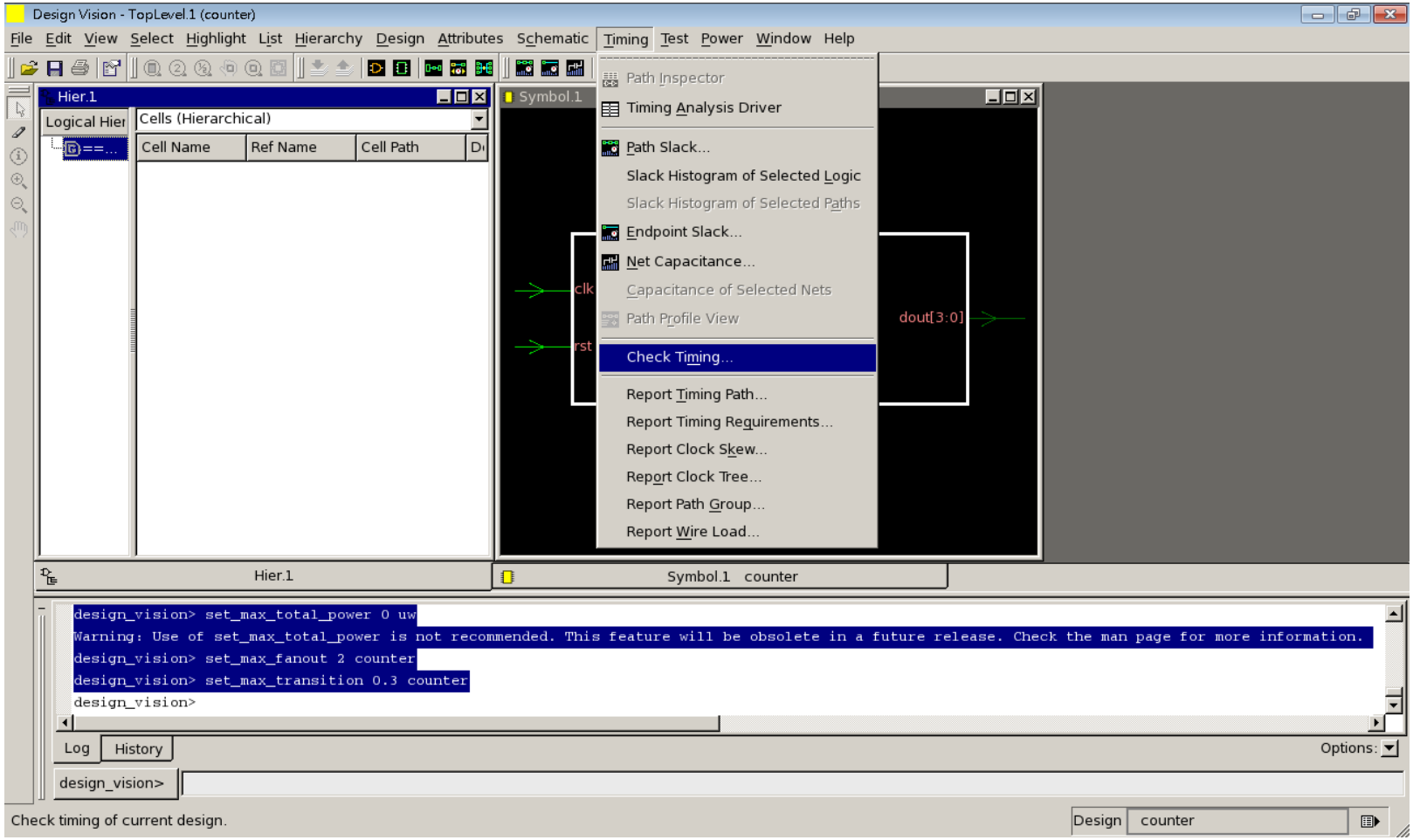



```
set_max_area 0
set_max_dynamic_power  0 uw
set_max_leakage_power 0 uw
set_max_total_power 0 uw
set_max_fanout 2 counter
set_max_transition 0.3 counter
```

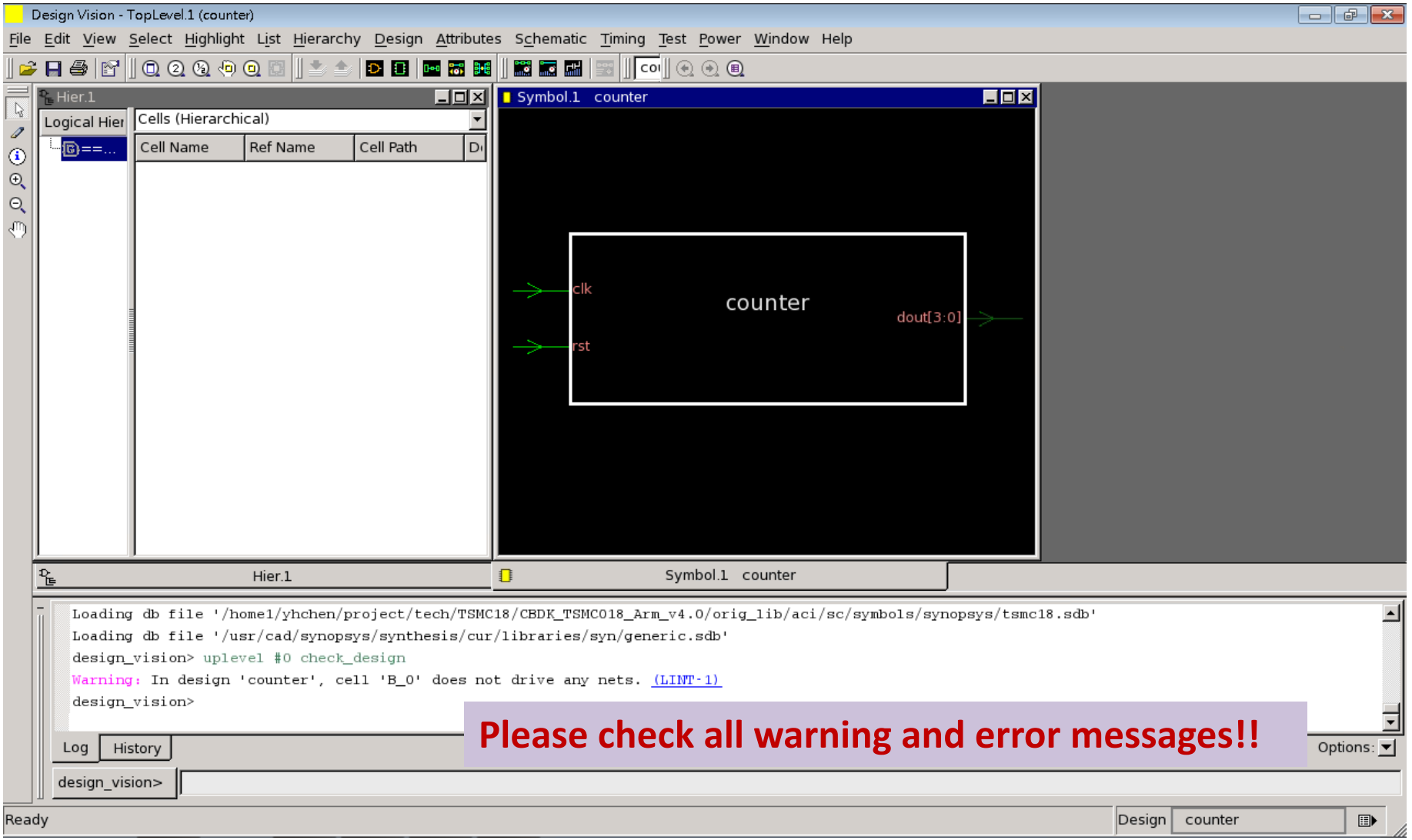
Setting Design Constraints

- **Optimization**
  - Specify clock
    - Period, waveform
    - Clock latency
    - Clock uncertainty
  - Power and area
- **Final check design**

Check Timing



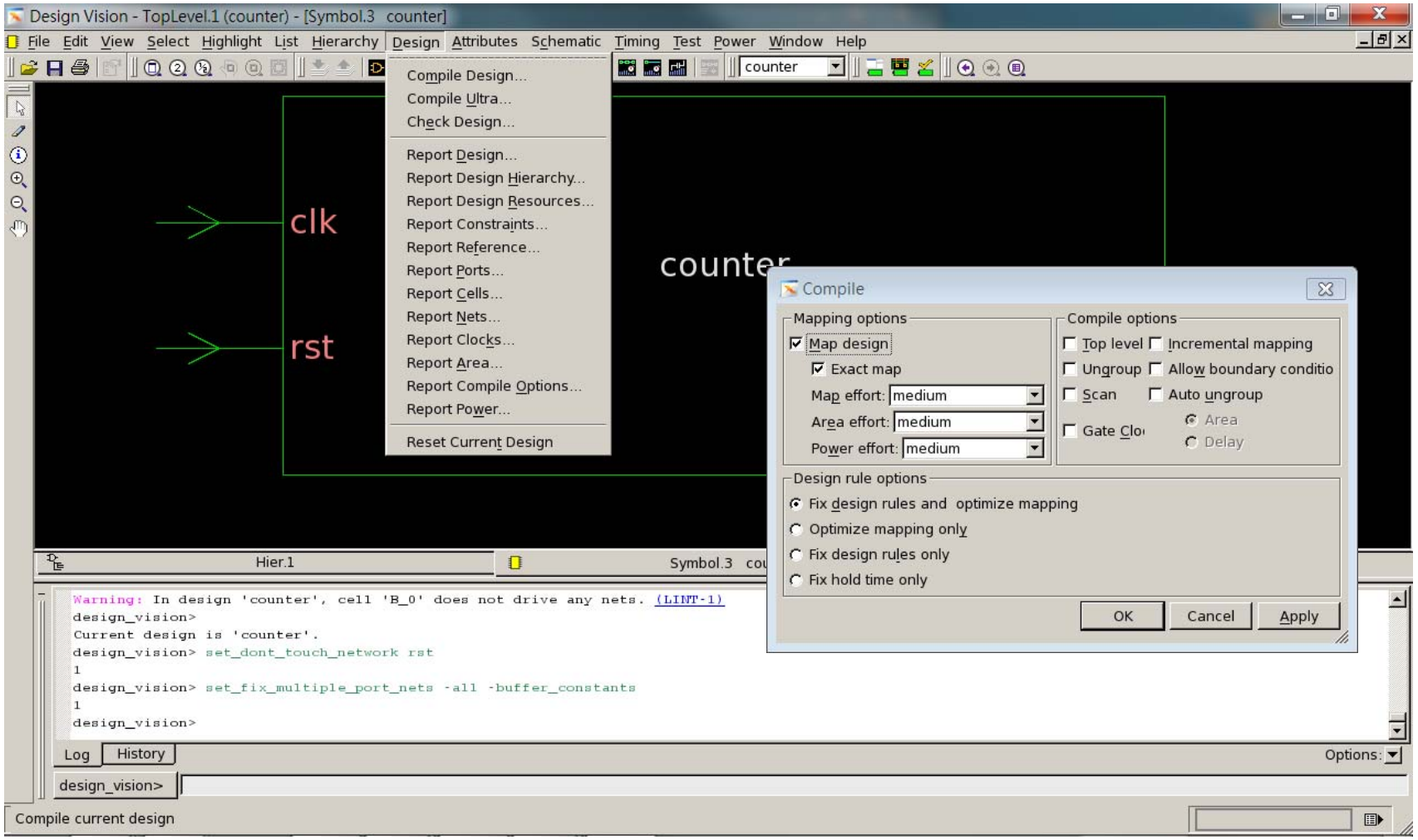
Check Design



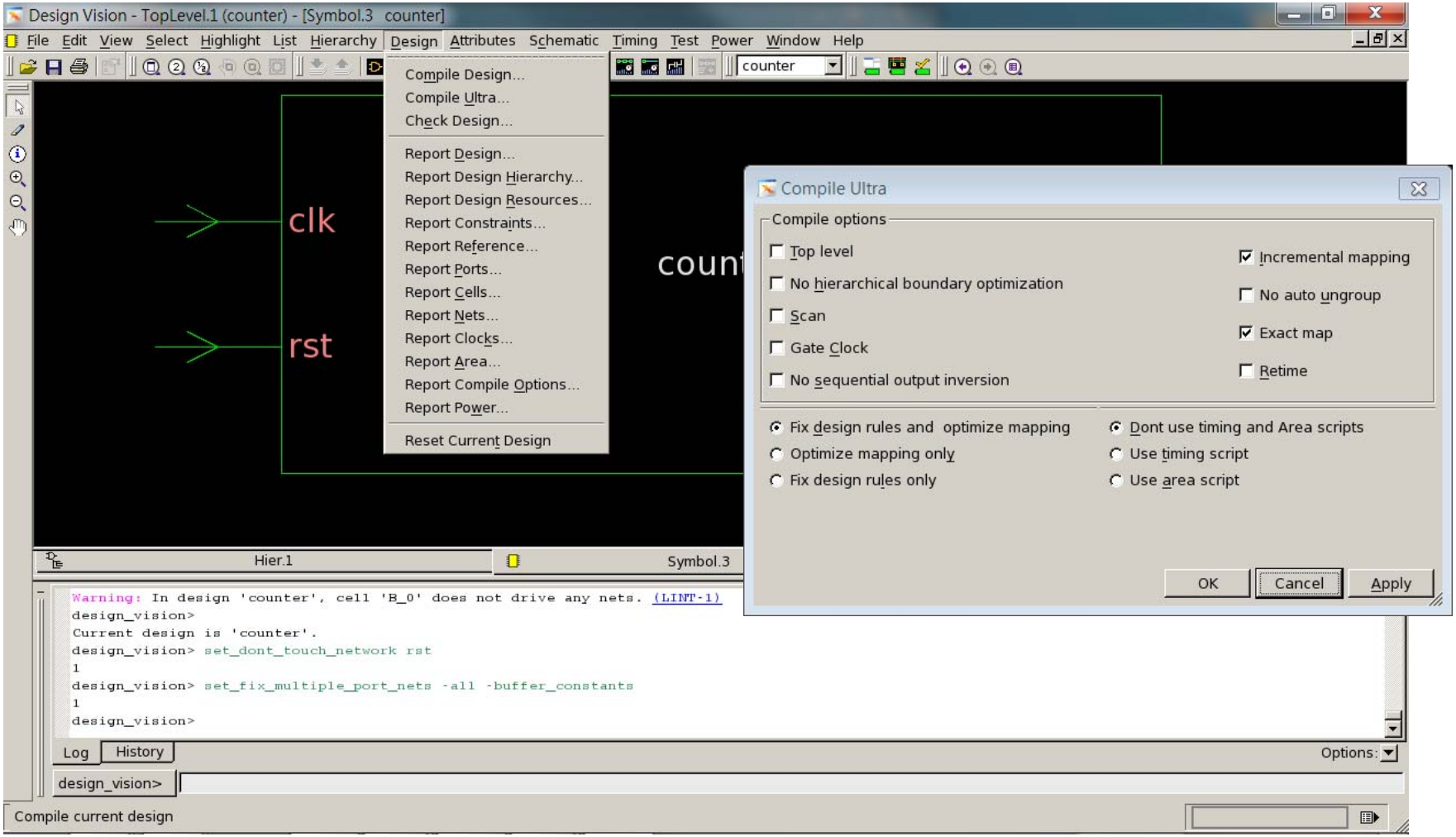
Compile and Report

- **Compile design**
  - Map effort
  - Area effort
  - Power effort
- **Report design**
  - Design
  - Area
  - Power
  - Delay

Compile Design



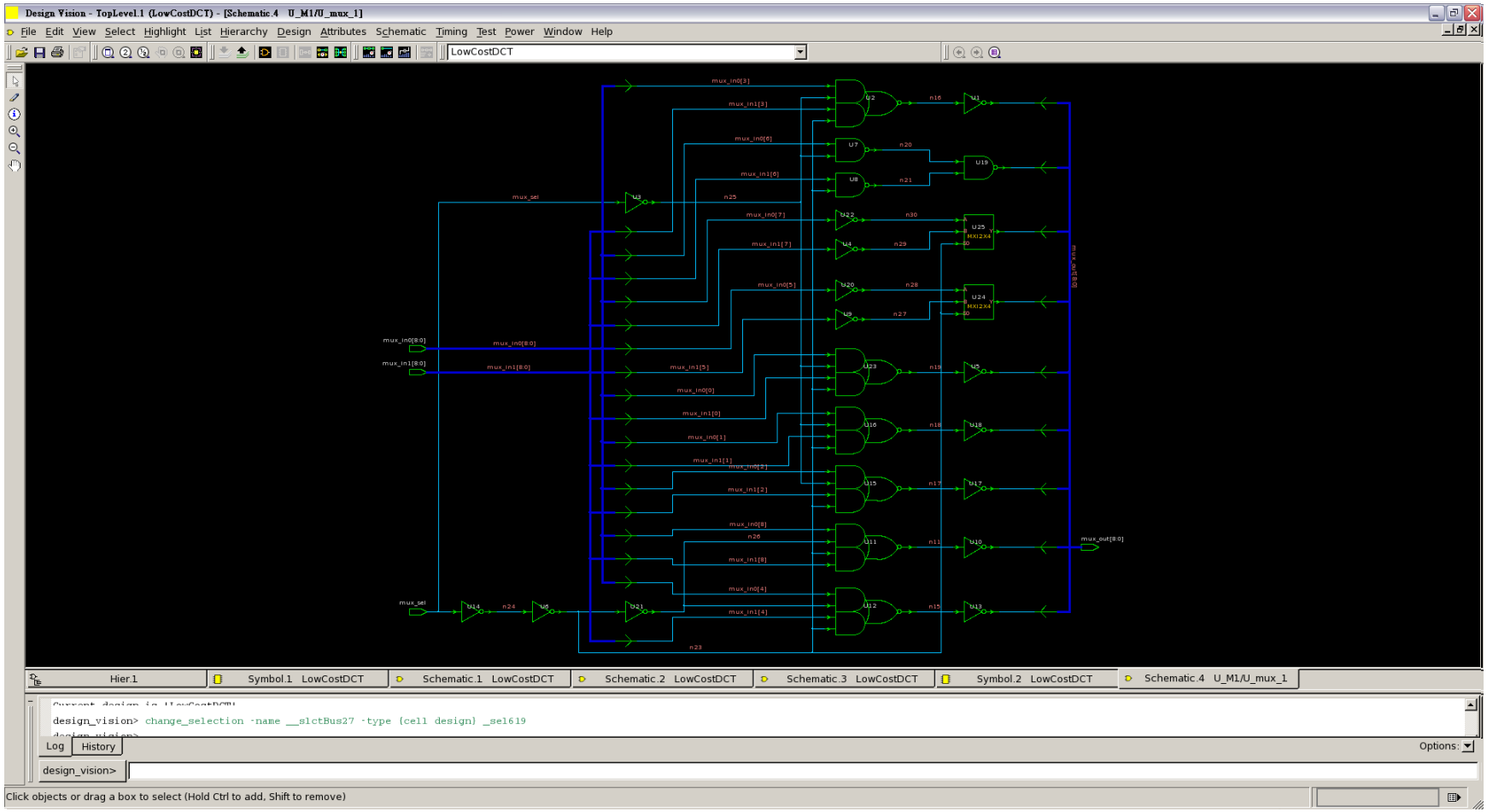
Compile Ultra



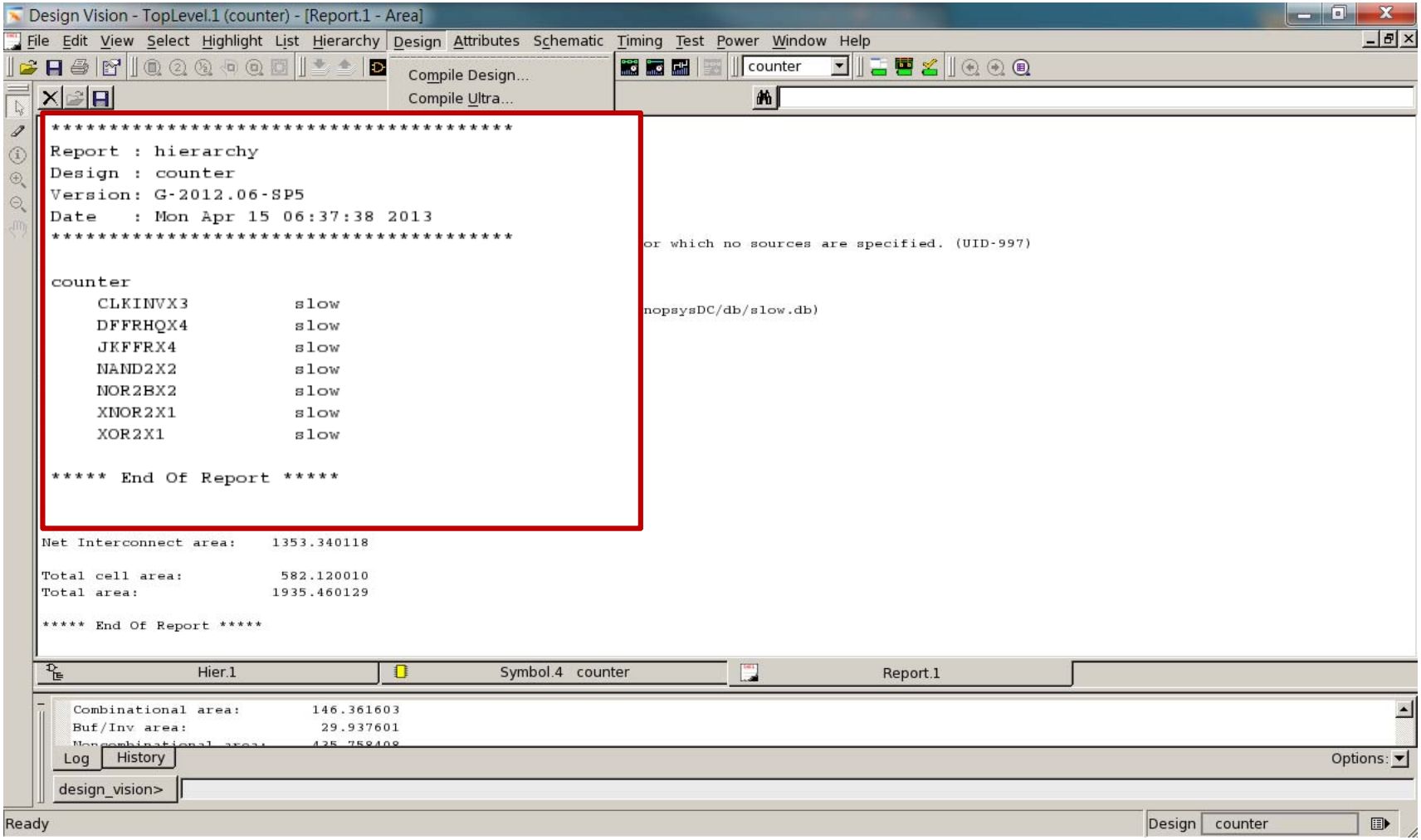
Compile and Report

- Compile design
  - Map effort
  - Area effort
  - Power effort
- **Report design**
  - Design
  - Area
  - Power
  - Delay

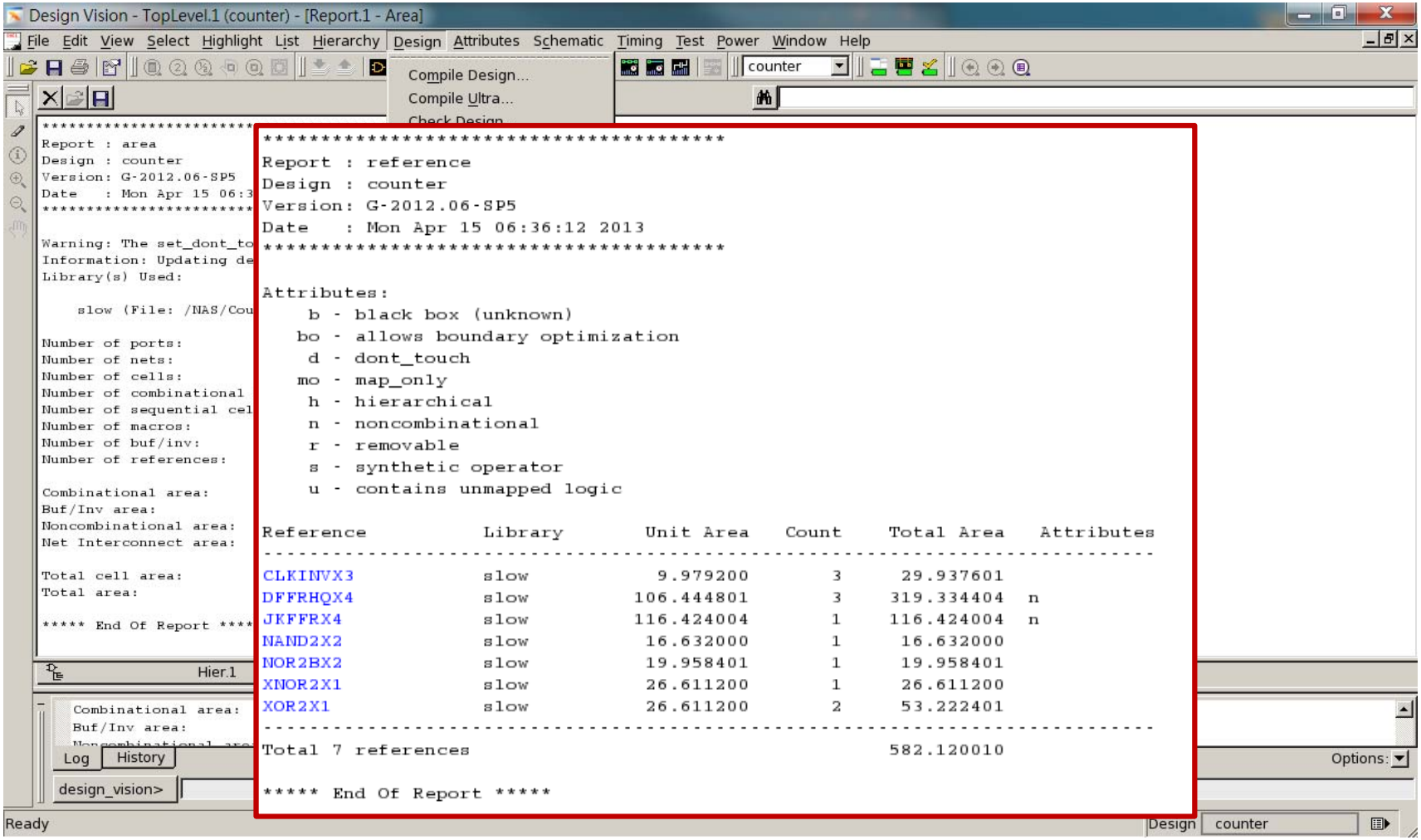
Design Hierarchy



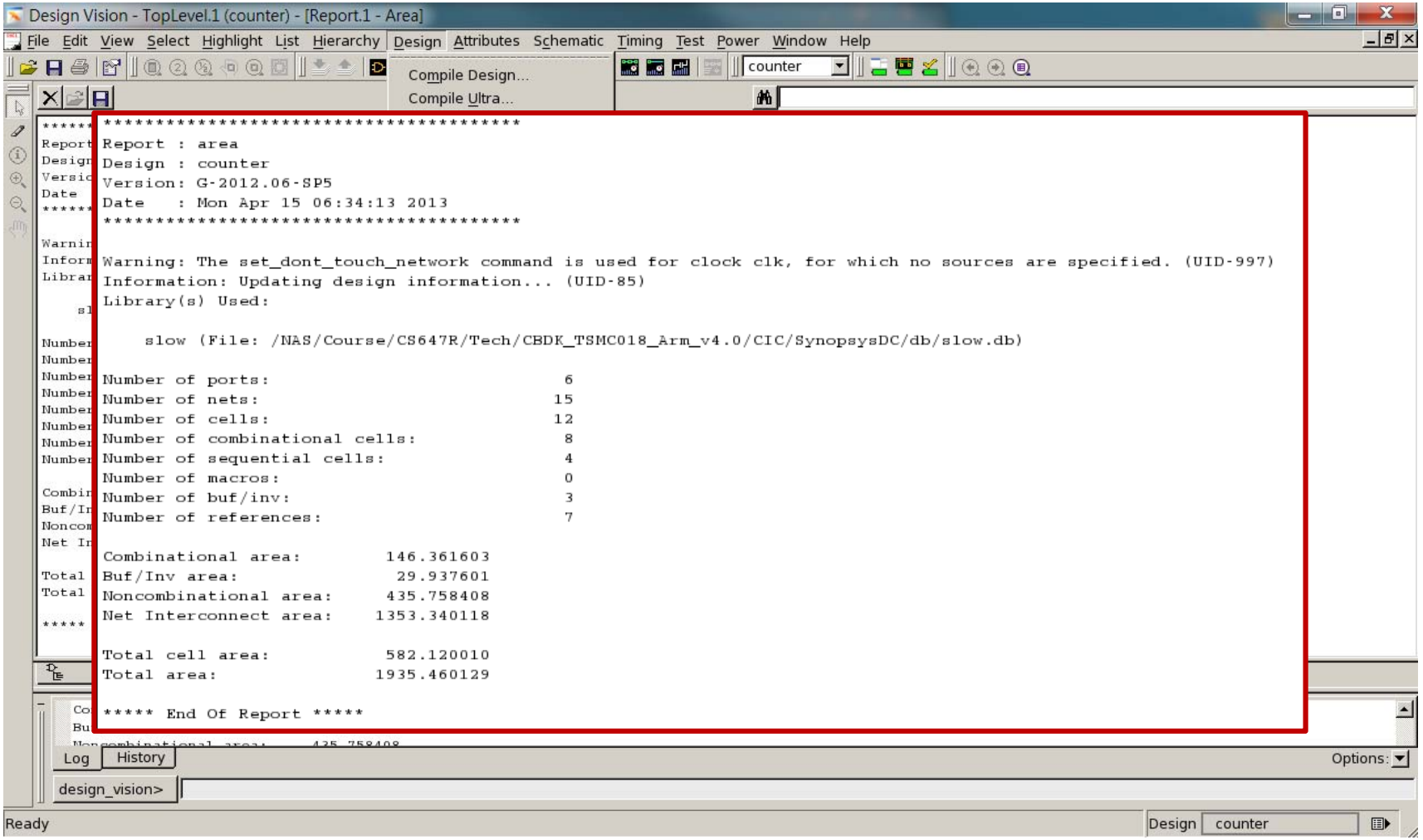
Report Hierarchy



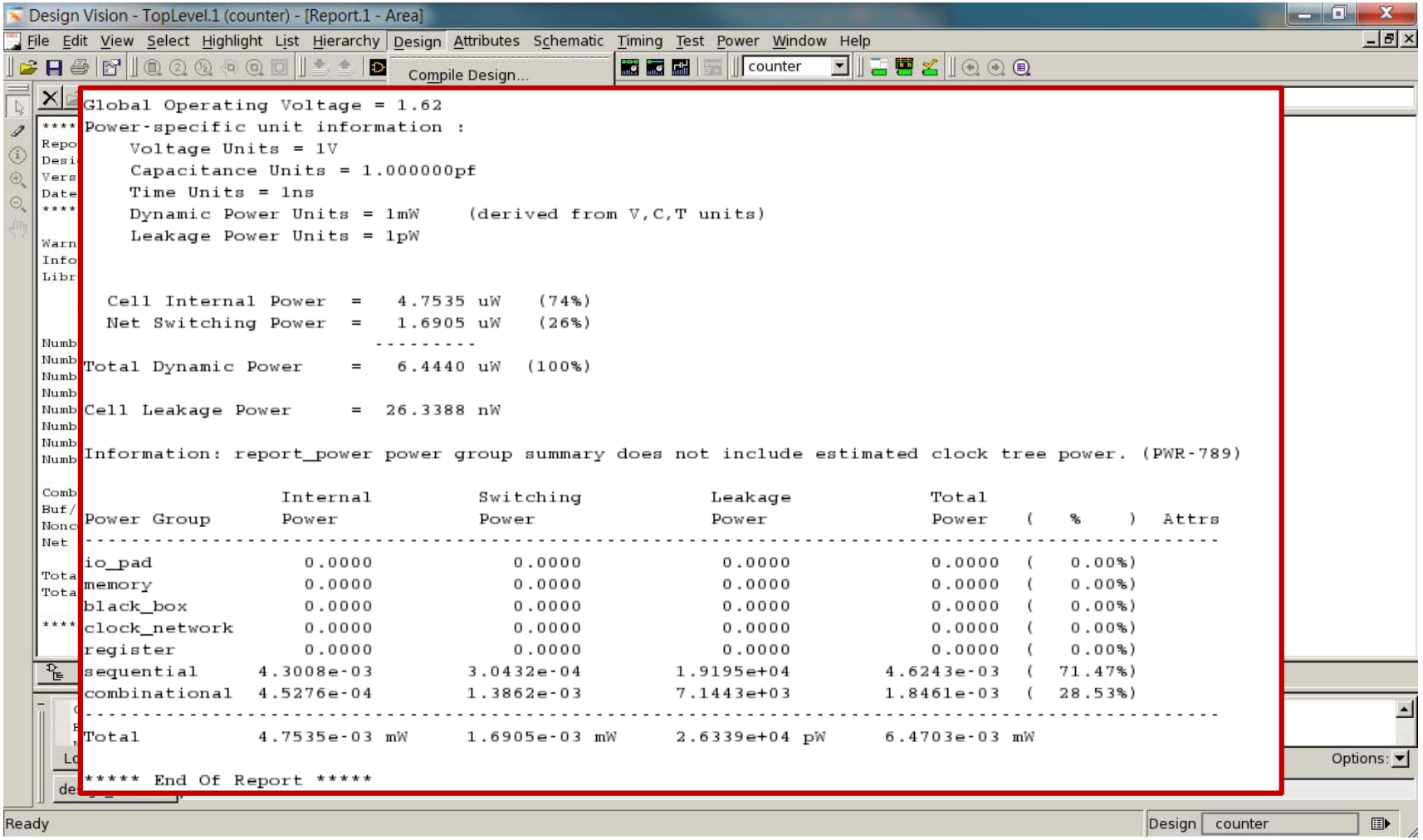
Report Reference



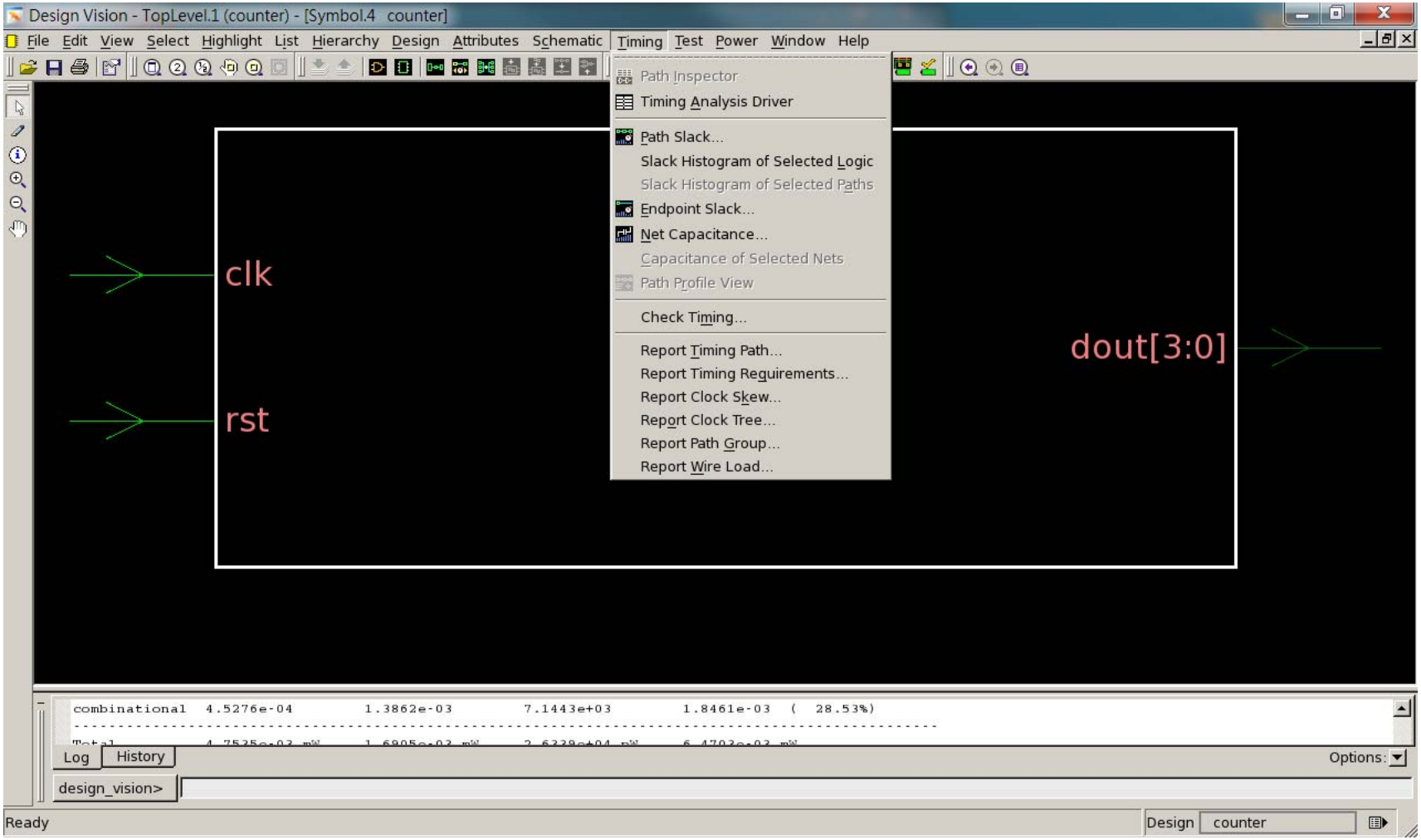
Report Area


Design Vision - TopLevel.1 (counter) - [Report.1 - Area]
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help
Compile Design...
Compile Ultra...
counter
****
Report : area
Design : counter
Version: G-2012.06-SP5
Date : Mon Apr 15 06:34:13 2013
****
Warning: The set_dont_touch_network command is used for clock clk, for which no sources are specified. (UID-997)
Information: Updating design information... (UID-85)
Library(s) Used:
slow (File: /NAS/Course/CS647R/Tech/CBDK_TSMC018_Arm_v4.0/CIC/SynopsysDC/db/slow.db)
Number of ports: 6
Number of nets: 15
Number of cells: 12
Number of combinational cells: 8
Number of sequential cells: 4
Number of macros: 0
Number of buf/inv: 3
Number of references: 7
Combinational area: 146.361603
Buf/Inv area: 29.937601
Noncombinational area: 435.758408
Net Interconnect area: 1353.340118
Total cell area: 582.120010
Total area: 1935.460129
***** End Of Report *****
Log History
Options:
design_vision>
Ready
Design counter

Report Power



Report Timing



Report Timing

```
****************************
Report : timing
         -path full
         -delay max
         -max_paths 1
Design : counter
Version: G-2012.06-SP5
Date   : Mon Apr 15 06:52:36
****************************

Operating Conditions: slow
Wire Load Model Mode: top

  Startpoint: dout_reg_0_/CK
              (internal path
  Endpoint: dout_reg_3_
            (rising edge-trig
  Path Group: clk
  Path Type: max
```

```
Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
counter            tsmc18_wl10           slow

Point                                    Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                    0.00       0.00
clock network delay (ideal)              0.00       0.00
input external delay                     0.00       0.00 r
dout_reg_0_/CK (JKFFRXL)                 0.00       0.00 r
dout_reg_0_/Q (JKFFRXL)                  1.55       1.55 r
U9/Y (NAND2X1)                           0.34       1.89 f
U11/Y (NOR2BX1)                          0.34       2.22 r
U10/Y (XOR2X1)                           0.33       2.56 f
dout_reg_3_/D (DFFRHQX1)                 0.00       2.56 f
data arrival time                                   2.56

clock clk (rise edge)                   10.00      10.00
clock network delay (ideal)              0.00      10.00
dout_reg_3_/CK (DFFRHQX1)                0.00      10.00 r
library setup time                      -0.37       9.63
data required time                                  9.63
-----------------------------------------------------------
data required time                                  9.63
data arrival time                                  -2.56
-----------------------------------------------------------
slack (MET)                                         7.07
```

Slack

- **Slack must be positive or zero in a design.**
- **Negative slack means violate constraints.**
- **Setup time (max delay):**
  - Slack = data required time - data arrival time >= 0;
- **Hold time (min delay):**
  - Slack = data arrival time - data required time >= 0;

Save Design

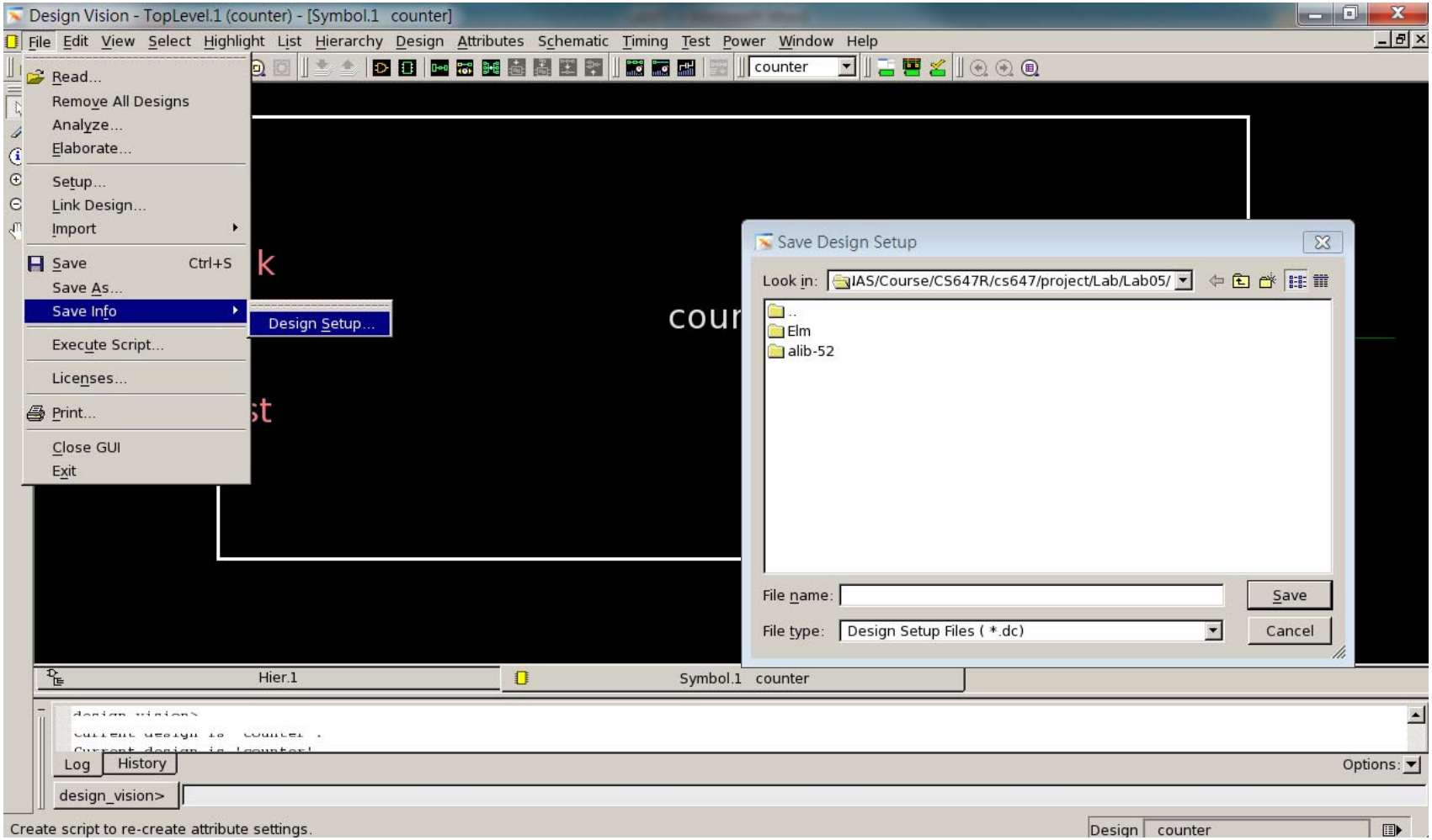
- **Change naming rule**
  - Script
- **Save design**
  - Design setup file
  - Timing file
  - Netlist
  - Design
  - Script

Change Naming Rule

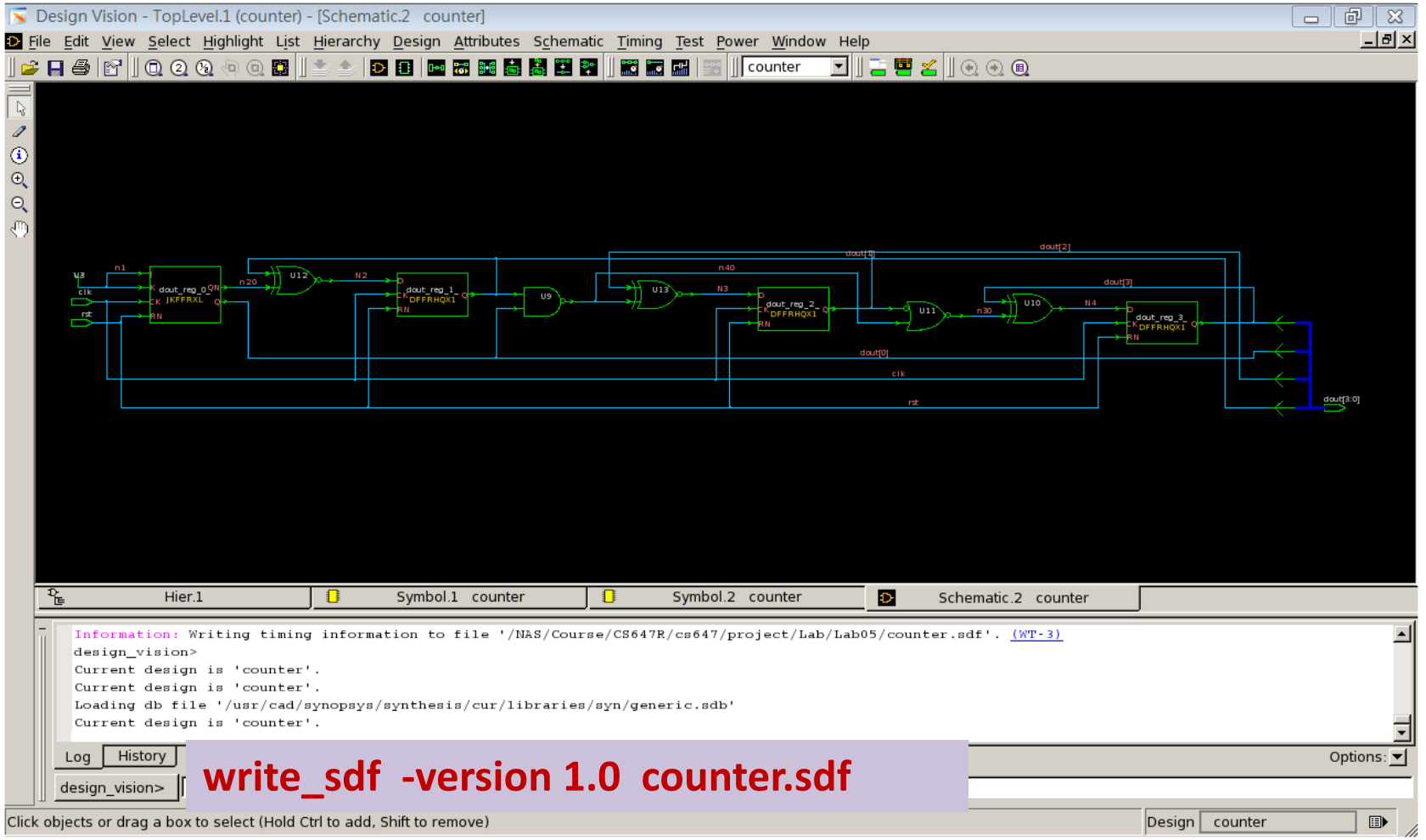
```
current_design [get_designs $mydesign]
remove_unconnected_ports -blast_buses [get_cells * -hier]
set bus_inference_style {%s[%d]}
set bus_naming_style {%s[%d]}
set hdlout_internal_busses true
change_names -hierarchy -rule verilog
define_name_rules name_rule -allowed {a-z A-Z 0-9 _} -max_length 255 -type cell
define_name_rules name_rule -allowed {a-z A-Z 0-9 _[]} -max_length 255 -type net
define_name_rules name_rule -map {{"\\*cell\\*" "cell"}}
define_name_rules name_rule -case_insensitive
change_names -hierarchy -rules name_rule
```

No assign or other key-word !!

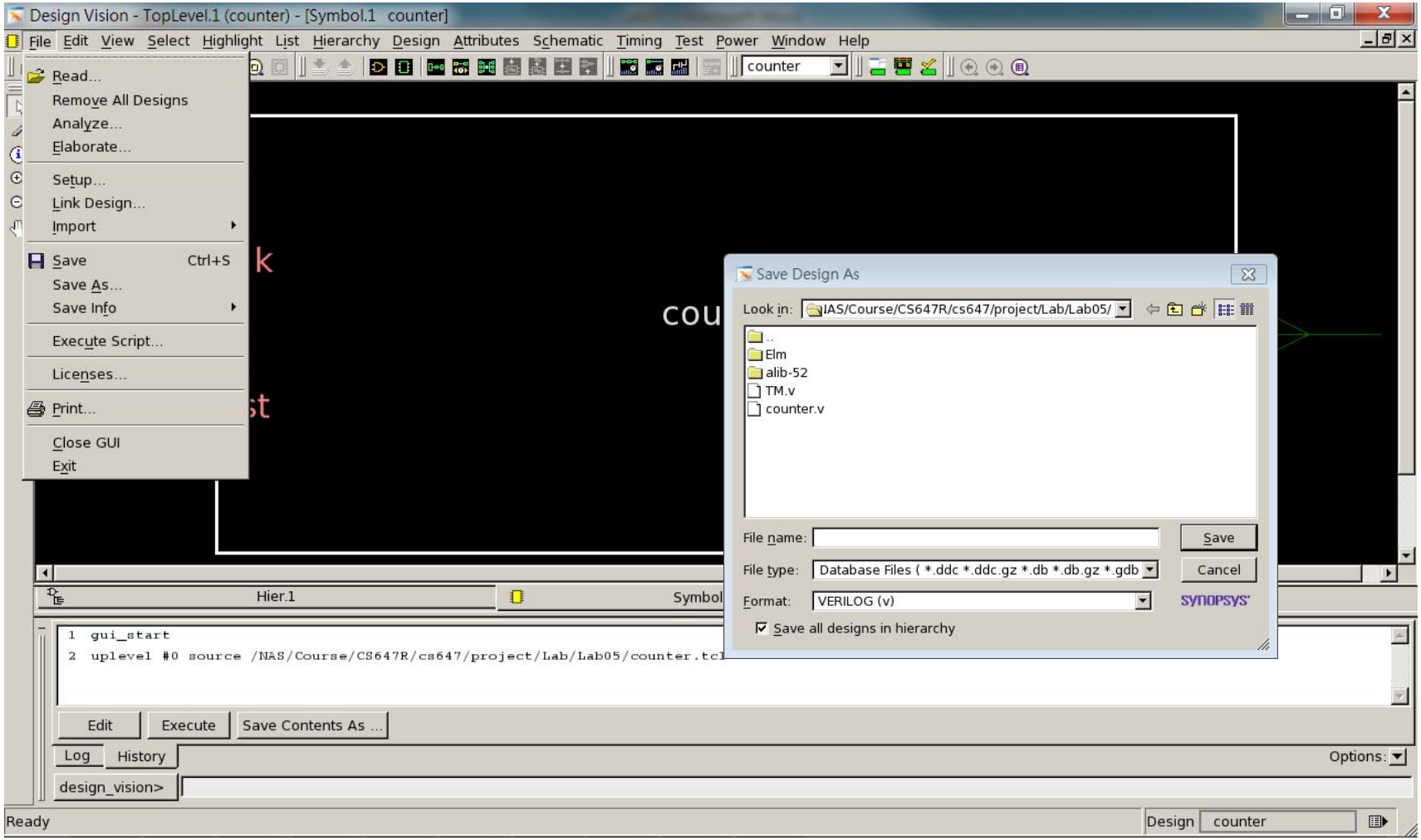
Save Design Setup File



Save Design Timing File



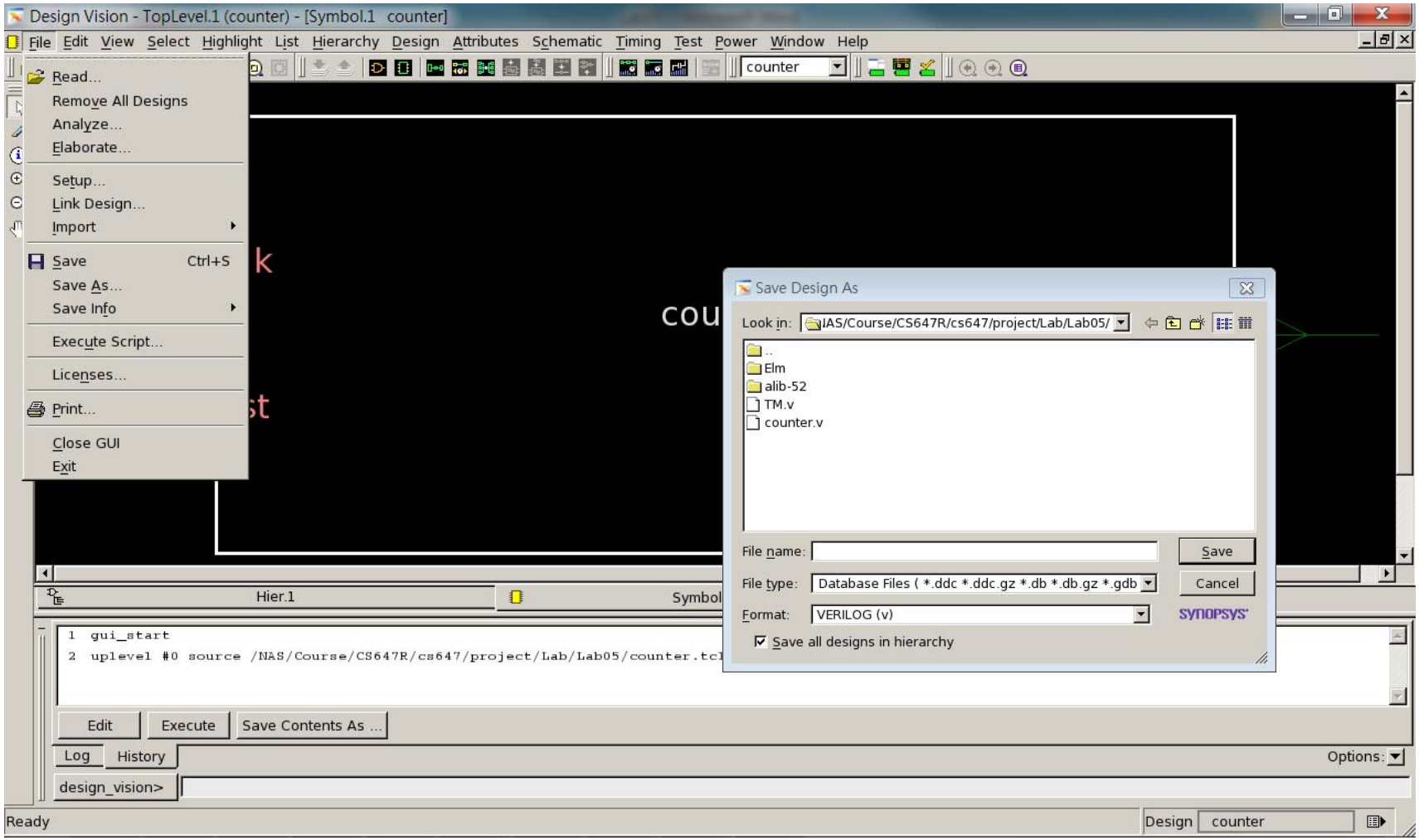
Save Netlist



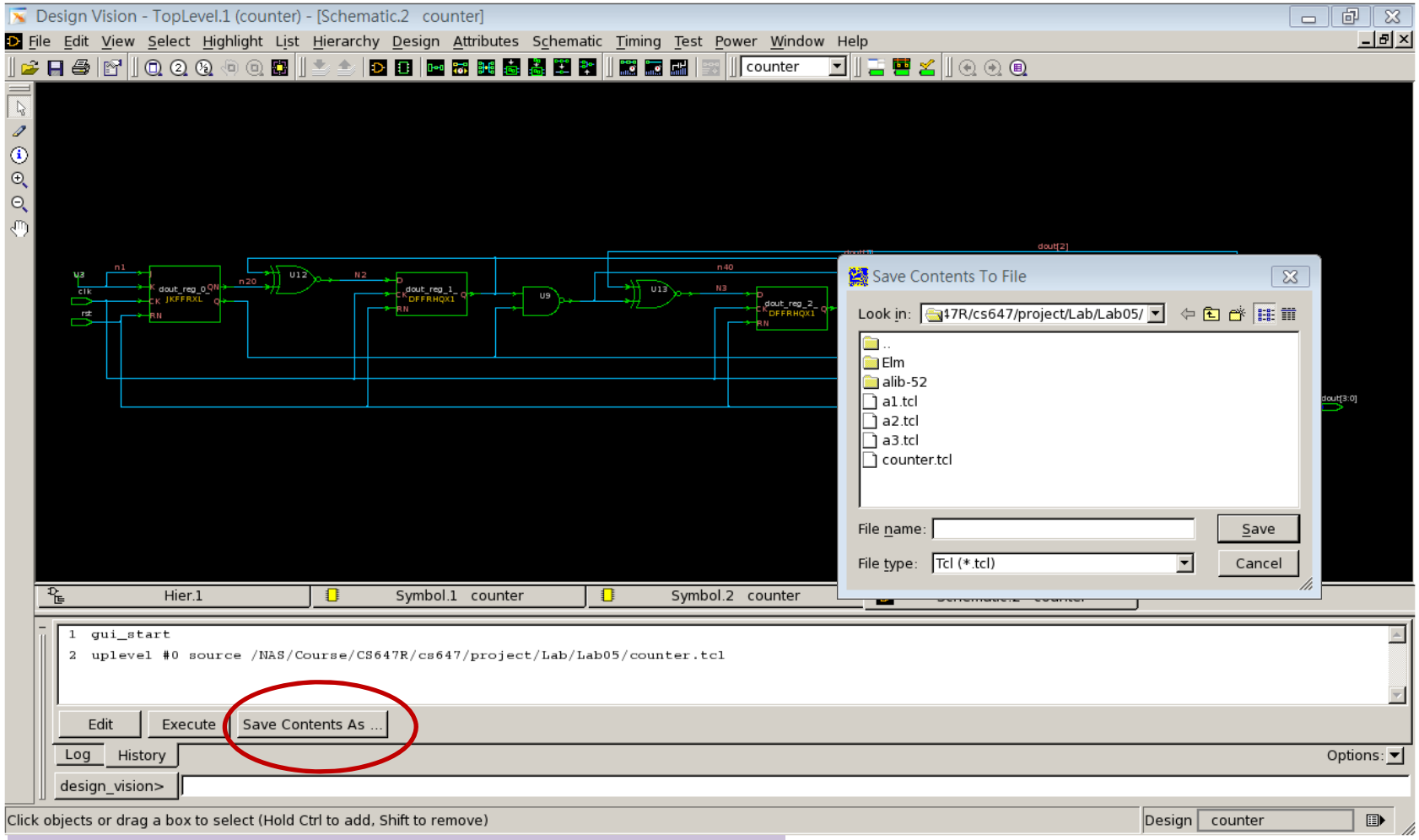
write -format verilog -hierarchy –output chip_syn.v

Save Design

- **Save the design as ddc (or db) format**

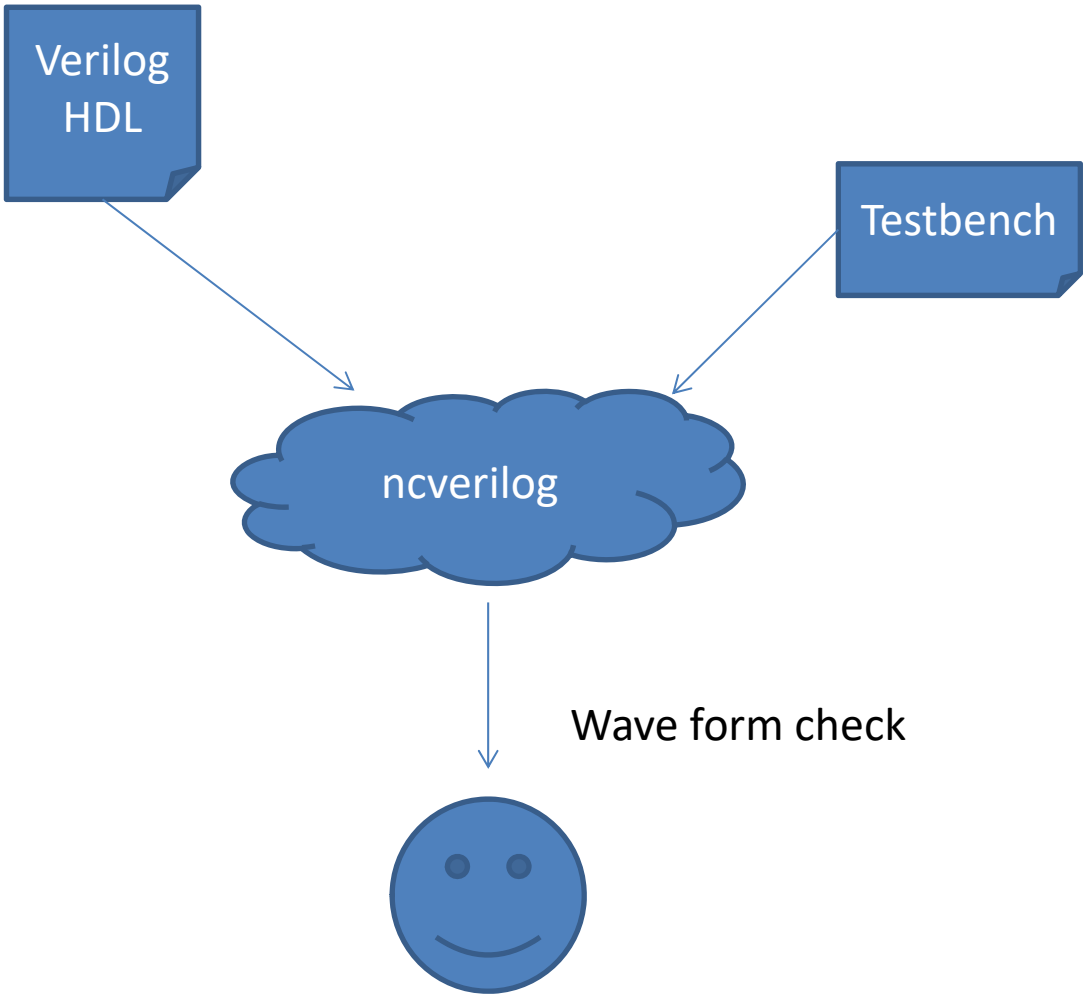


Save Script

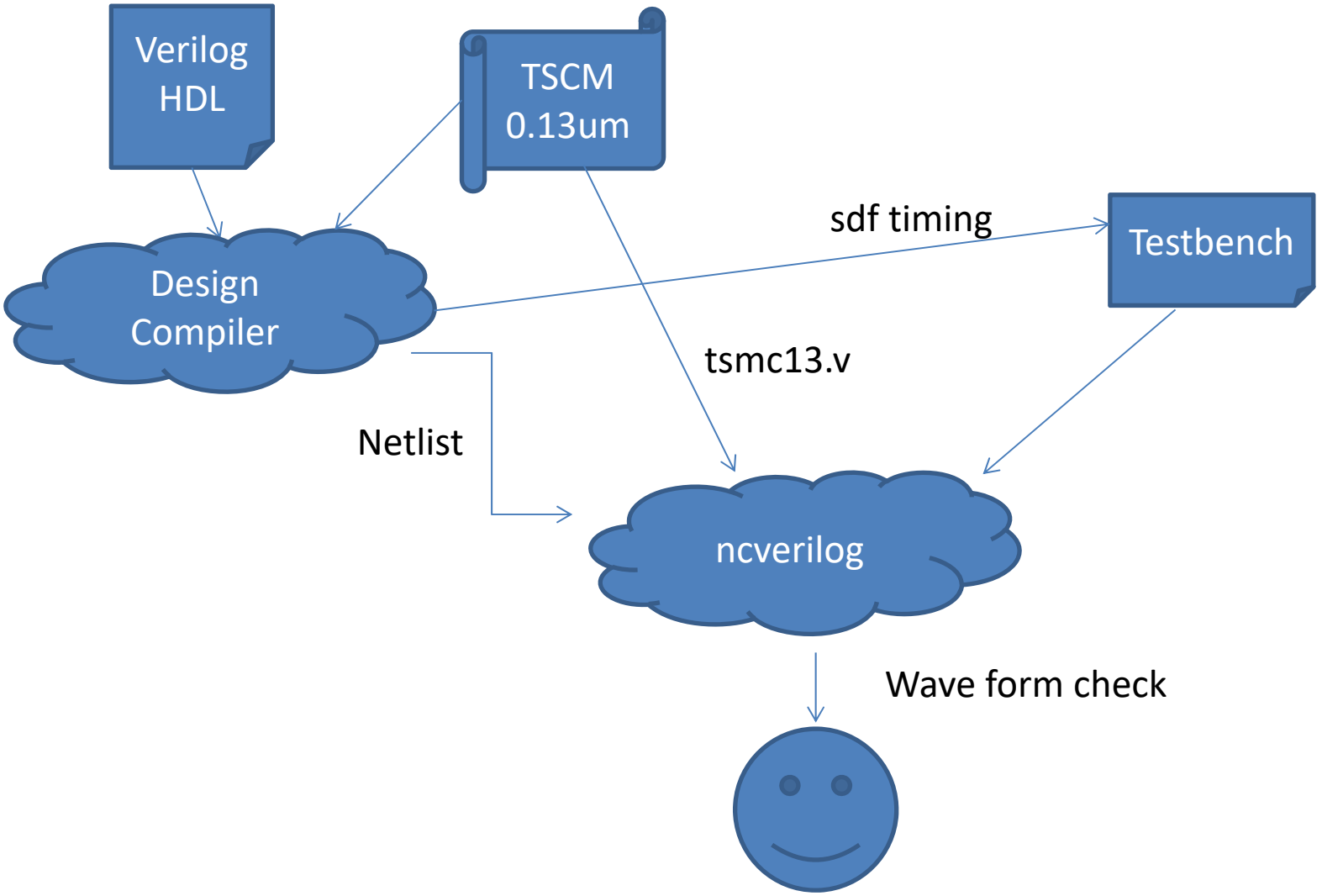


%dc_shell-xg-t -f xxx.tcl

Function Simulation



Gate Level Simulation



Testbench SDF Annotation

- **Include timing information in the simulations**
  - Standard Delay Format (SDF) file
  - $sdf_annotate(sdf_file, module_instance, log_file, scale_factor, scale_type);

```
initial
   $sdf_annotate("../rtl/Chip.sdf", U_Core);
```

```
CHIP       U_Core(
                .clk      (clk),
                .rst      (rst),
                .xin      (xin),
                .zout     (zout)
);
```