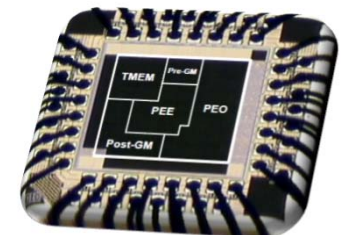


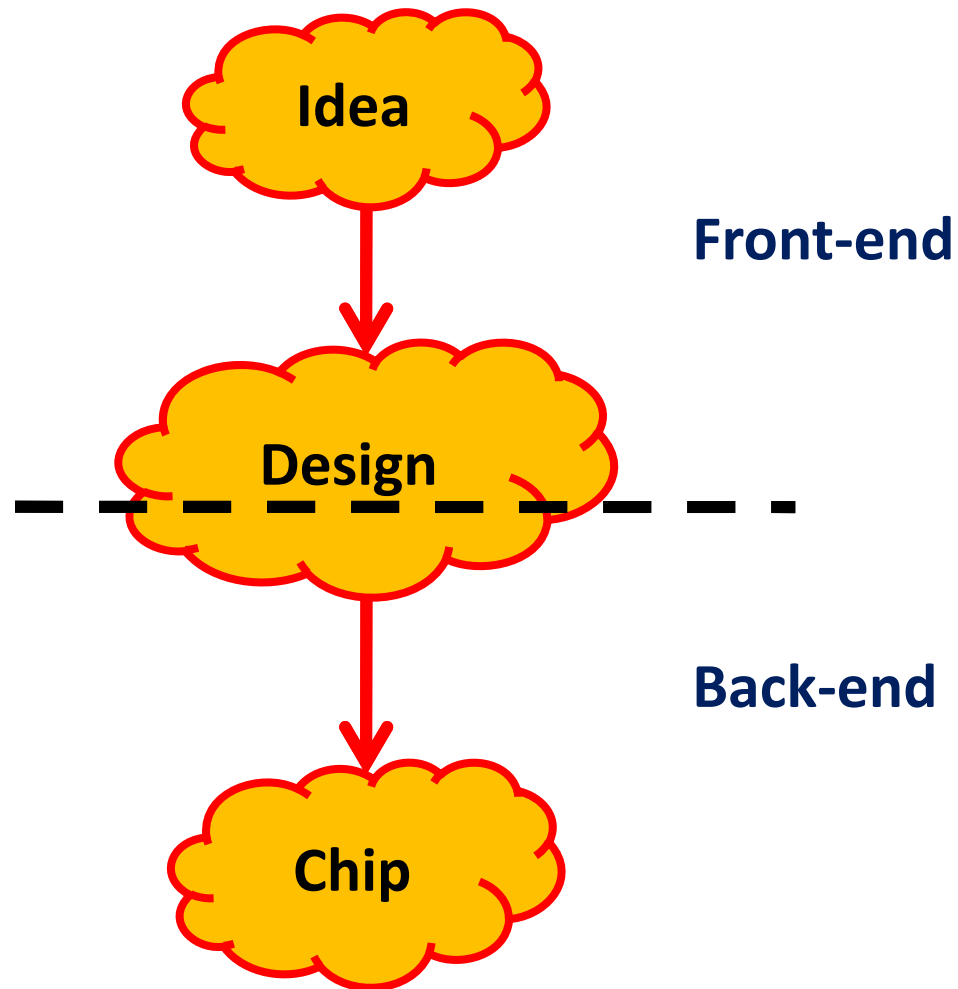
Logic Synthesis with Design Compiler

Yuan-Ho Chen

Department of Electronic Engineering
Chang Guan University
chenyh@mail.cgu.edu.tw



Cell-based Design Flow



- **Front-end**

- System partitioning
- Design entry: HDL/Schematic
- Logic synthesis
- Pre-layout simulation

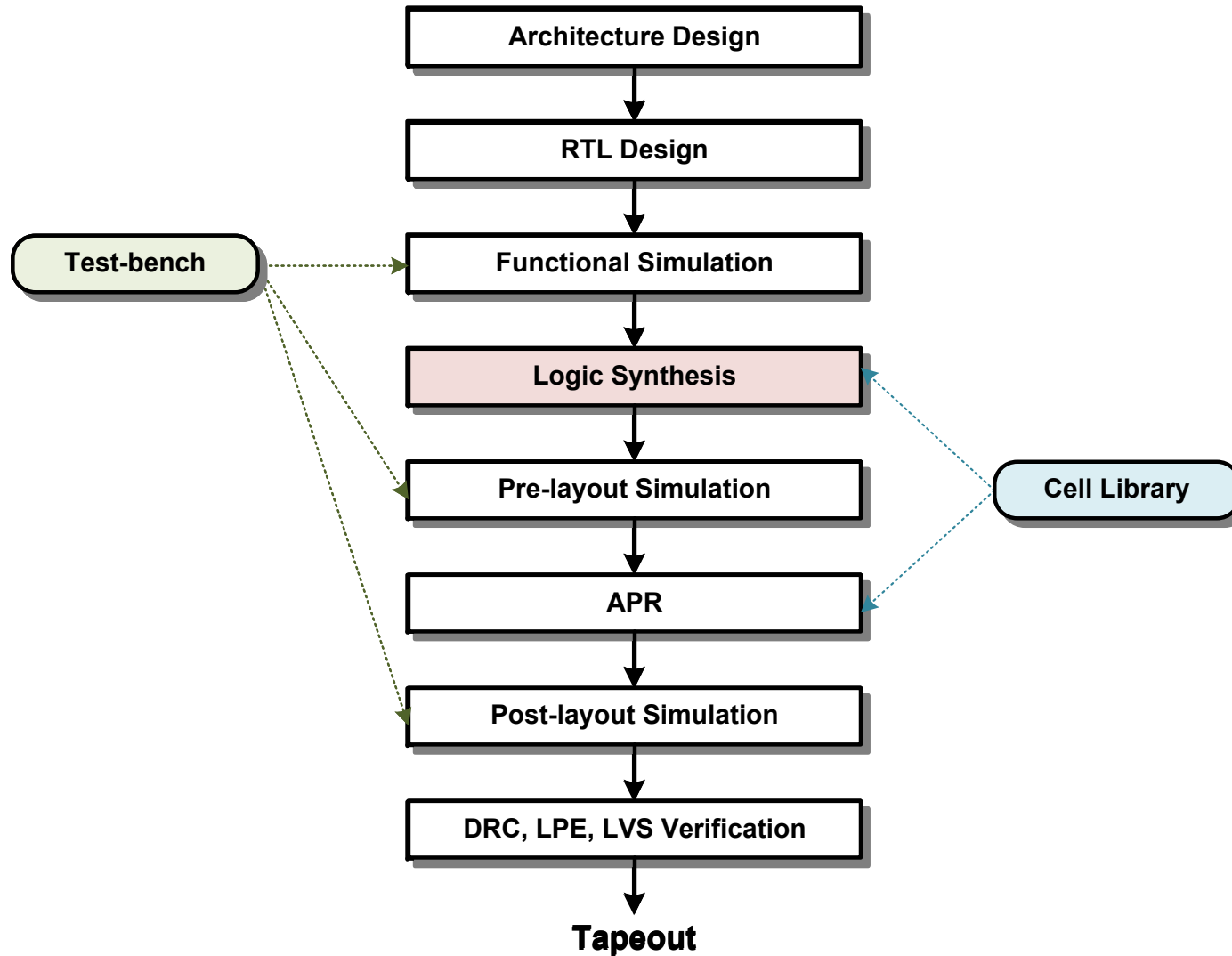
- **Back-end**

- Floor plan
- Placement
- Routing
- Extraction
- Post-layout simulation

References

- *Logic Synthesis with Design Compiler*, CIC Training Manual.
- *Handout of Introduction to Integrated Circuits Design*, T.-Y. Chang, EE, NTHU.
- *Larc Synthesis Course*, EE, NTHU.

Cell-based Design Flow



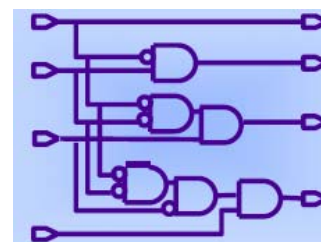
Synthesis

- Convert a high-level RTL into an optimized gate-level netlist.
 - Standard cell library *Provide from Fab., such TSMC or UMC*
 - Constraints
 - Translation + Optimization + Mapping

```
residue = 16'h0000;  
if (high_bits == 2'b10)  
    residue = state_table[index];  
else state_table[index] = 16'h0000;
```

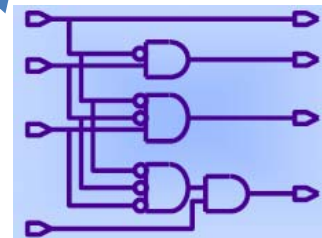
RTL code

Translate



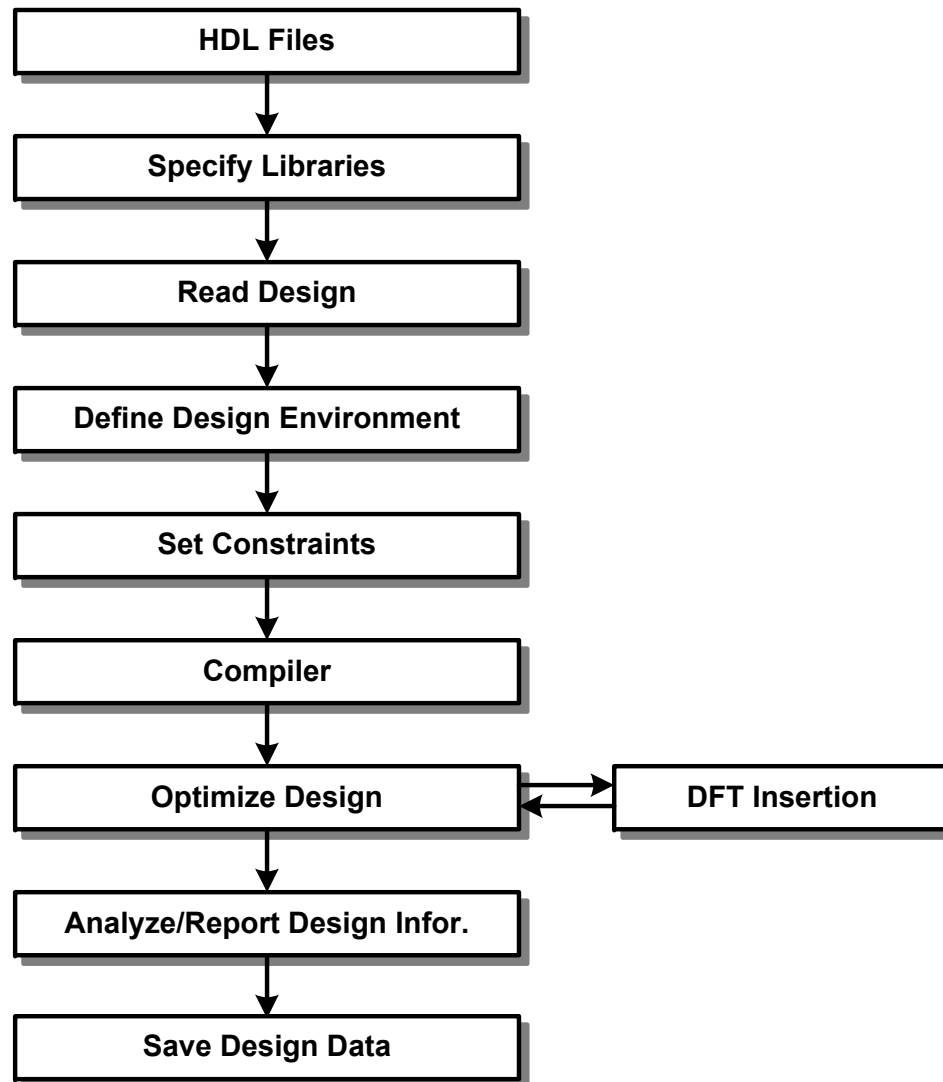
Generic Boolean

Optimize + Map



Target Technology

Basic Synthesis Flow



Getting Start

- **Setup file**
 - Put `.synopsys_dc.setup` in your local home directory
 - `$HOME/.synopsys_dc.setup`
- **Start design compiler**
 - `dv`
 - `design_vision-xg`
 - `dc_shell-xg-t` (script mode)

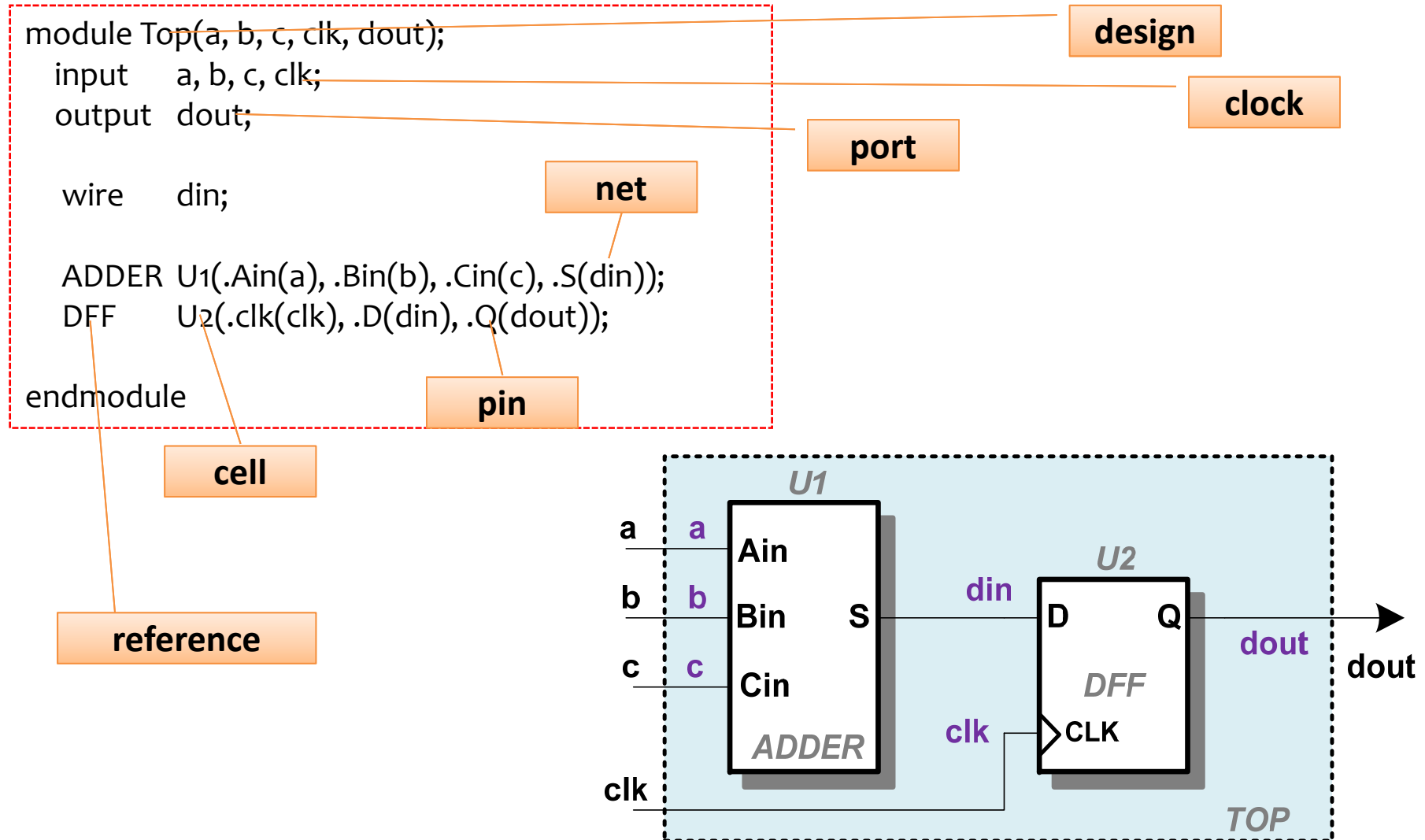
.synopsys_dc.setup File

```
set designer "Yuan-Ho Chen"
set company "ICLab. ELE. CGU."

set search_path "~/.tech/Synth/ $search_path"
set link_library "* slow.db fast.db dw_foundation.sldb"
set target_library "slow.db fast.db"
set symbol_library "generic.sdb"
set synthetic_library "dw_foundation.sldb"

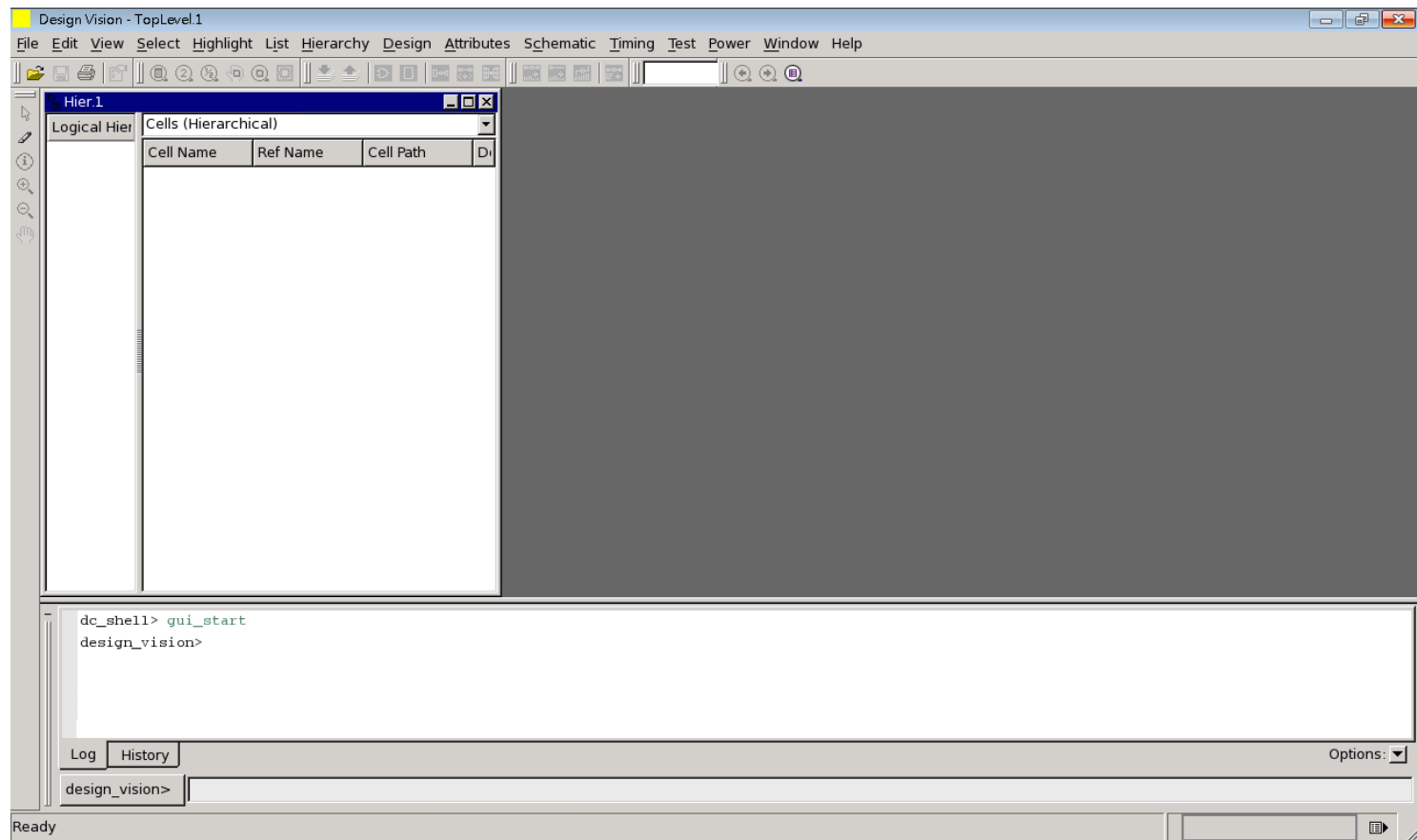
set verilogout_no_tri true
set sh_enable_line_editing true
set sh_line_editing_mode emacs
history keep 100
alias h history
```


Design Objects

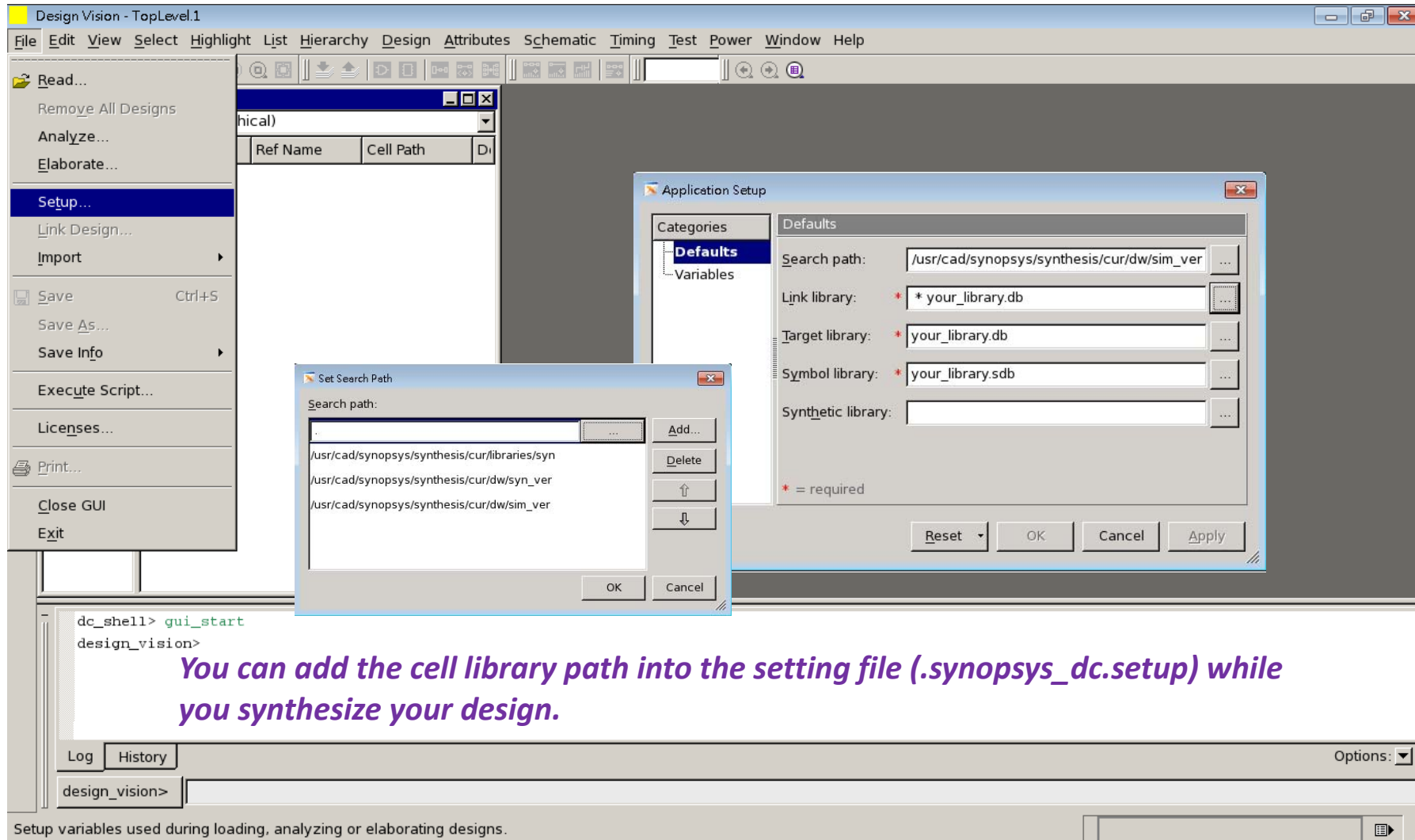


Invoke Design Compiler

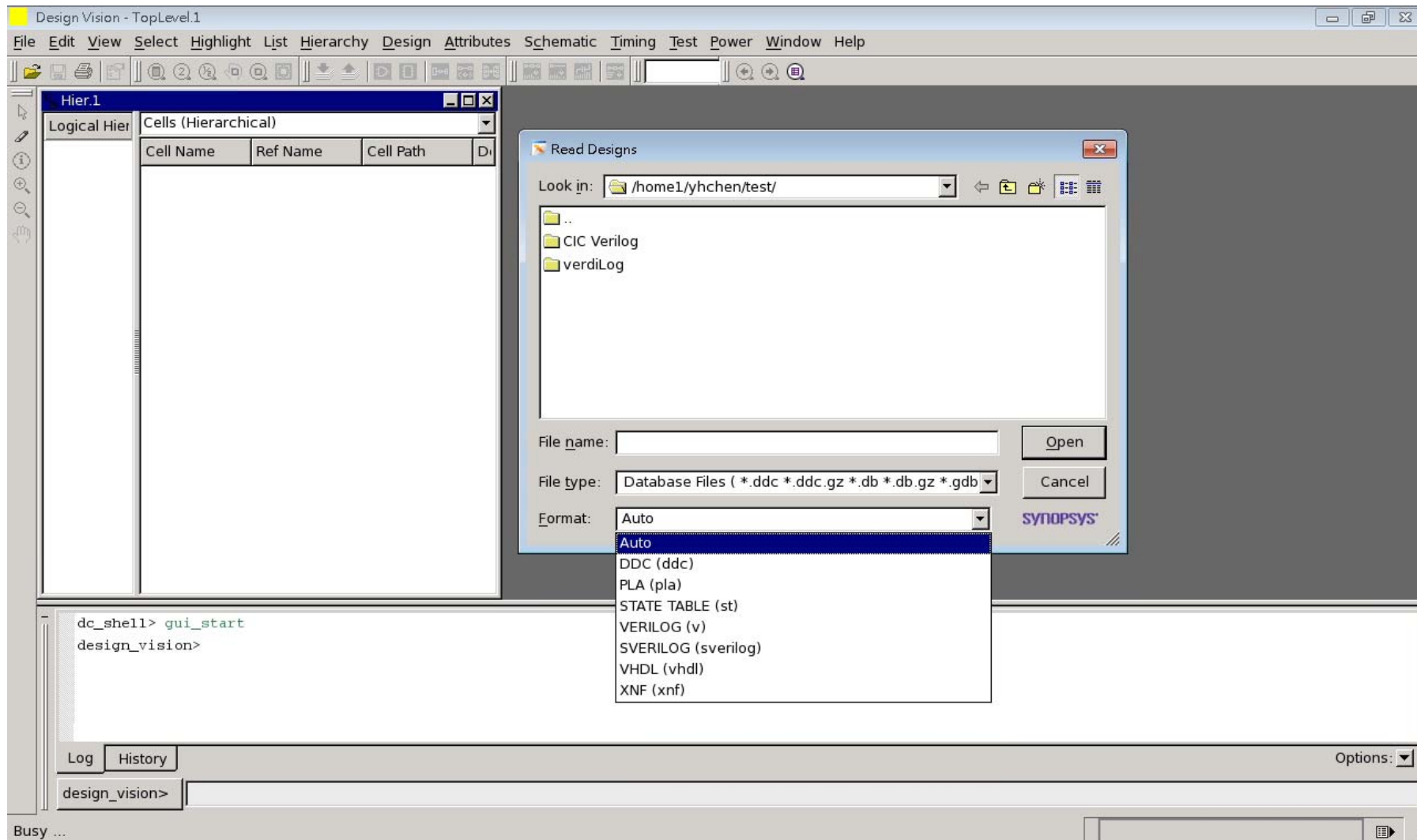
- `%> design_vision-xg`
- `%> dv`



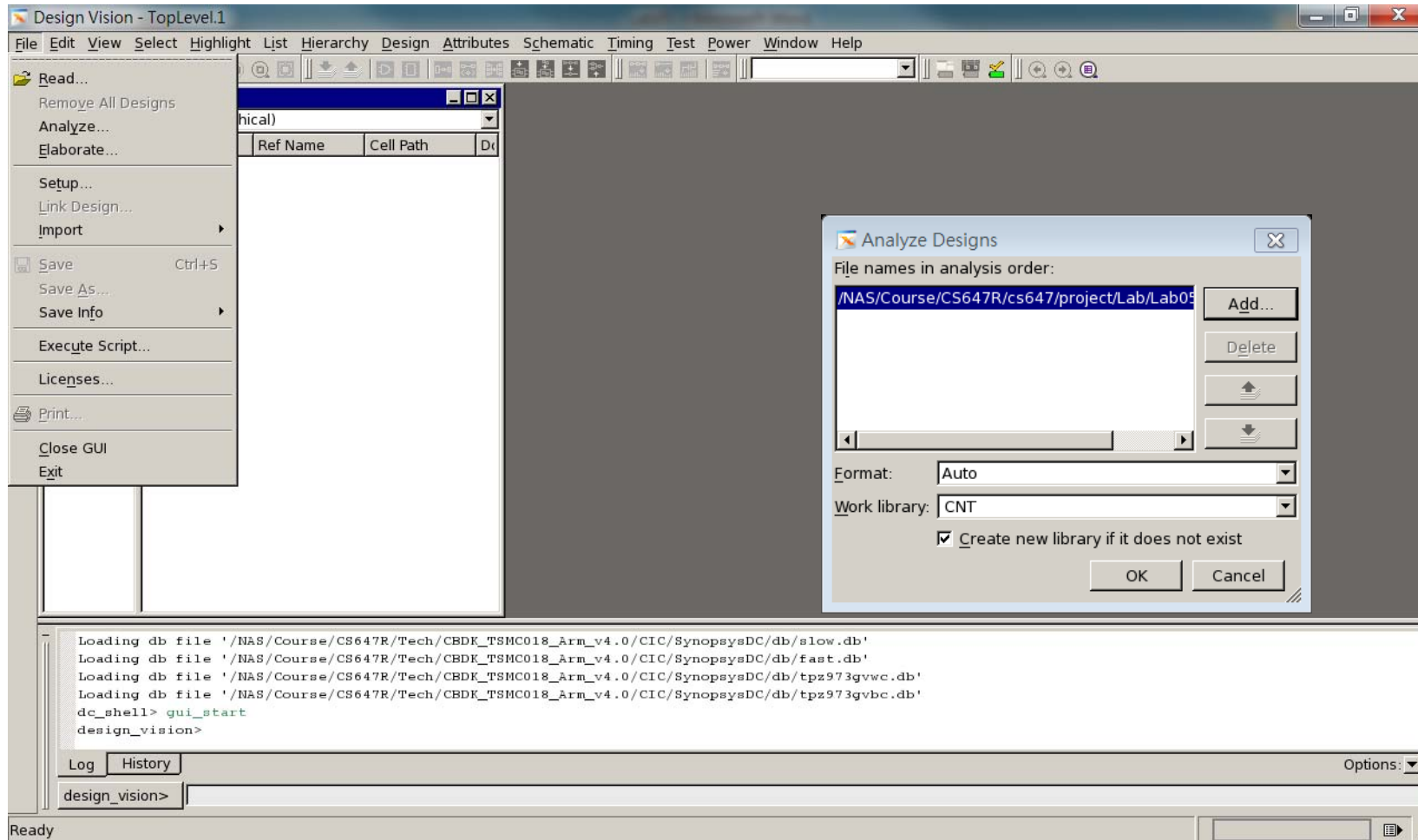
Add Cell Library Path



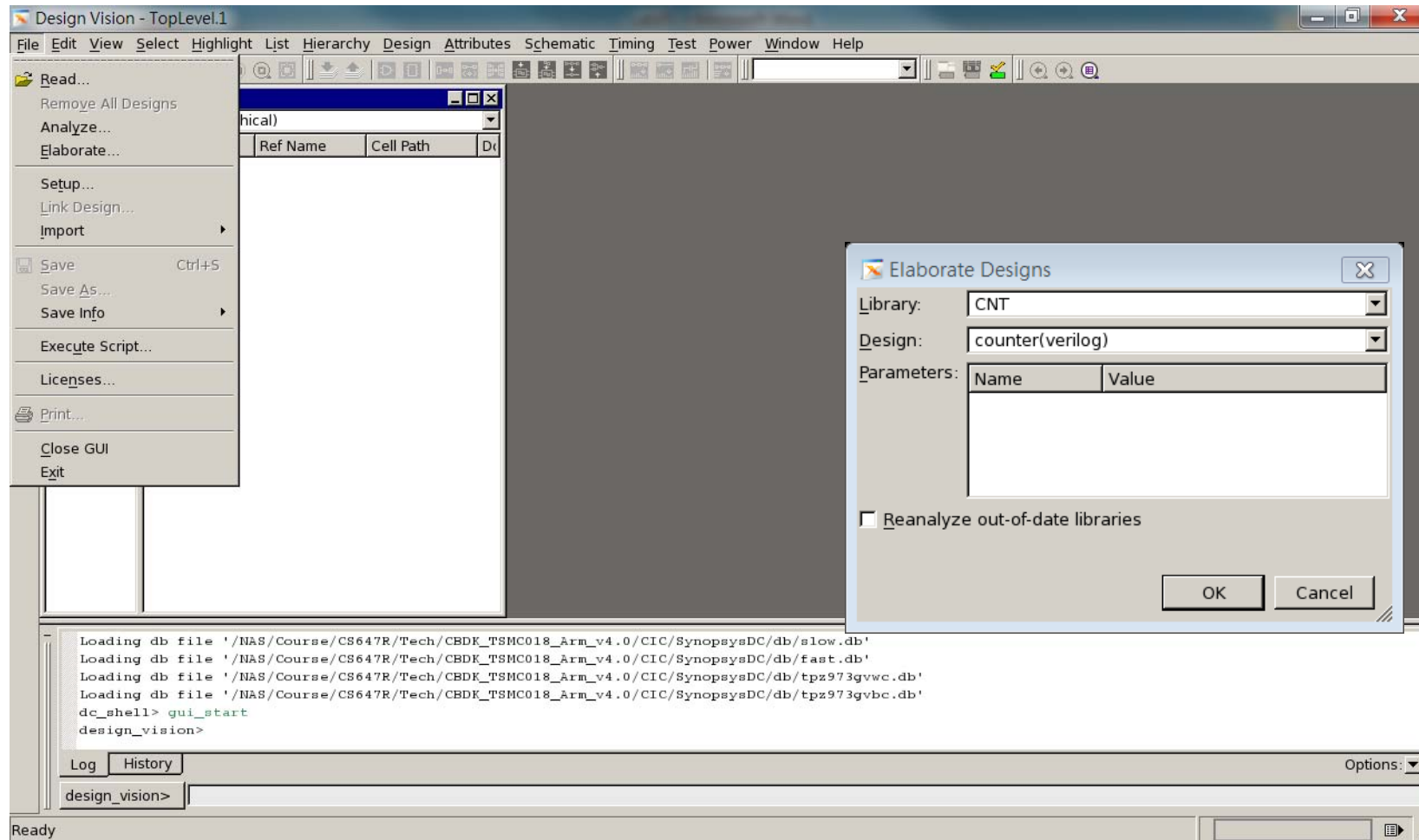
Read Design – Method 1: Read File



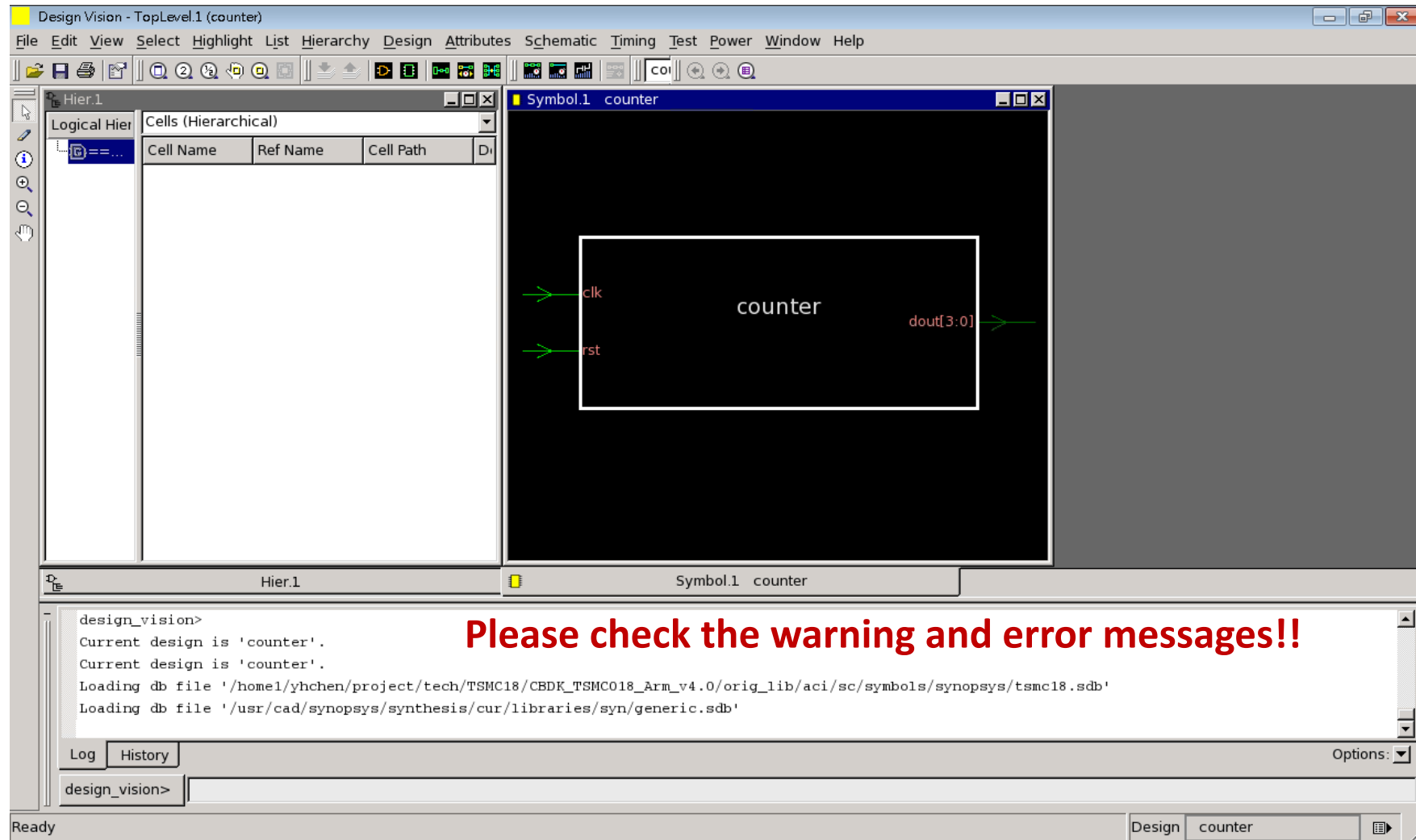
Read Design – Method 2: Analyze



Read Design – Method 2: Elaborate



Read Design

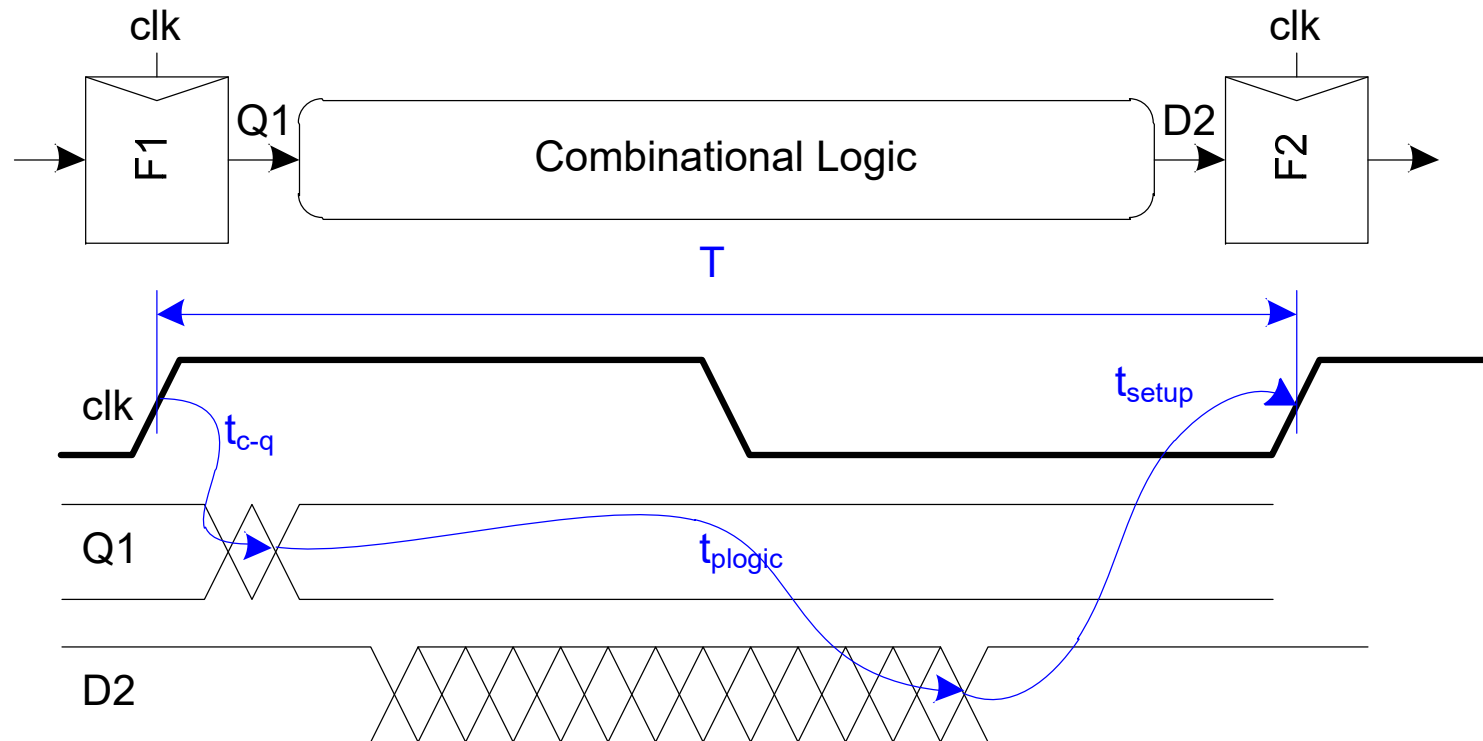


Setting Design Environment

- Operation condition
- Input driving strength
- Output loading
- Input/output delay
- Wire load model

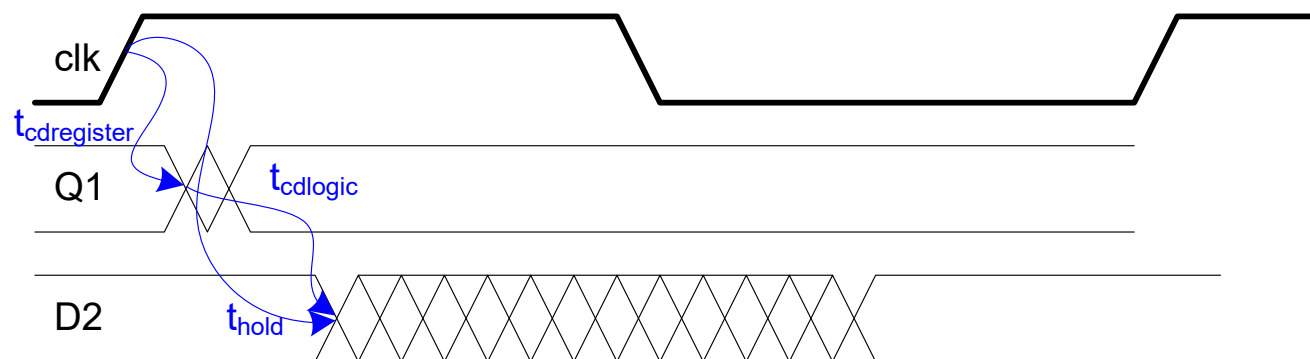
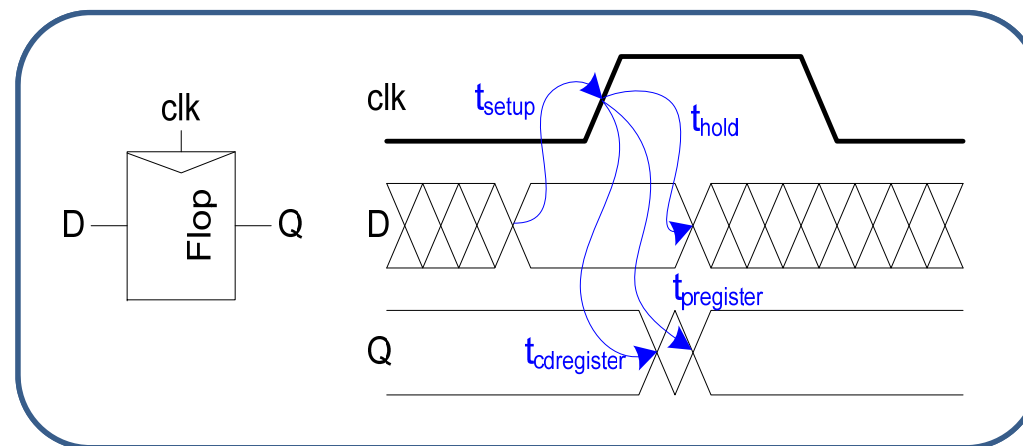
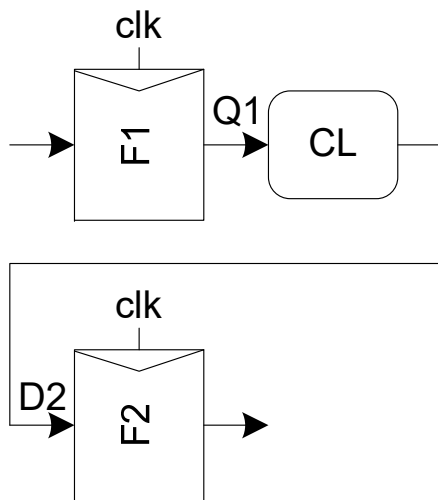
Setup Time → Max. Delay

$$t_{plogic} \leq T - \underbrace{(t_{setup} + t_{c-q})}_{\text{sequencing overhead}}$$

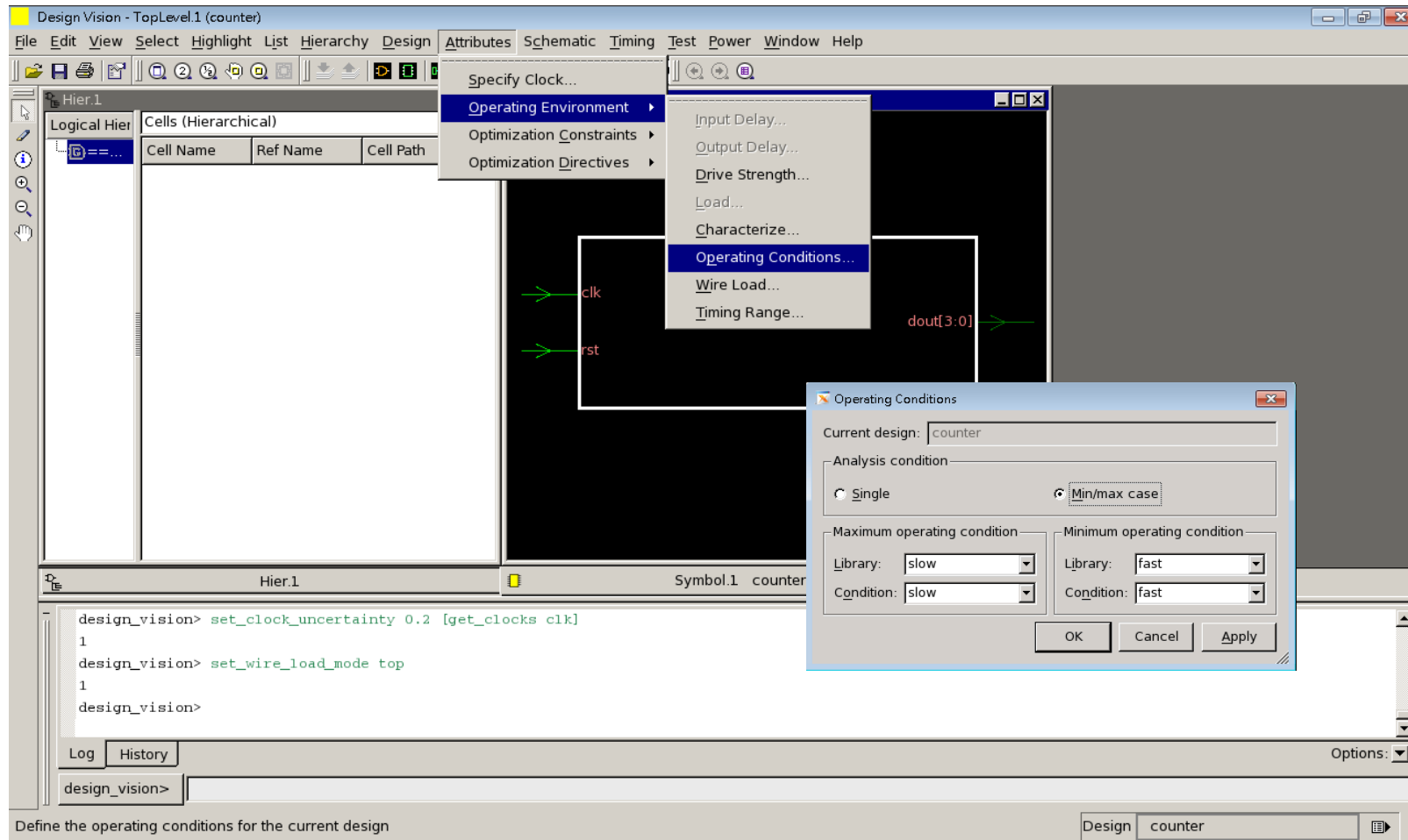


Hold Time → Min. Delay

$$t_{cd\ logic} \geq t_{hold} - t_{cd\ register}$$



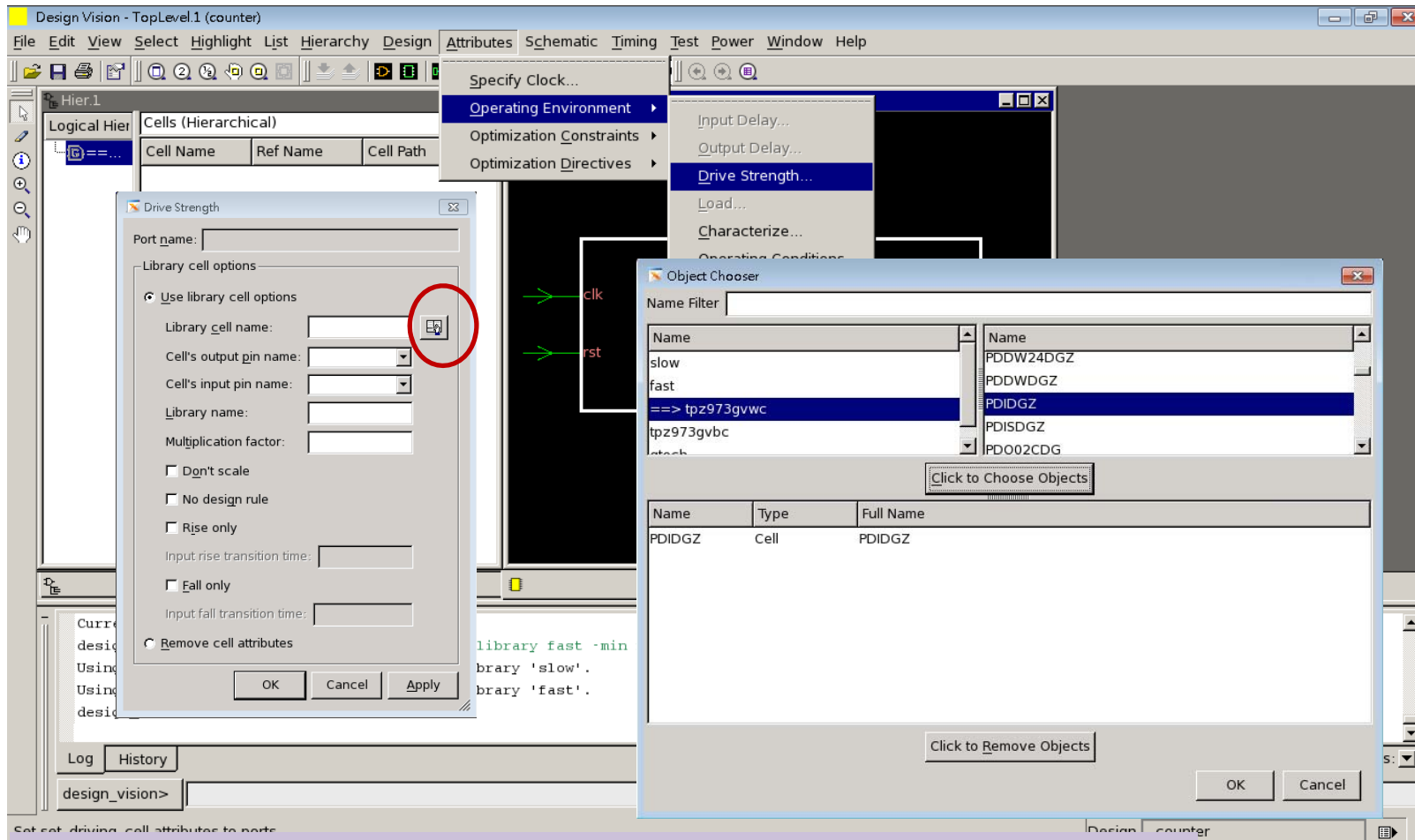
Operation Condition



Max. → setup time check

Min. → hold time check

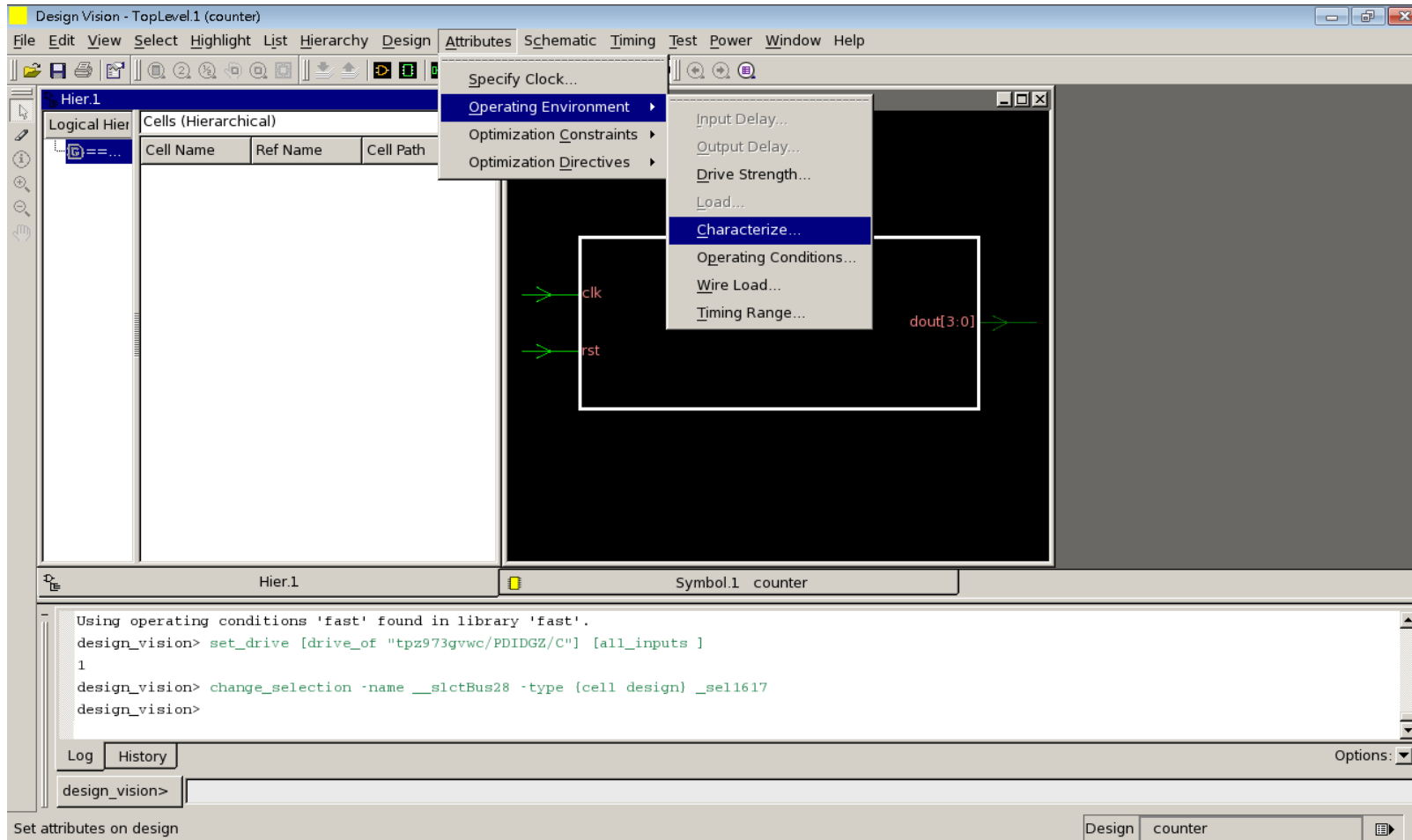
Input Driving Strength



```
set_drive [drive_of "tpz973gvwc/PDIDGZ/C"] [all_inputs]
```

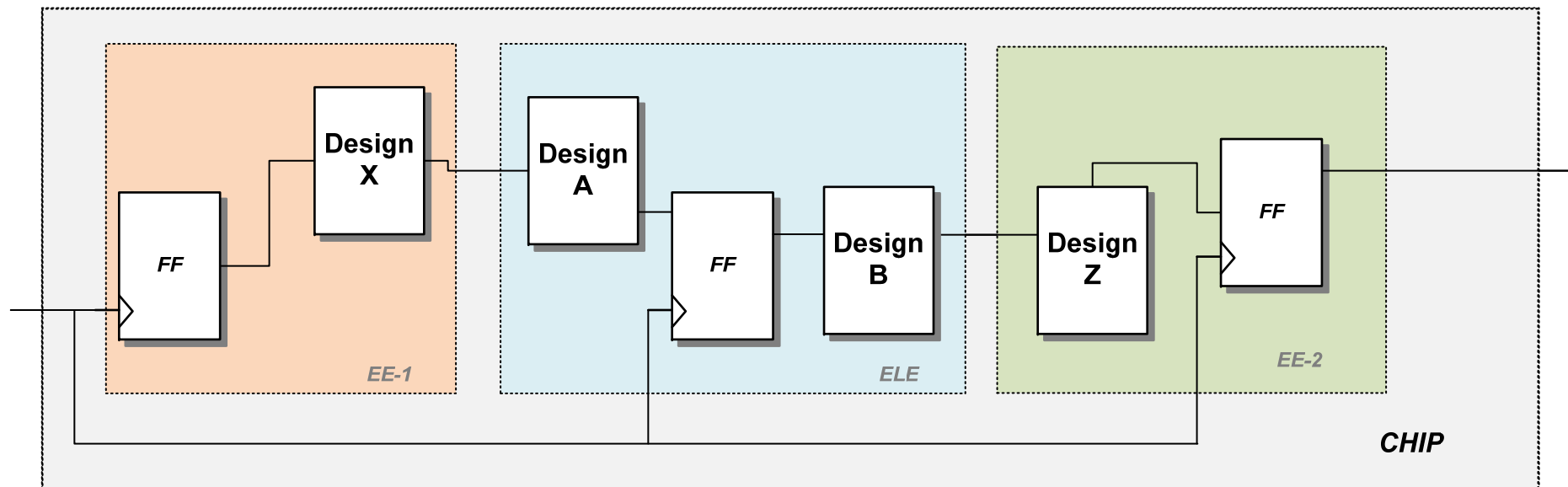
```
set_driving_cell -library tpz973gvwc -lib_cell PDIDGZ -pin {C} [all_inputs]
```

Output Loading



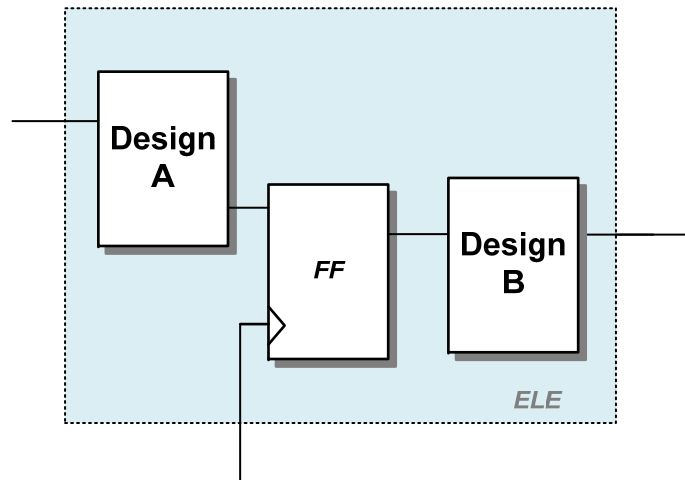
set_load [load_of "tpz973gvwc/PDO08CDG/I"] [all_outputs]

Input/output Delay



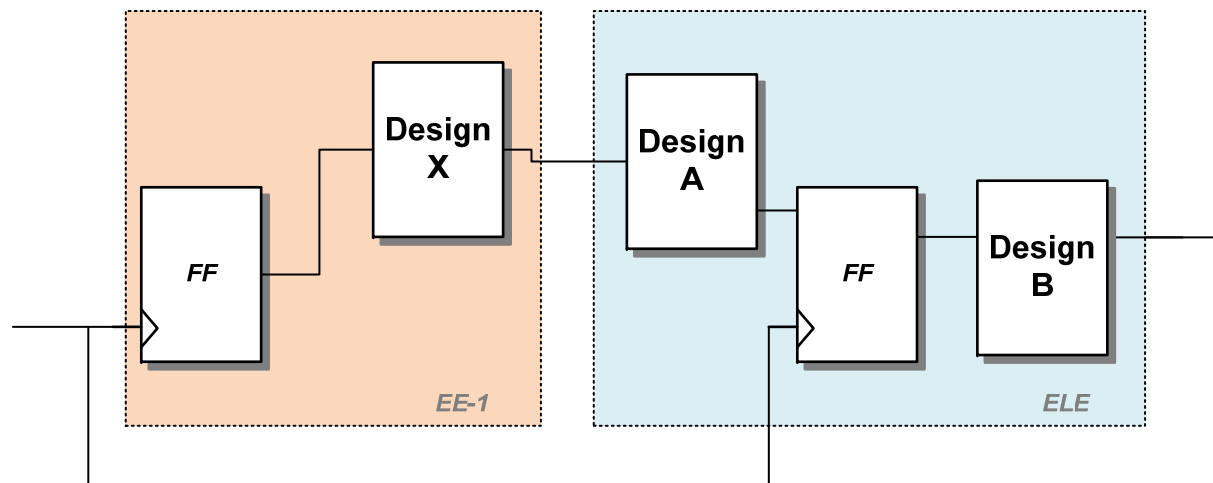
Clock Frequency

- $T = \max(T_A + T_{ff-w}, T_{ff-r} + T_B)$



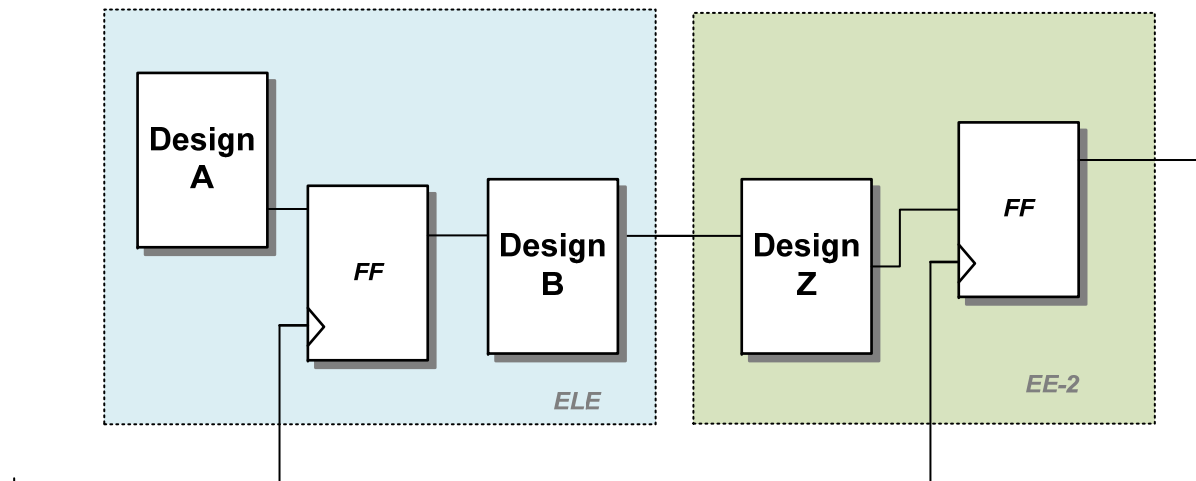
Input Delay

- EE-1: $T_{ff-r} + T_X$
- $T = T_{ff-r} + T_X + T_A + T_{ff-w}$
- **Input Delay = $T_{ff-r} + T_X$**

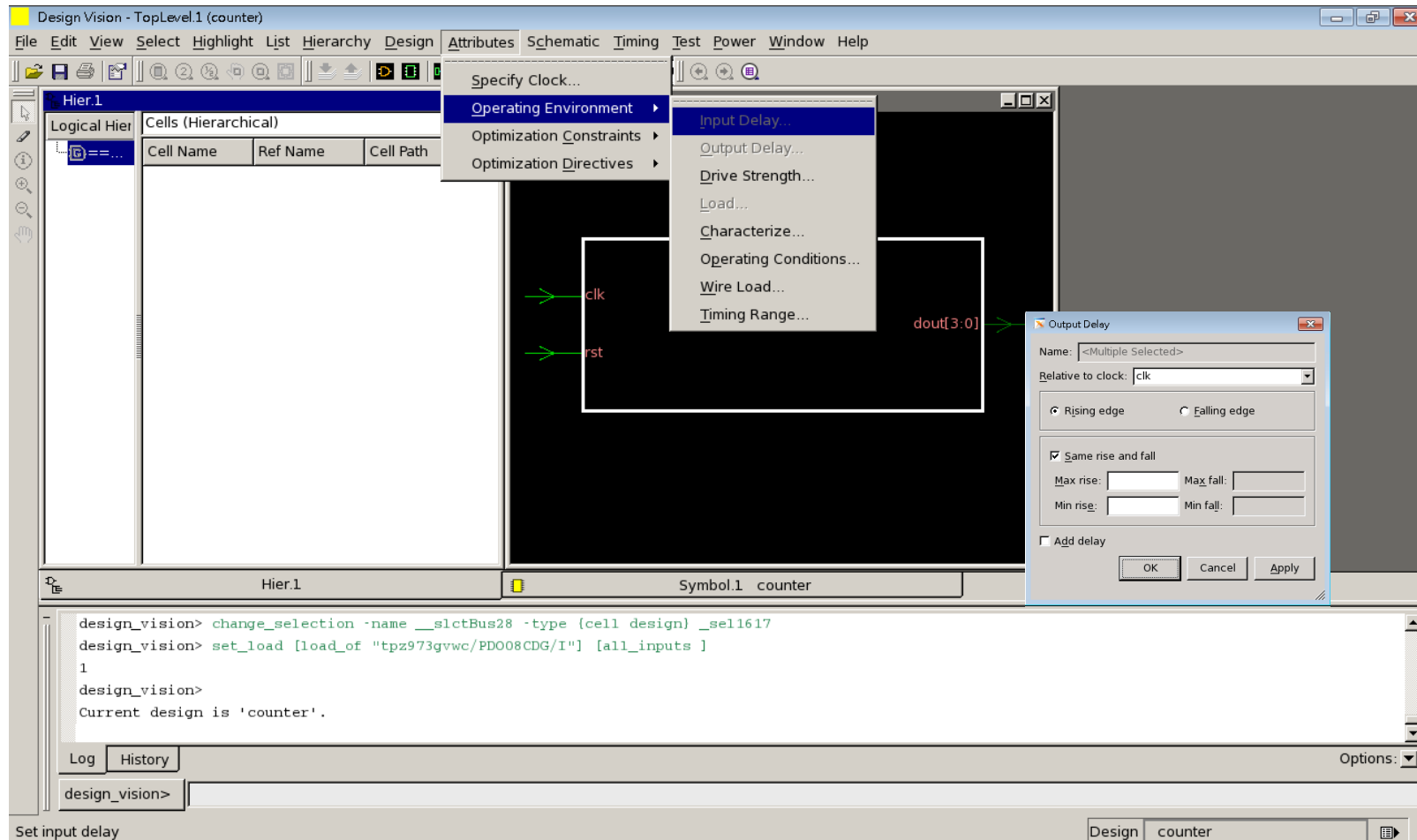


Output Delay

- EE-2: $T_Z + T_{ff-w}$
- $T = T_{ff-r} + T_B + T_Z + T_{ff-w}$
- **Output Delay = $T_Z + T_{ff-w}$**



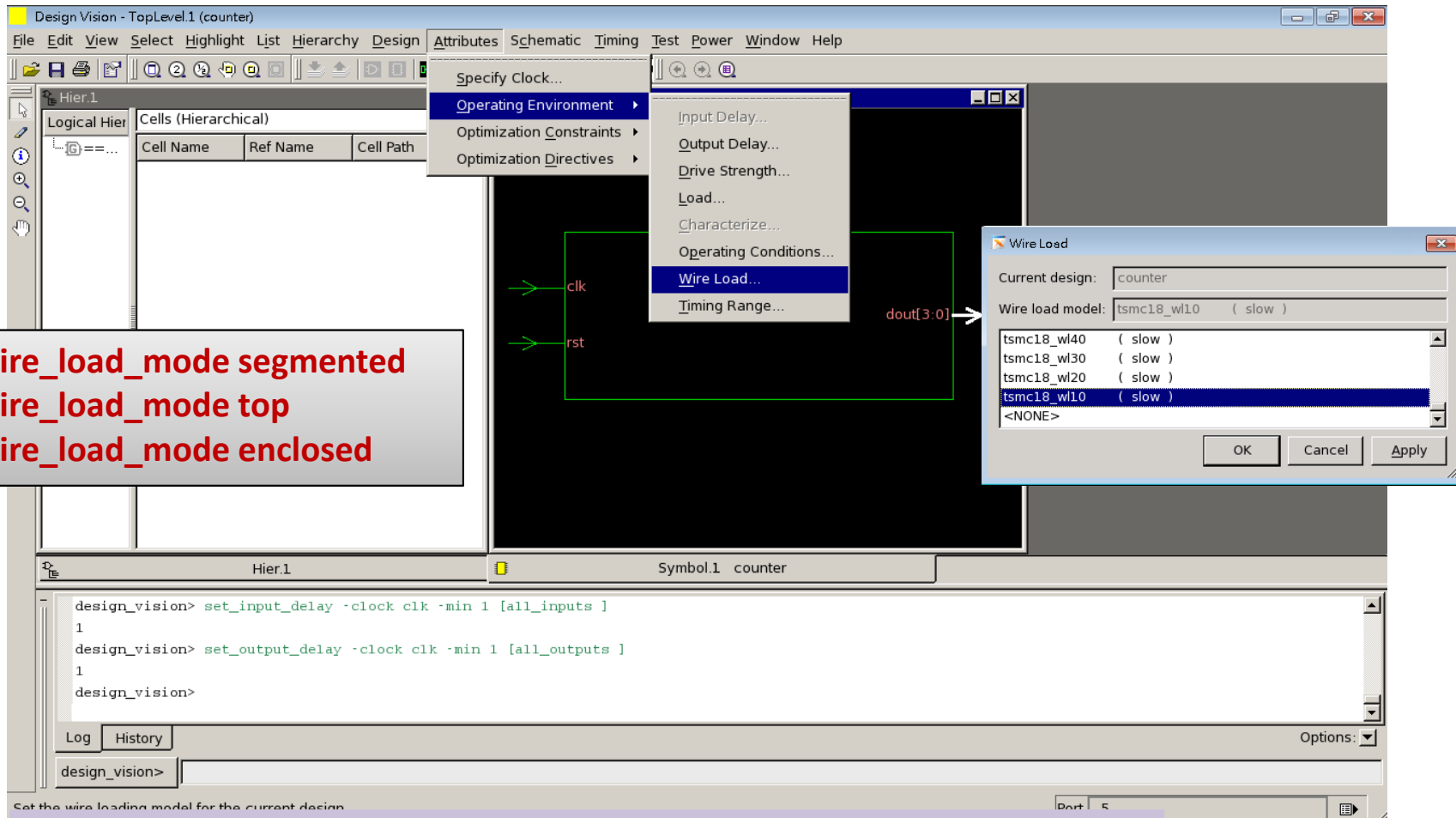
Input/output Delay



set_input_delay -clock clk -max 2 [all_inputs]
set_input_delay -clock clk -min 1 [all_inputs]

set_output_delay -clock clk -max 2 [all_outputs]
set_output_delay -clock clk -min 1 [all_outputs]

Wire Load Model



set_wire_load_mode segmented
set_wire_load_mode top
set_wire_load_mode enclosed

set_wire_load_mode top

set_wire_load_model -name tsmc18_wl10 -library slow

Setting Design Constraints

- **Optimization**
 - Specify clock
 - Period, waveform
 - Clock latency
 - Clock uncertainty
 - Power and area
- **Final check design**

Specify Clock

The screenshot shows the Design Vision software interface. The 'Specify Clock' dialog box is open, showing the 'Clock name' as 'clk', 'Port name' as an empty field, and 'Period' as 10. The 'Clock creation' section shows a table with 'Edge' and 'Value' columns, with 'Rising' at 0 and 'Falling' at 5. The 'Don't touch network' and 'Fix hold' checkboxes are checked. The 'OK' button is highlighted.

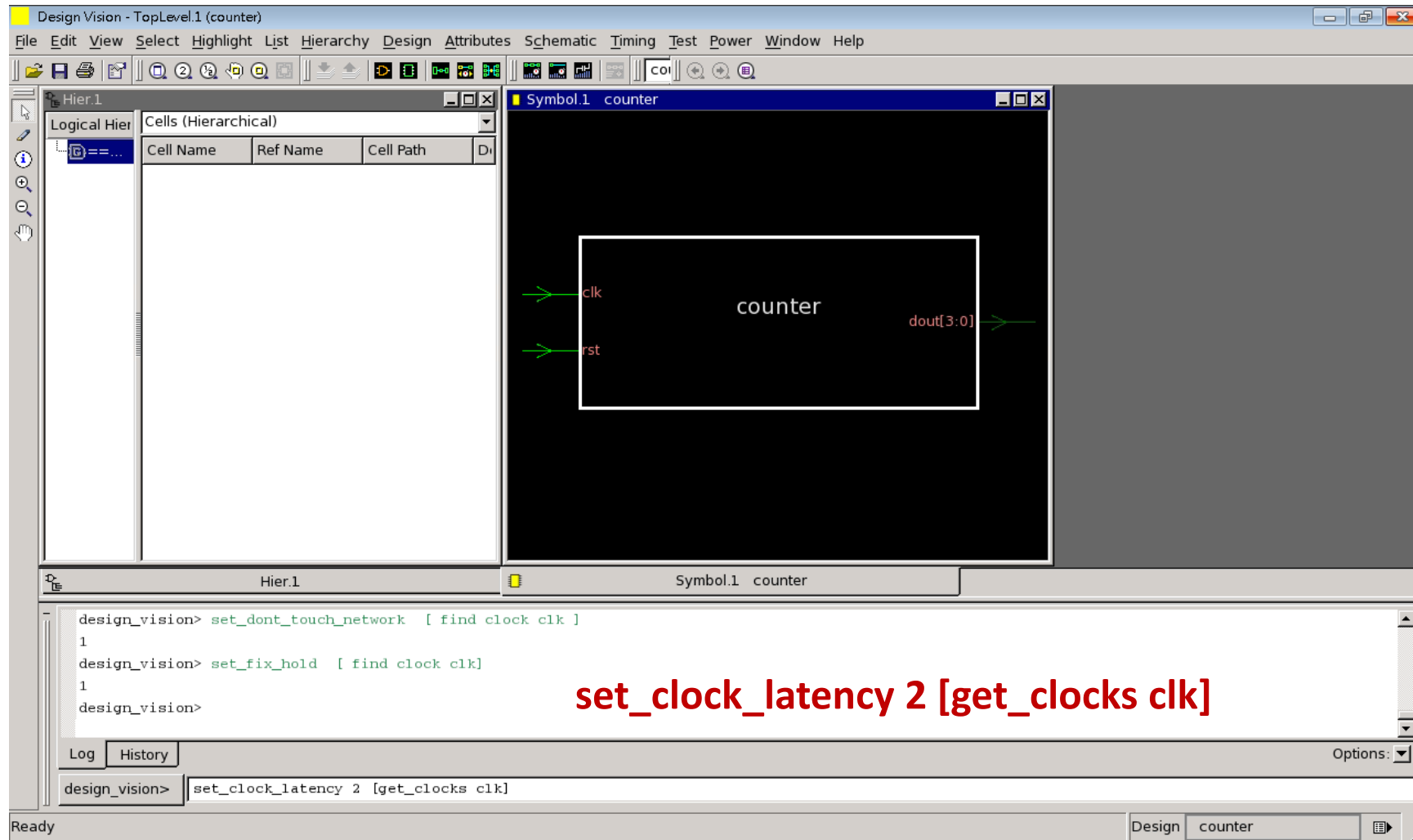
The command window at the bottom shows the following commands and output:

```
design_vision> uplevel #0 check_design
Warning: In design 'counter', cell 'B_0' does not drive any nets. (LINT-1)
design_vision>
```

Below the command window, the following commands are listed in a blue box:

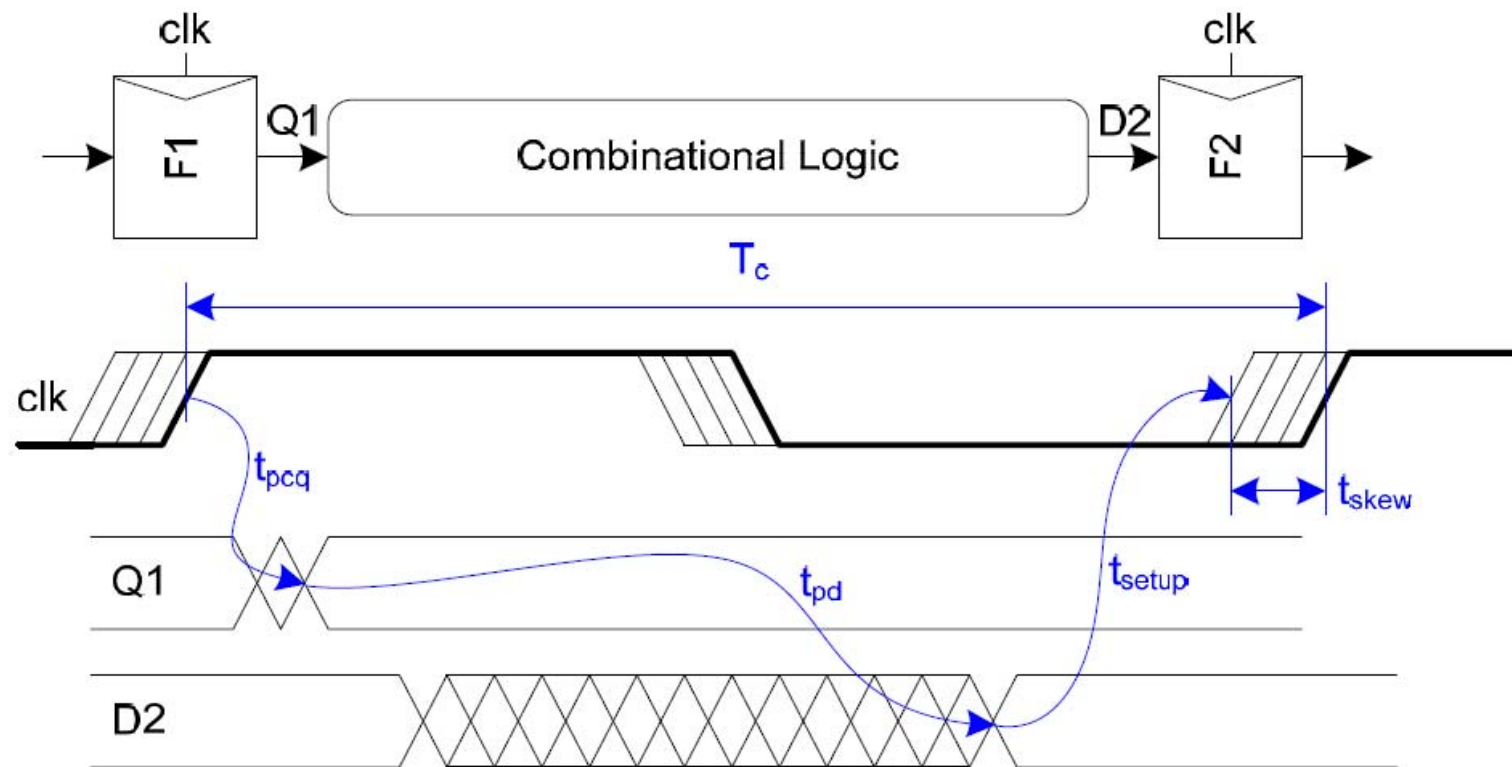
```
create_clock "clk" -period 10 -waveform {0 5}
set_dont_touch_network [ find clock clk ]
set_fix_hold [ find clock clk]
```

Clock Latency

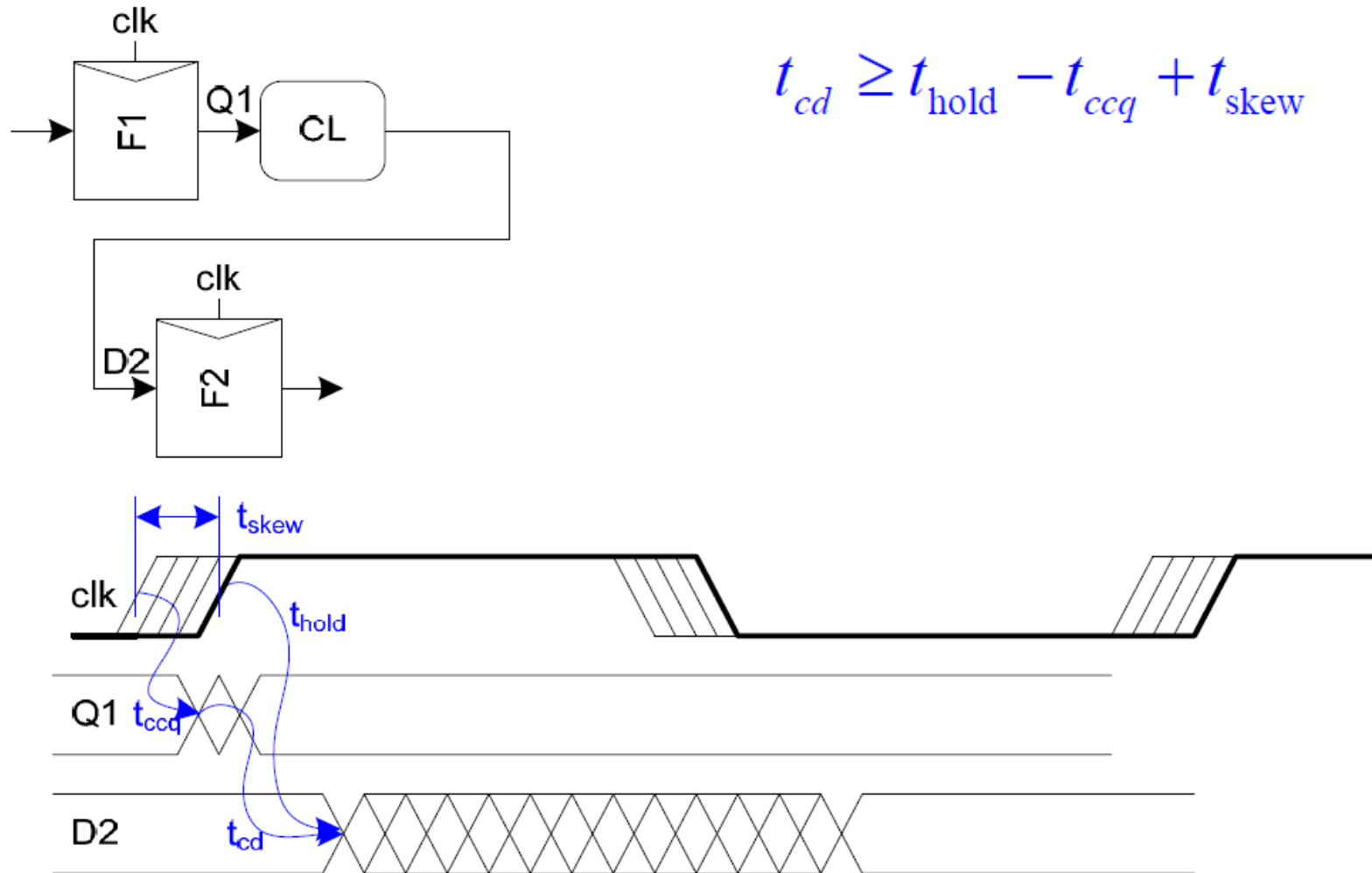


Clock Skew : Setup Time \rightarrow Max. Delay

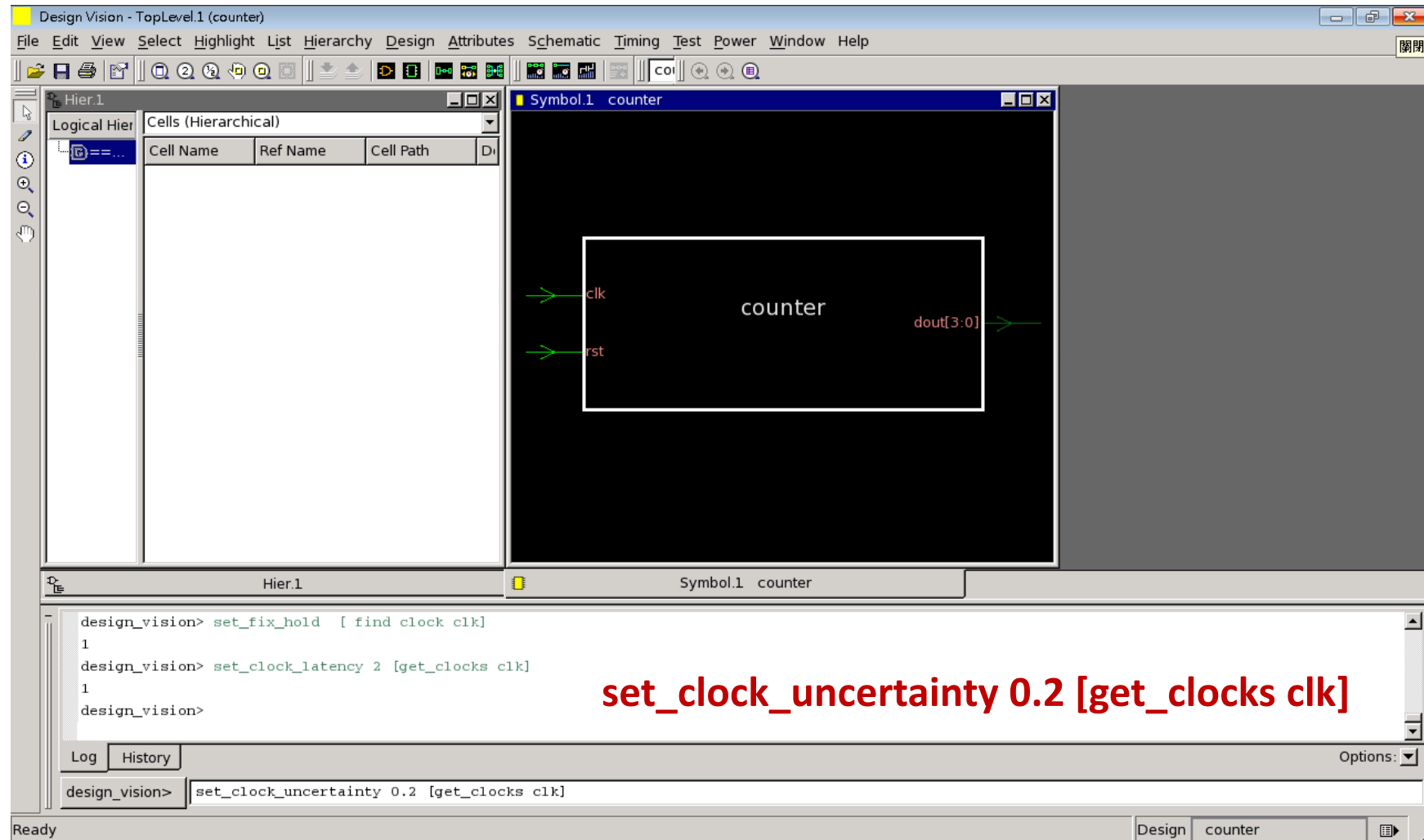
$$t_{pd} \leq T_c - \underbrace{(t_{pcq} + t_{setup} + t_{skew})}_{\text{sequencing overhead}}$$



Clock Skew : Hold Time \rightarrow Min. Delay



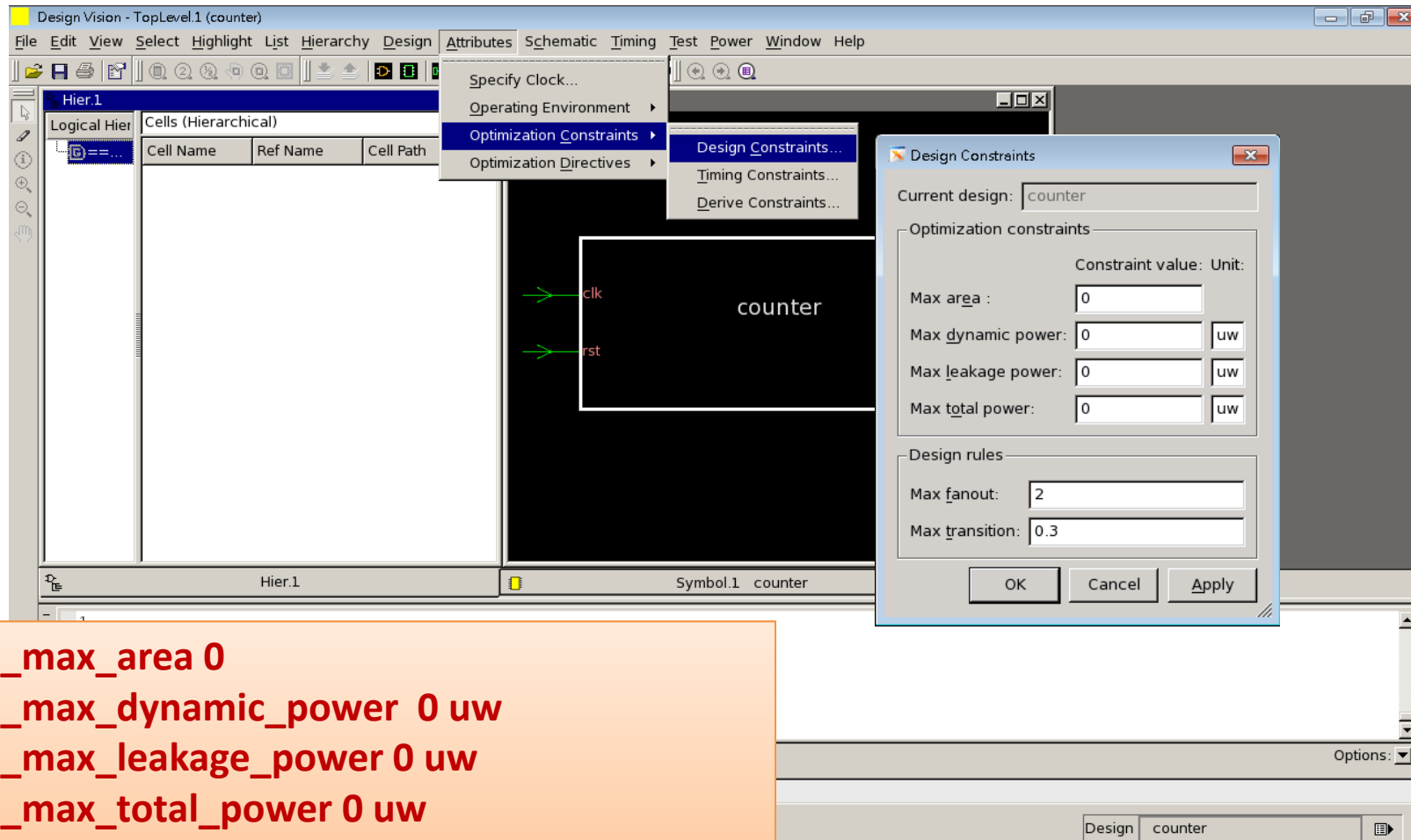
Clock Uncertainty (Skew)



Setting Design Constraints

- Optimization
 - Specify clock
 - Period, waveform
 - Clock latency
 - Clock uncertainty
 - Power and area
- Final check design

Power and Area

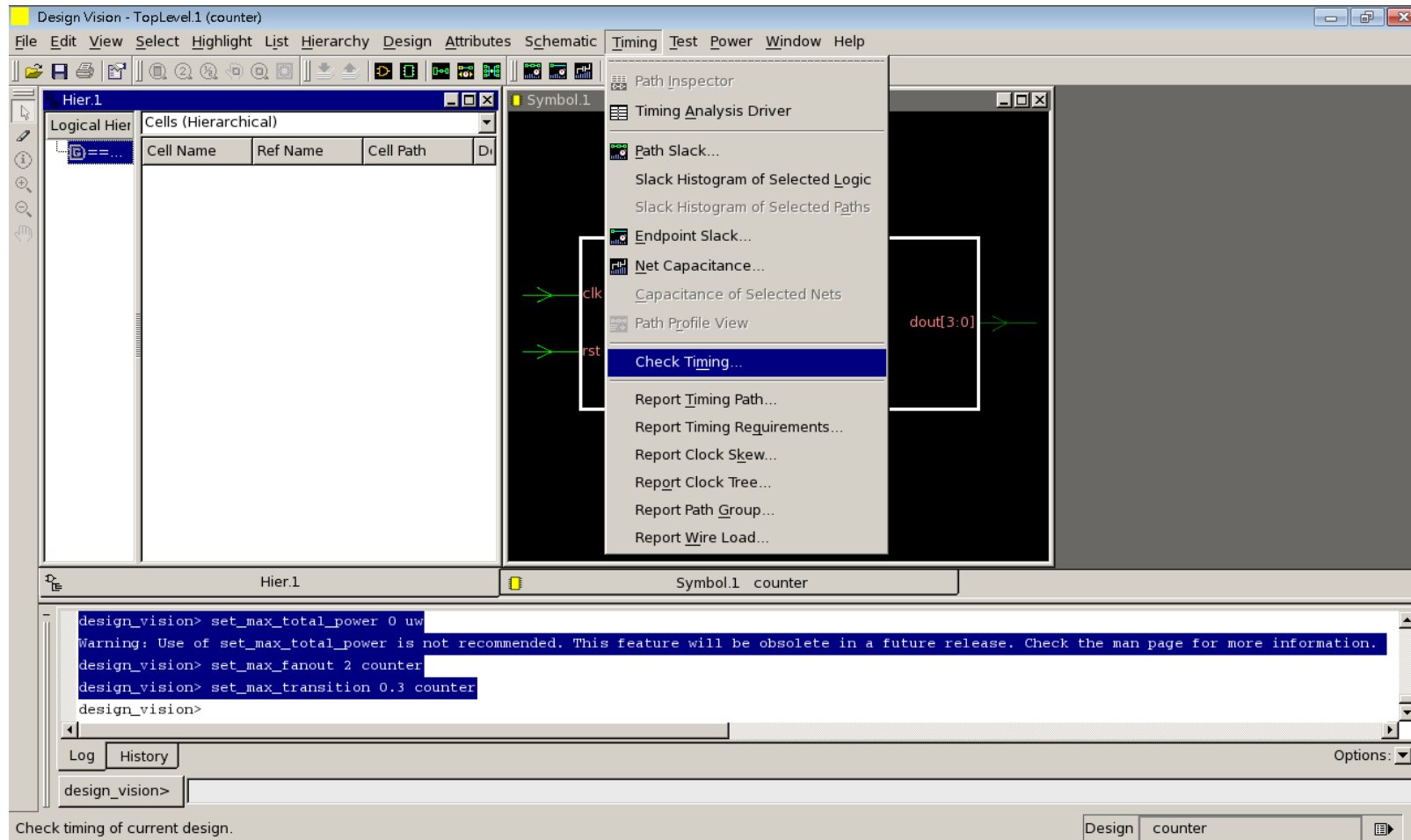


```
set_max_area 0
set_max_dynamic_power 0 uw
set_max_leakage_power 0 uw
set_max_total_power 0 uw
set_max_fanout 2 counter
set_max_transition 0.3 counter
```

Setting Design Constraints

- **Optimization**
 - Specify clock
 - Period, waveform
 - Clock latency
 - Clock uncertainty
 - Power and area
- **Final check design**

Check Timing



Check Design

The screenshot shows the Design Vision software interface. The top menu bar includes File, Edit, View, Select, Highlight, List, Hierarchy, Design, Attributes, Schematic, Timing, Test, Power, Window, and Help. The toolbar contains various icons for file operations and design functions. The main workspace is divided into two panes. The left pane, titled 'Hier.1', shows a hierarchical view of the design with a table for 'Cells (Hierarchical)'. The right pane, titled 'Symbol.1 counter', shows a schematic view of the counter cell. The schematic shows a box labeled 'counter' with two input ports on the left: 'clk' and 'rst', and one output port on the right: 'dout[3:0]'. The bottom pane shows a command window with the following text:

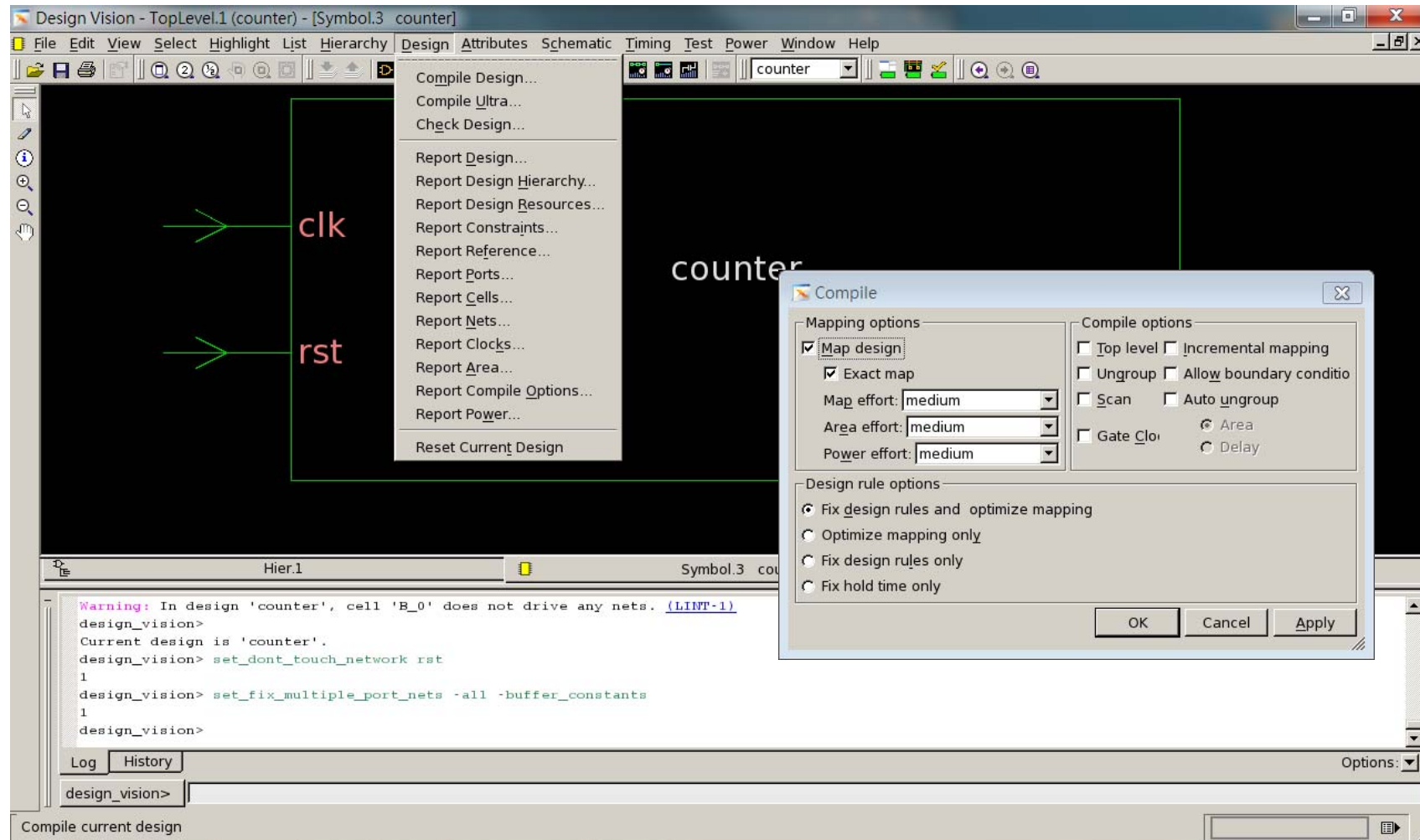
```
Loading db file '/home1/yhchen/project/tech/TSMC18/CBDK_TSMC018_Arm_v4.0/orig_lib/aci/sc/symbols/synopsys/tsmc18.sdb'  
Loading db file '/usr/cad/synopsys/synthesis/cur/libraries/syn/generic.sdb'  
design_vision> uplevel #0 check_design  
Warning: In design 'counter', cell 'B_0' does not drive any nets. (LINT-1)  
design_vision>
```

A red text box with the message "Please check all warning and error messages!!" is overlaid on the command window. The status bar at the bottom shows "Ready" and "Design counter".

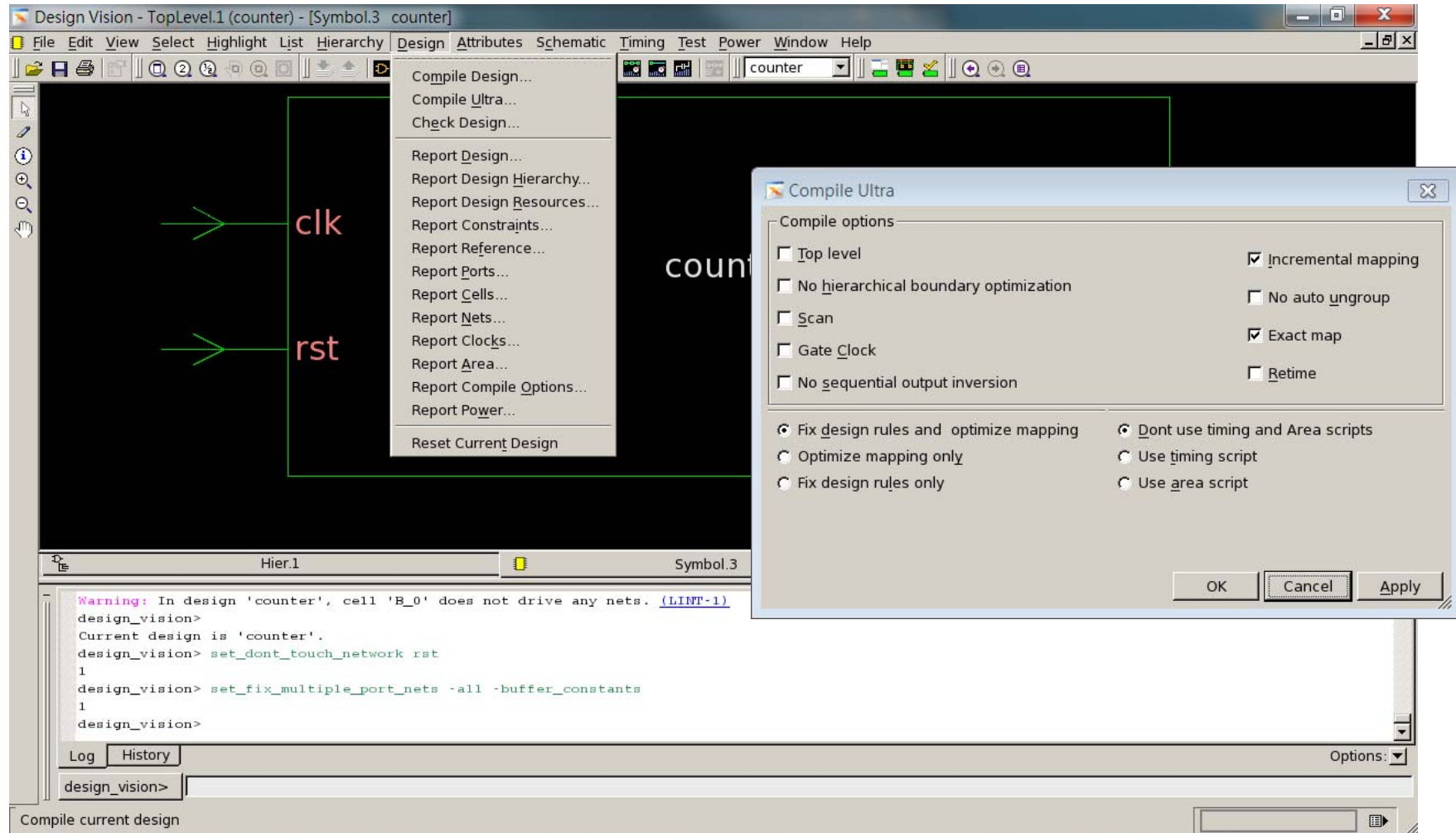
Compile and Report

- **Compile design**
 - Map effort
 - Area effort
 - Power effort
- **Report design**
 - Design
 - Area
 - Power
 - Delay

Compile Design



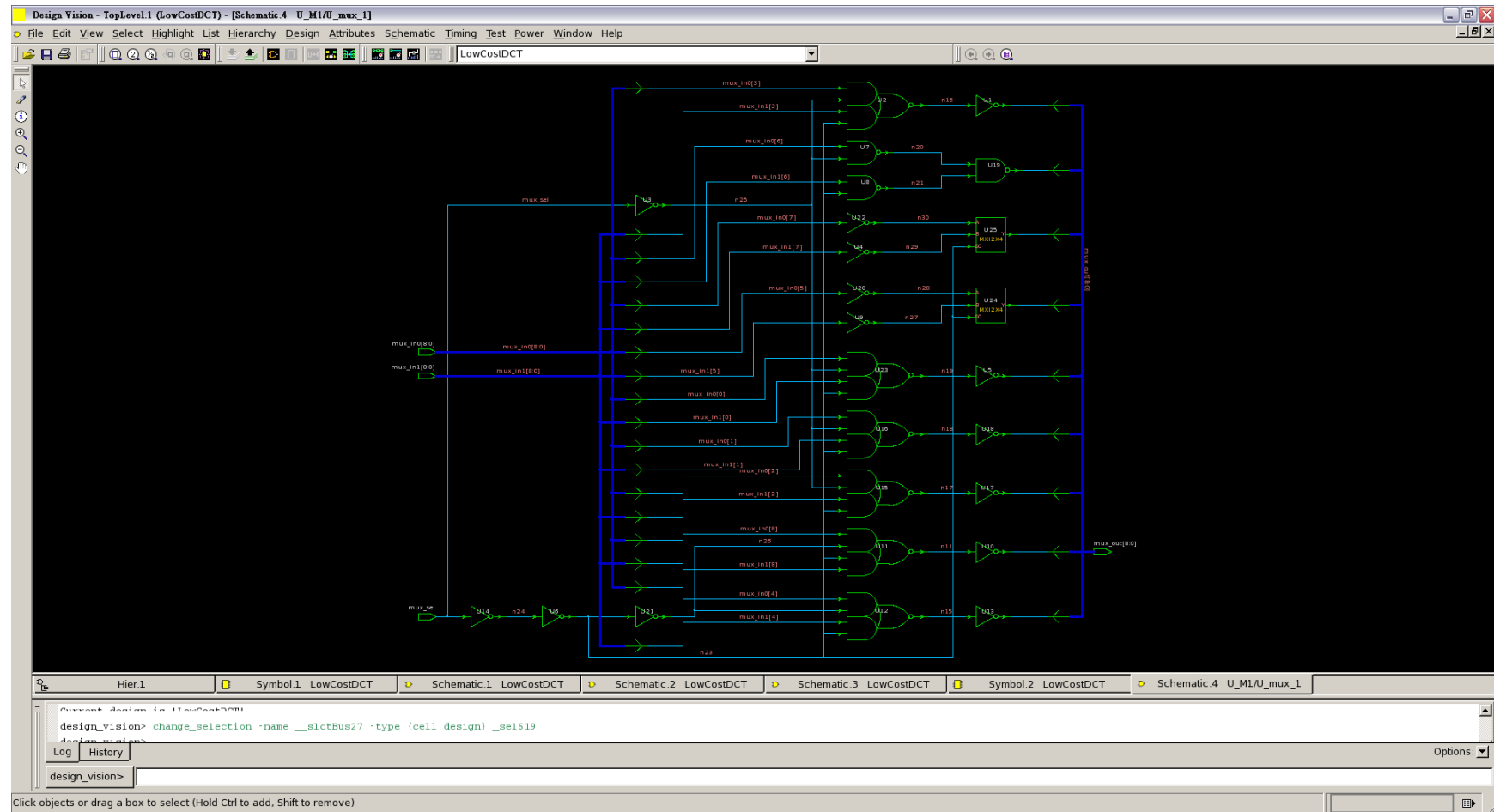
Compile Ultra



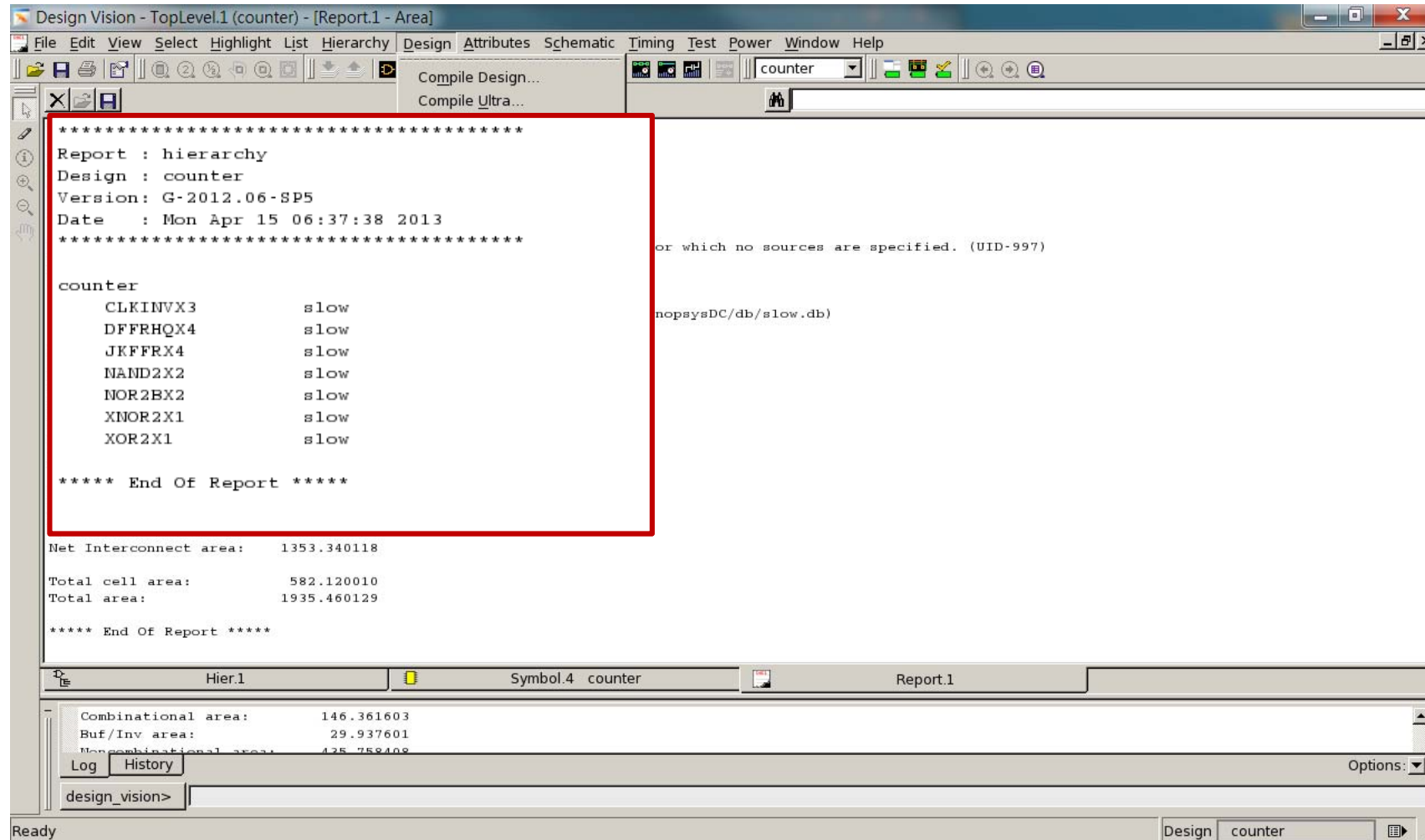
Compile and Report

- **Compile design**
 - Map effort
 - Area effort
 - Power effort
- **Report design**
 - Design
 - Area
 - Power
 - Delay

Design Hierarchy



Report Hierarchy



Report Reference

Design Vision - TopLevel1 (counter) - [Report.1 - Area]

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help

Compile Design...
Compile Ultra...
Check Design...

counter

Report : area
Design : counter
Version: G-2012.06-SP5
Date : Mon Apr 15 06:36:12 2013

Warning: The set_dont_touch...
Information: Updating de...
Library(s) Used:

slow (File: /NAS/Cou...)

Number of ports:
Number of nets:
Number of cells:
Number of combinational
Number of sequential cel
Number of macros:
Number of buf/inv:
Number of references:

Combinational area:
Buf/Inv area:
Noncombinational area:
Net Interconnect area:

Total cell area:
Total area:

***** End Of Report *****

Report : reference
Design : counter
Version: G-2012.06-SP5
Date : Mon Apr 15 06:36:12 2013

Attributes:

- b - black box (unknown)
- bo - allows boundary optimization
- d - dont_touch
- mo - map_only
- h - hierarchical
- n - noncombinational
- r - removable
- s - synthetic operator
- u - contains unmapped logic

Reference	Library	Unit Area	Count	Total Area	Attributes
CLKINVX3	slow	9.979200	3	29.937601	
DFFRHQX4	slow	106.444801	3	319.334404	n
JKFFRX4	slow	116.424004	1	116.424004	n
NAND2X2	slow	16.632000	1	16.632000	
NOR2BX2	slow	19.958401	1	19.958401	
XNOR2X1	slow	26.611200	1	26.611200	
XOR2X1	slow	26.611200	2	53.222401	
Total 7 references				582.120010	

***** End Of Report *****

Hier.1

Combinational area:
Buf/Inv area:
Noncombinational area:

Log History

design_vision>

Ready

Design counter

Report Area

```
*****
Report : area
Design : counter
Version : G-2012.06-SP5
Date : Mon Apr 15 06:34:13 2013
*****

Warning: The set_dont_touch_network command is used for clock clk, for which no sources are specified. (UID-997)
Information: Updating design information... (UID-85)
Library(s) Used:

slow (File: /NAS/Course/CS647R/Tech/CBDK_TSMC018_Arm_v4.0/CIC/SynopsysDC/db/slow.db)

Number of ports: 6
Number of nets: 15
Number of cells: 12
Number of combinational cells: 8
Number of sequential cells: 4
Number of macros: 0
Number of buf/inv: 3
Number of references: 7

Combinational area: 146.361603
Total Buf/Inv area: 29.937601
Total Noncombinational area: 435.758408
Net Interconnect area: 1353.340118

Total cell area: 582.120010
Total area: 1935.460129

***** End Of Report *****
```

Report Power

Design Vision - TopLevel1 (counter) - [Report.1 - Area]

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help

Compile Design...

counter

Global Operating Voltage = 1.62

**** Power-specific unit information :
 Voltage Units = 1V
 Capacitance Units = 1.000000pf
 Time Units = 1ns
 Dynamic Power Units = 1mW (derived from V,C,T units)
 Leakage Power Units = 1pW

Cell Internal Power = 4.7535 uW (74%)
 Net Switching Power = 1.6905 uW (26%)

 Total Dynamic Power = 6.4440 uW (100%)

Cell Leakage Power = 26.3388 nW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

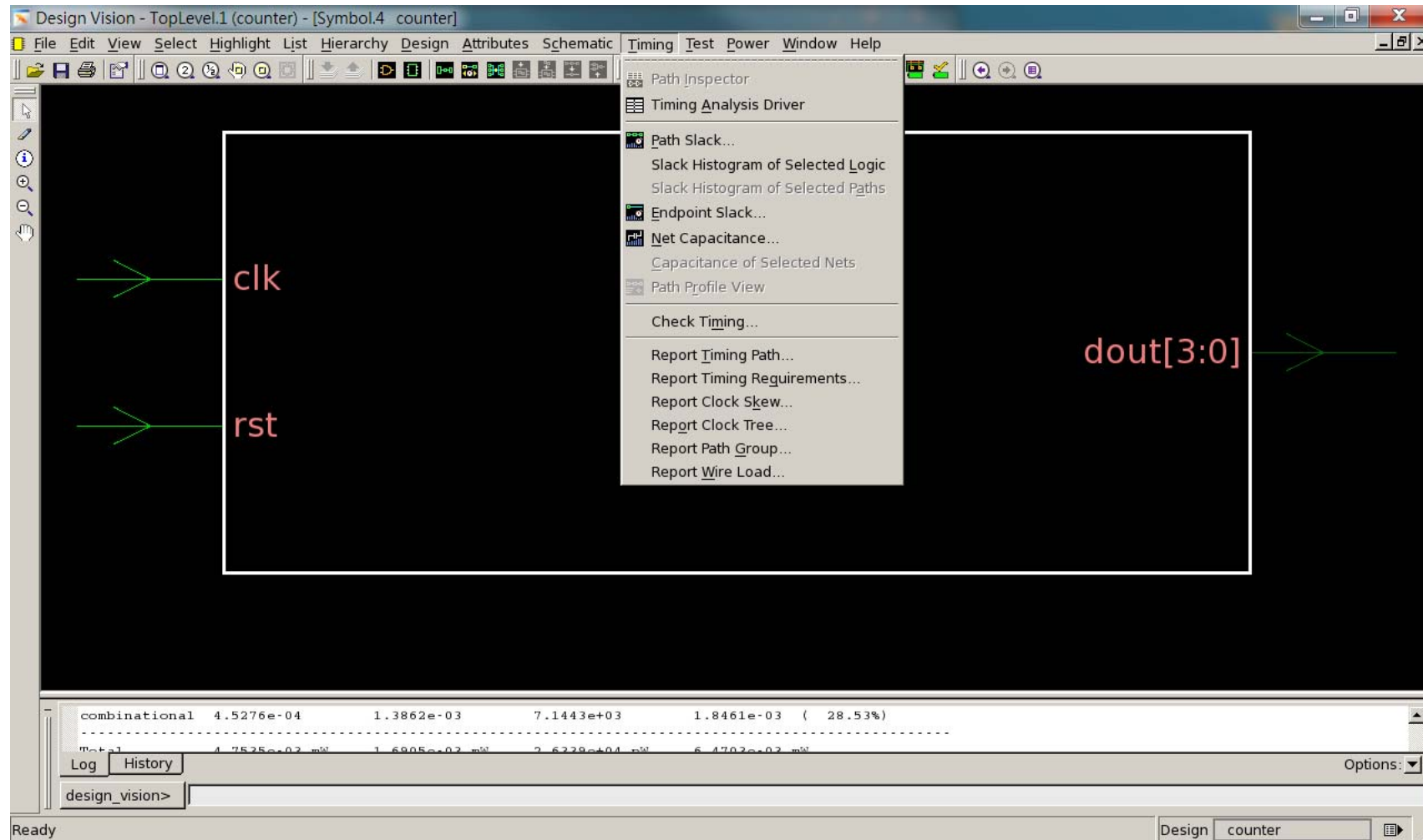
Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)	
register	0.0000	0.0000	0.0000	0.0000	(0.00%)	
sequential	4.3008e-03	3.0432e-04	1.9195e+04	4.6243e-03	(71.47%)	
combinational	4.5276e-04	1.3862e-03	7.1443e+03	1.8461e-03	(28.53%)	
Total	4.7535e-03 mW	1.6905e-03 mW	2.6339e+04 pW	6.4703e-03 mW		

***** End Of Report *****

Ready

Design counter

Report Timing



Report Timing

	Des/Clust/Port	Wire Load Model	Library
Report : timing	counter	tsmc18_wl10	slow
-path full			
-delay max	Point		Incr Path
-max_paths 1			
Design : counter	clock clk (rise edge)		0.00 0.00
Version: G-2012.06-SP5	clock network delay (ideal)		0.00 0.00
Date : Mon Apr 15 06:52:36	input external delay		0.00 0.00 r
*****	dout_reg_0_/CK (JKFFRXL)		0.00 0.00 r
	dout_reg_0_/Q (JKFFRXL)		1.55 1.55 r
Operating Conditions: slow	U9/Y (NAND2X1)		0.34 1.89 f
Wire Load Model Mode: top	U11/Y (NOR2BX1)		0.34 2.22 r
	U10/Y (XOR2X1)		0.33 2.56 f
	dout_reg_3_/D (DFFRHQX1)		0.00 2.56 f
Startpoint: dout_reg_0_/CK	data arrival time		2.56
(internal path			
Endpoint: dout_reg_3_	clock clk (rise edge)		10.00 10.00
(rising edge-trig	clock network delay (ideal)		0.00 10.00
Path Group: clk	dout_reg_3_/CK (DFFRHQX1)		0.00 10.00 r
Path Type: max	library setup time		-0.37 9.63
	data required time		9.63
	data required time		9.63
	data arrival time		-2.56
	slack (MET)		7.07

Slack

- **Slack must be positive or zero in a design.**
- **Negative slack means violate constraints.**
- **Setup time (max delay):**
 - $\text{Slack} = \text{data required time} - \text{data arrival time} \geq 0;$
- **Hold time (min delay):**
 - $\text{Slack} = \text{data arrival time} - \text{data required time} \geq 0;$

Save Design

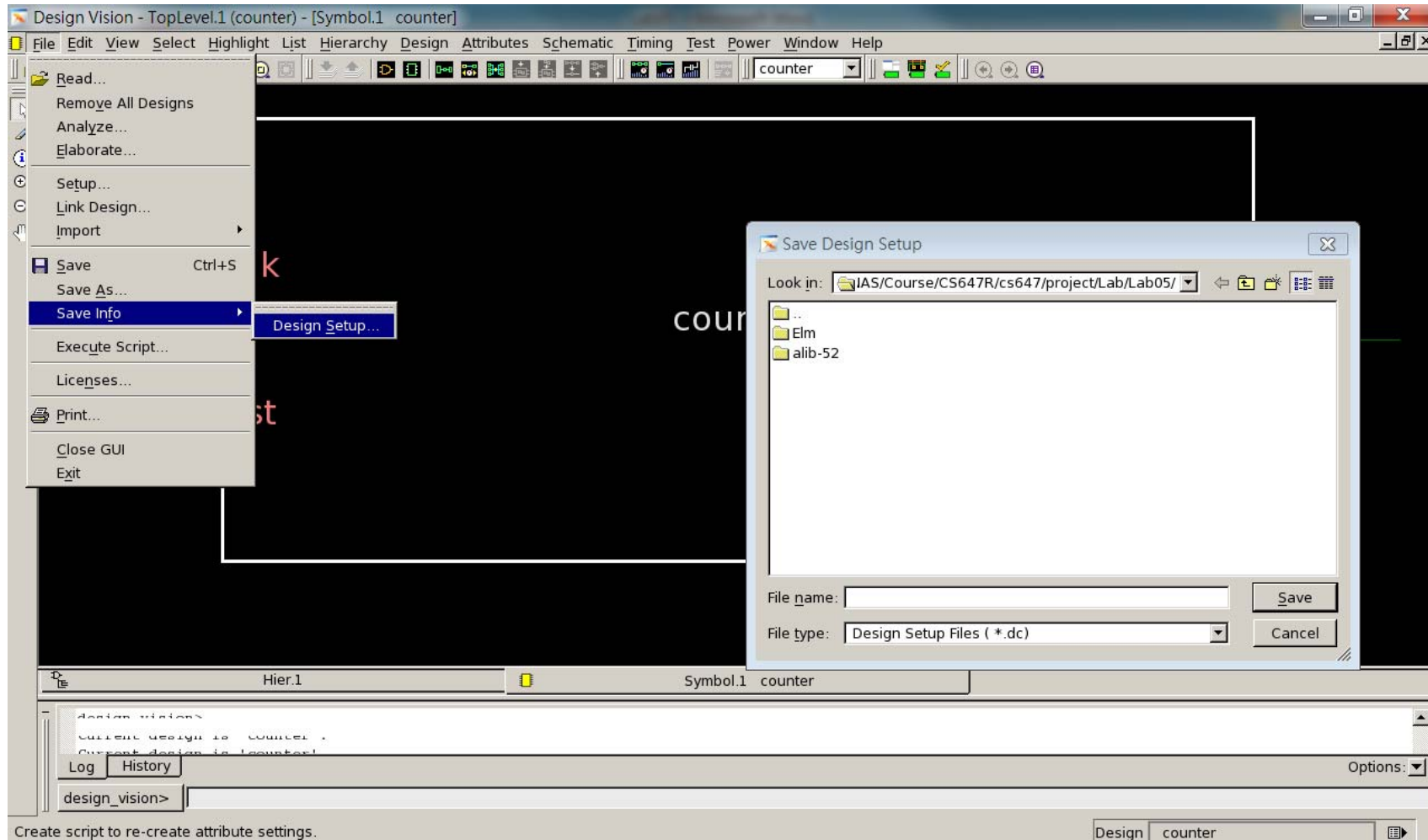
- **Change naming rule**
 - Script
- **Save design**
 - Design setup file
 - Timing file
 - Netlist
 - Design
 - Script

Change Naming Rule

```
current_design [get_designs $mydesign]
remove_unconnected_ports -blast_buses [get_cells * -hier]
set bus_inference_style {%s[%d]}
set bus_naming_style {%s[%d]}
set hdlout_internal_busses true
change_names -hierarchy -rule verilog
define_name_rules name_rule -allowed {a-z A-Z 0-9 _} -max_length 255 -type cell
define_name_rules name_rule -allowed {a-z A-Z 0-9 _[]} -max_length 255 -type net
define_name_rules name_rule -map {"\\*cell\\" "*" "cell"}
define_name_rules name_rule -case_insensitive
change_names -hierarchy -rules name_rule
```

No assign or other key-word !!

Save Design Setup File



Save Design Timing File

The screenshot displays the Design Vision software interface. The top window shows a schematic diagram of a counter circuit with components like registers (dout_reg_0, dout_reg_1, dout_reg_2, dout_reg_3) and logic gates (U12, U13, U11, U10). The bottom window shows a terminal with the following text:

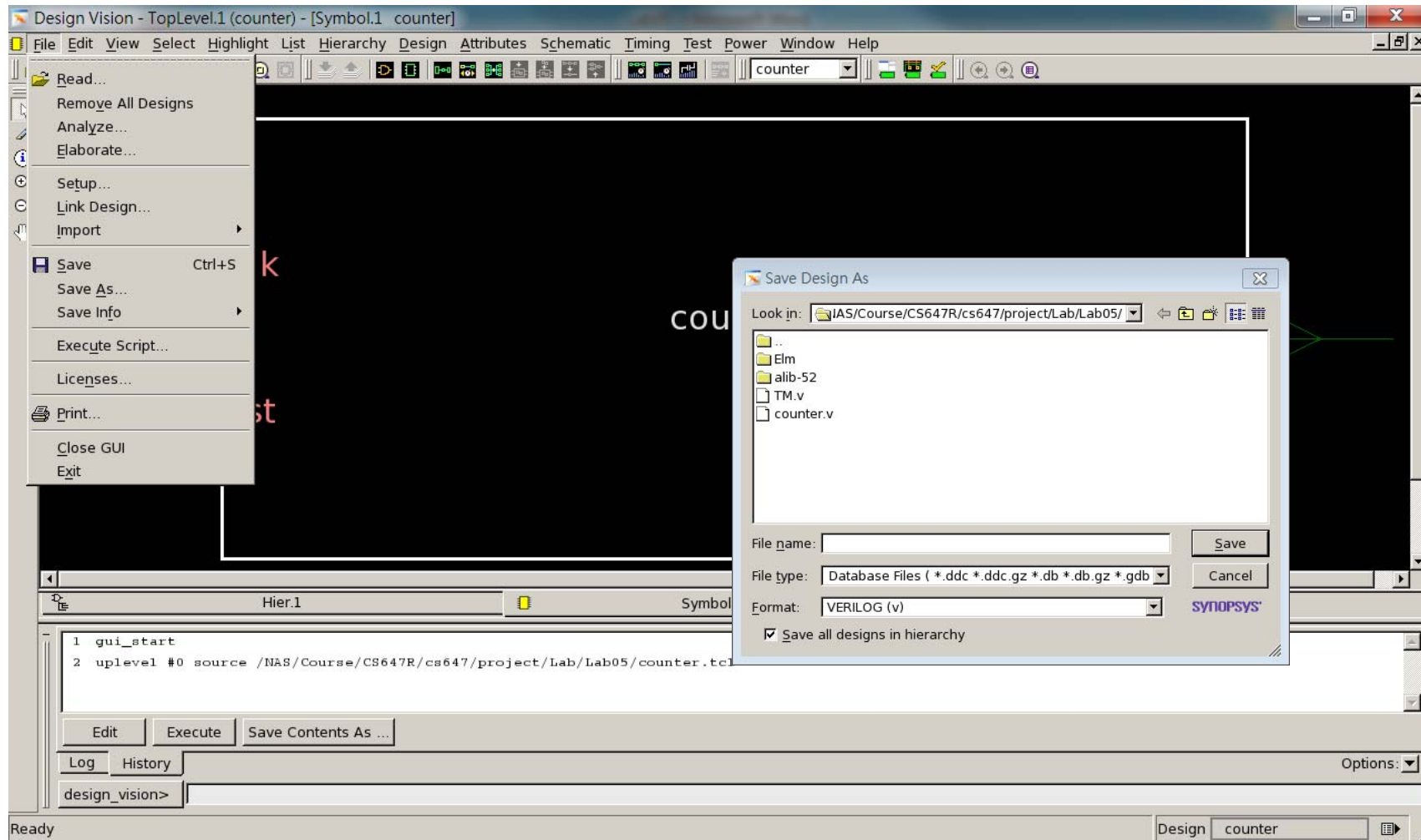
```
Information: Writing timing information to file '/NAS/Course/CS647R/cs647/project/Lab/Lab05/counter.sdf'. (WT-3)
design_vision>
Current design is 'counter'.
Current design is 'counter'.
Loading db file '/usr/cad/synopsys/synthesis/cur/libraries/syn/generic.sdb'
Current design is 'counter'.
```

Below the terminal, a red text box contains the command:

```
write_sdf -version 1.0 counter.sdf
```

The bottom status bar shows the design name 'counter'.

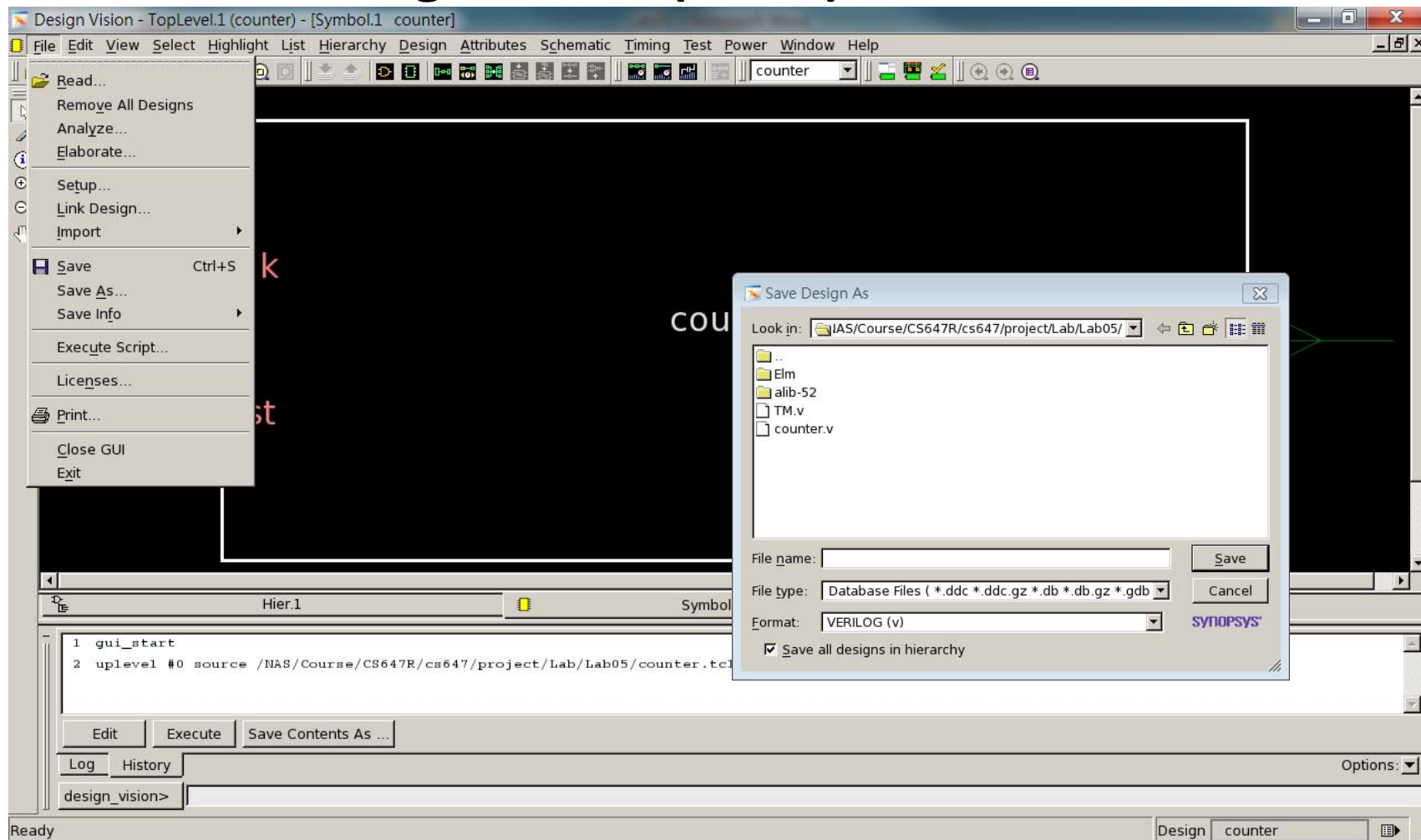
Save Netlist



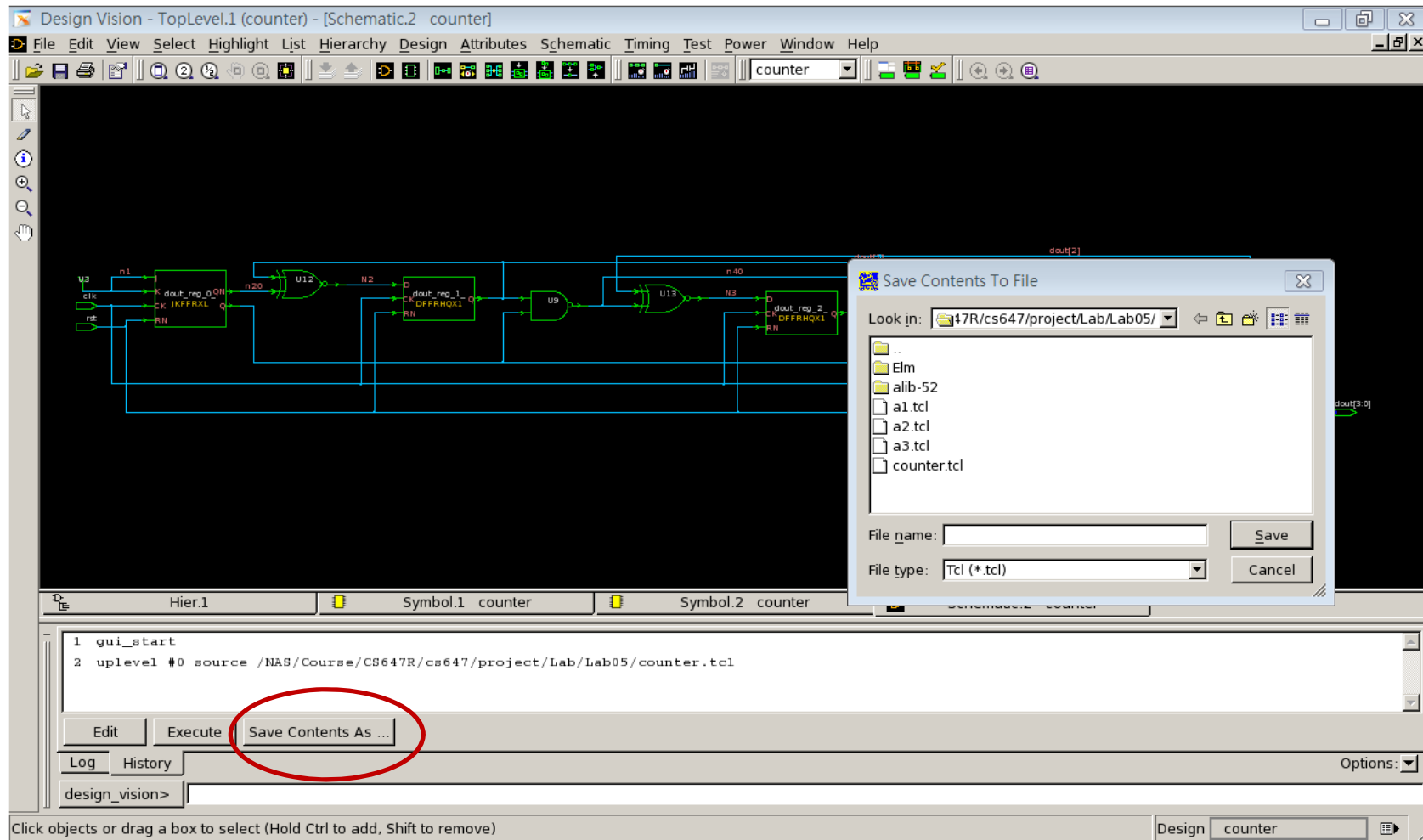
write -format verilog -hierarchy -output chip_syn.v

Save Design

- Save the design as ddc (or db) format

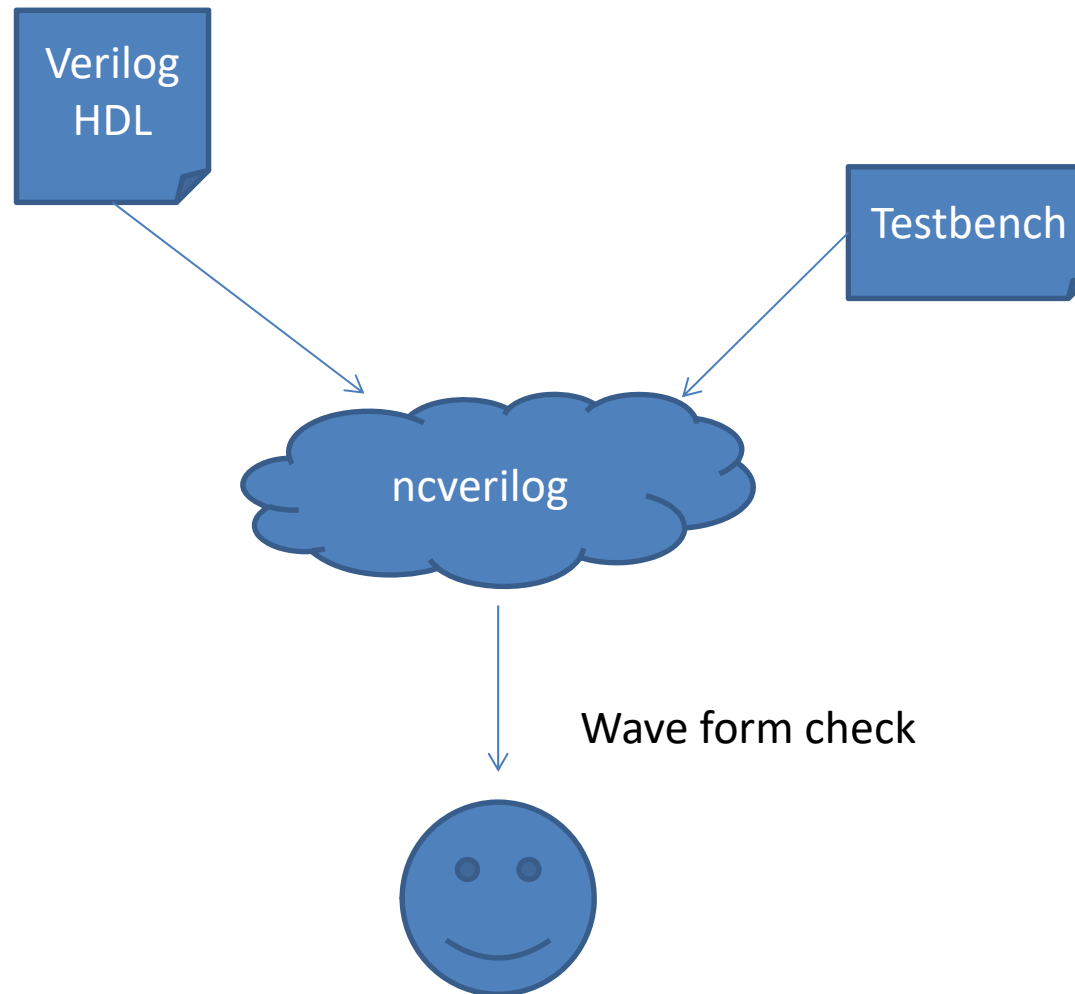


Save Script

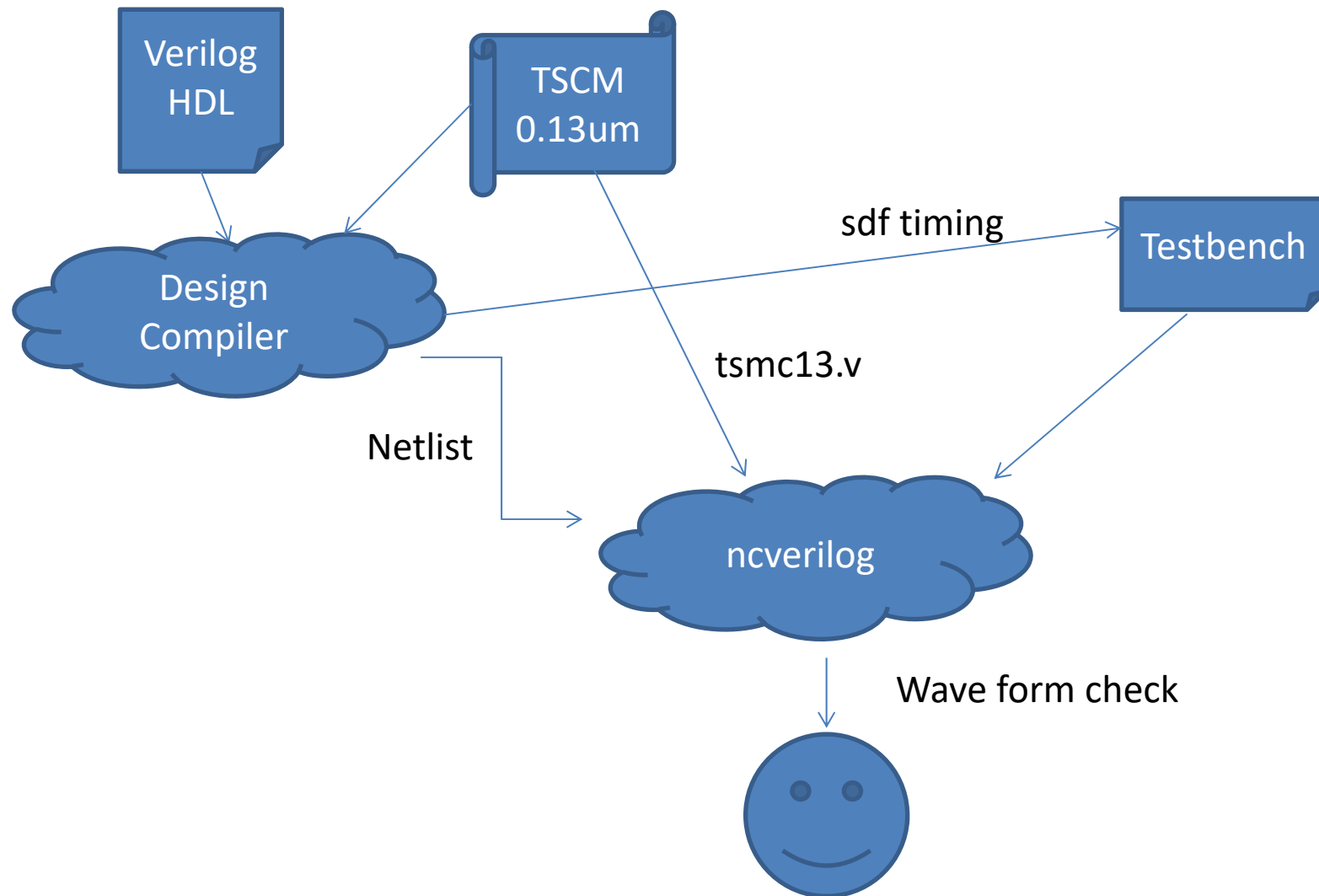


%dc_shell-xg-t -f xxx.tcl

Function Simulation



Gate Level Simulation



Testbench SDF Annotation

- **Include timing information in the simulations**
 - Standard Delay Format (SDF) file
 - `$sdf_annotate(sdf_file, module_instance, log_file, scale_factor, scale_type);`

```
initial
    $sdf_annotate("../rtl/Chip.sdf", U_Core);

CHIP      U_Core(
    .clk    (clk),
    .rst    (rst),
    .xin    (xin),
    .zout   (zout)
);
```