Advance FPGA Design

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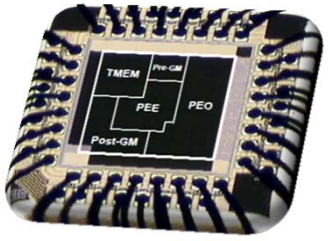


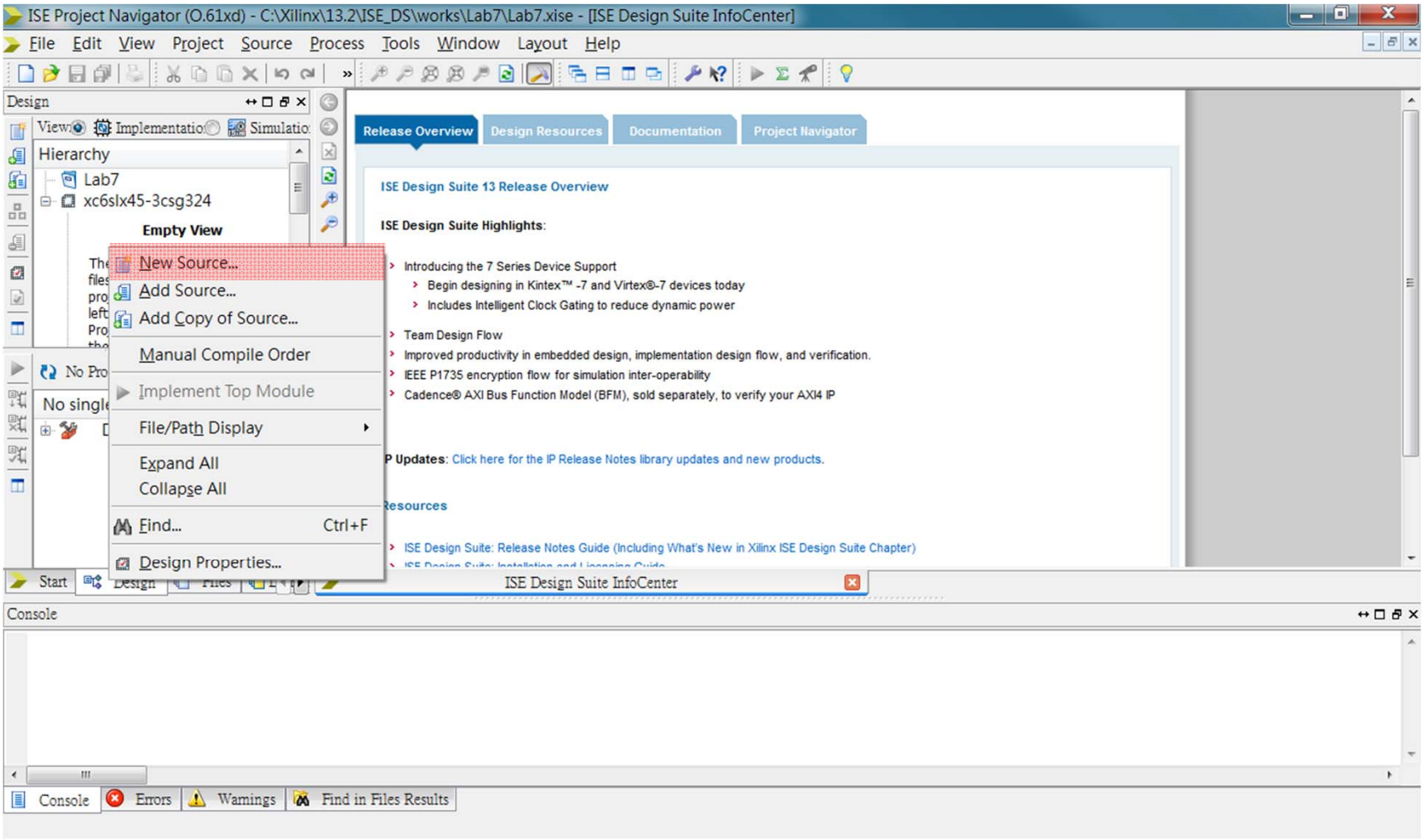
Outline

- **Memory Design**
- Clock Design

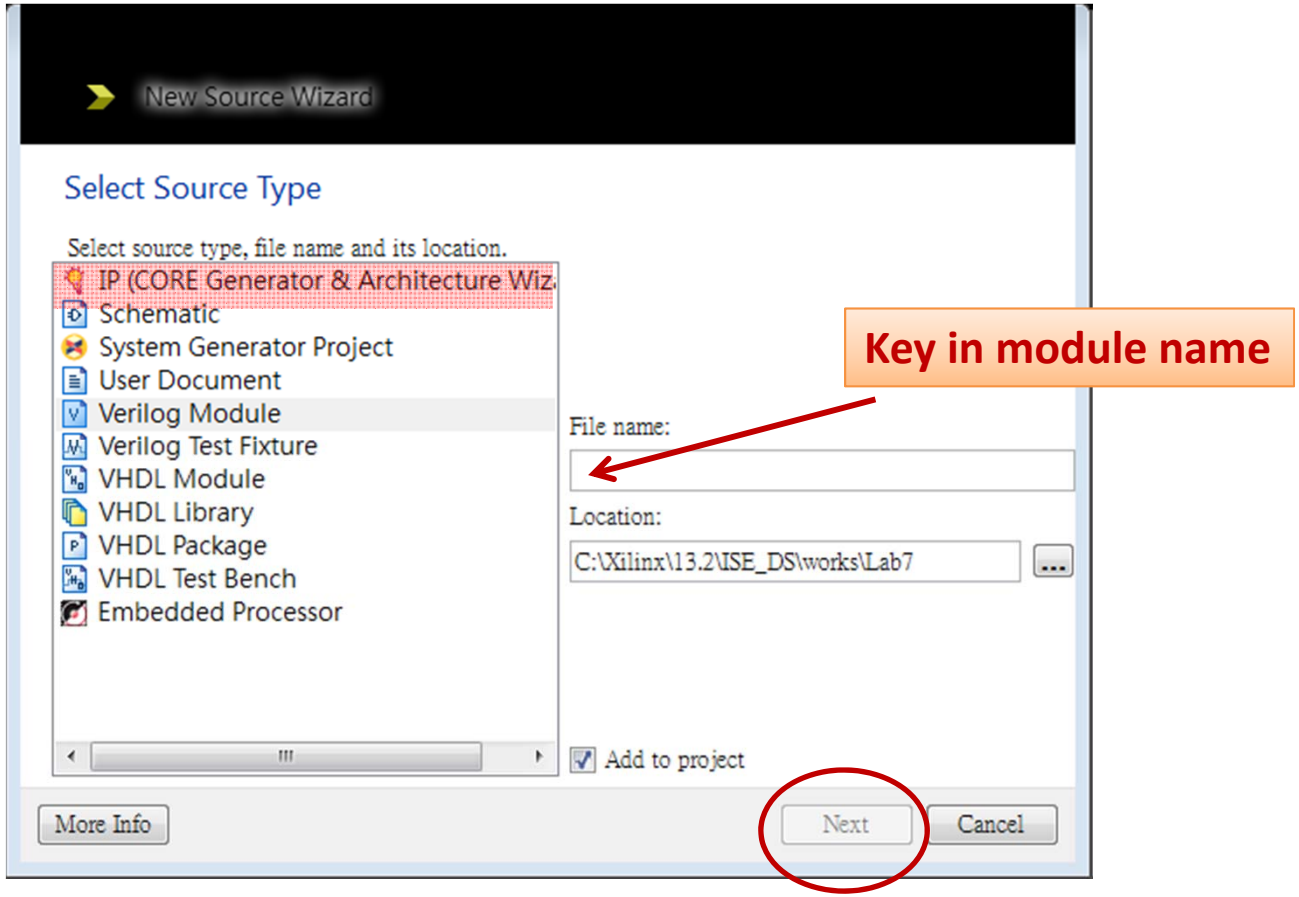
RAM for Verilog

```
module RAM_word5_bit8( cs, rw, address, din, dout);

parameter words = 5;

input       cs, wr;
input       [2:0]       address;
input       [7:0]       din;
output      [7:0]       dout;

reg         [7:0]       ram_data[0:words-1];
reg         [7:0]       dout;

always @(negedge cs)
begin
        if(~wr)
                dout = ram_data[address[2:0]];
            else
                if(rw)
                                ram_data[address[2:0]] = din;
                else
                                dout = 8'bz;
end

endmodule
```

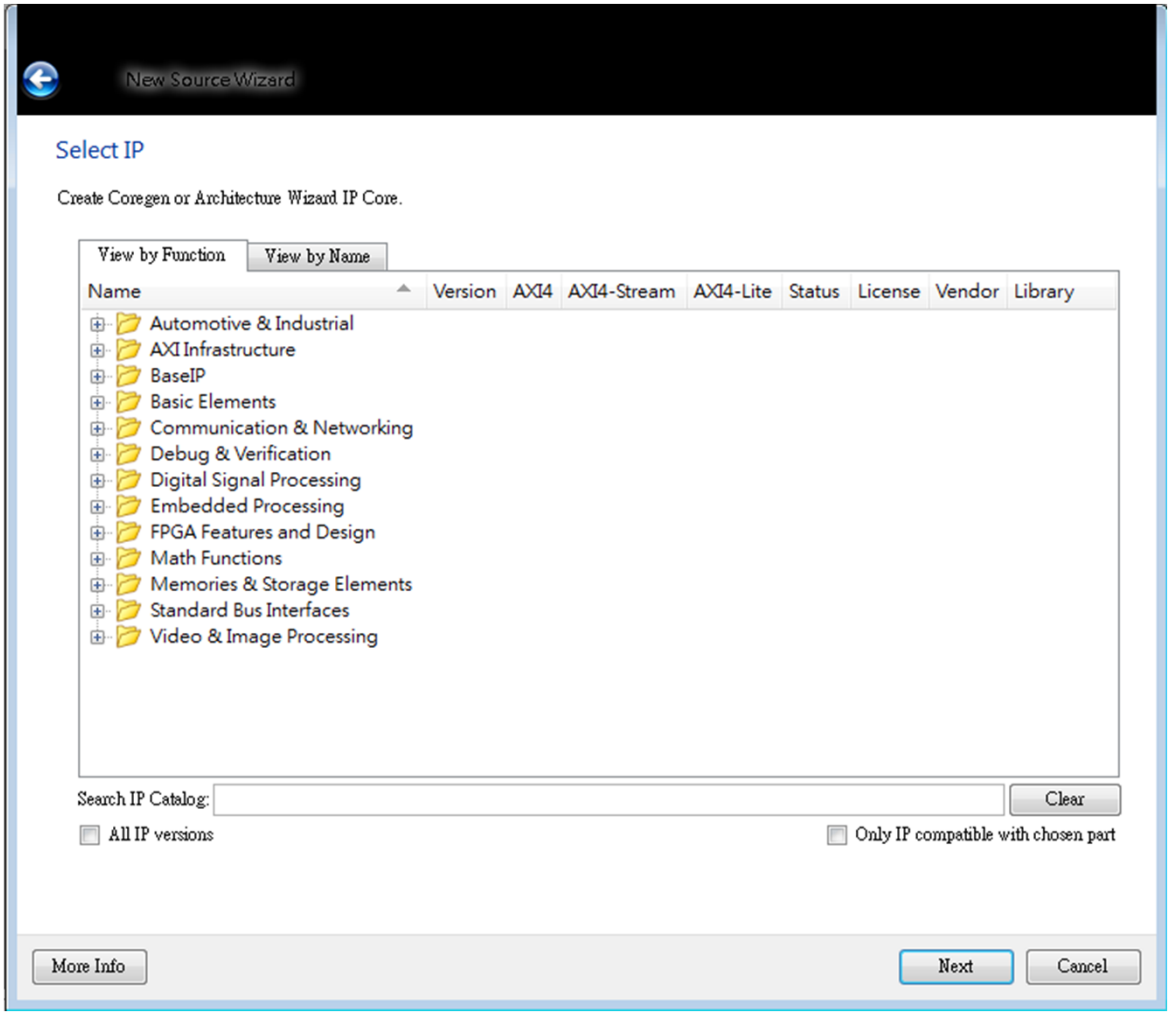
New Source


ISE Project Navigator (O.61xd) - C:\Xilinx\13.2\ISE_DS\works\Lab7\Lab7.xise - [ISE Design Suite InfoCenter]
File Edit View Project Source Process Tools Window Layout Help
Design
Hierarchy
Lab7
xc6slx45-3csg324
Empty View
New Source...
Add Source...
Add Copy of Source...
Manual Compile Order
Implement Top Module
File/Path Display
Expand All
Collapse All
Find... Ctrl+F
Design Properties...
Release Overview
Design Resources
Documentation
Project Navigator
ISE Design Suite 13 Release Overview
ISE Design Suite Highlights:
Introducing the 7 Series Device Support
Begin designing in Kintex™ -7 and Virtex®-7 devices today
Includes Intelligent Clock Gating to reduce dynamic power
Team Design Flow
Improved productivity in embedded design, implementation design flow, and verification.
IEEE P1735 encryption flow for simulation inter-operability
Cadence® AXI Bus Function Model (BFM), sold separately, to verify your AXI4 IP
P Updates: Click here for the IP Release Notes library updates and new products.
Resources
ISE Design Suite: Release Notes Guide (Including What's New in Xilinx ISE Design Suite Chapter)
Start
ISE Design Suite InfoCenter
Console
Console
Errors
Warnings
Find in Files Results

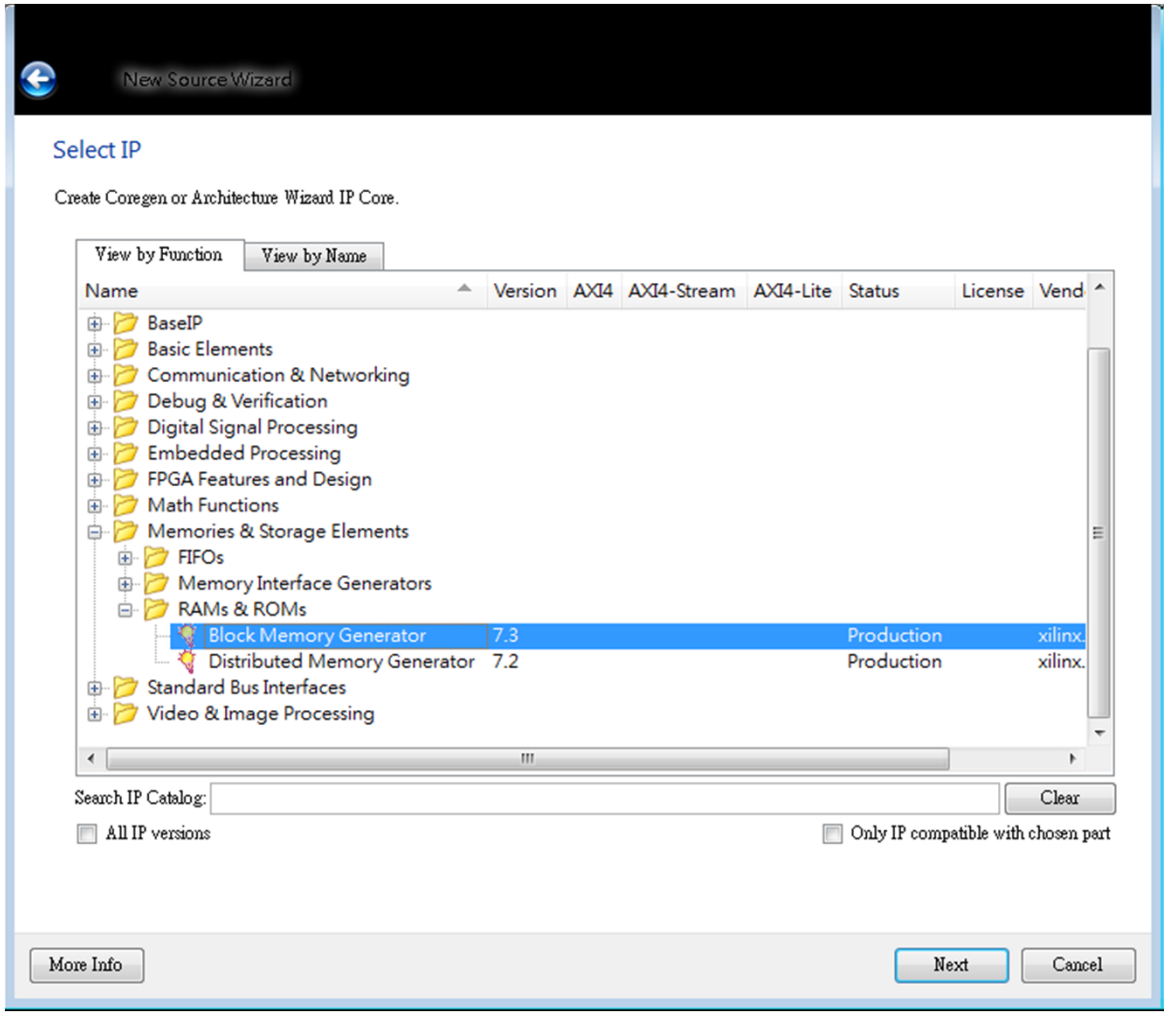
New Source


New Source Wizard
Select Source Type
Select source type, file name and its location.
IP (CORE Generator & Architecture Wiz
Schematic
System Generator Project
User Document
Verilog Module
Verilog Test Fixture
VHDL Module
VHDL Library
VHDL Package
VHDL Test Bench
Embedded Processor
Key in module name
File name:
Location:
C:\Xilinx\13.2\ISE_DS\works\Lab7
...
Add to project
More Info
Next
Cancel

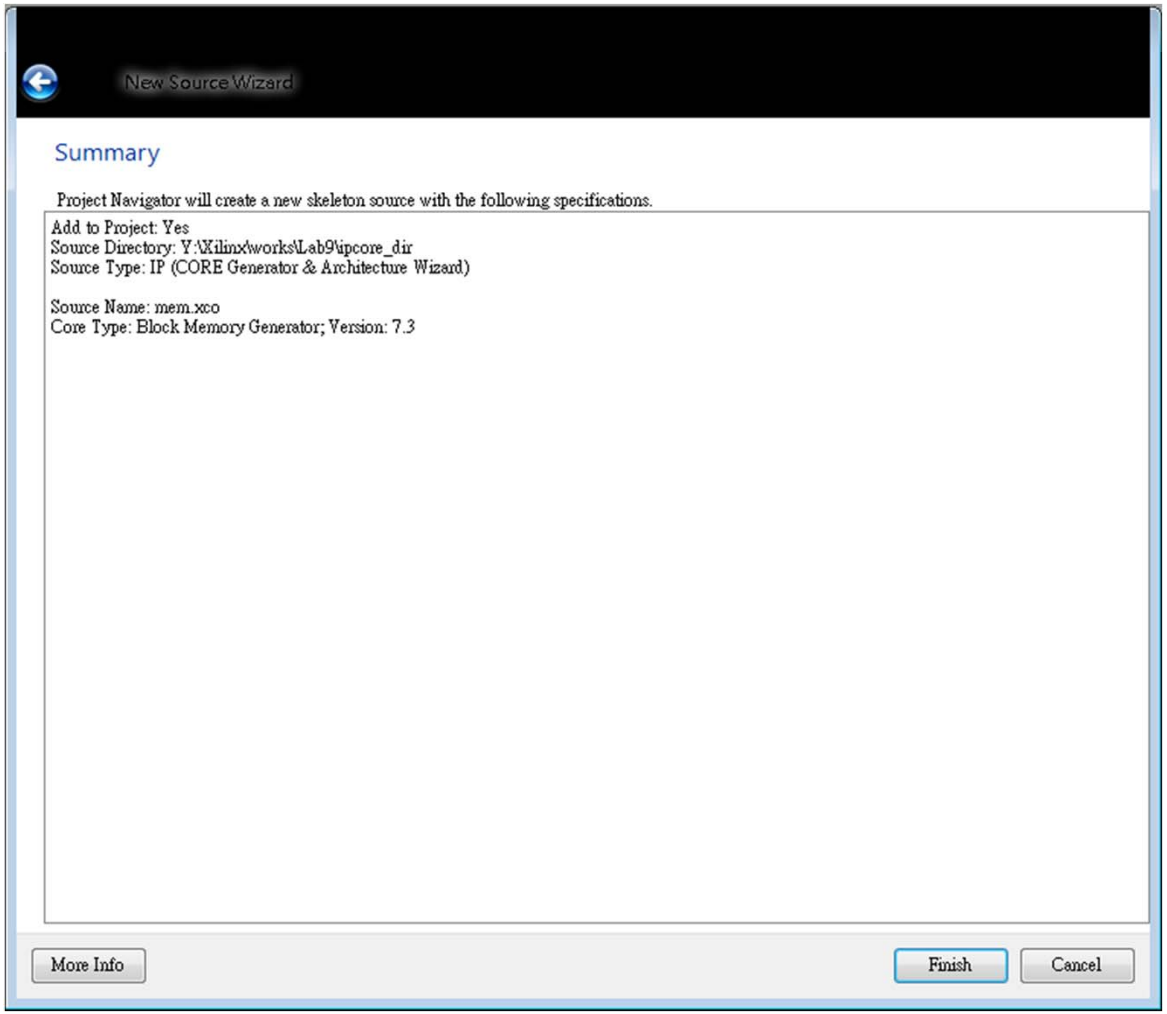
Use the Dedicated Memory



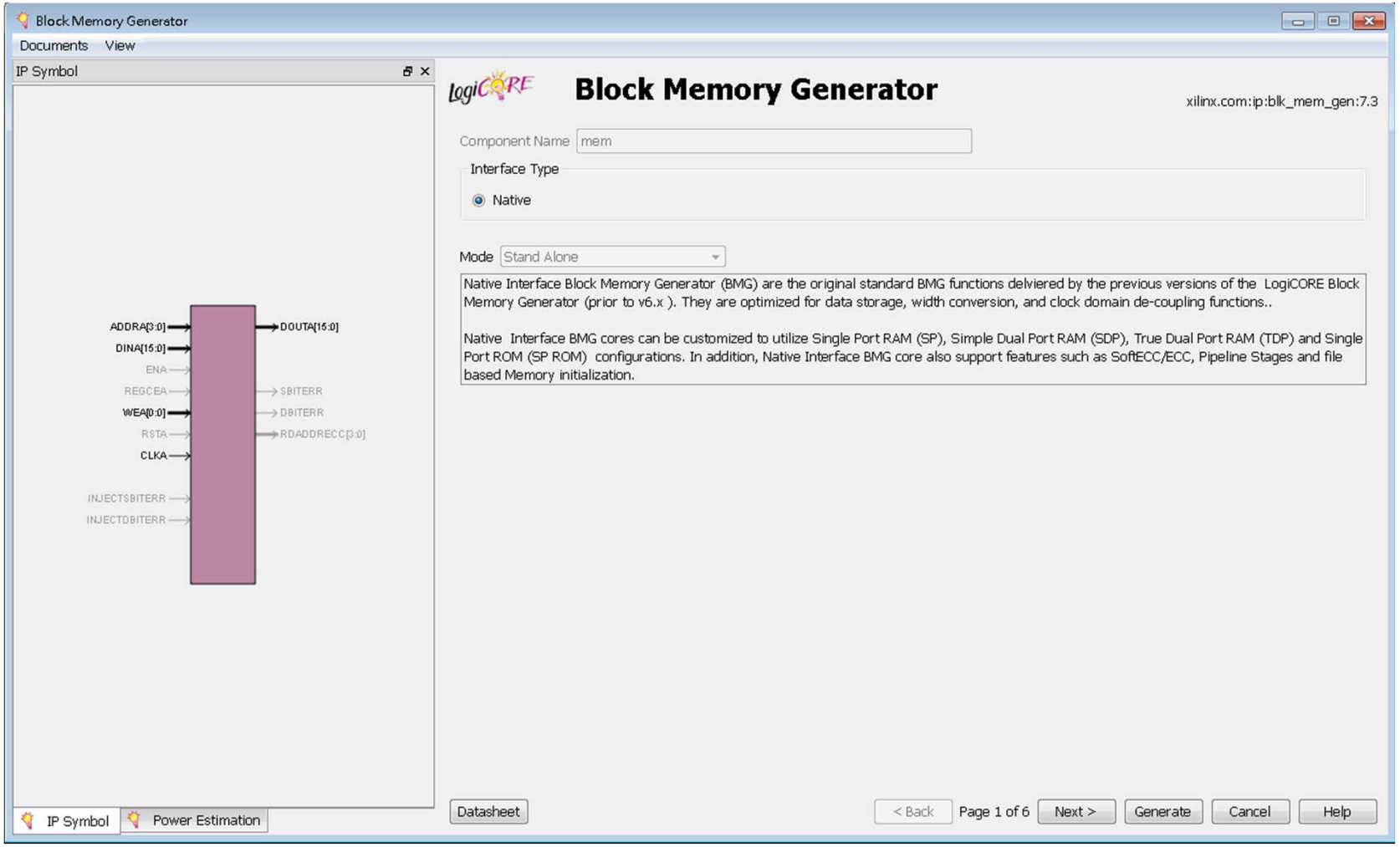
Use the Dedicated Memory



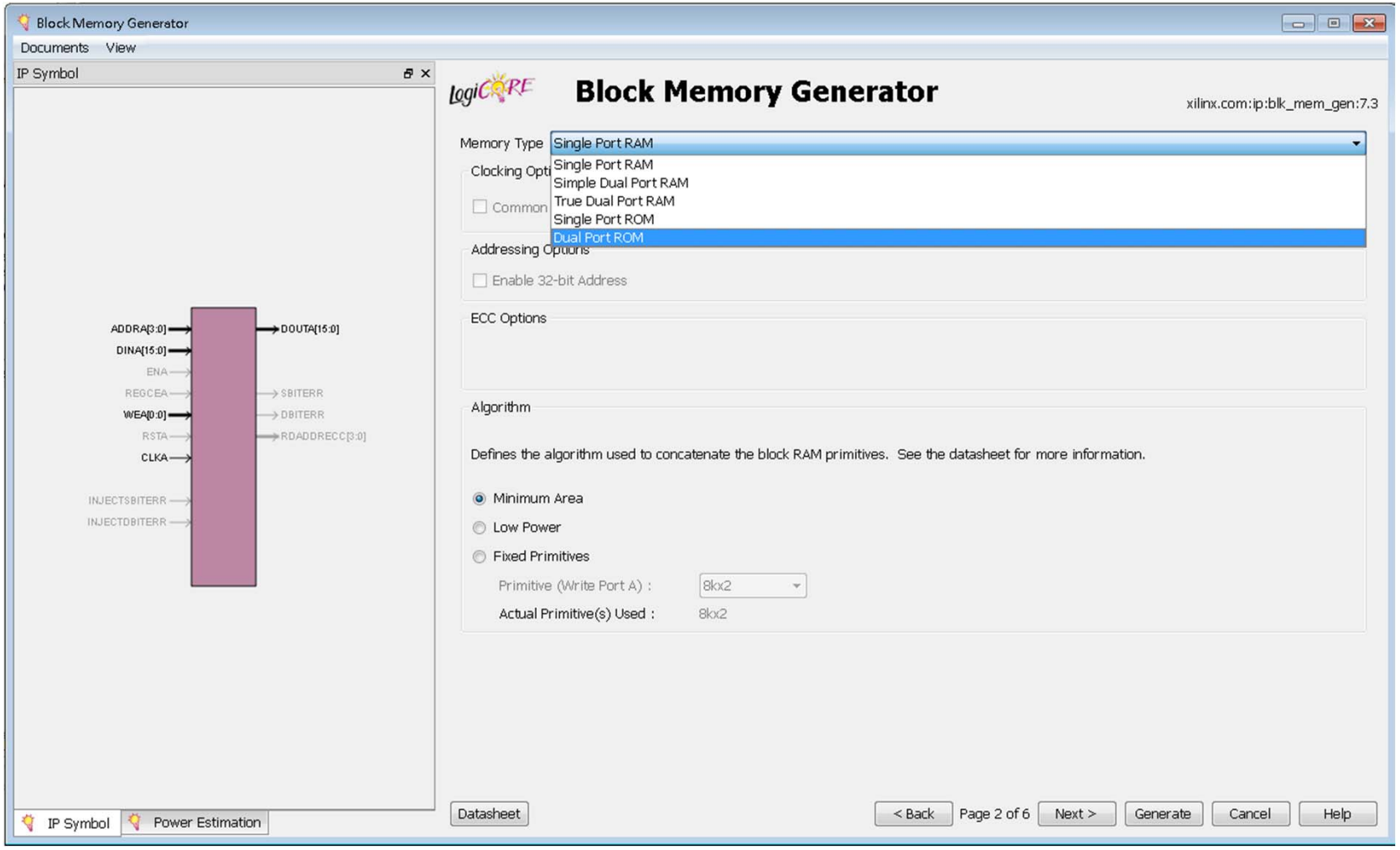
Use the Dedicated Memory



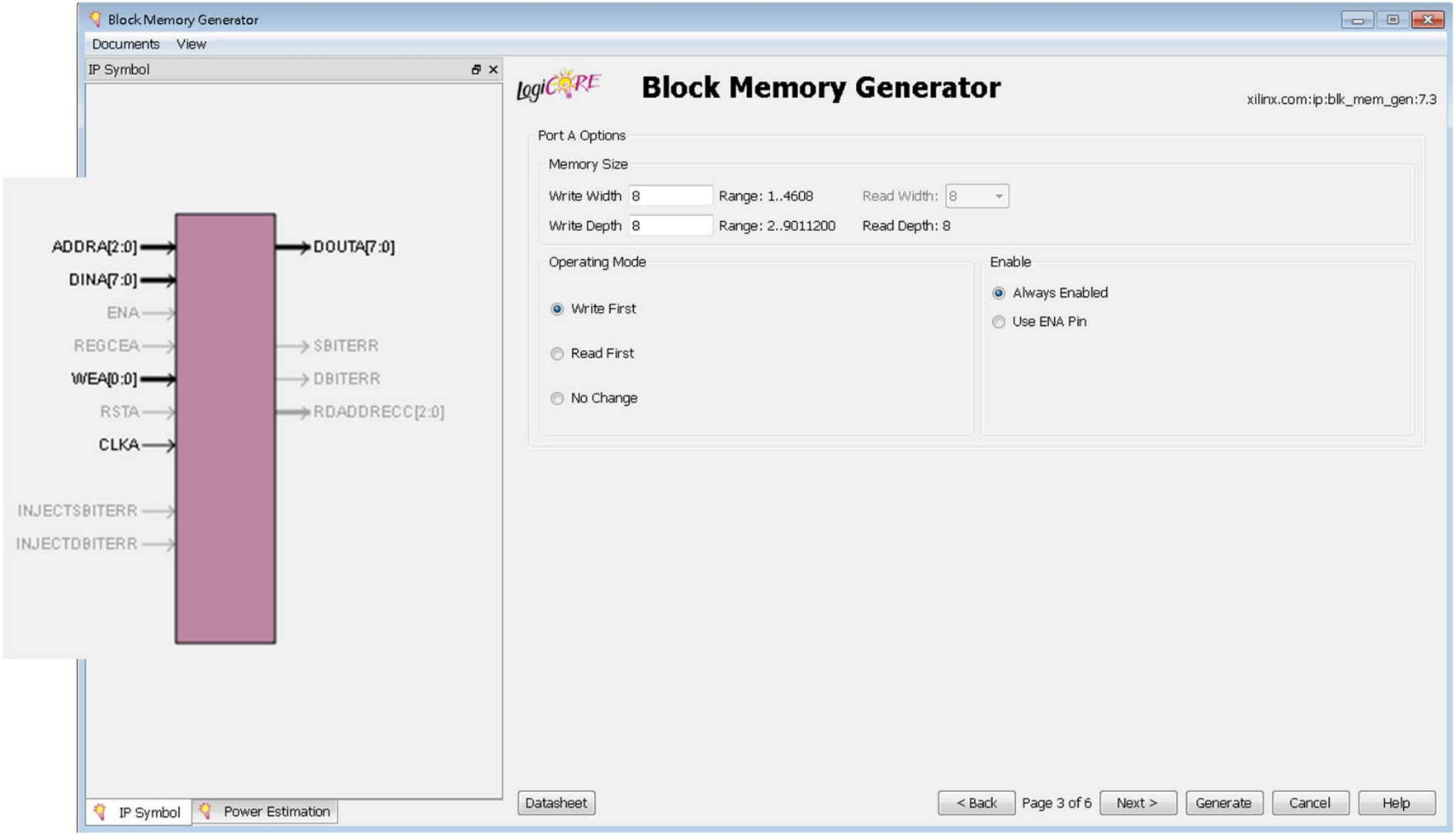
Core Generator



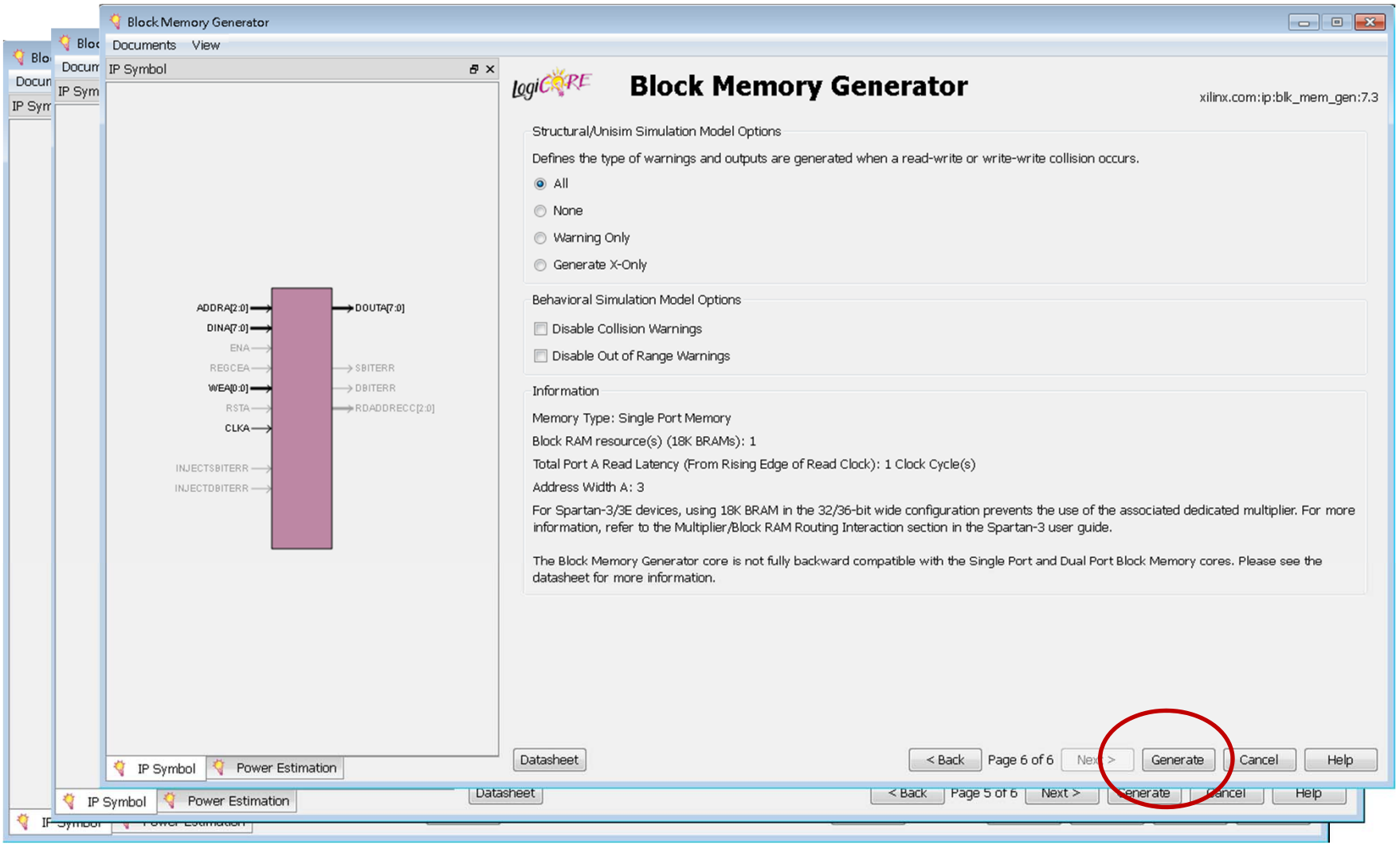
Core Generator



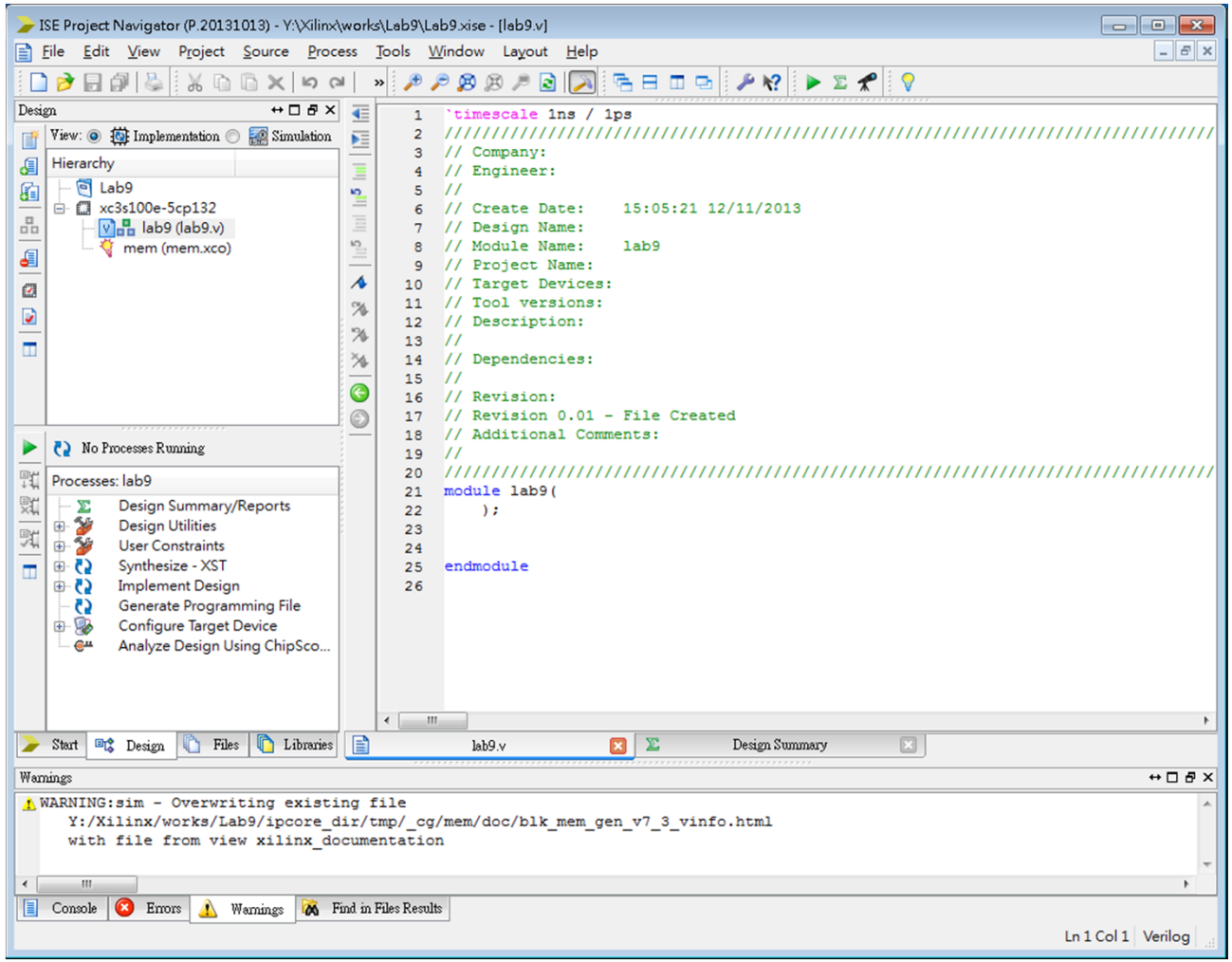
Core Generator



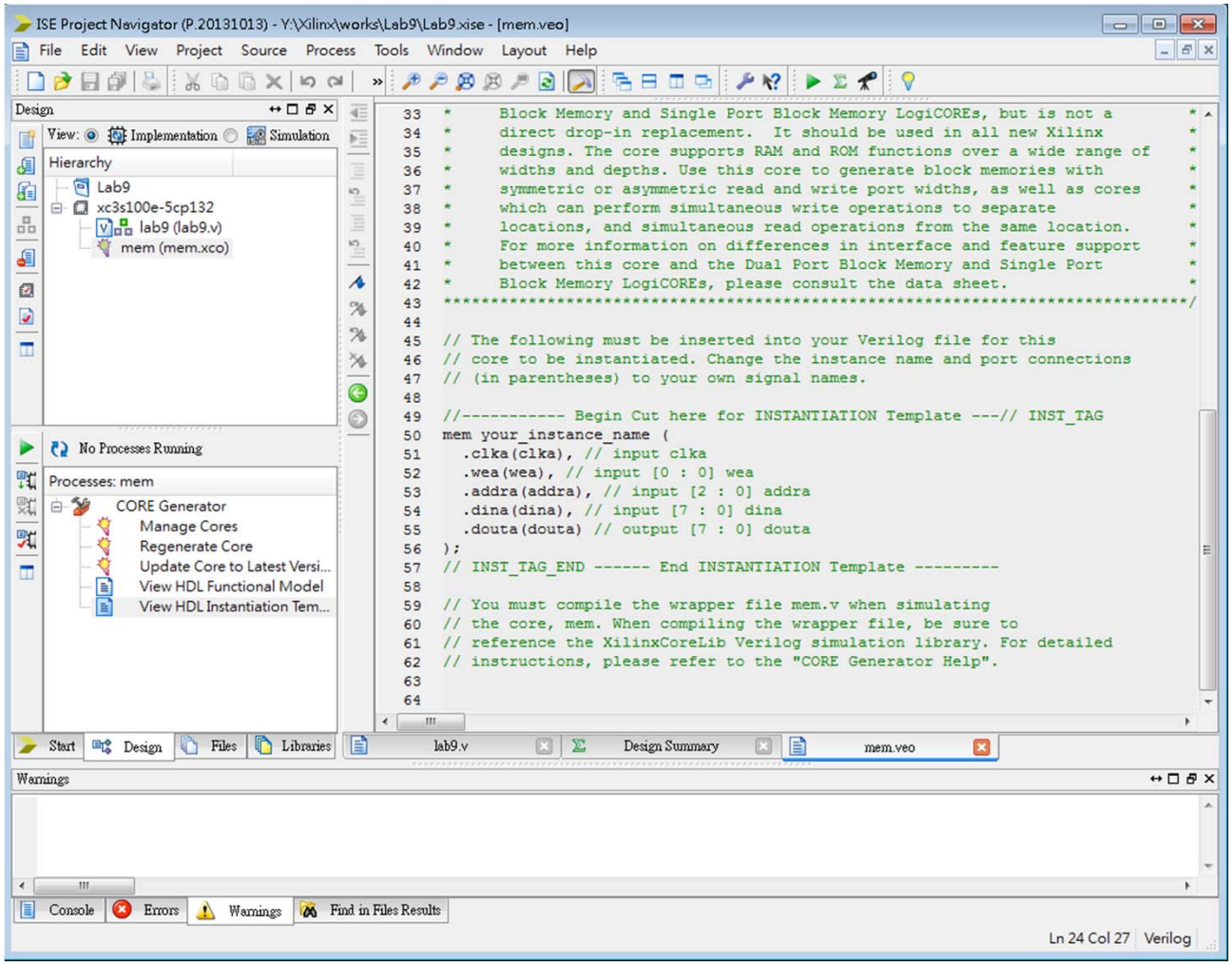
Core Generator



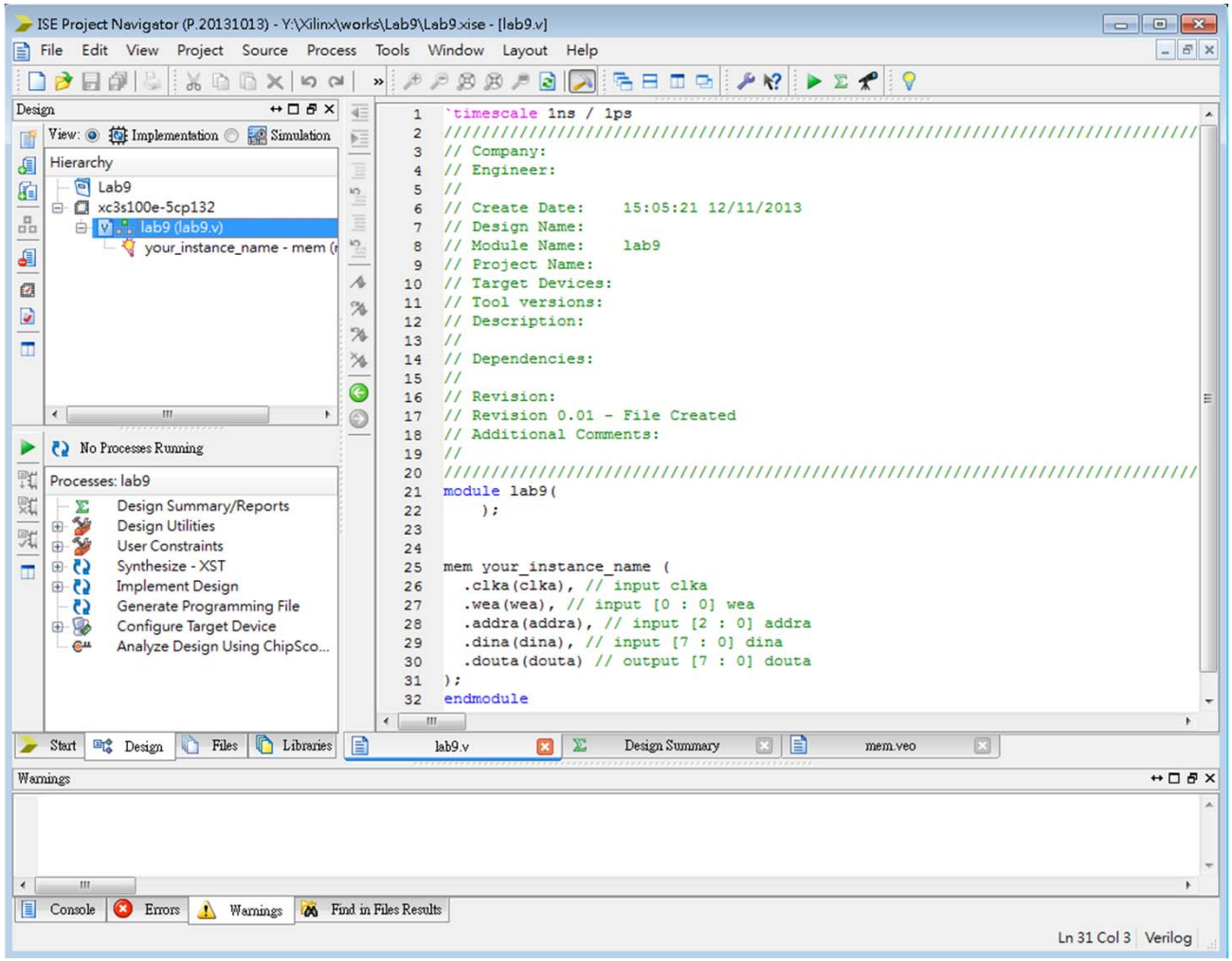
Generator


ISE Project Navigator (P.20131013) - Y:\Xilinx\works\Lab9\Lab9.xise - [lab9.v]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Lab9
xc3s100e-5cp132
lab9 (lab9.v)
mem (mem.xco)
No Processes Running
Processes: lab9
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipSco...
1 `timescale 1ns / 1ps
2 //
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 15:05:21 12/11/2013
7 // Design Name:
8 // Module Name: lab9
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module lab9(
22);
23
24
25 endmodule
26
Start Design Files Libraries
lab9.v
Design Summary
Warnings
WARNING:sim - Overwriting existing file
Y:/Xilinx/works/Lab9/ipcore_dir/tmp/_cg/mem/doc/blk_mem_gen_v7_3_vinfo.html
with file from view xilinx_documentation
Console Errors Warnings Find in Files Results
Ln 1 Col 1 Verilog

Include Memory Instance



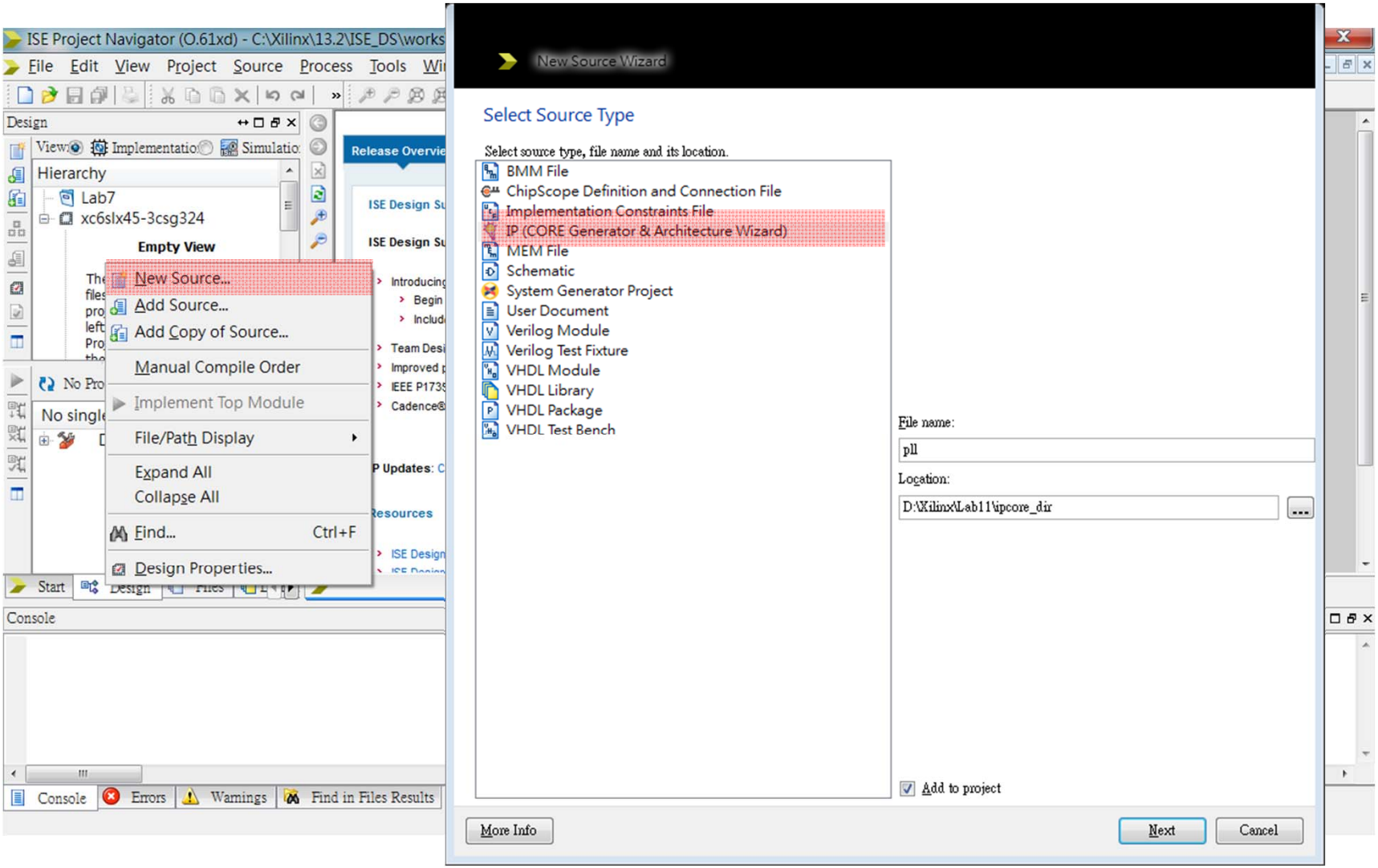
Include Memory Instance



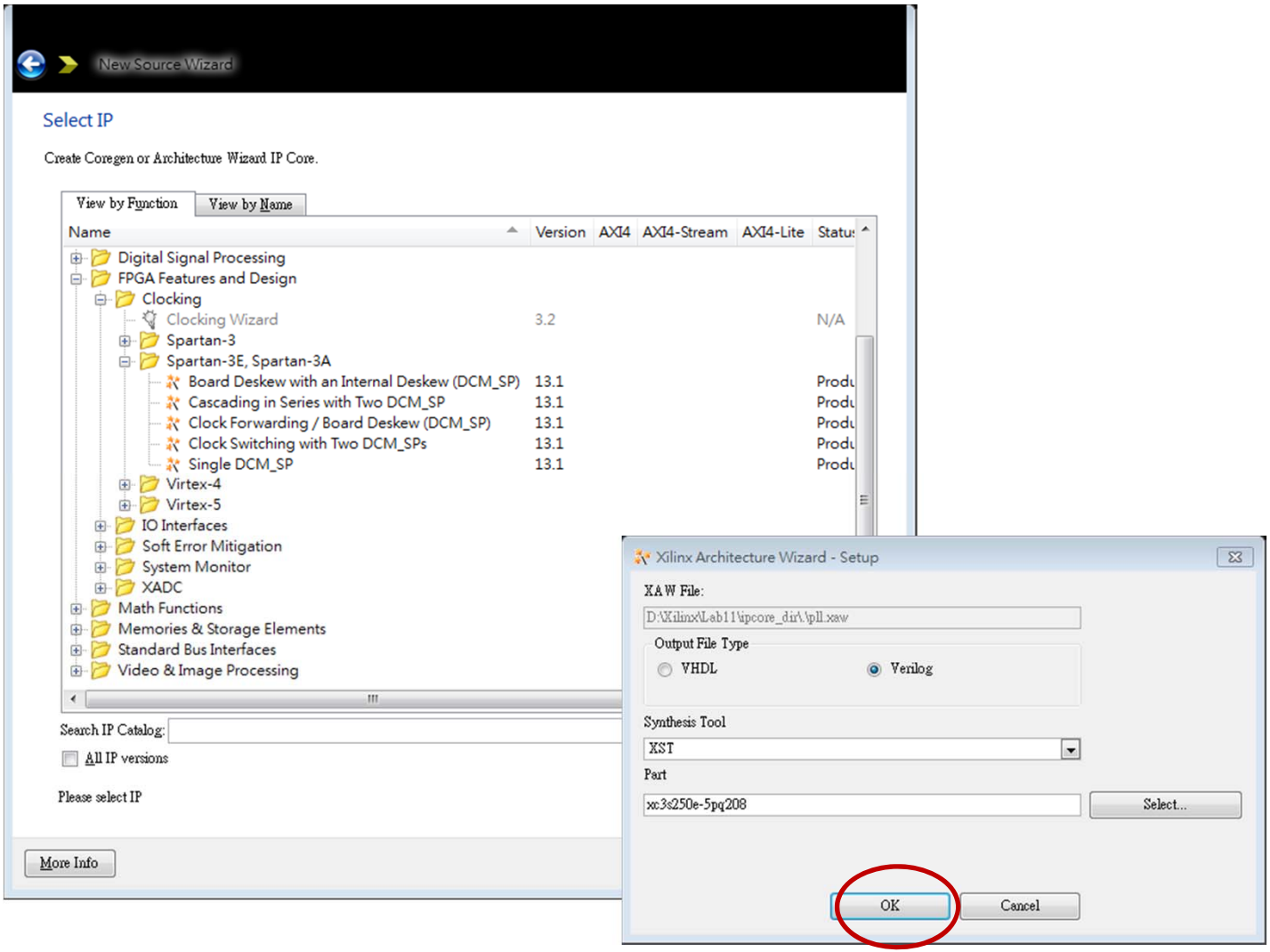
Outline

- Memory Design
- **Clock Design**

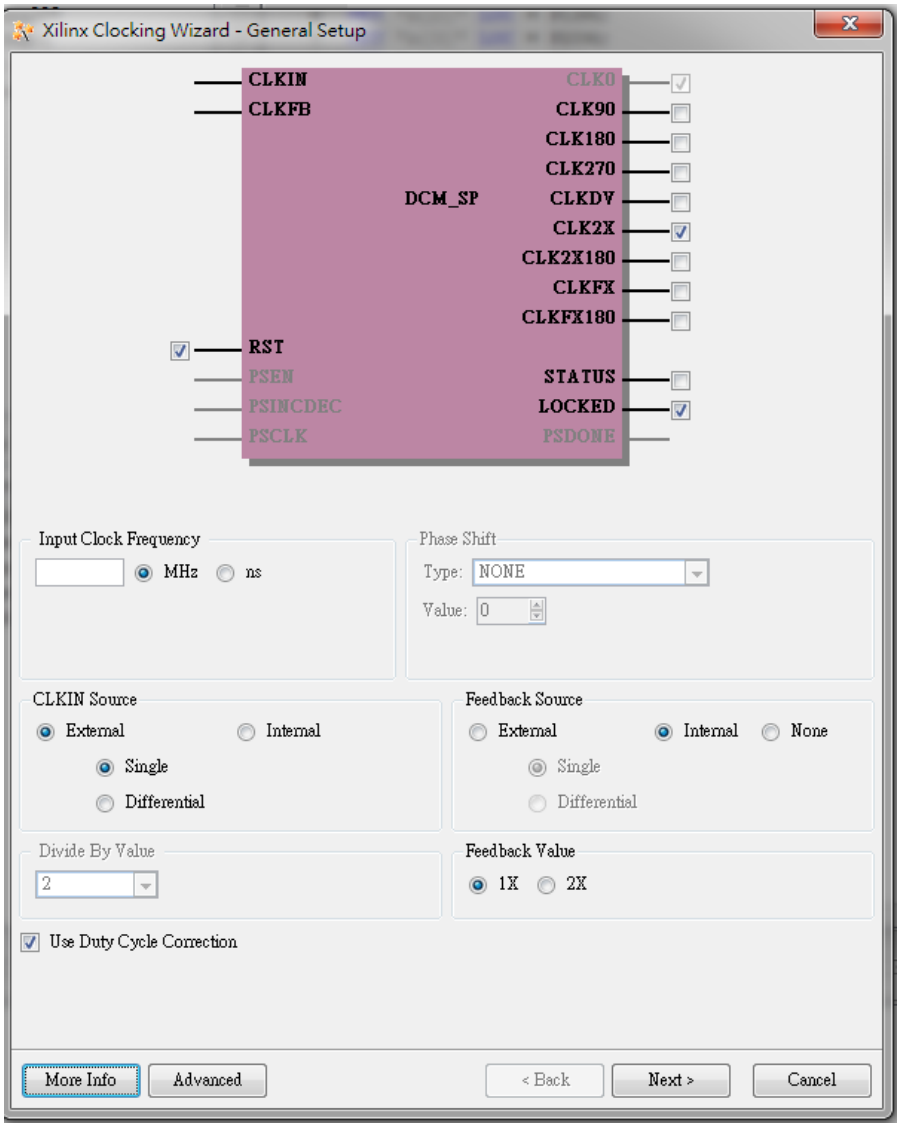
New IP Core


ISE Project Navigator (O.61xd) - C:\Xilinx\13.2\ISE_DS\works
File Edit View Project Source Process Tools
Design
Hierarchy
Lab7
xc6slx45-3csg324
Empty View
New Source...
Add Source...
Add Copy of Source...
Manual Compile Order
Implement Top Module
File/Path Display
Expand All
Collapse All
Find... Ctrl+F
Design Properties...
Console
Errors
Warnings
Find in Files Results
New Source Wizard
Select Source Type
Select source type, file name and its location.
BMM File
ChipScope Definition and Connection File
Implementation Constraints File
IP (CORE Generator & Architecture Wizard)
MEM File
Schematic
System Generator Project
User Document
Verilog Module
Verilog Test Fixture
VHDL Module
VHDL Library
VHDL Package
VHDL Test Bench
File name:
pll
Location:
D:\Xilinx\Lab11\ipcore_dir
Add to project
More Info
Next
Cancel

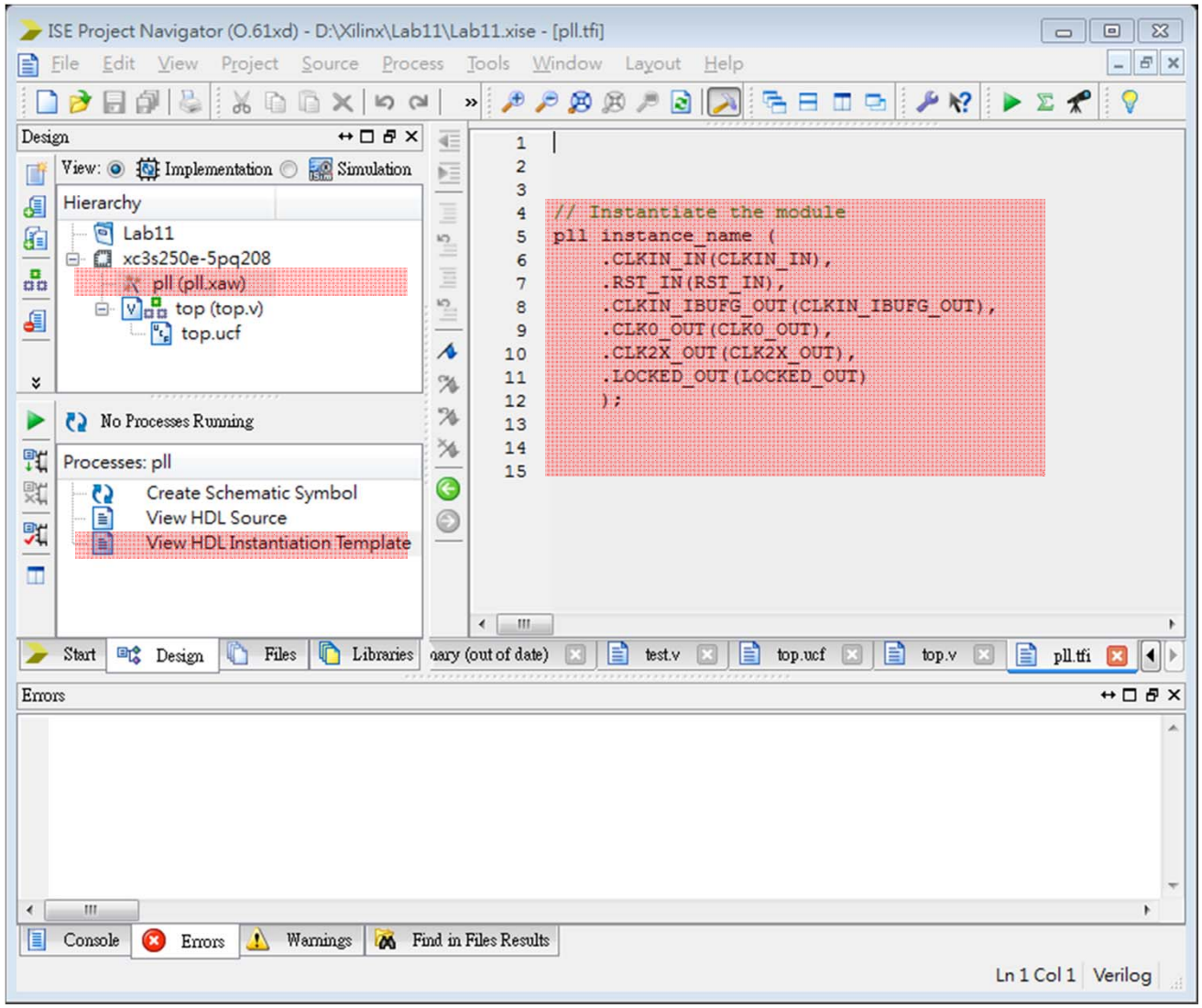
Select IP


New Source Wizard
Select IP
Create Coregen or Architecture Wizard IP Core.
View by Function
View by Name
Name
Version
AXI4
AXI4-Stream
AXI4-Lite
Digital Signal Processing
FPGA Features and Design
Clocking
Clocking Wizard 3.2 N/A
Spartan-3
Spartan-3E, Spartan-3A
Board Deskew with an Internal Deskew (DCM_SP) 13.1
Cascading in Series with Two DCM_SP 13.1
Clock Forwarding / Board Deskew (DCM_SP) 13.1
Clock Switching with Two DCM_SPs 13.1
Single DCM_SP 13.1
Virtex-4
Virtex-5
IO Interfaces
Soft Error Mitigation
System Monitor
XADC
Math Functions
Memories & Storage Elements
Standard Bus Interfaces
Video & Image Processing
Search IP Catalog:
All IP versions
Please select IP
More Info
Xilinx Architecture Wizard - Setup
XAW File:
D:\Xilinx\Lab11\ipcore_dir\pll.xaw
Output File Type
VHDL
Verilog
Synthesis Tool
XST
Part
xc3s250e-5pq208
Select...
OK
Cancel

Set IP


Xilinx Clocking Wizard - General Setup
CLKIN
CLKFB
RST
PSEN
PSINCDEC
PSCLK
DCM_SP
CLK0
CLK90
CLK180
CLK270
CLKDV
CLK2X
CLK2X180
CLKFX
CLKFX180
STATUS
LOCKED
PSDONE
Input Clock Frequency
MHz
ns
Phase Shift
Type:
NONE
Value:
0
CLKIN Source
External
Internal
Single
Differential
Feedback Source
External
Internal
None
Single
Differential
Divide By Value
2
Feedback Value
1X
2X
Use Duty Cycle Correction
More Info
Advanced
< Back
Next >
Cancel

Include DCM Instance



Include DCM Instance