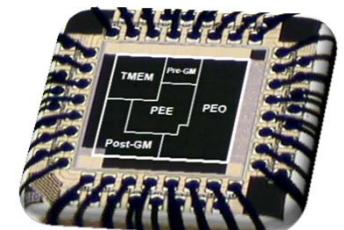


Introduction to FPGA Design

Yuan-Ho Chen

Department of Information & Computer Engineering
Chung Yuan Christian University
yhchen@ice.cycu.edu.tw



Outline

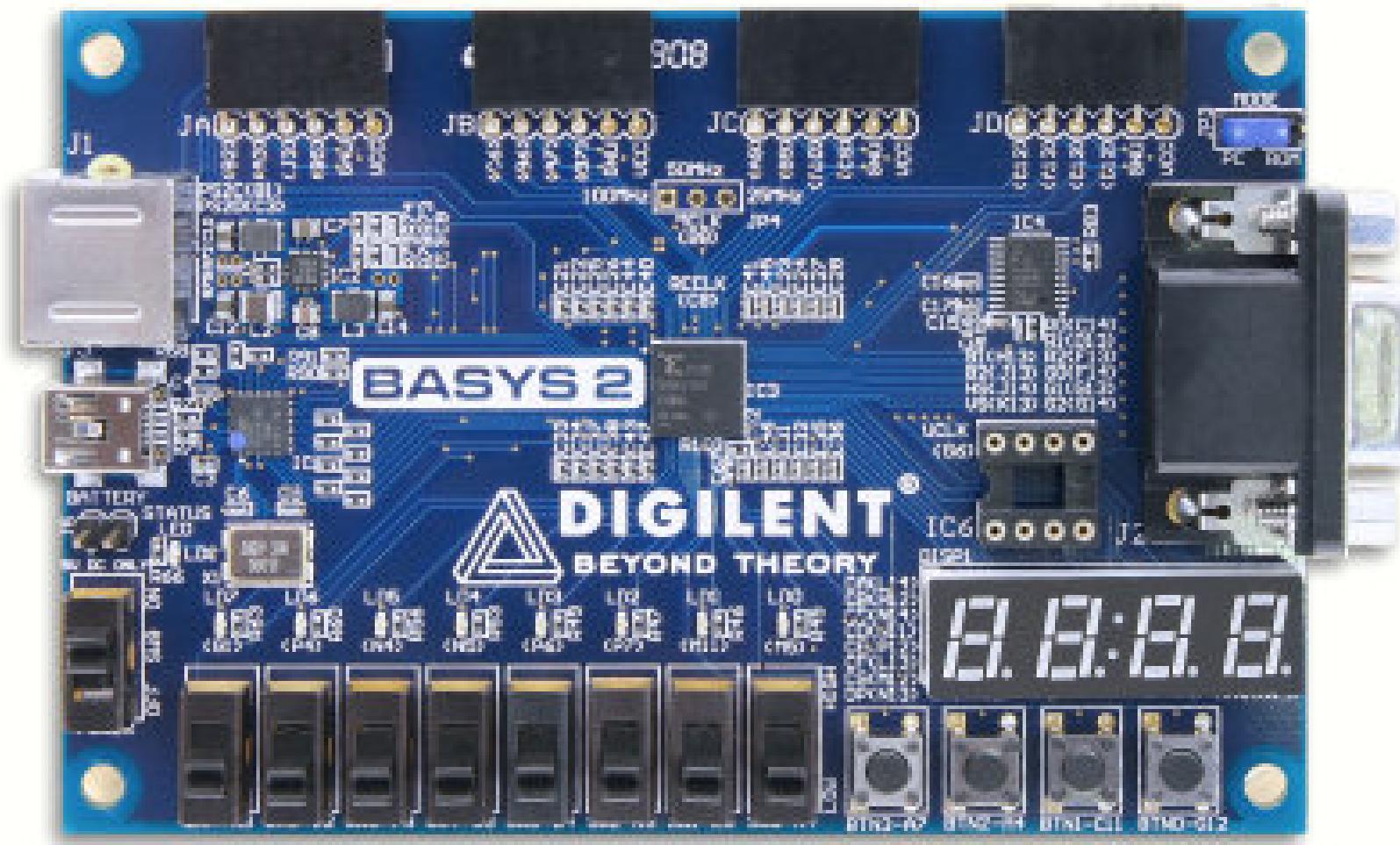
- **Xilinx FPGA Design Flow**
 - Synthesize
 - Implement Design
 - Generate bit-stream
 - Configure Target Device

Xilinx FPGA Design Flow

- **Design RTL code (.v)**
- **Find device type**
- **Use ISE tools**
 - Synthesize
 - Verilog code
 - Pre-sim (generate test bench)
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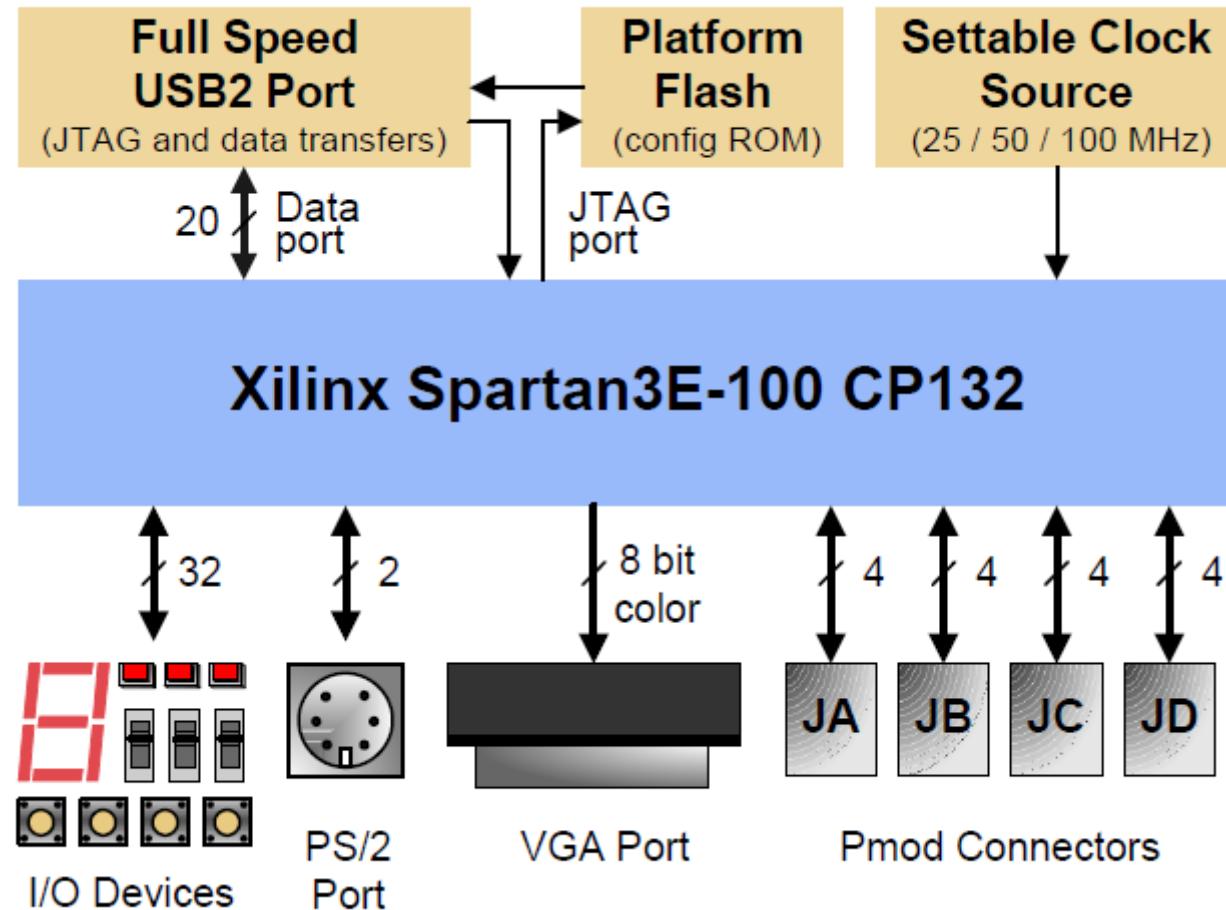


FPGA Evaluation Board





FPGA Evaluation Board



Xilinx FPGA Device Type

- **FPGA**
 - Xilinx*

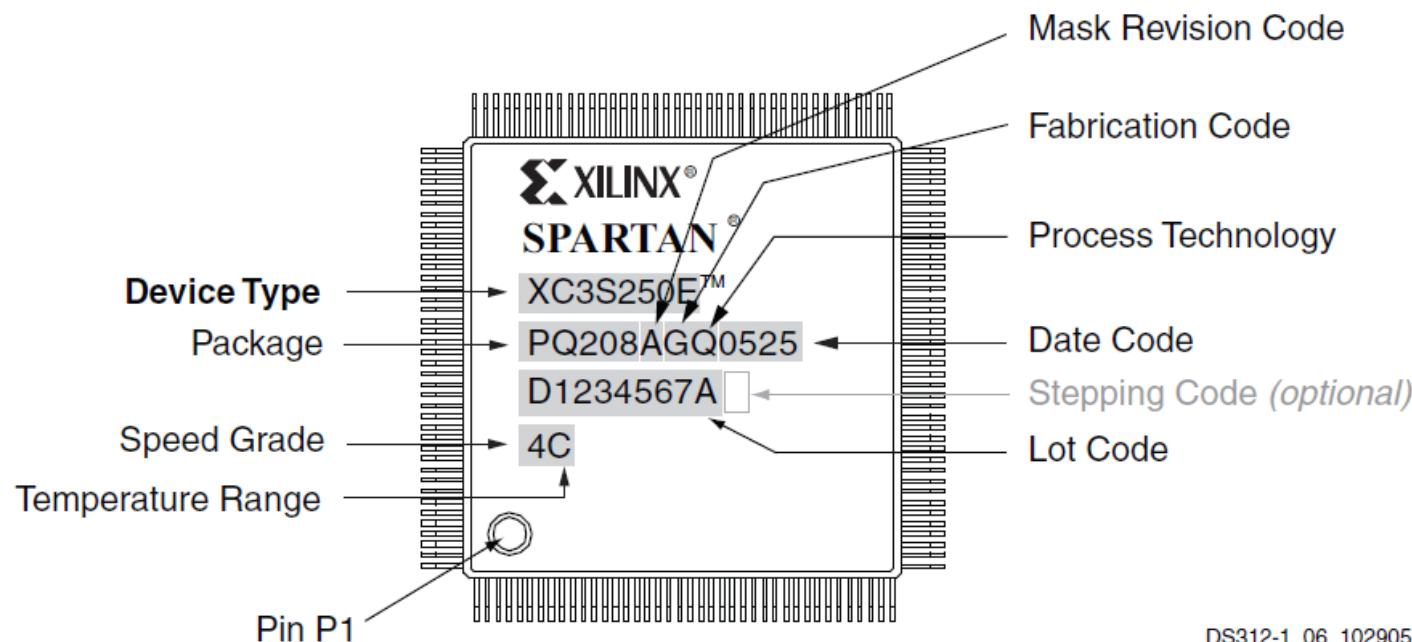
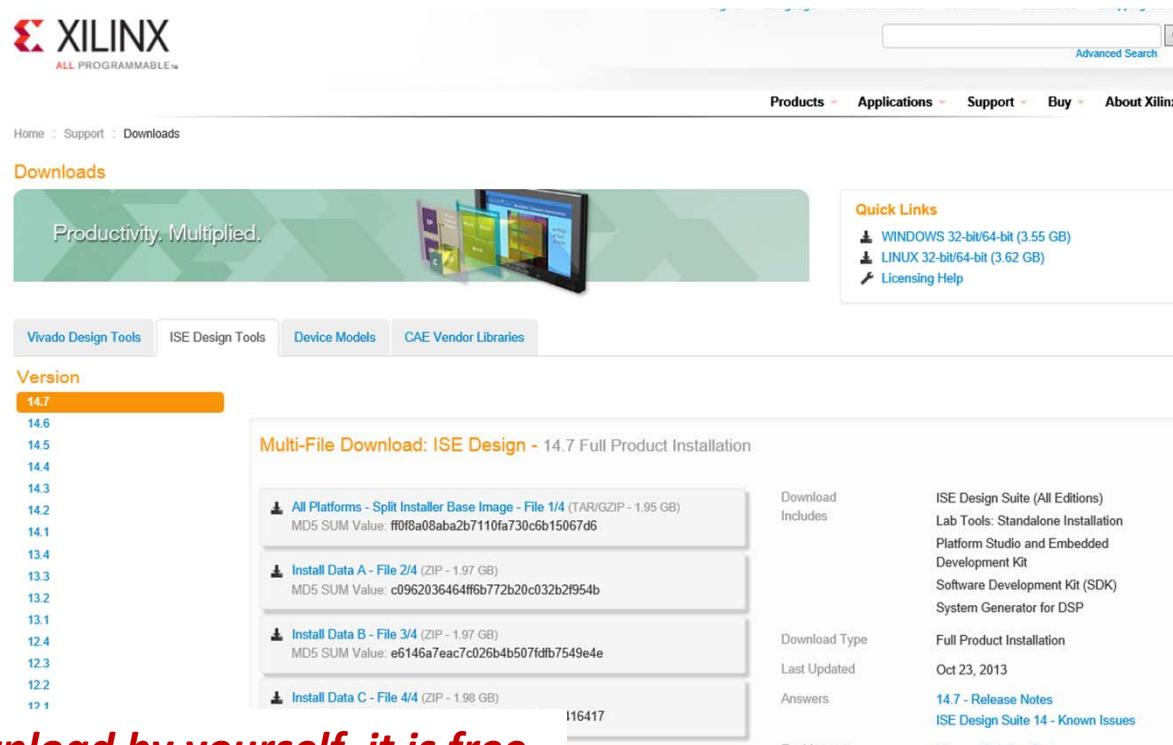


Figure 2: Spartan-3E QFP Package Marking Example

From Xilinx datasheet

Xilinx FPGA Tool

- **ISE Design Suite (14.7)**
 - <http://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/design-tools.html>

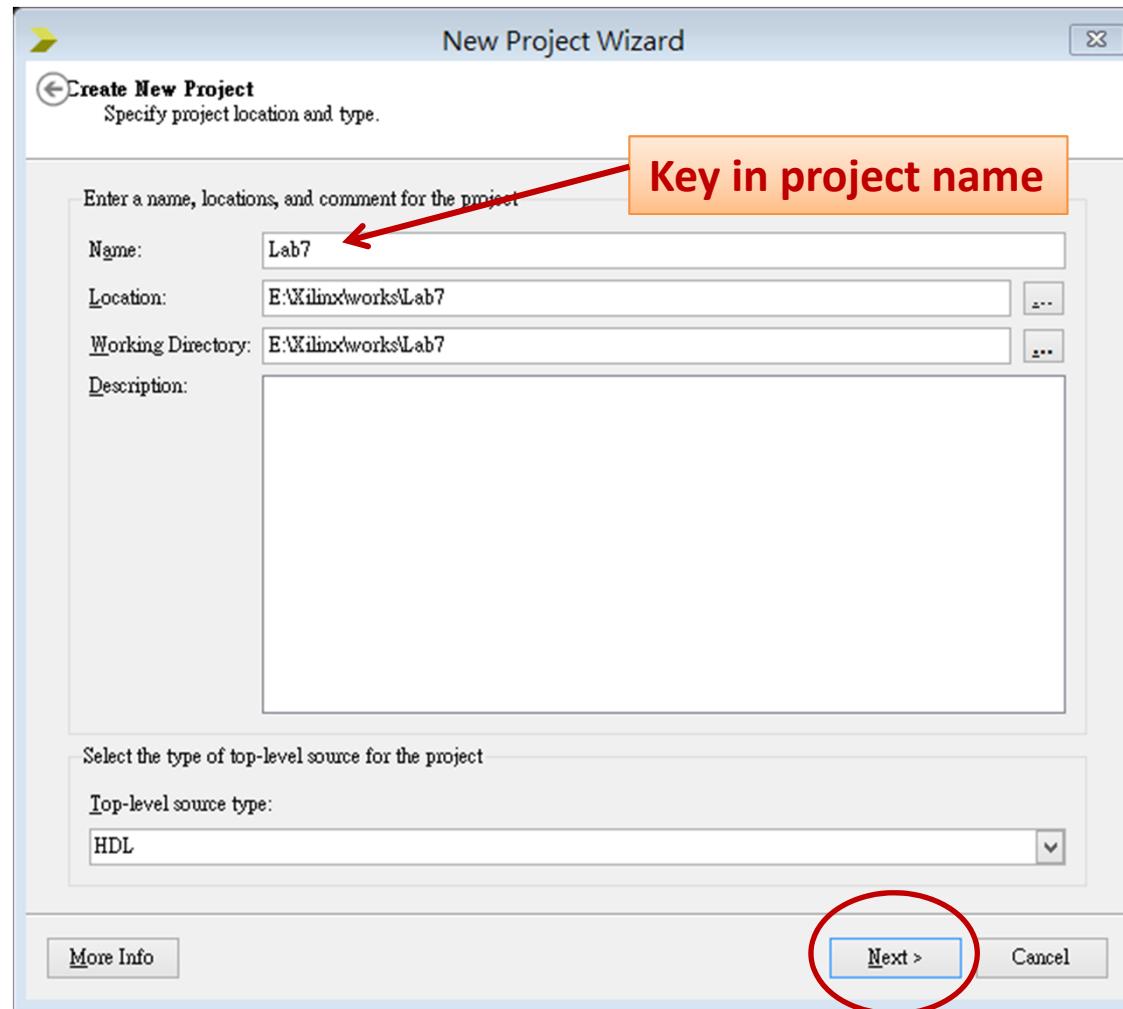


You can download by yourself, it is free.

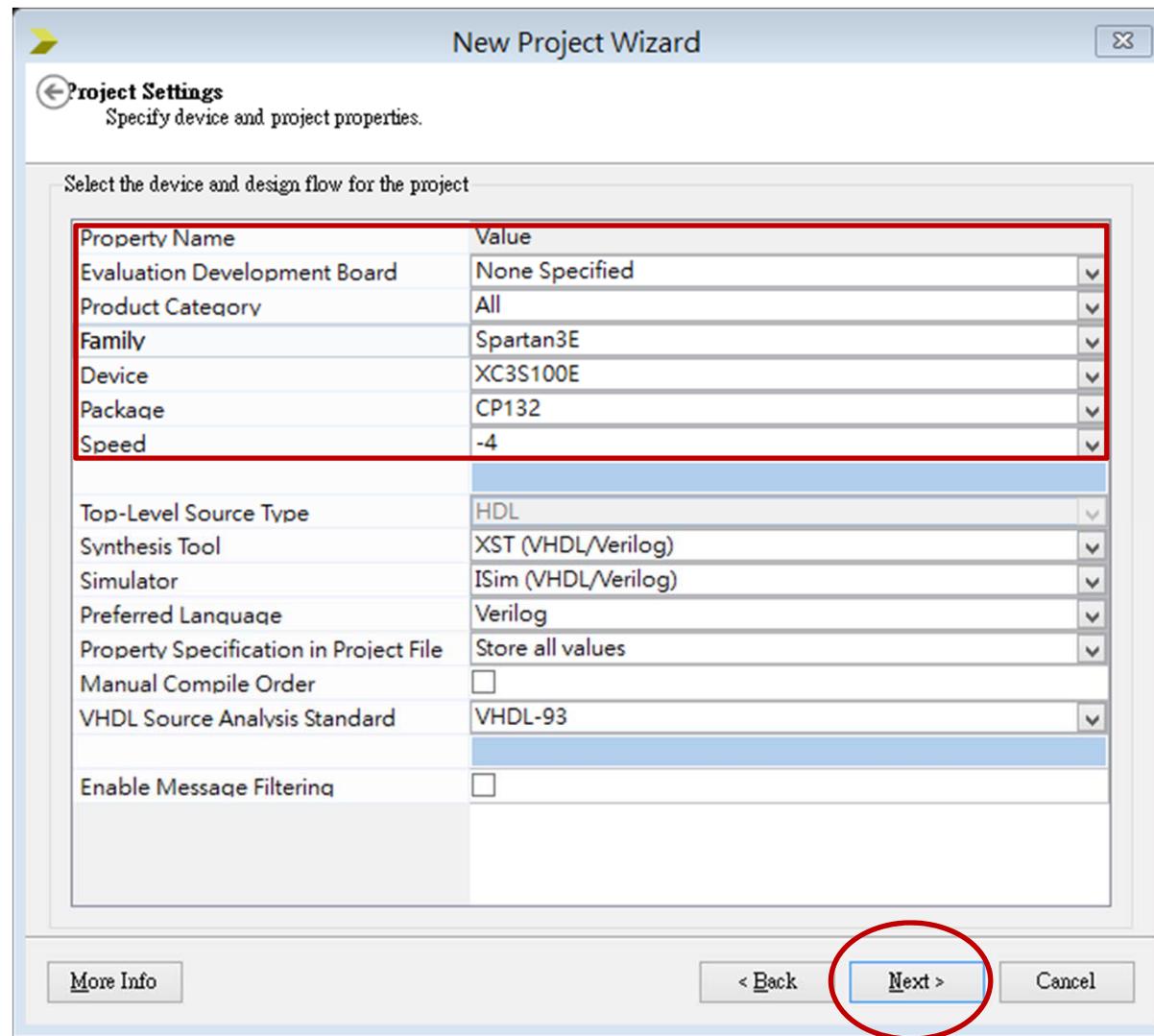
Xilinx FPGA Design Flow

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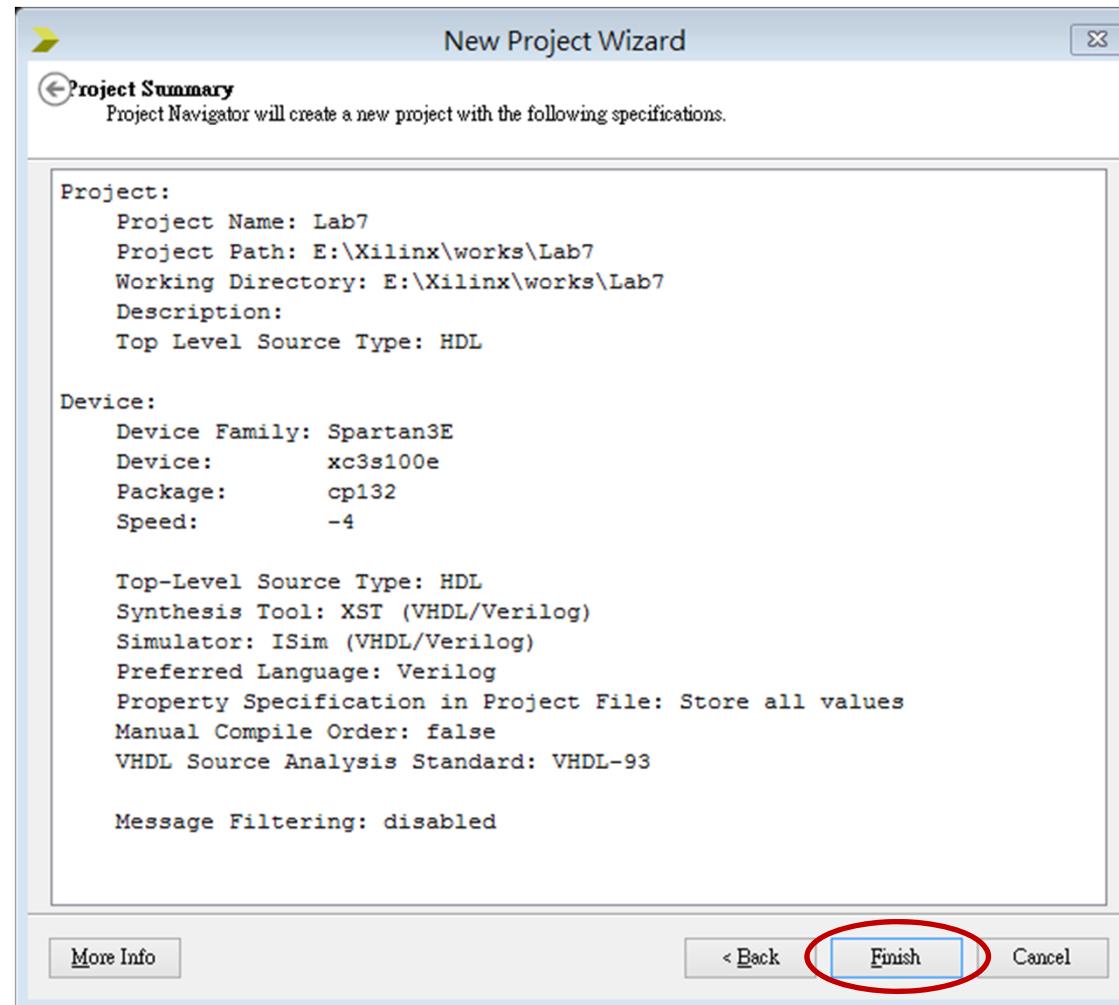
New Project



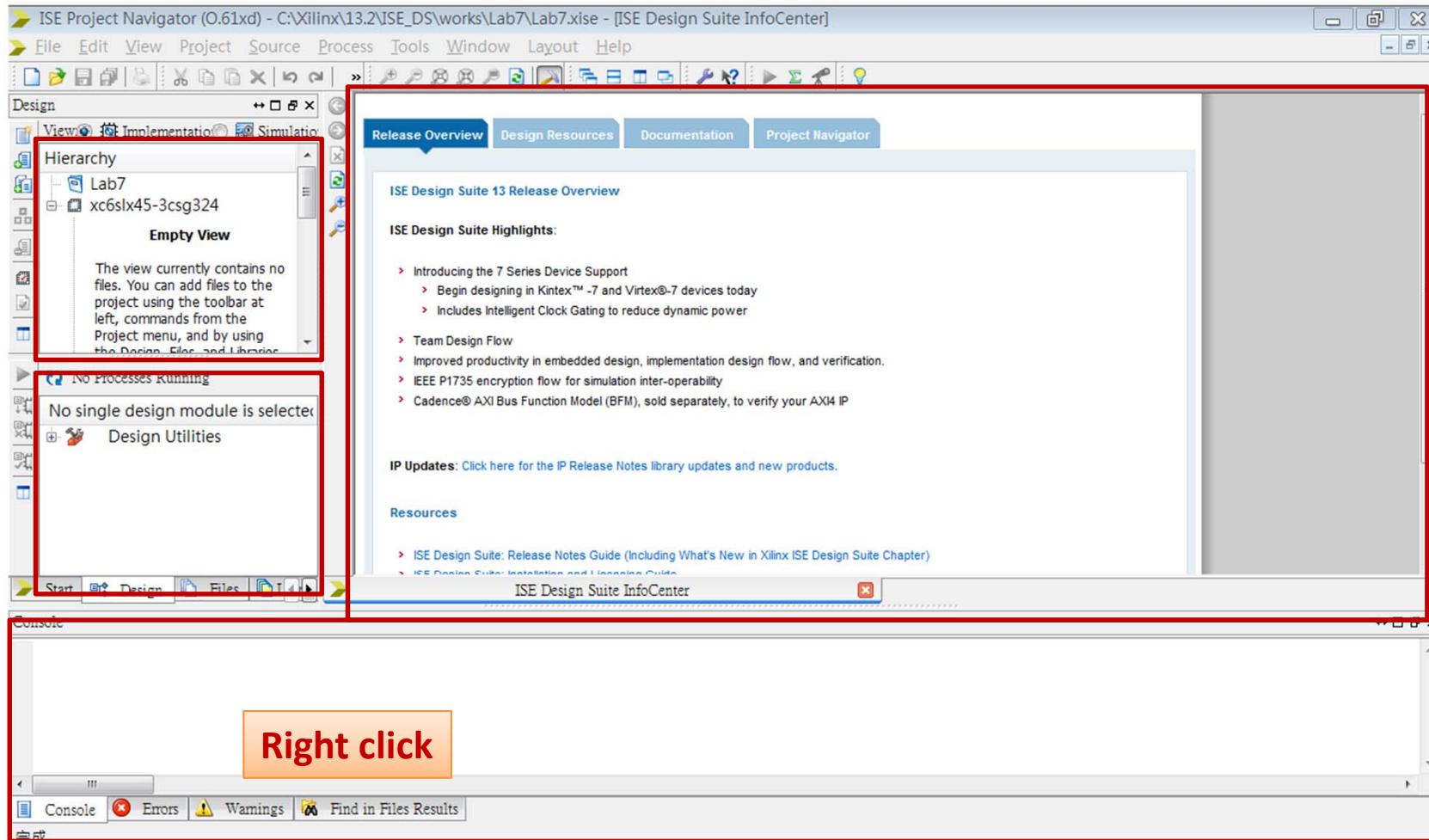
Project Settings



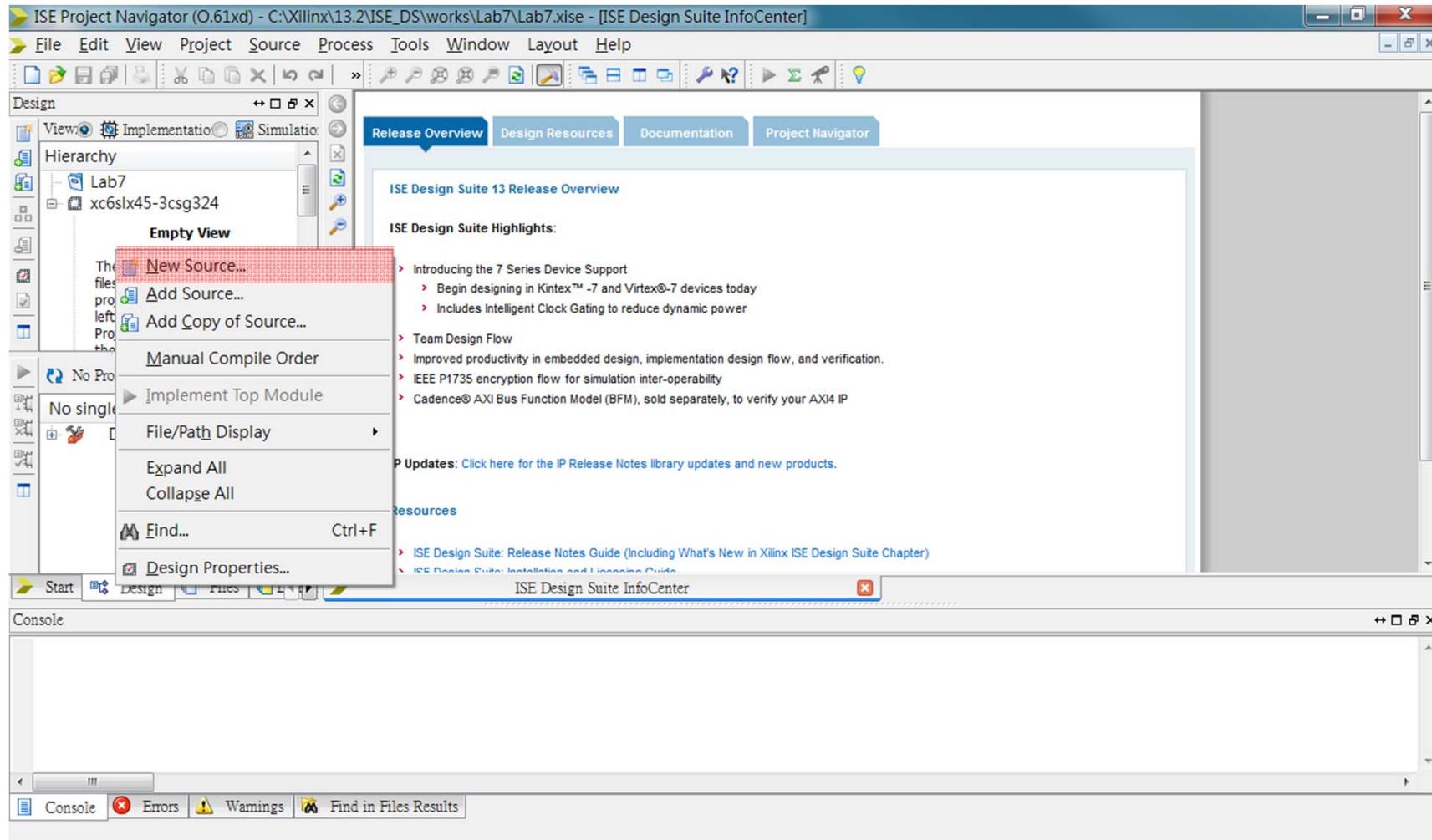
Project Summary



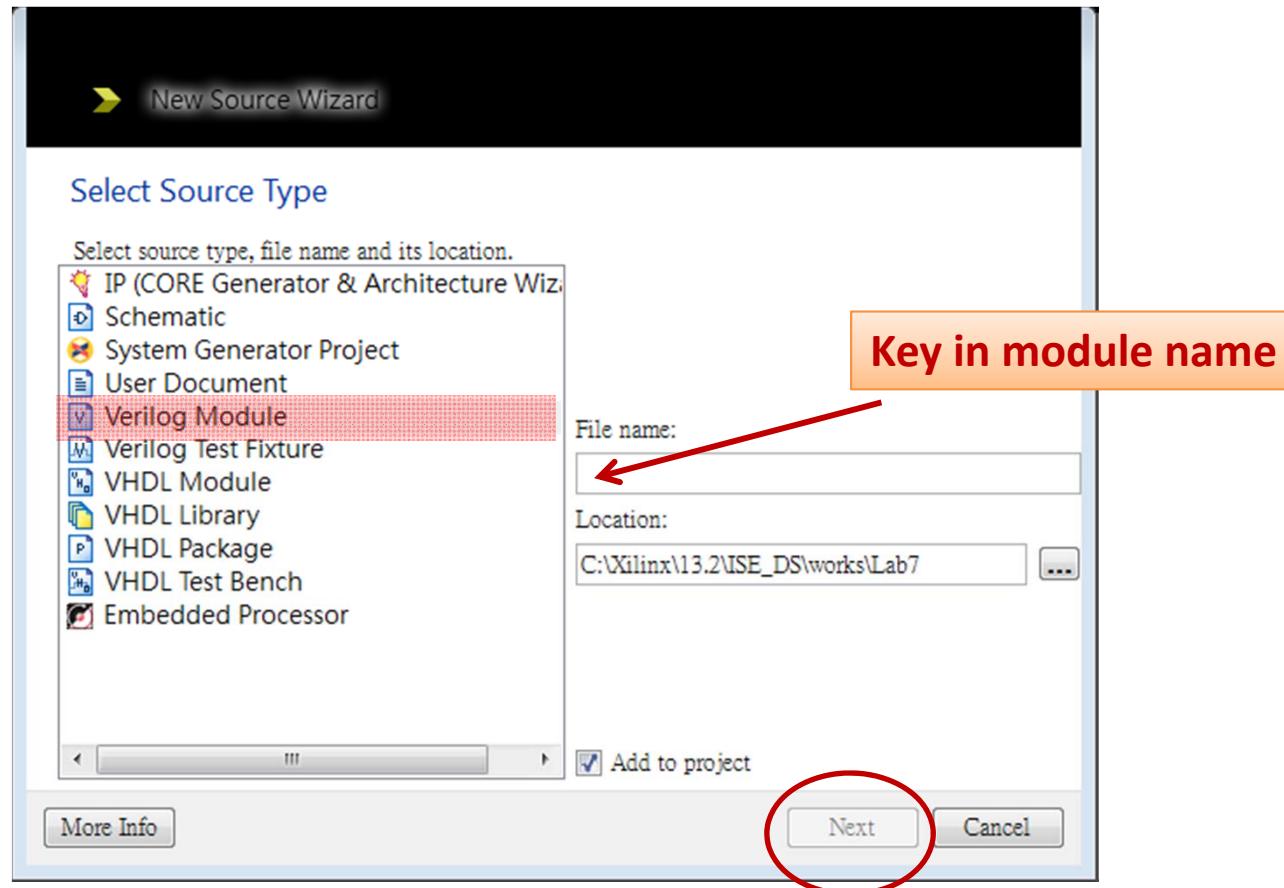
GUI Window



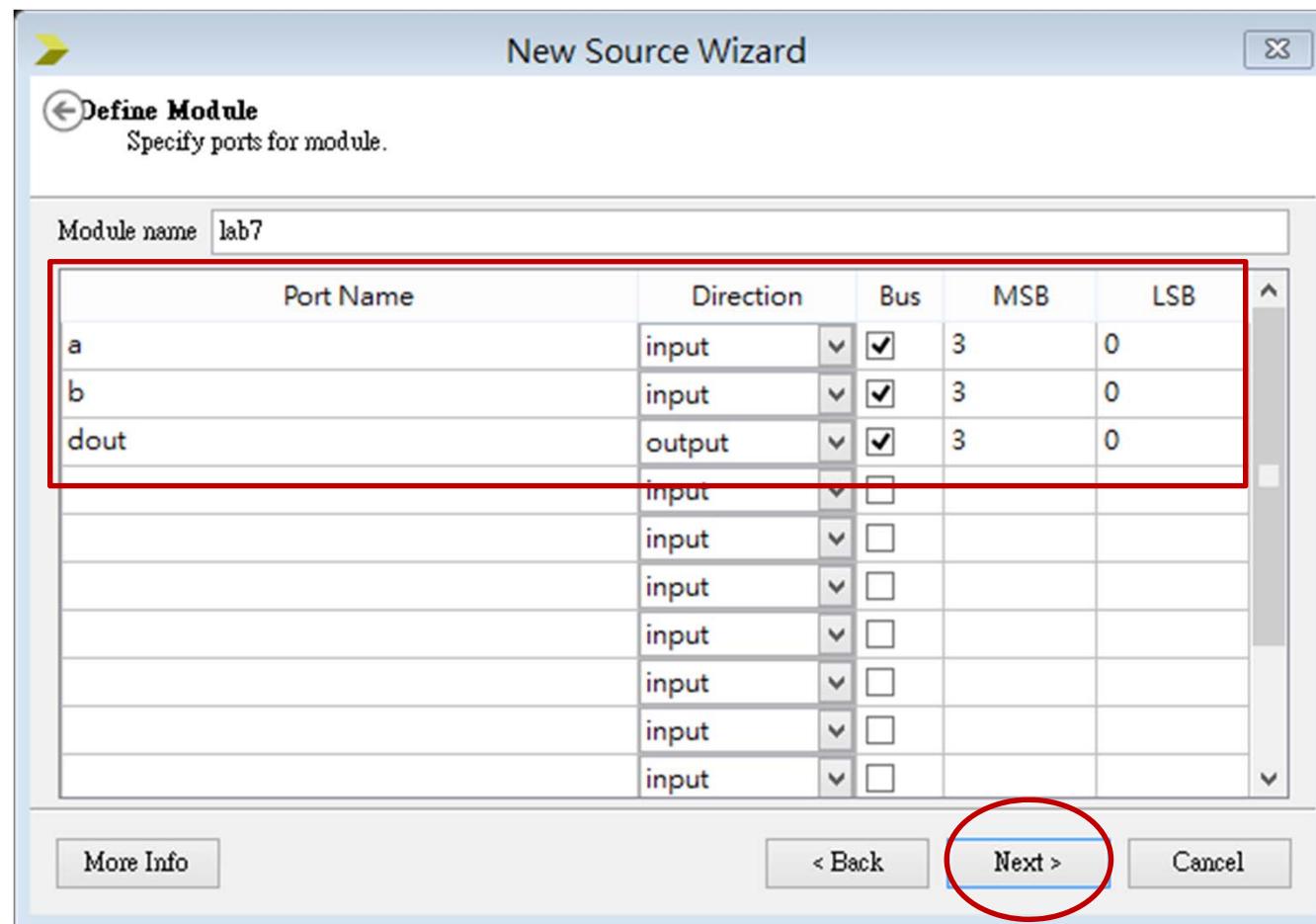
New Source



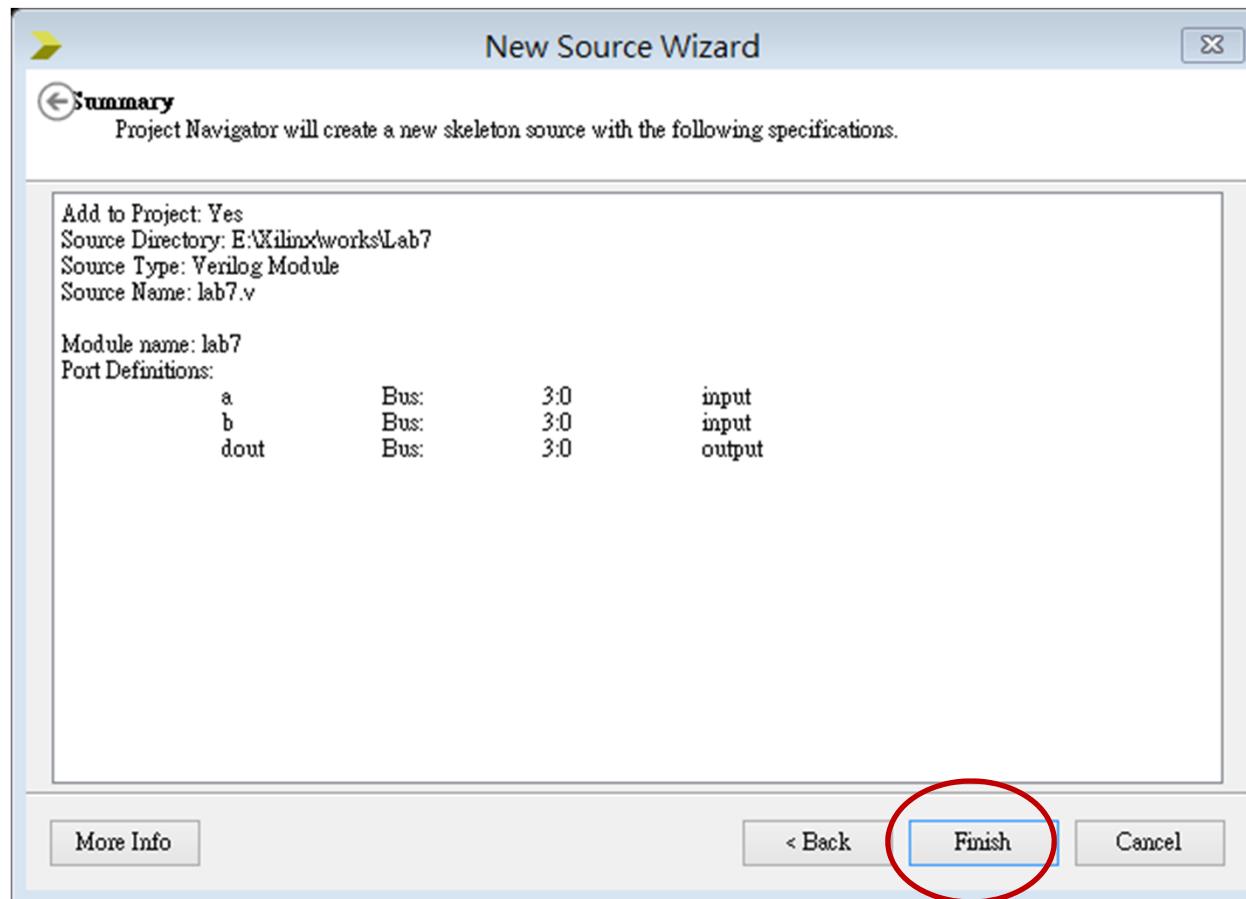
New Source



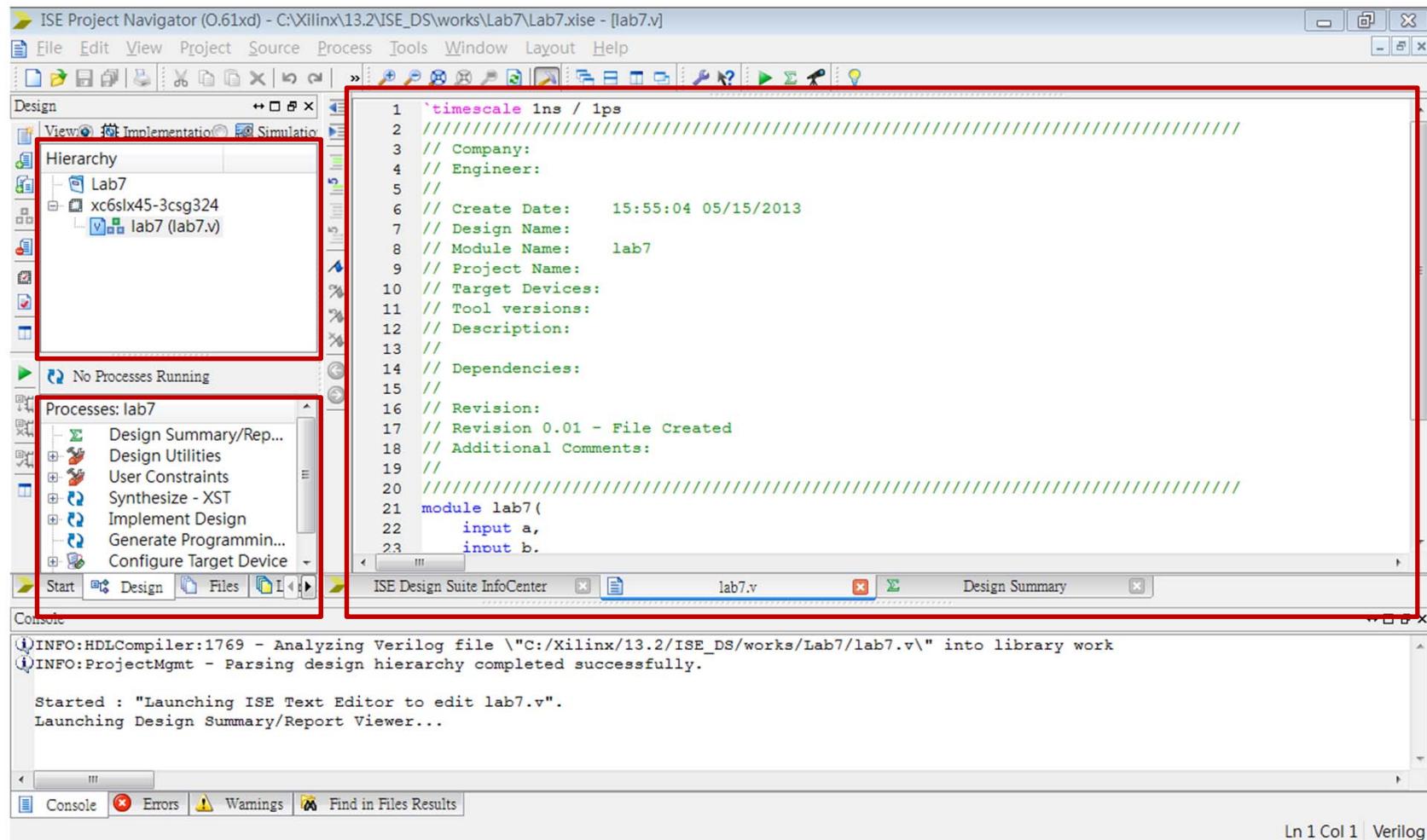
Port Define



Summary



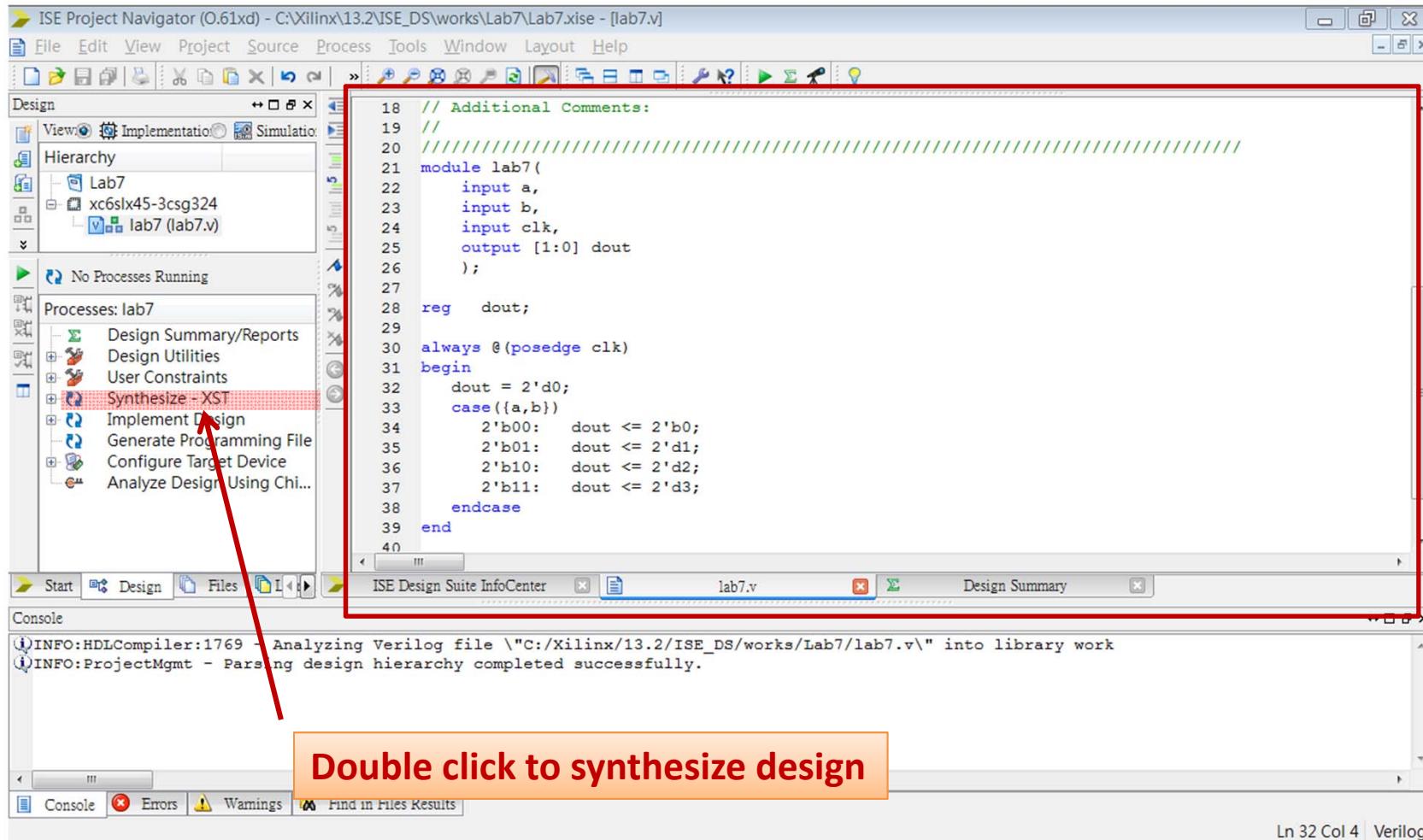
Verilog Generation



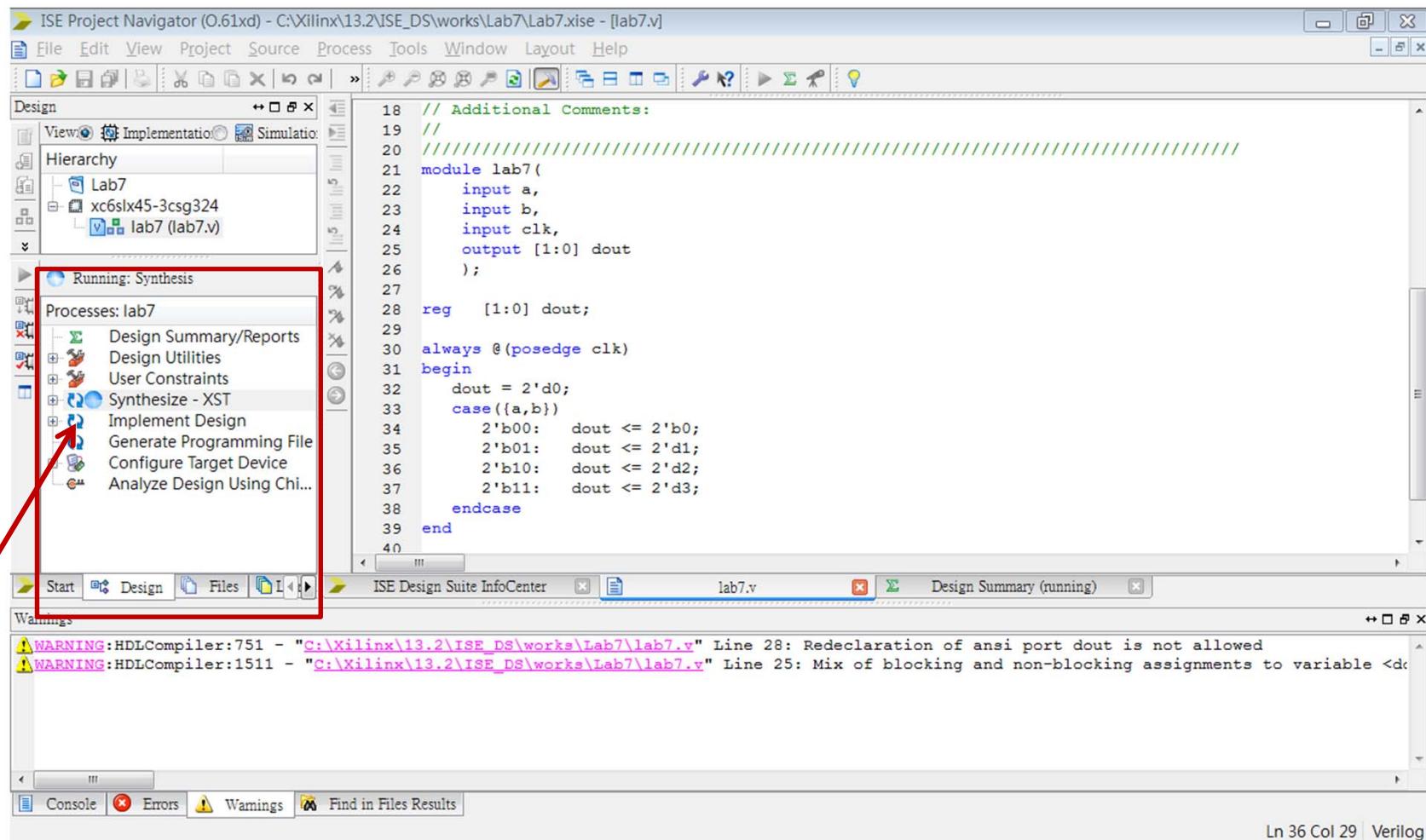
Verilog code

```
1 `timescale 1ns / 1ps
2 ///////////////////////////////////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 15:57:34 11/27/2013
7 // Design Name:
8 // Module Name: lab7
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21 module lab7(
22     input [3:0] a,
23     input [3:0] b,
24     output [3:0] dout
25 );
26
27
28     assign dout = a + b;
29
30 endmodule
31 |
```

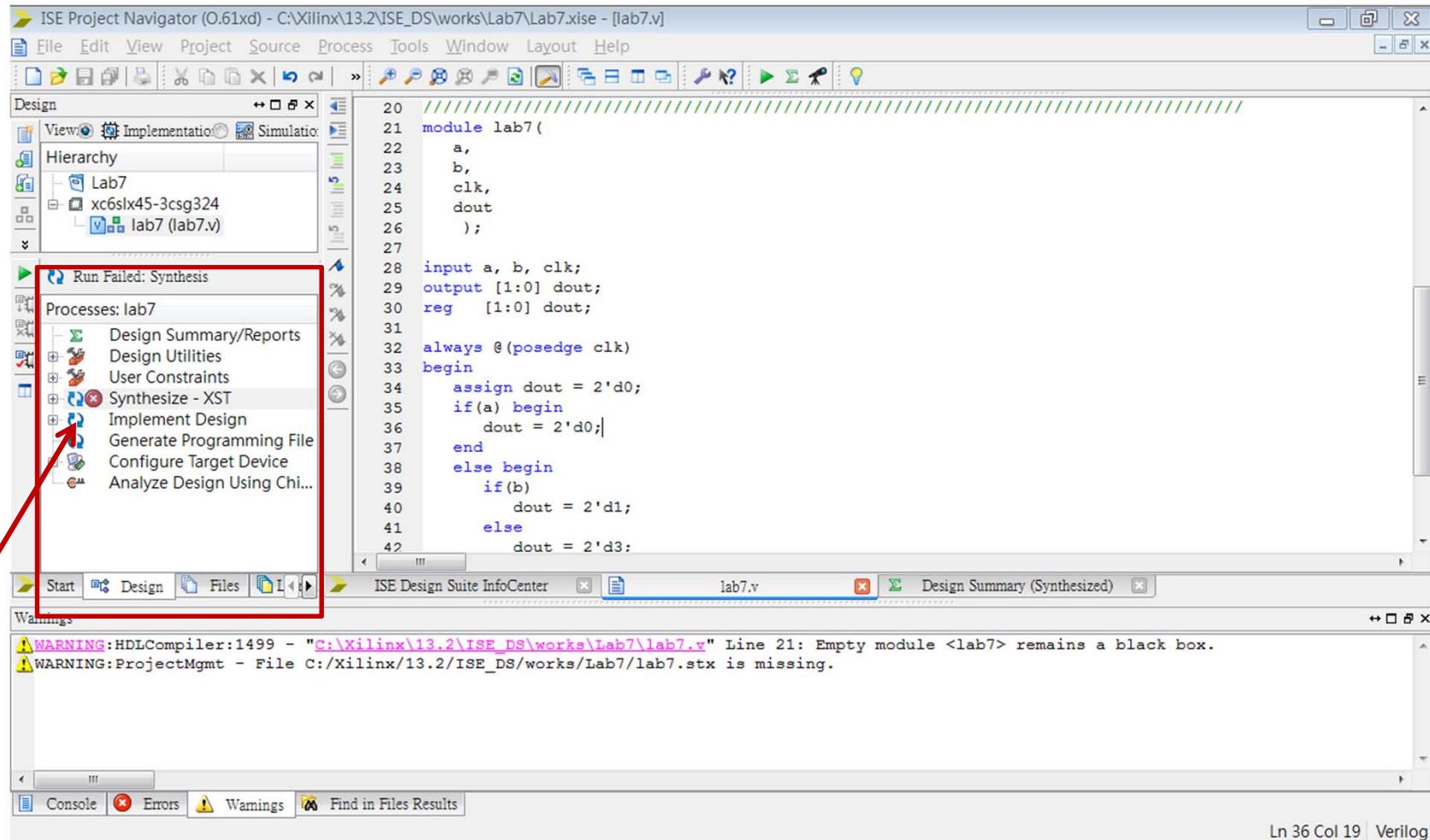
Coding Design



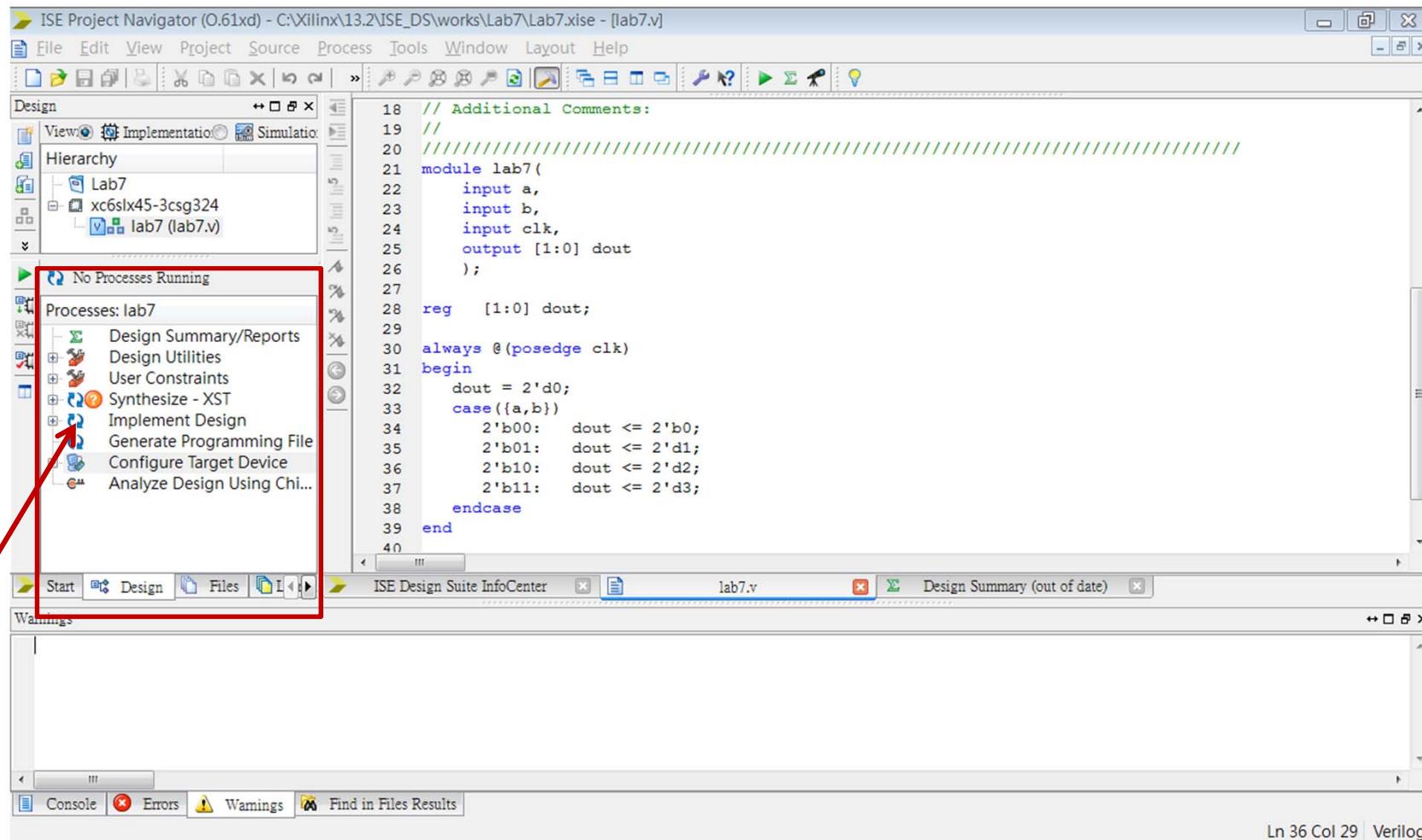
Run Synthesizing



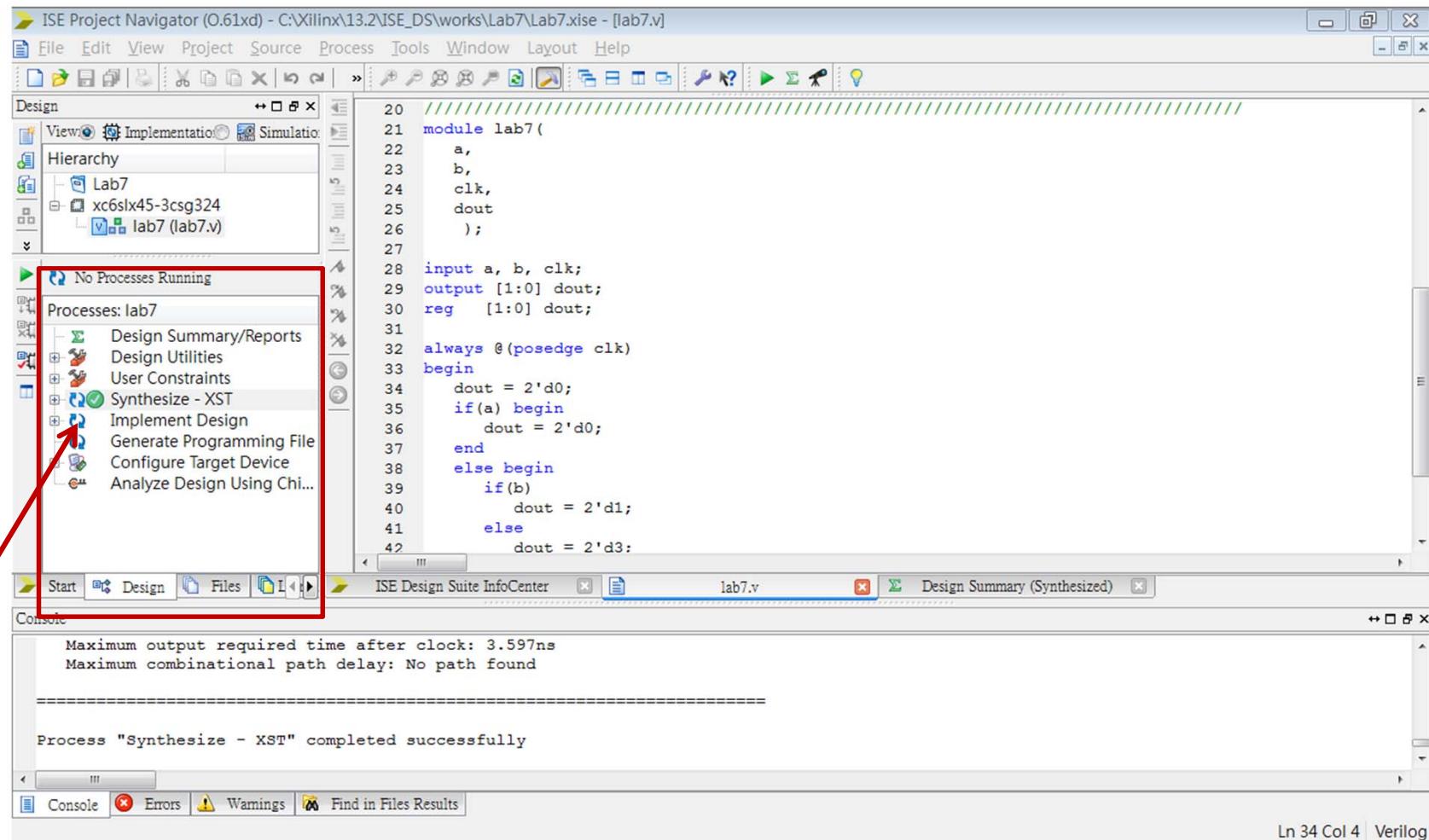
Synthesis Fail



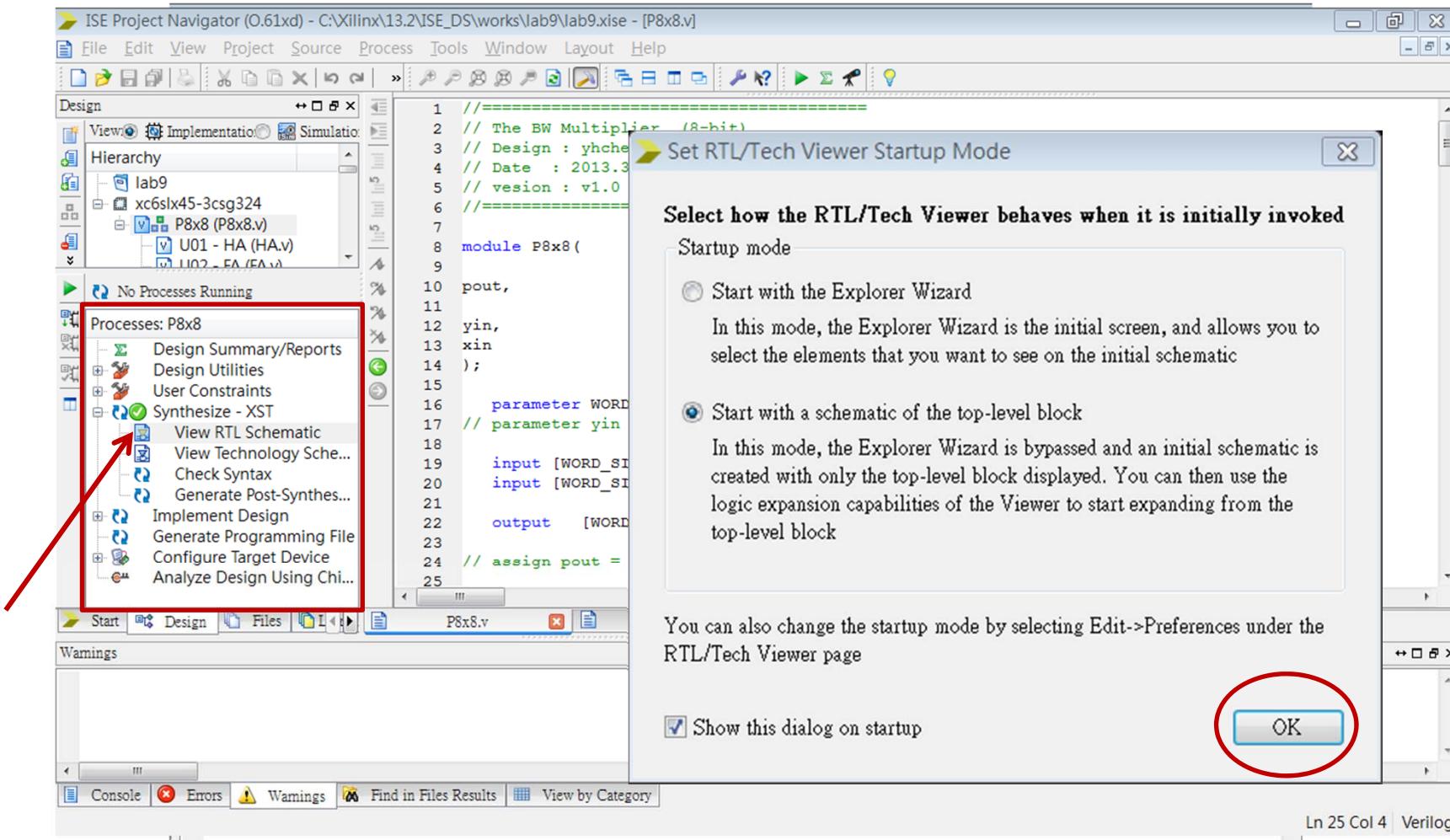
Modify Design



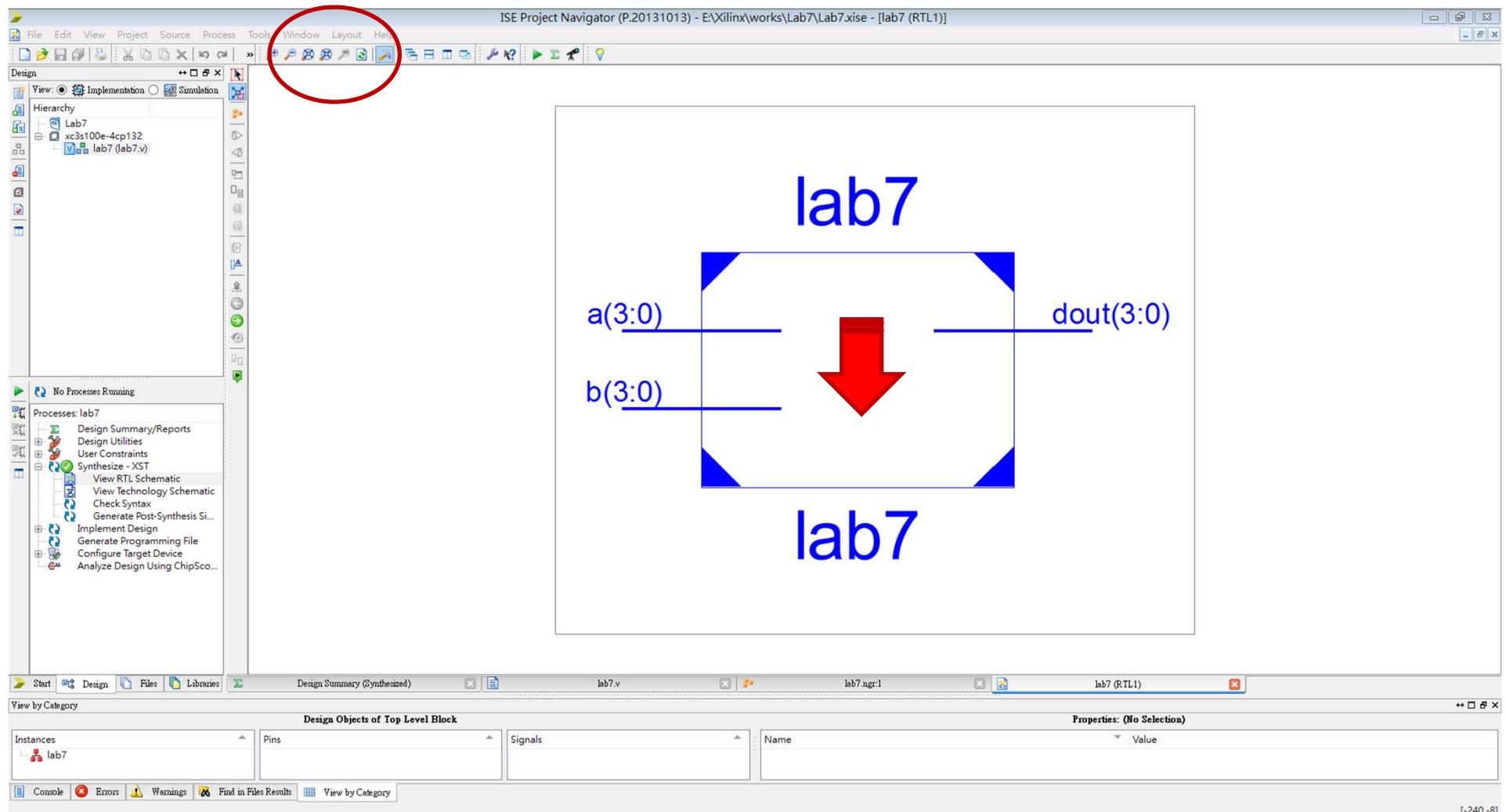
Synthesis Pass



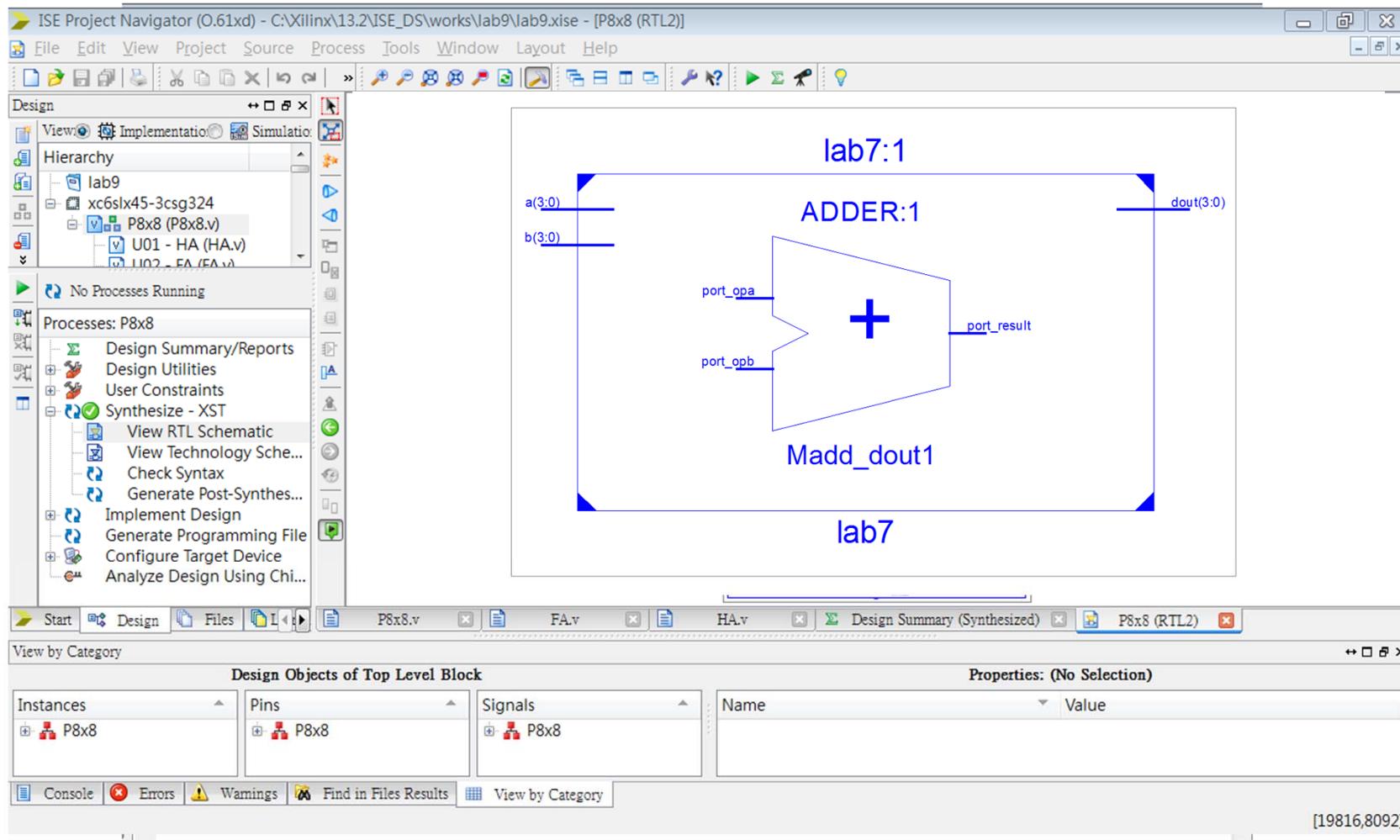
View RTL Schematic



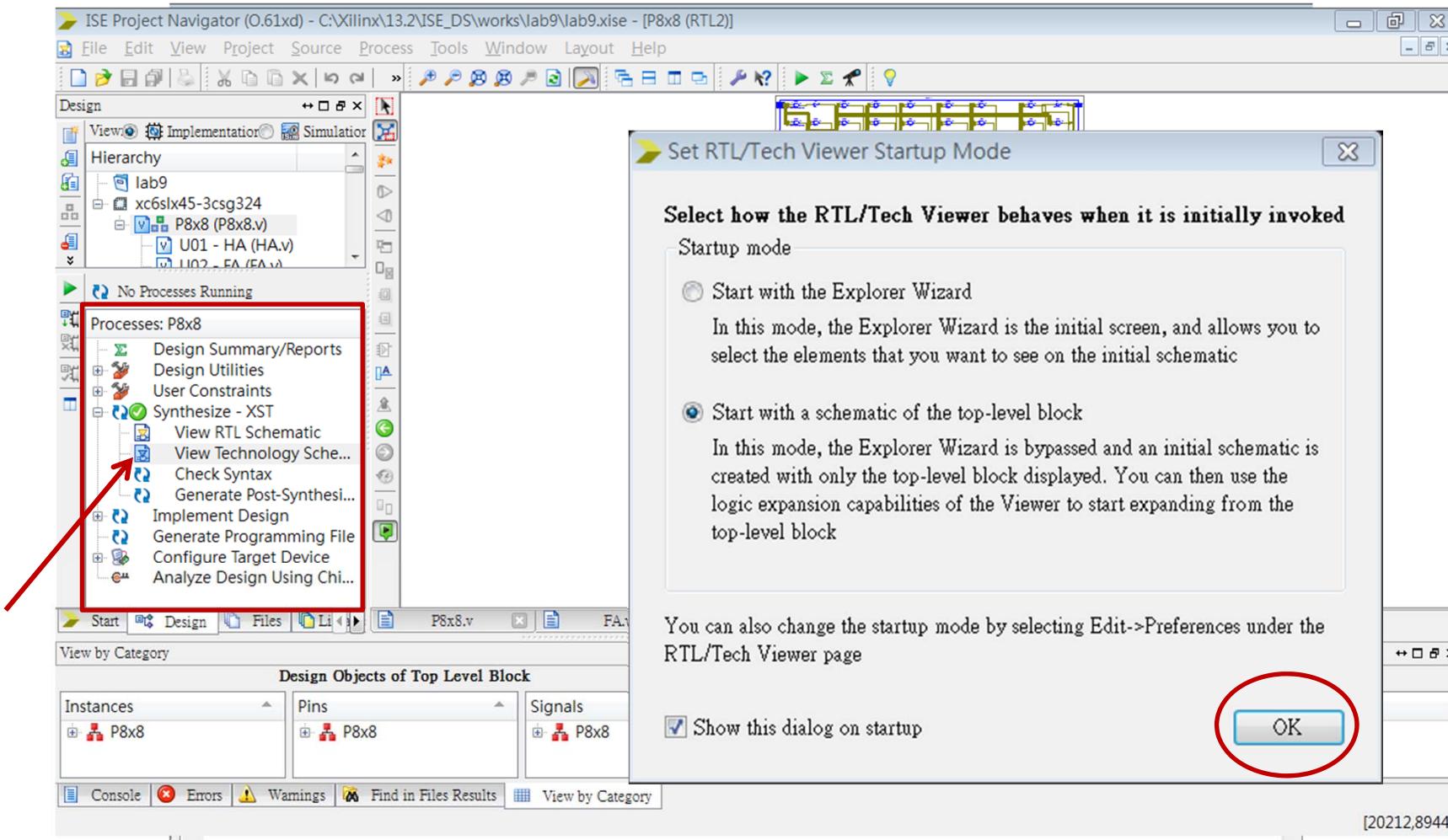
View RTL Schematic



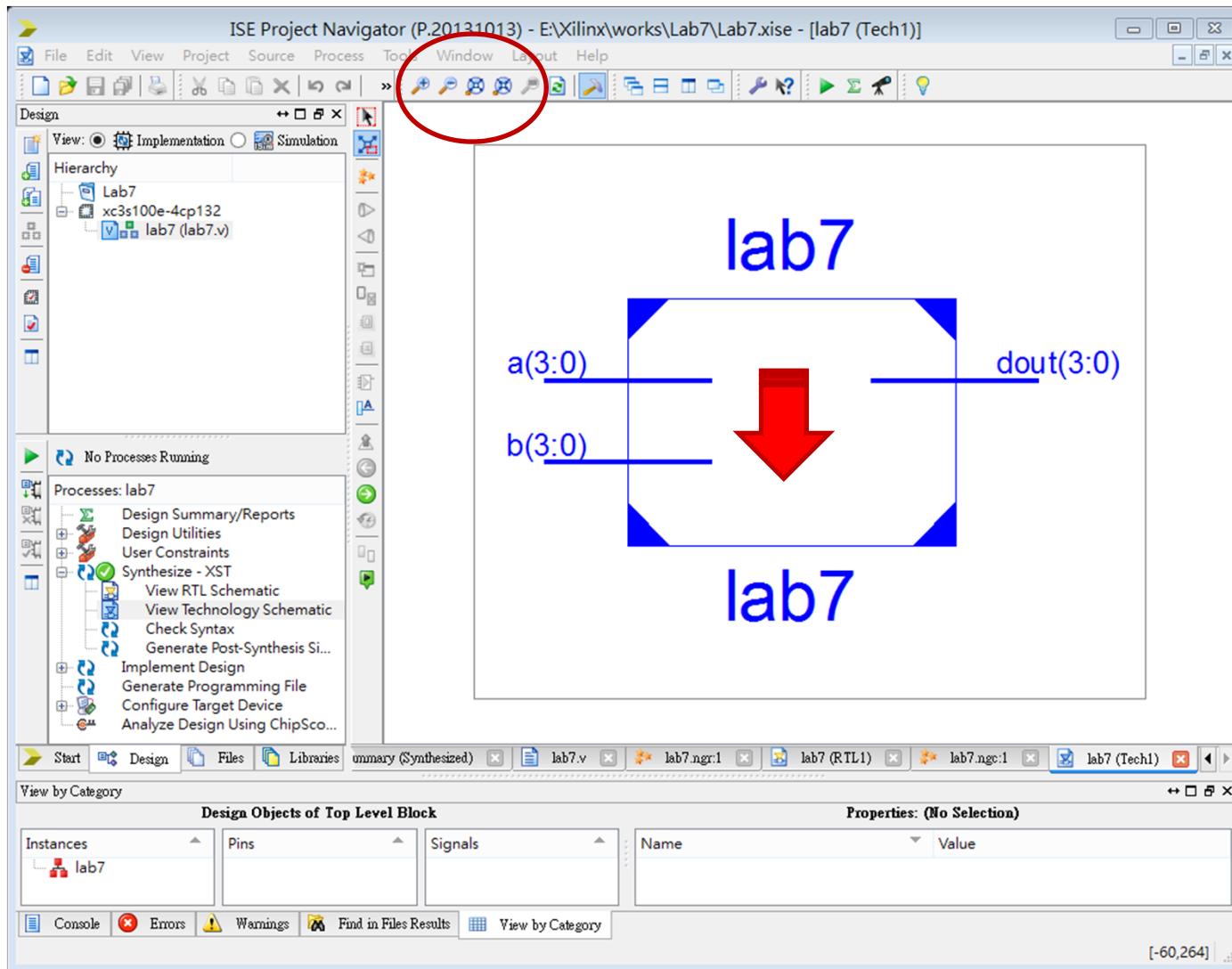
View RTL Schematic



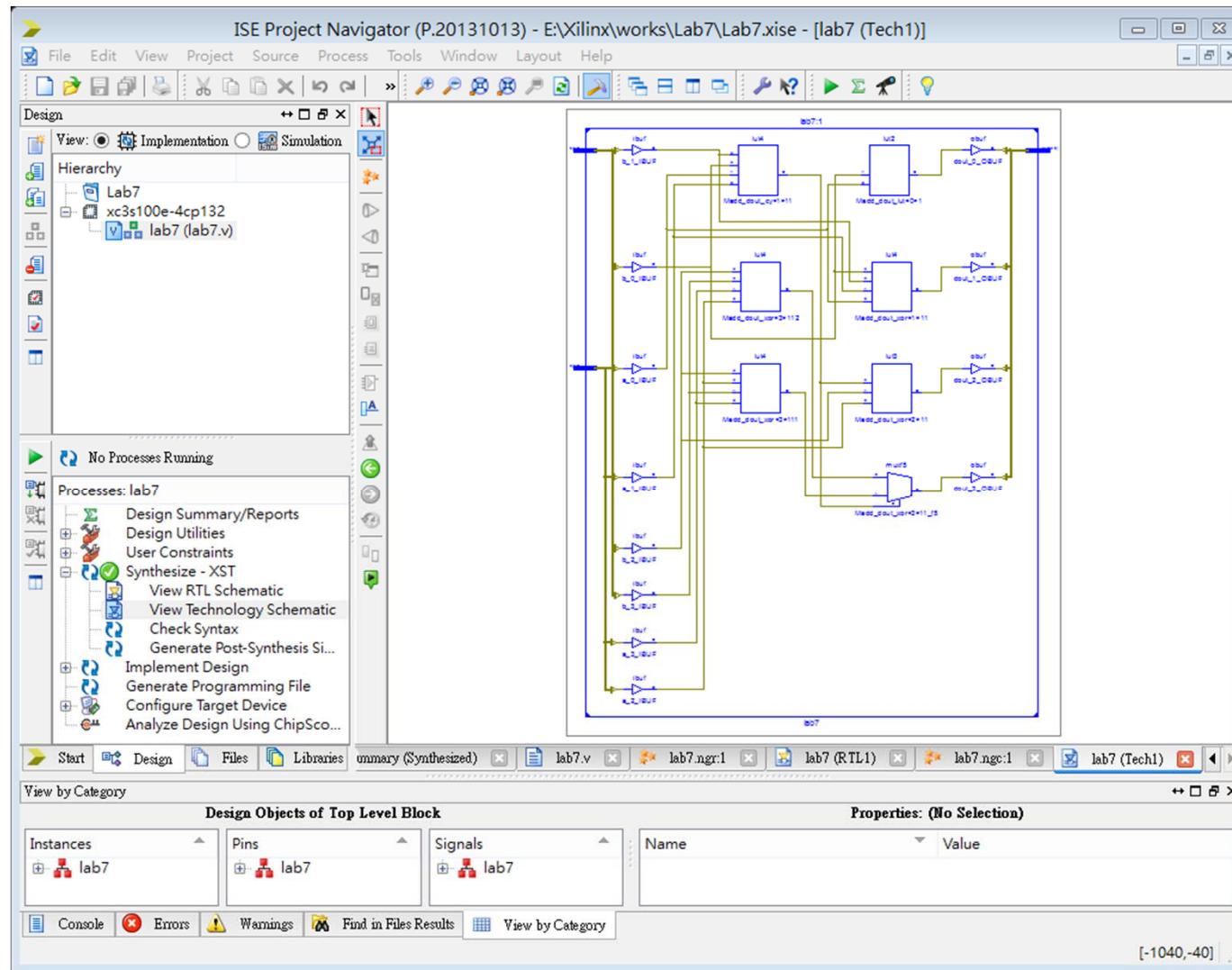
View Technology Schematic



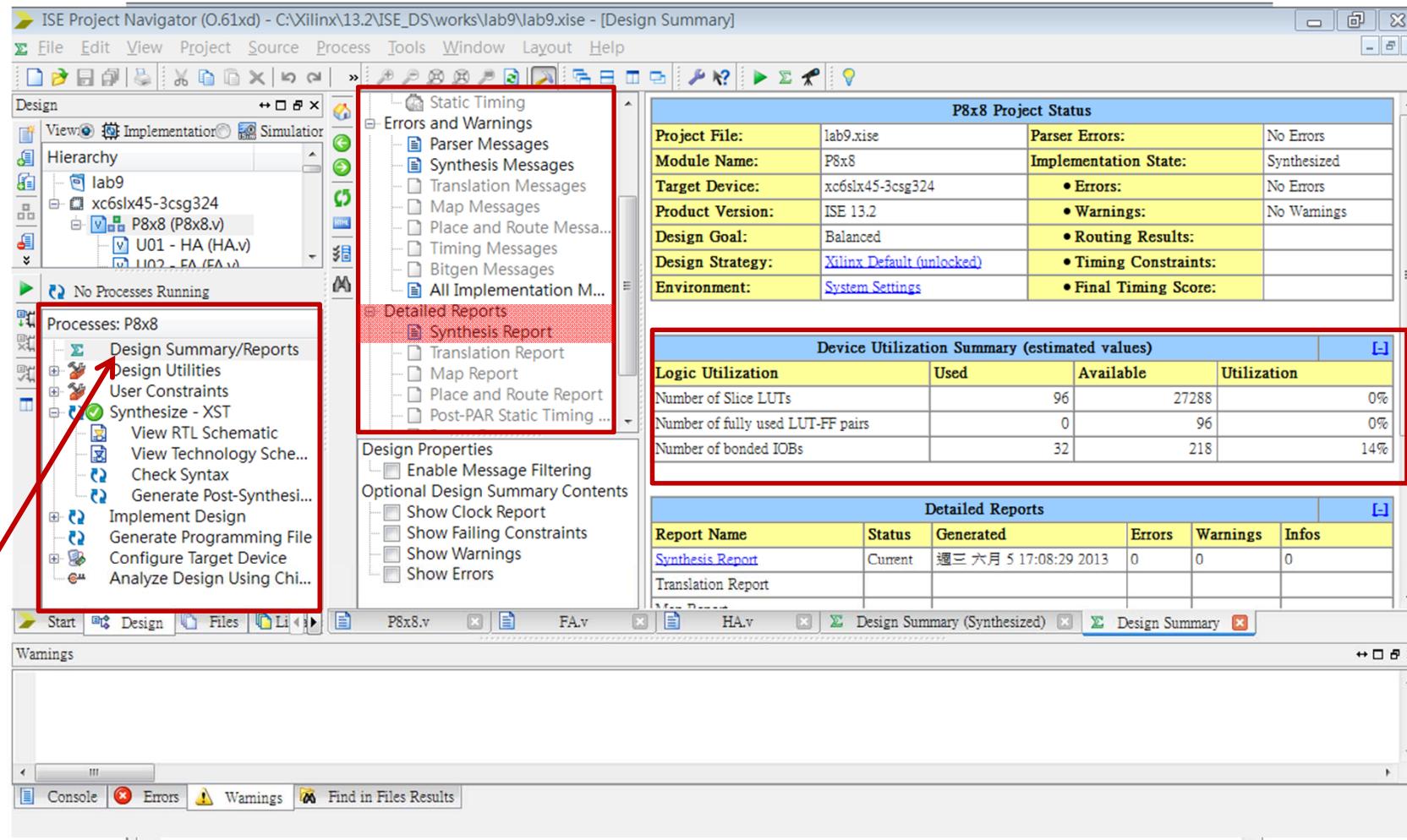
View Technology Schematic



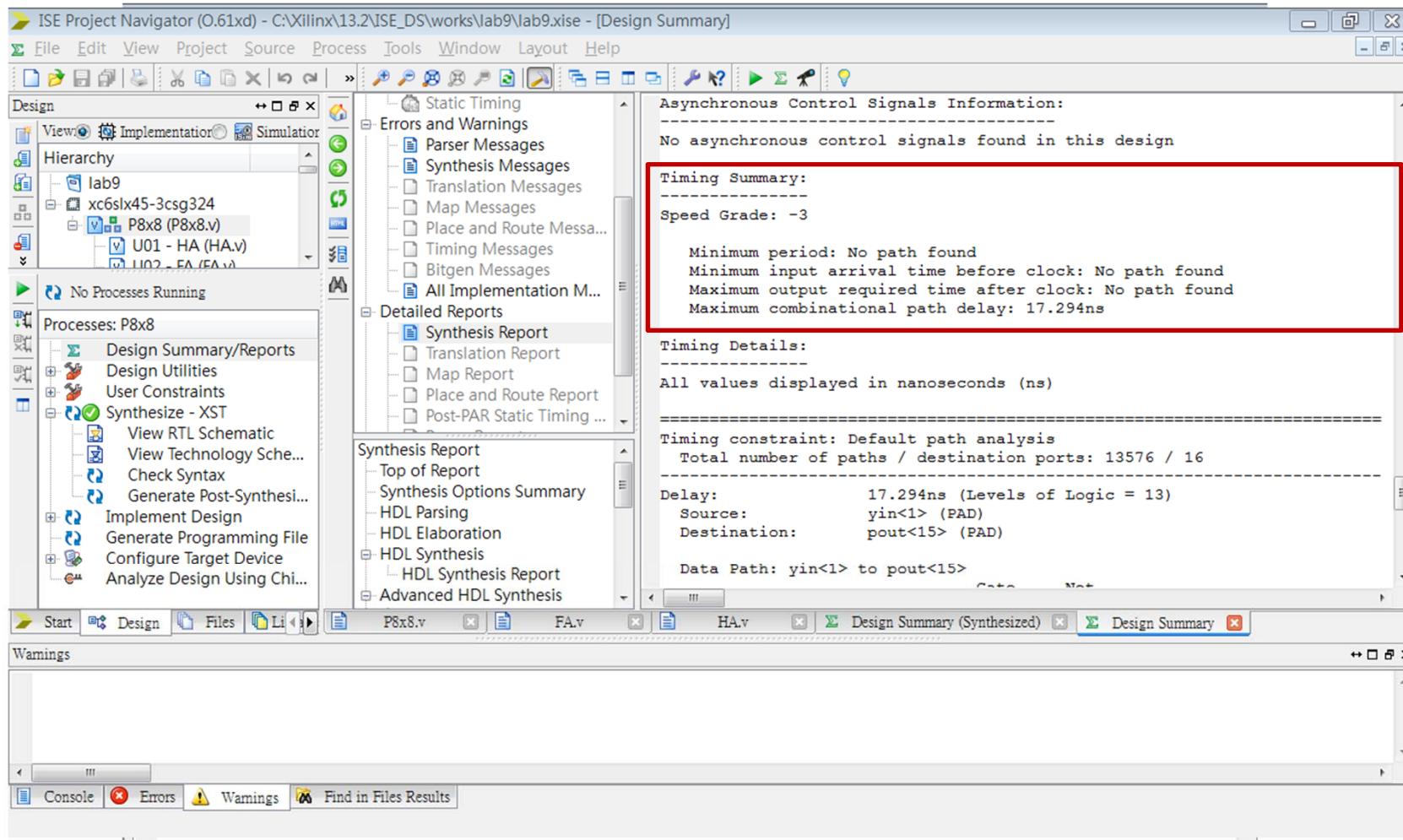
View Technology Schematic



View Design Summary



View Timing Report

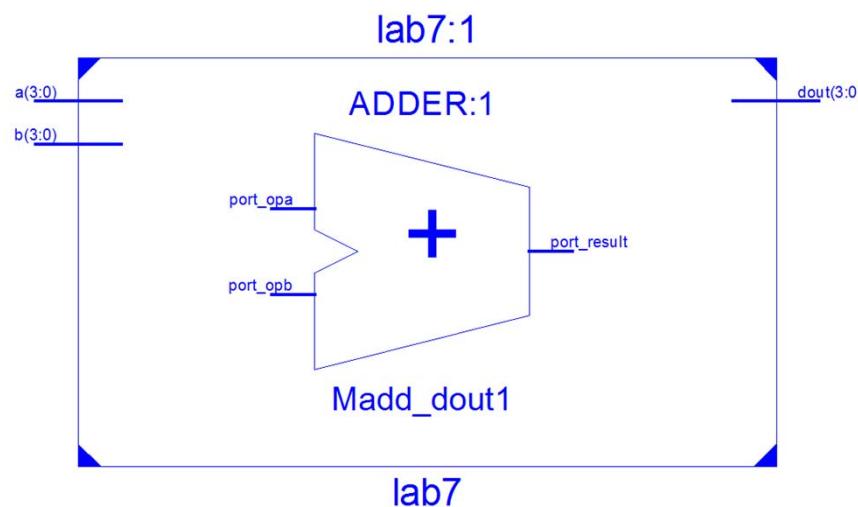


Xilinx FPGA Design Flow

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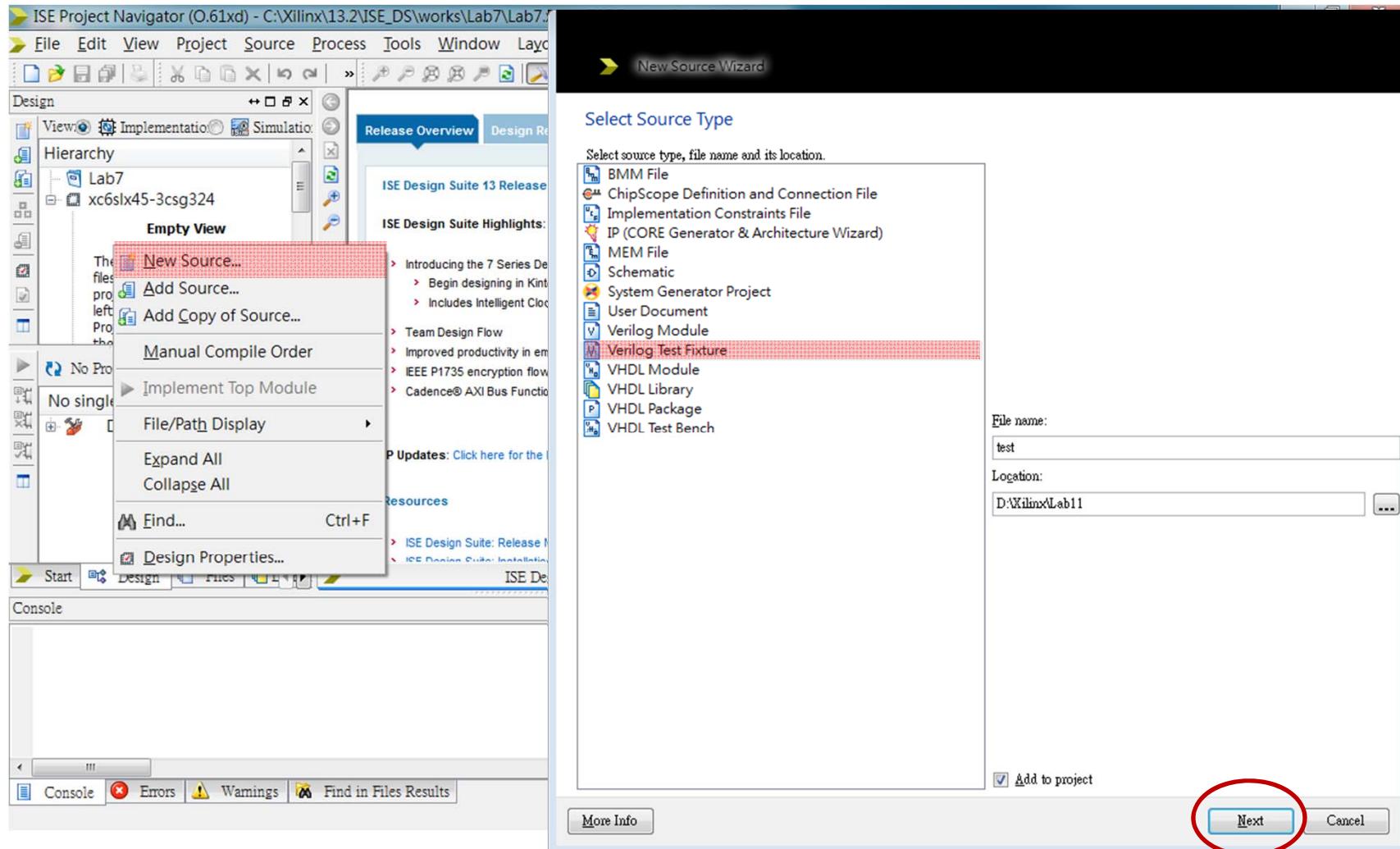
Pre-simulation

- **DUT- mult**

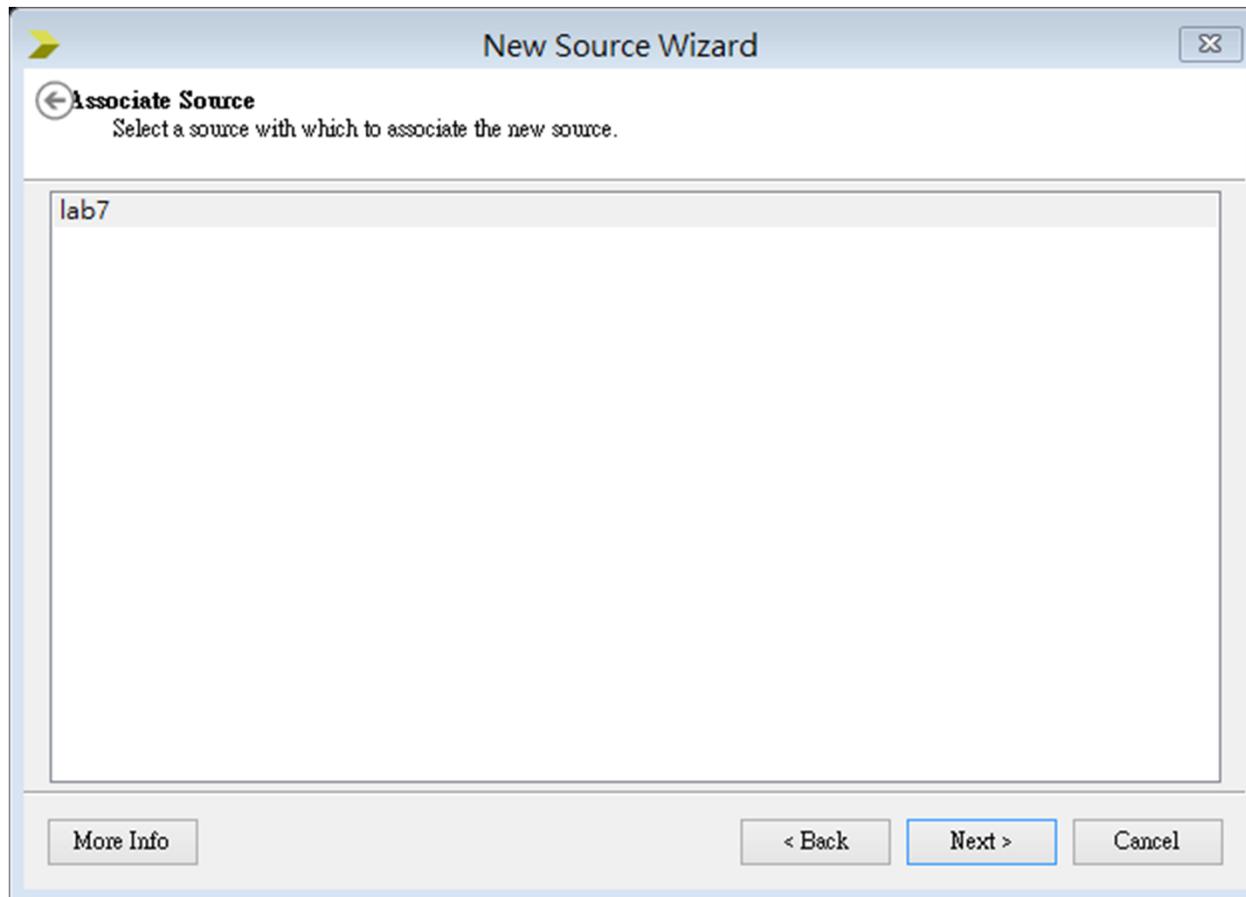


- input [3:0] a ;
- input [3:0] b ;
- output [3:0] $dout$;

Pre-sim Test Bench (User Design)



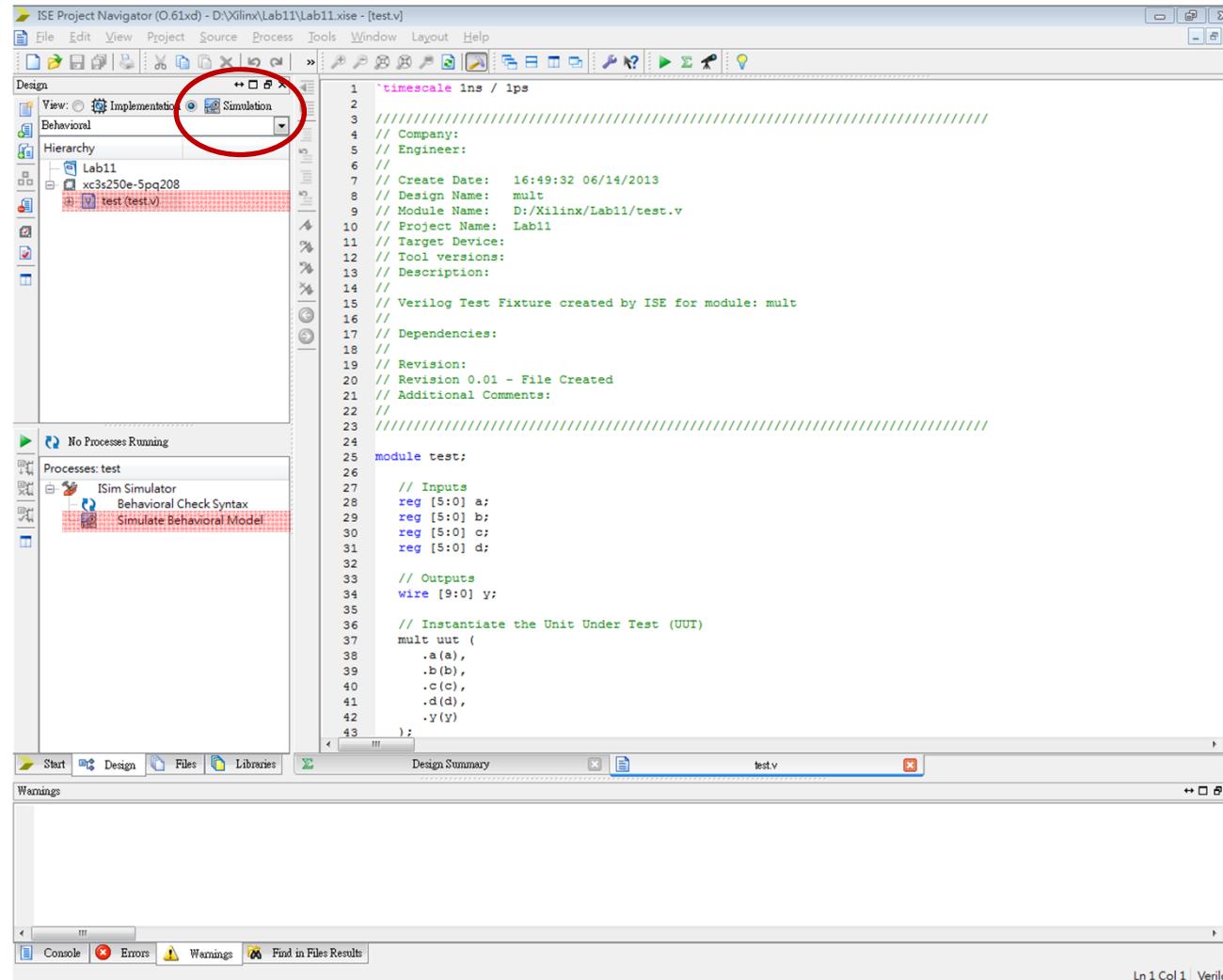
Pre-sim Test Bench (User Design)



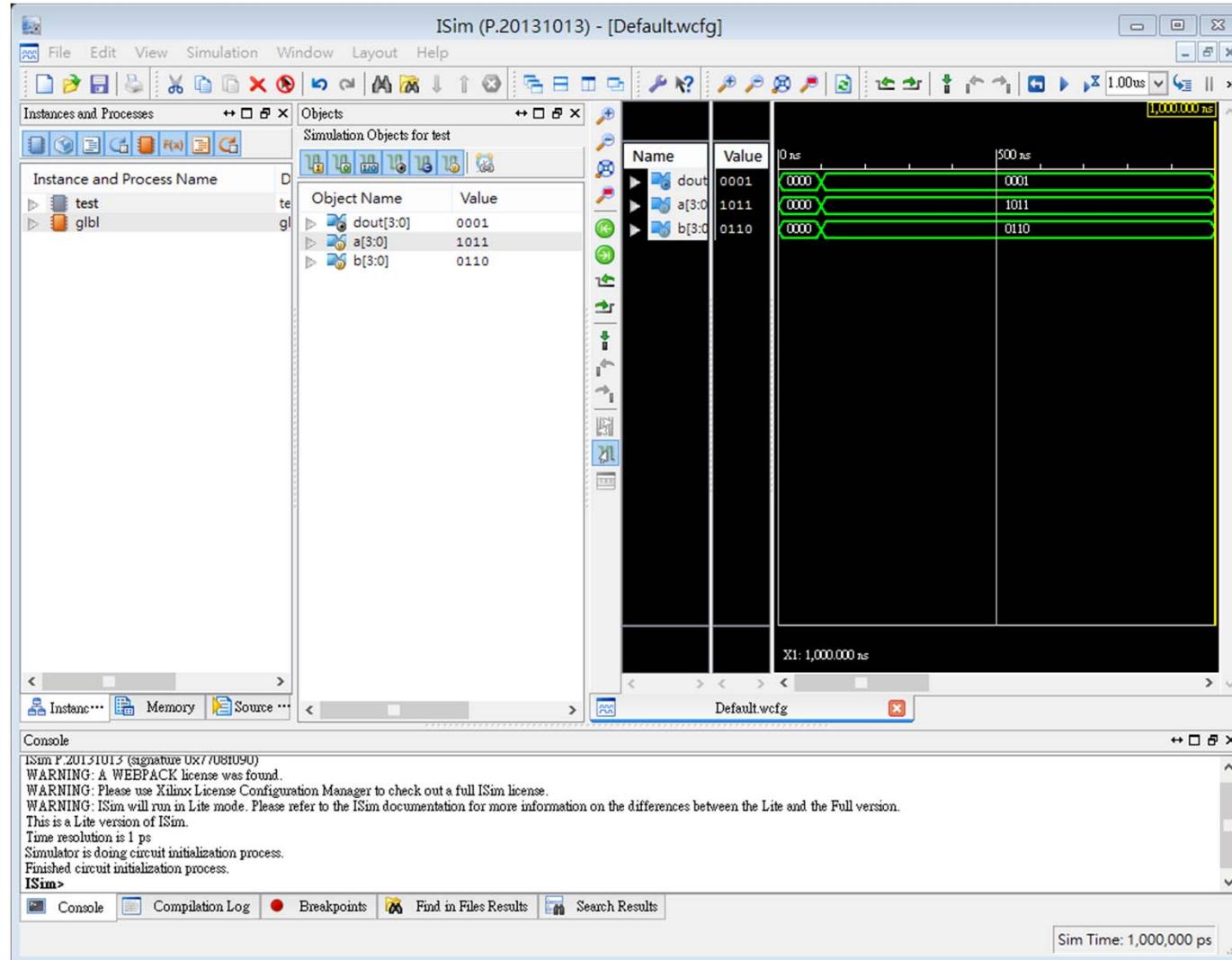
Pre-sim Test Bench (User Design)

```
25 module test;
26
27     // Inputs
28     reg [3:0] a;
29     reg [3:0] b;
30
31     // Outputs
32     wire [3:0] dout;
33
34     // Instantiate the Unit Under Test (UUT)
35     lab7 uut (
36         .a(a),
37         .b(b),
38         .dout(dout)
39     );
40
41     initial begin
42         // Initialize Inputs
43         a = 0;
44         b = 0;
45
46         // Wait 100 ns for global reset to finish
47         #100;
48
49         a = 4'b1011;
50         b = 4'b0110;
51         // Add stimulus here
52
53     end
54
55 endmodule
```

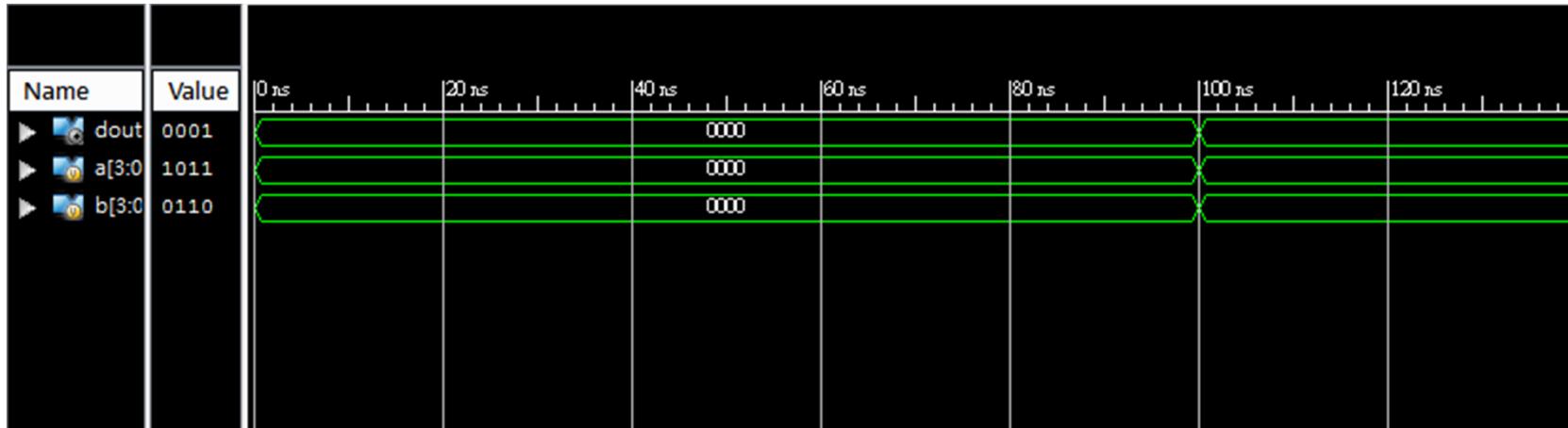
Pre-sim Test Bench (User Design)



Pre-sim Wave Form



Pre-sim Waveform Results



$$dout = a + b$$

fixed – point Operation :

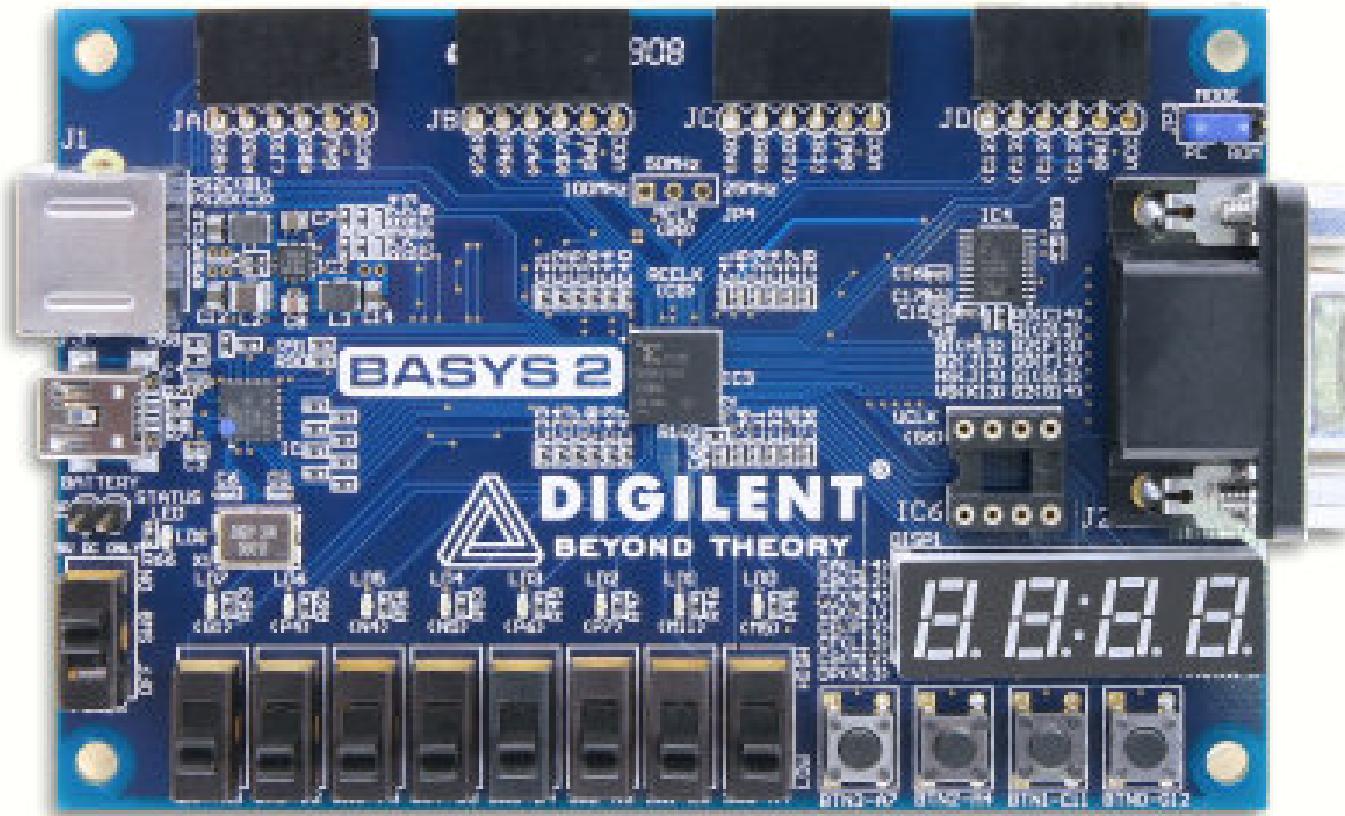
$$1011 + 0110 = 0001$$

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User Constraint File (UCF)

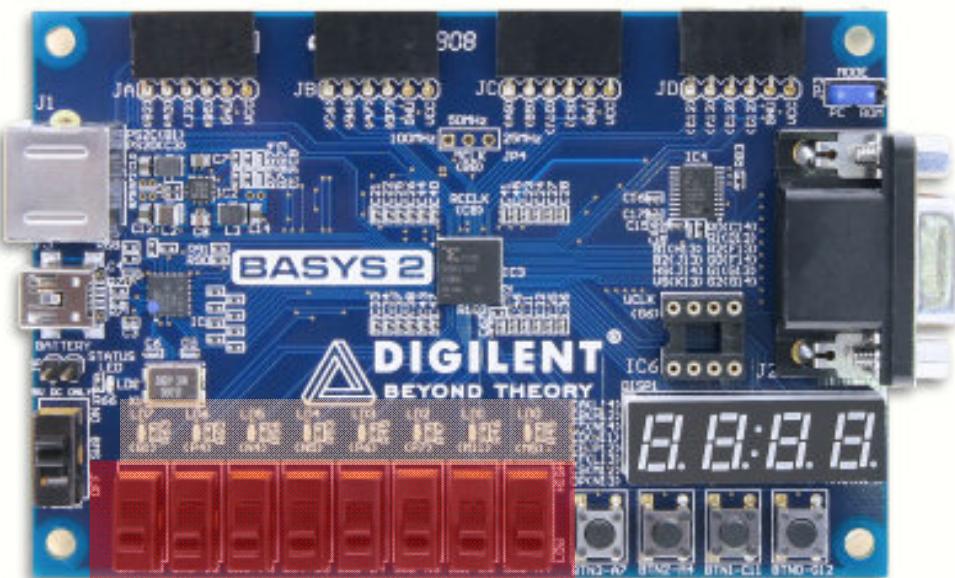
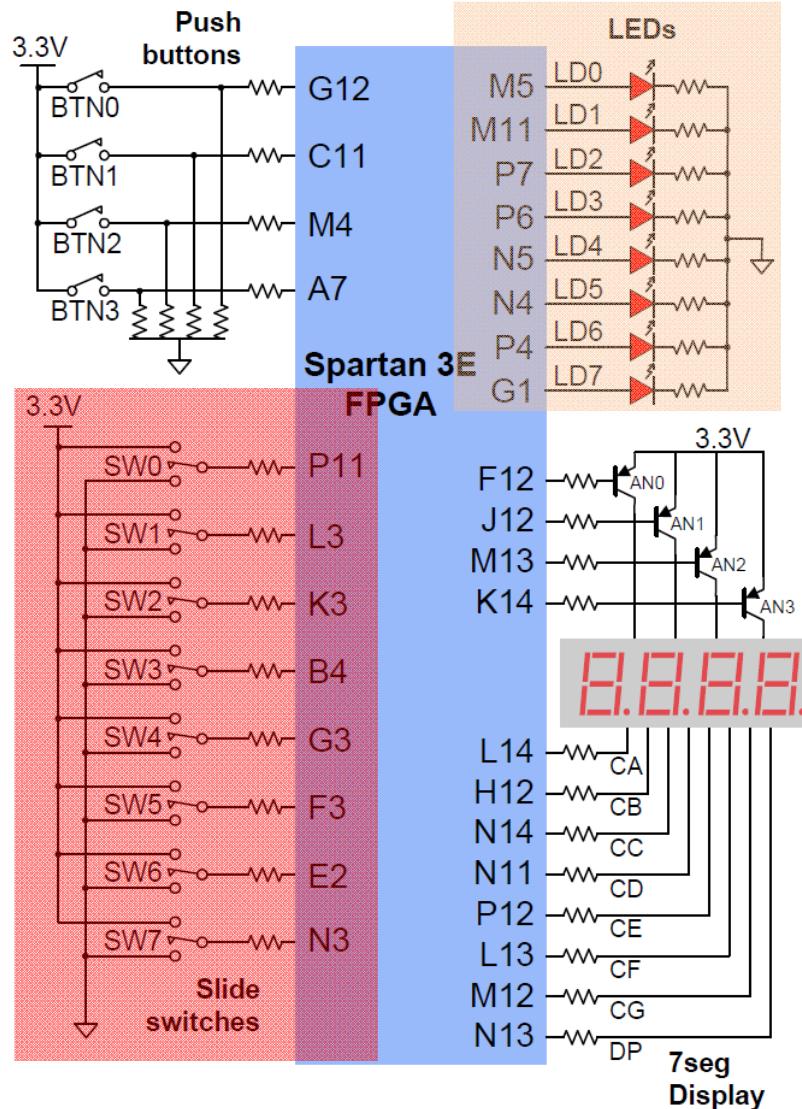
- Read pin list from manual



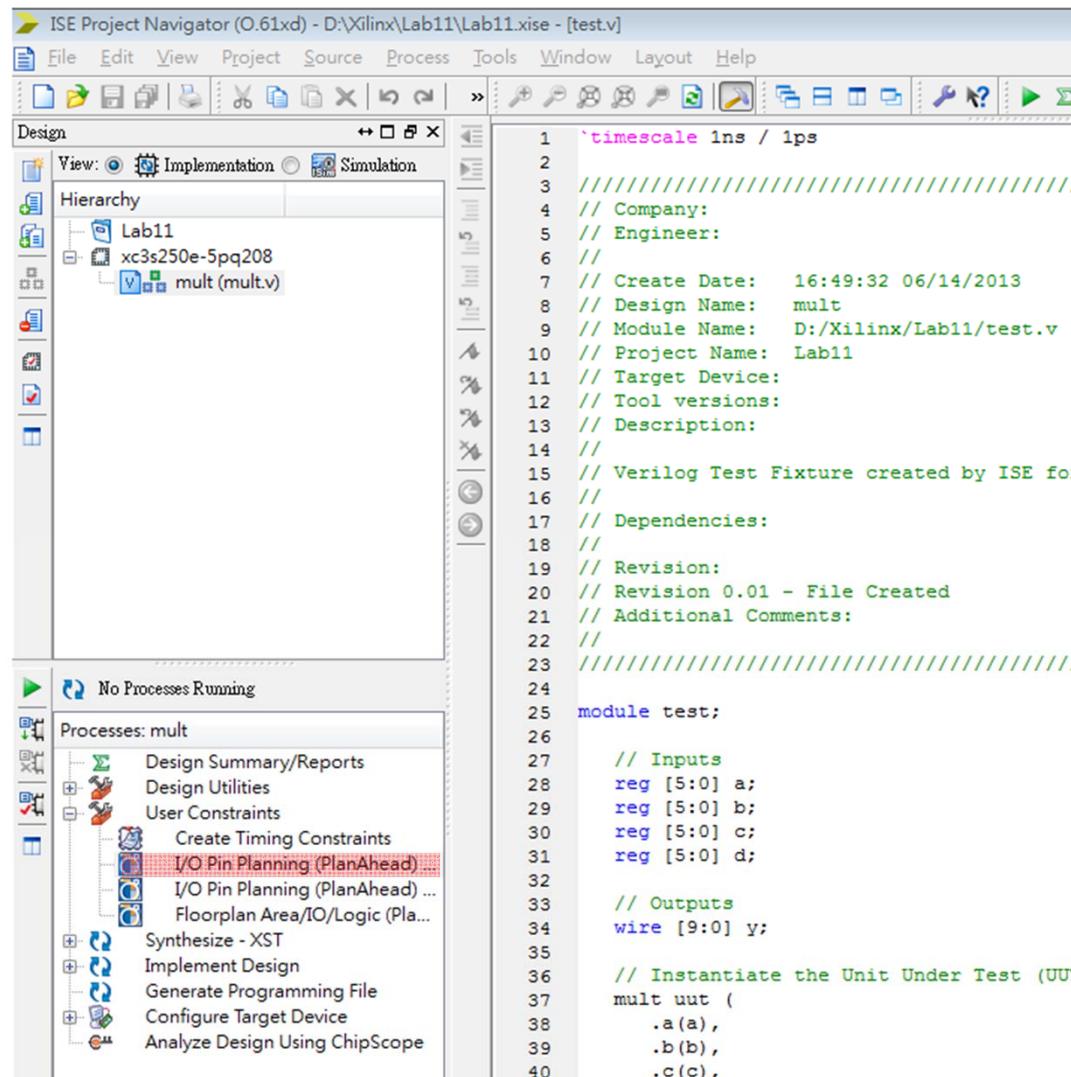
Pin List

Basys2 Spartan-3E pin definitions												
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
C12	JD1	P11	SW0	N14	CC	B2	JA1	P8	MODE0	M7	GND	
A13	JD2	M2	USB-DB1	N13	DP	C2	USB-WRITE	N7	MODE1	P5	GND	
A12	NC	N2	USB-DB0	M13	AN2	C3	PS2D	N6	MODE2	P10	GND	
B12	NC	M9	NC	M12	CG	D1	NC	N12	CCLK	P14	GND	
B11	NC	N9		L14	CA	D2	USB-WAIT	P13	DONE	A6	VDDO-3	
C11	BTN1	M10		L13	CF	L2	USB-DB4	A1	PROG	B10	VDDO-3	
C6	JB1	N10		F13	RED2	L1	USB-DB3	N8	DIN	E13	VDDO-3	
B6	JB2	M11	LD1	F14	GRN0	M1	USB-DB2	N1	INIT	M14	VDDO-3	
C5	JB3	N11	CD	D12	JD4	L3	SW1	P1	NC	P3	VDDO-3	
B5	JA4	P12	CE	D13	RED1	E2	SW6	B3	GND	M8	VDDO-3	
C4	NC	N3	SW7	C13	JD3	F3	SW5	A4		E1	VDDO-3	
B4	SW3	M6	UCLK	C14	RED0	F2	USB-ASTB	A8		J2	VDDO-3	
A3	JA2	P6	LD3	G12	BTN0	F1	USB-DSTB	C1		A5	VDDO-2	
A10	JC3	P7	LD2	K14	AN2	G1	LD7	C7	GND	E12	VDDO-2	
C9	JC4	M4	BTN2	J12	AN1	G3	SW4	C10		K1	VDDO-2	
B9	JC2	N4	LD5	J13	BLU2	H1	USB-DB6	E3		P9	VDDO-2	
A9	JC1	M5	LD0	J14	HSYNC	H2	USB-DB5	E14		A11	VDDO-1	
B8	MCLK	N5	LD4	H13	BLU1	H3	USB-DB7	G2	GND	D3	VDDO-1	
C8	RCCLK	G14	GRN2	H12	CB	B14	TMS	H14		D14	VDDO-1	
A7	BTN3	G13	GRN1	J3	JA3	B13	TCK-FPGA	J1		K2	VDDO-1	
B7	JB4	F12	AN0	K3	SW2	A2	TDO-USB	K12		L12	VDDO-1	
P4	LD6	K13	VSYNC	B1	PS2C	A14	TDO-S3	M3	GND	P2	VDDO-1	

Define Input/Output Pins



User Constraint File (UCF)

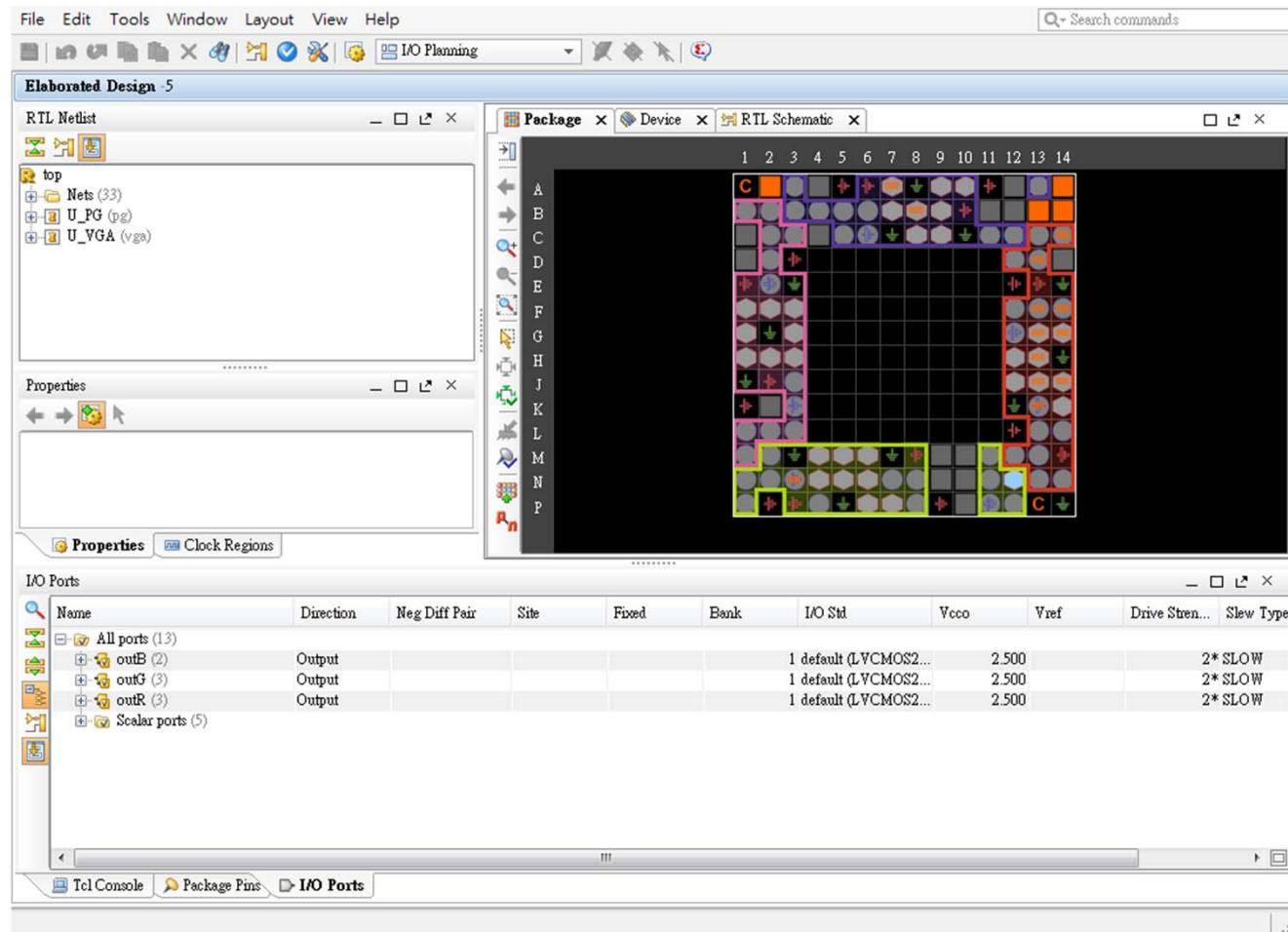


The screenshot shows the ISE Project Navigator interface with the following details:

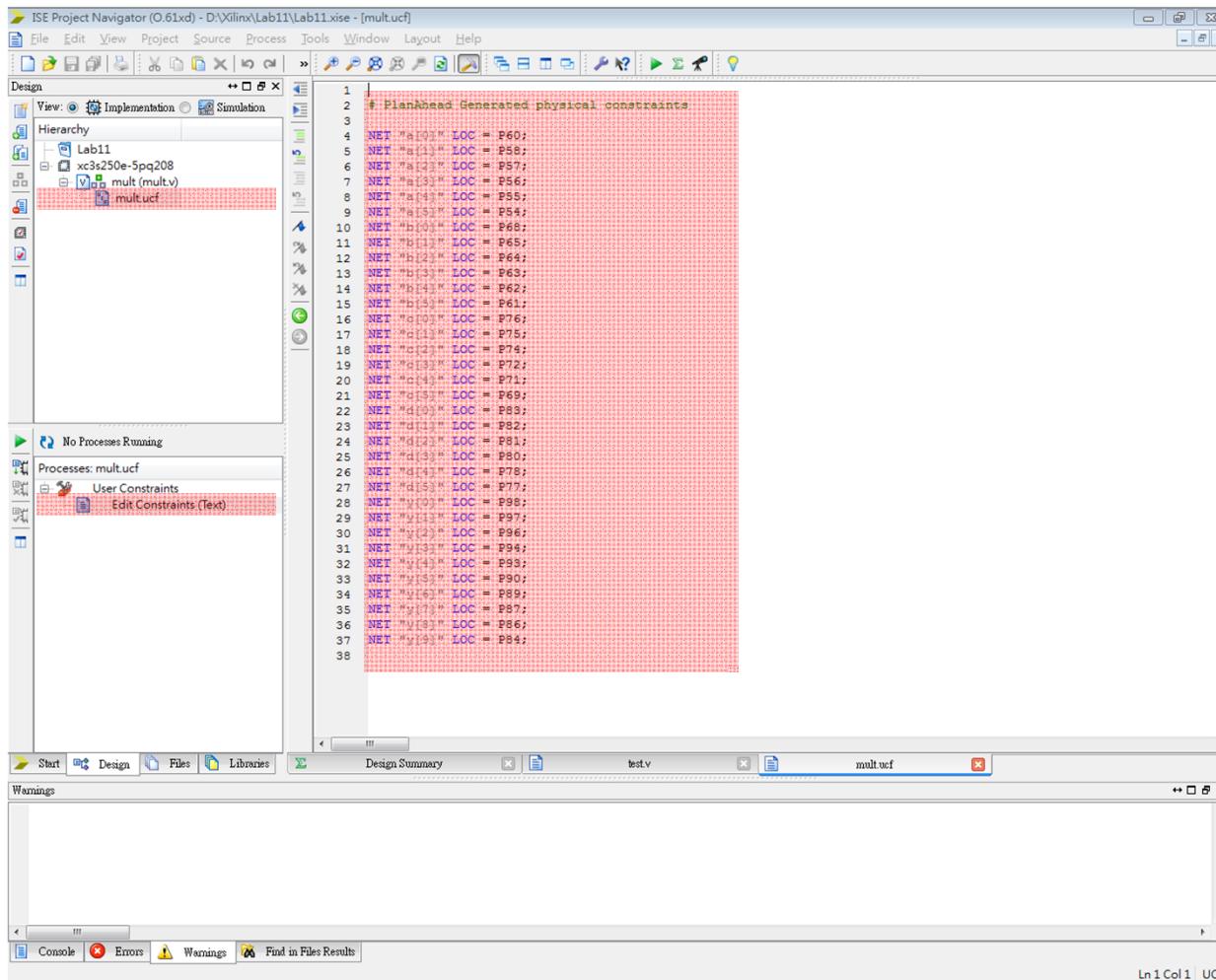
- Project Hierarchy:** Lab11 > xc3s250e-5pq208 > mult (mult.v)
- Processes:** mult
- Selected Process:** Create Timing Constraints
- Code Editor Content:** A Verilog test fixture with comments and module declarations.

```
1 `timescale 1ns / 1ps
2
3 ///////////////////////////////////////////////////////////////////
4 // Company:
5 // Engineer:
6 //
7 // Create Date: 16:49:32 06/14/2013
8 // Design Name: mult
9 // Module Name: D:/Xilinx/Lab11/test.v
10 // Project Name: Lab11
11 // Target Device:
12 // Tool versions:
13 // Description:
14 //
15 // Verilog Test Fixture created by ISE for:
16 //
17 // Dependencies:
18 //
19 // Revision:
20 // Revision 0.01 - File Created
21 // Additional Comments:
22 //
23 ///////////////////////////////////////////////////////////////////
24
25 module test;
26
27     // Inputs
28     reg [5:0] a;
29     reg [5:0] b;
30     reg [5:0] c;
31     reg [5:0] d;
32
33     // Outputs
34     wire [9:0] y;
35
36     // Instantiate the Unit Under Test (UUT)
37     mult uut (
38         .a(a),
39         .b(b),
40         .c(c),
```

User Constraint File (UCF)



User Constrain File (UCF)



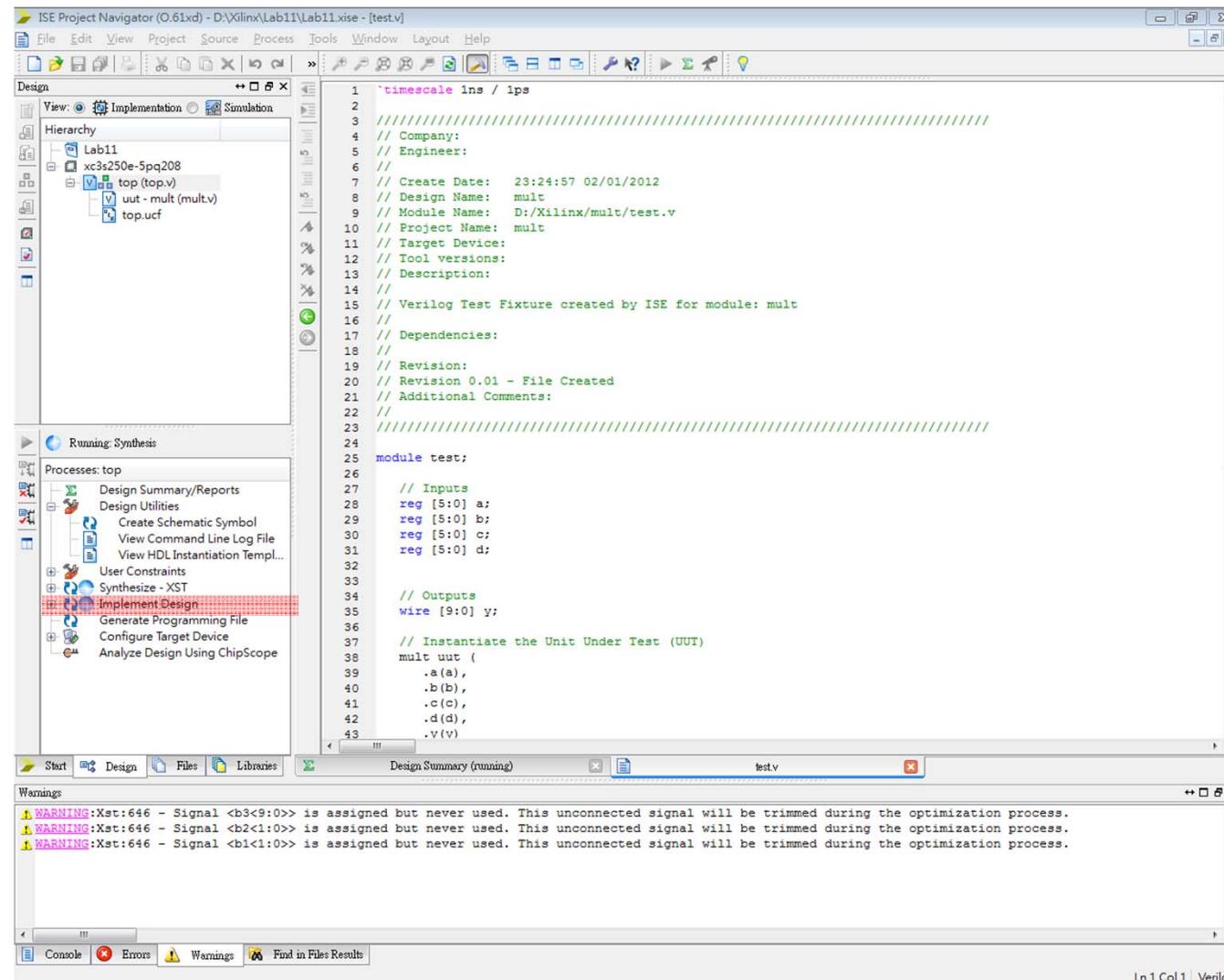
User Constrain File (UCF)

```
1 ## Pin assignment for LEDs
2 NET "dout<3>" LOC = "P6" ; # Bank = 2, Signal name = LD3
3 NET "dout<2>" LOC = "P7" ; # Bank = 3, Signal name = LD2
4 NET "dout<1>" LOC = "M11" ; # Bank = 2, Signal name = LD1
5 NET "dout<0>" LOC = "M5" ; # Bank = 2, Signal name = LD0
6 #
7 ## Pin assignment for SWs
8 NET "b<3>" LOC = "N3"; # Bank = 2, Signal name = SW7
9 NET "b<2>" LOC = "E2"; # Bank = 3, Signal name = SW6
10 NET "b<1>" LOC = "F3"; # Bank = 3, Signal name = SW5
11 NET "b<0>" LOC = "G3"; # Bank = 3, Signal name = SW4
12 NET "a<3>" LOC = "B4"; # Bank = 3, Signal name = SW3
13 NET "a<2>" LOC = "K3"; # Bank = 3, Signal name = SW2
14 NET "a<1>" LOC = "L3"; # Bank = 3, Signal name = SW1
15 NET "a<0>" LOC = "P11"; # Bank = 2, Signal name = SW0
16
```

Xilinx FPGA Design Flow

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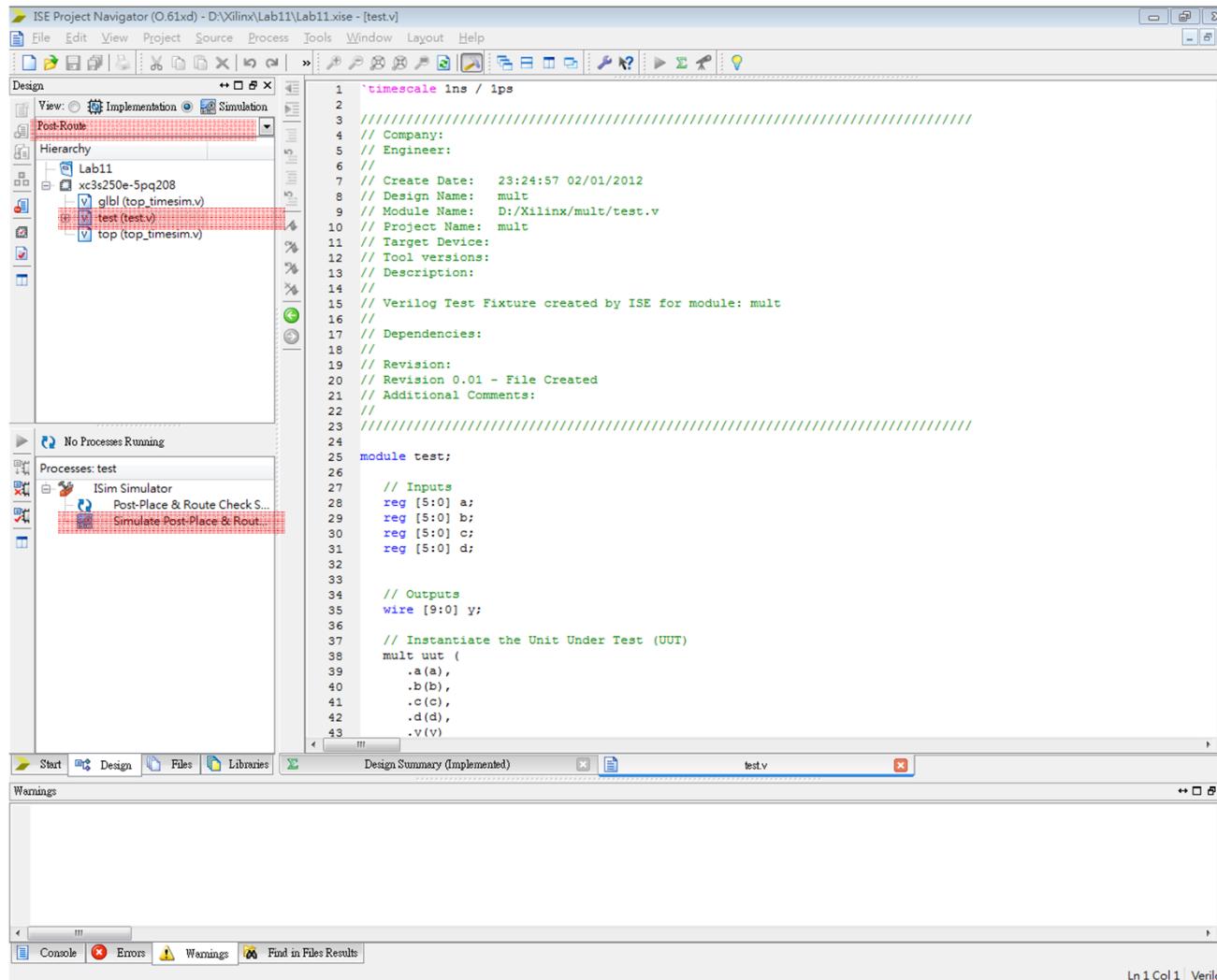
Implement Design



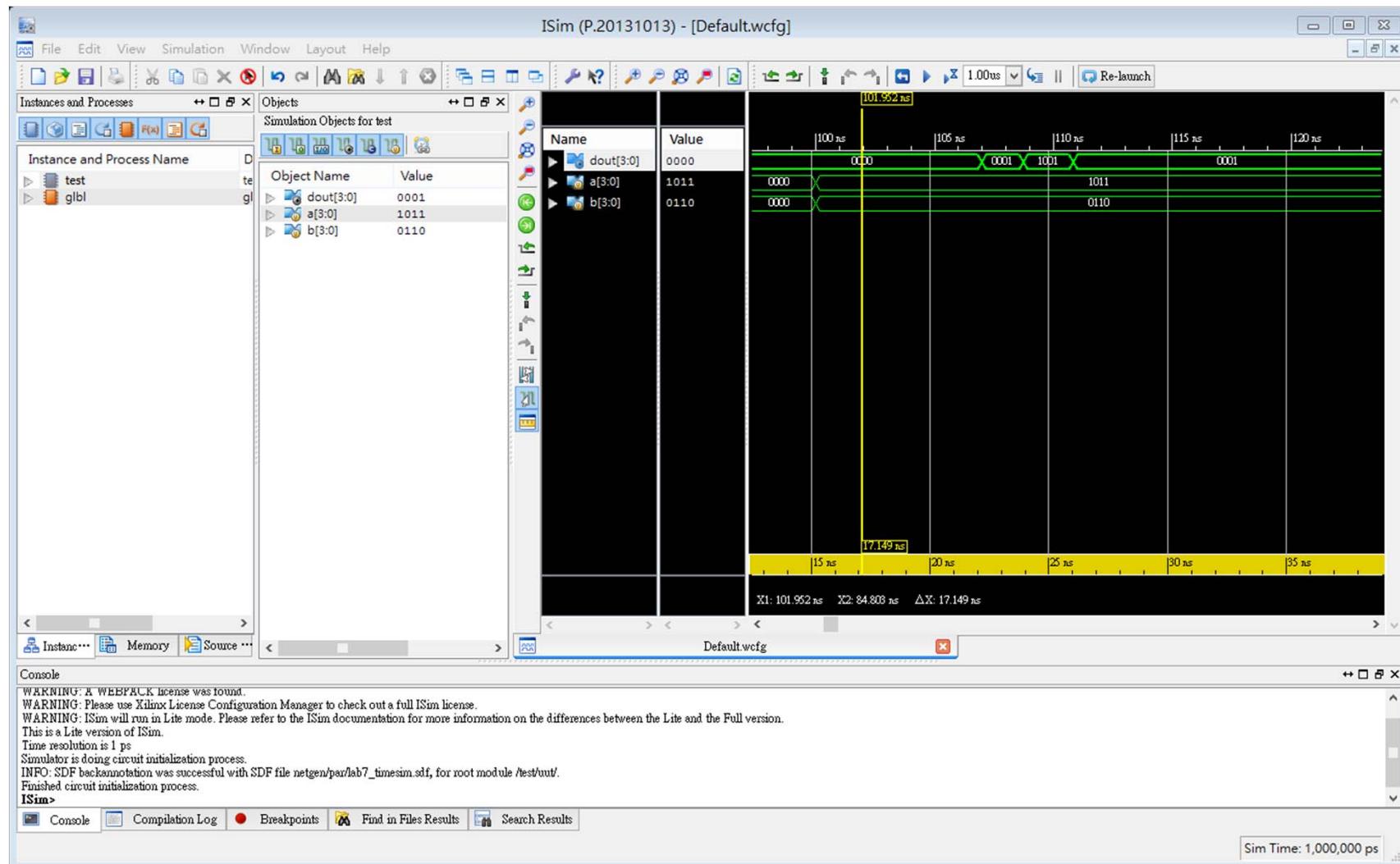
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Post-simulation

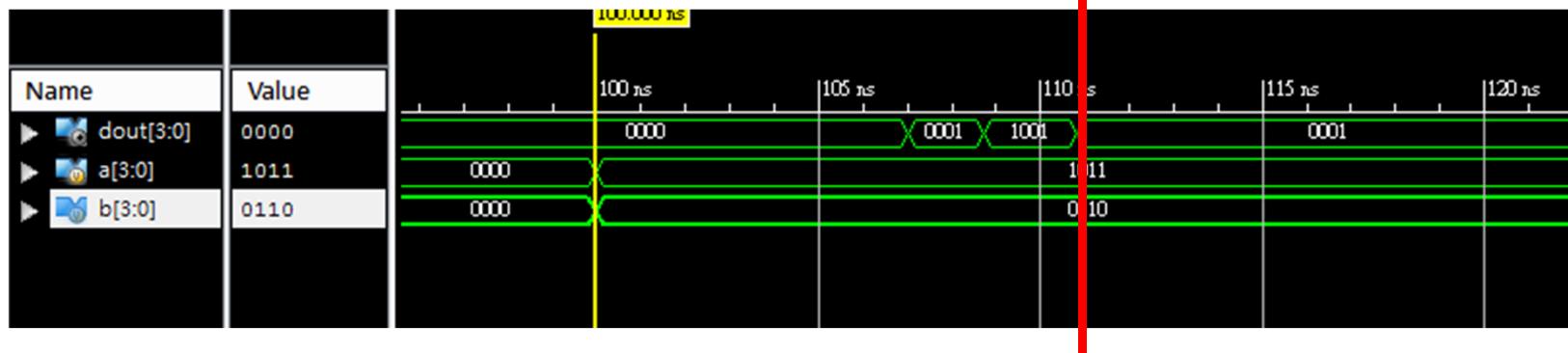


Post-simulation Wave Form

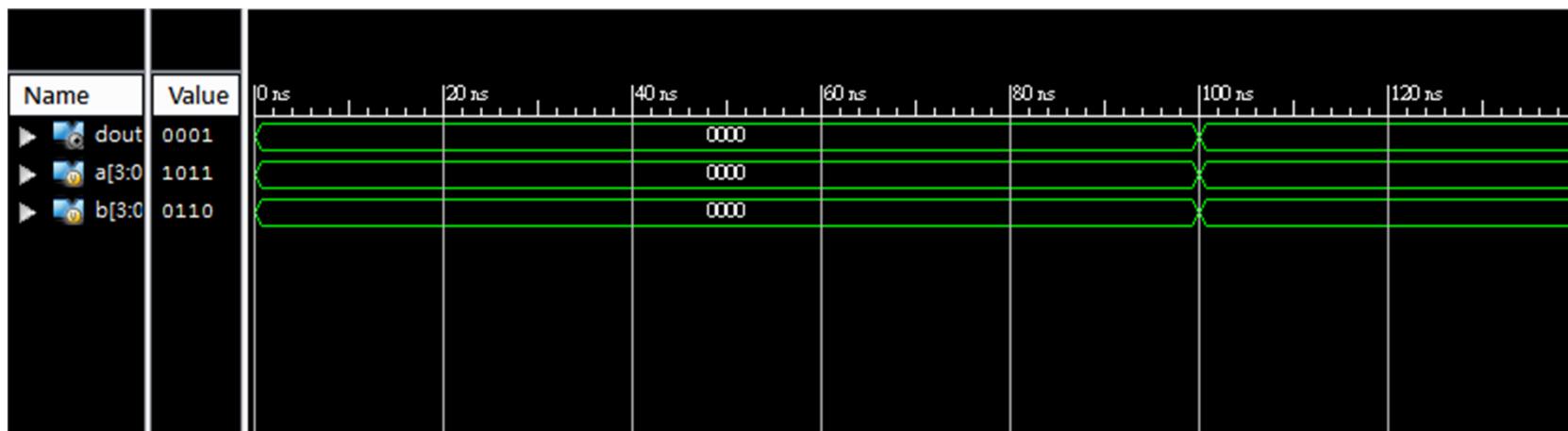


Post-simulation

- Post-sim



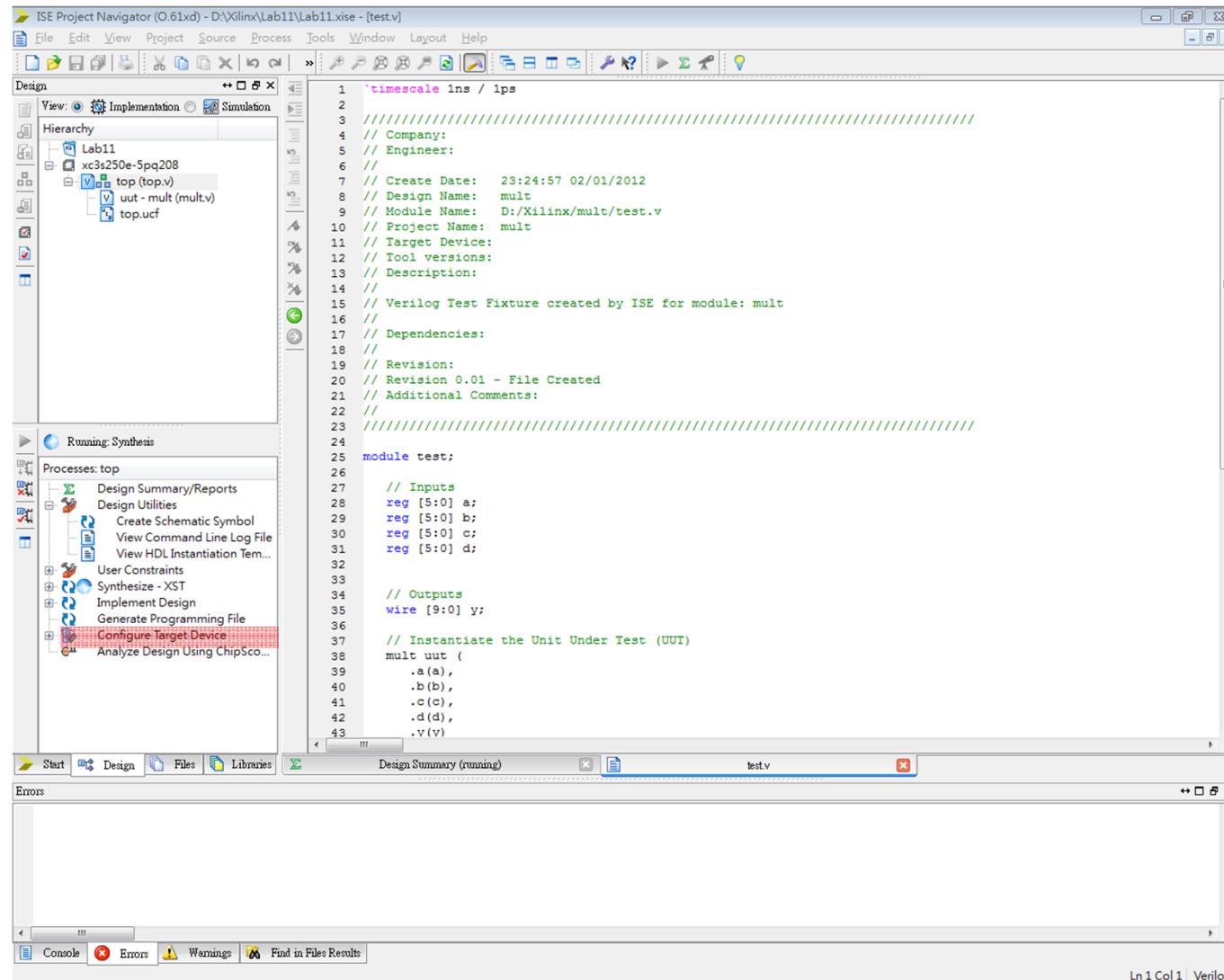
- Pre-sim



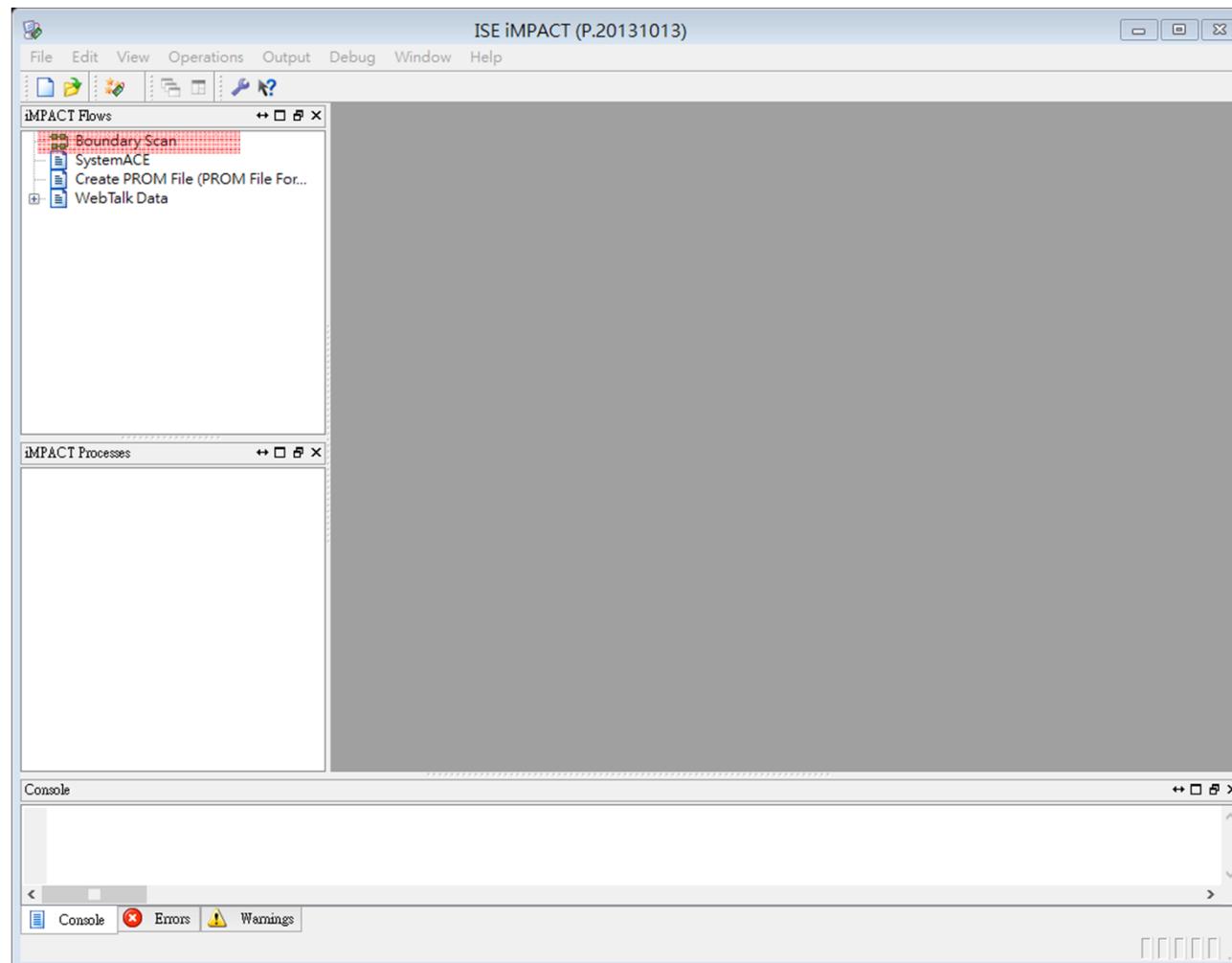
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Generate and Download Bit-stream



Download Bit-Stream



Power On

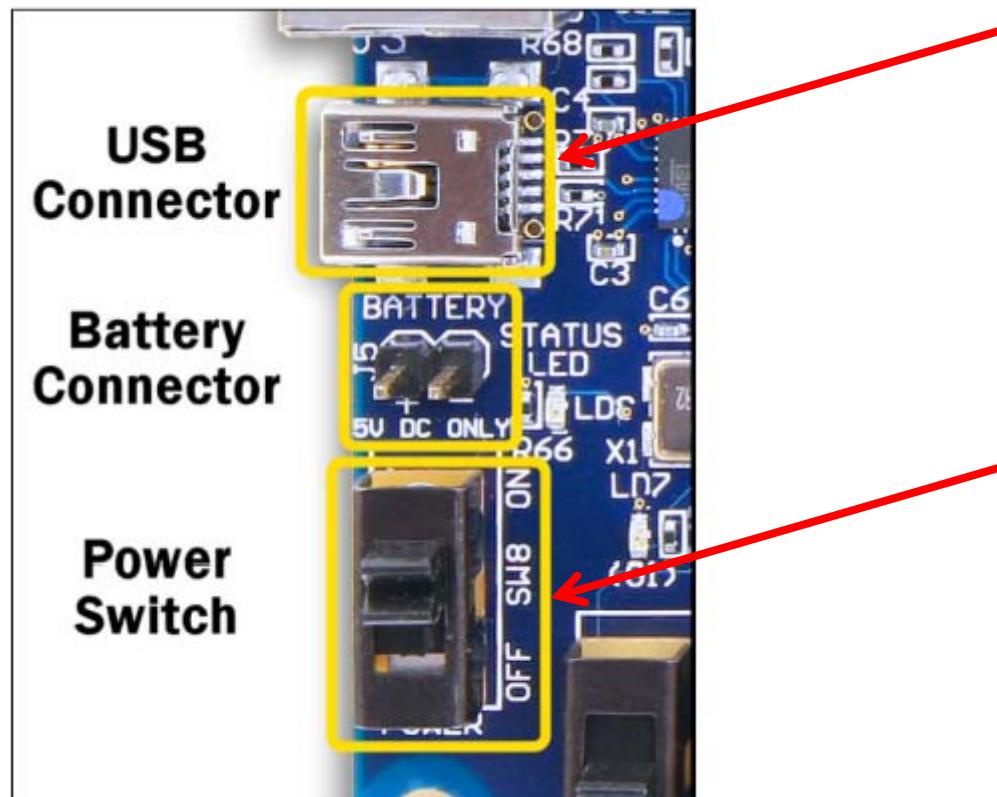
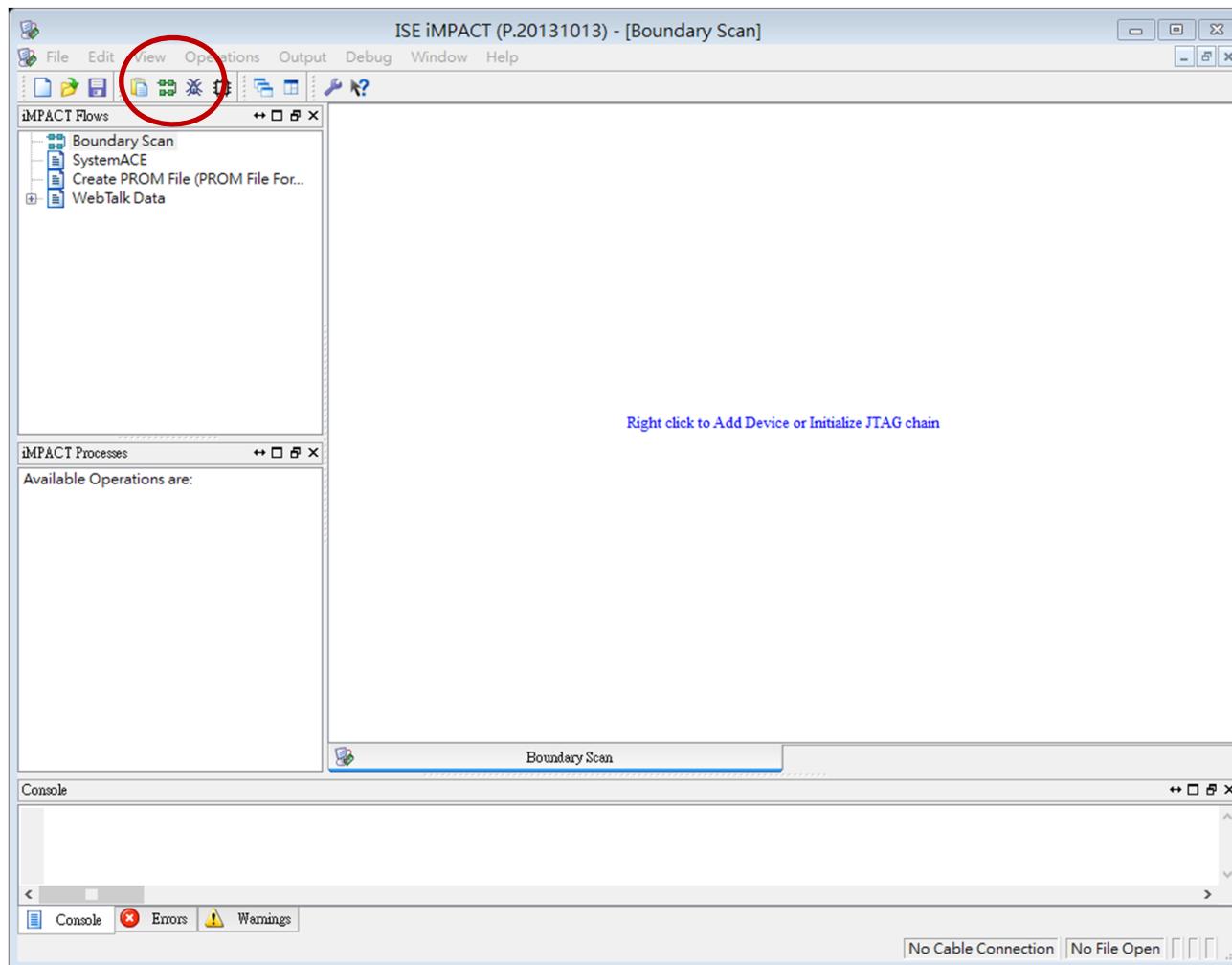
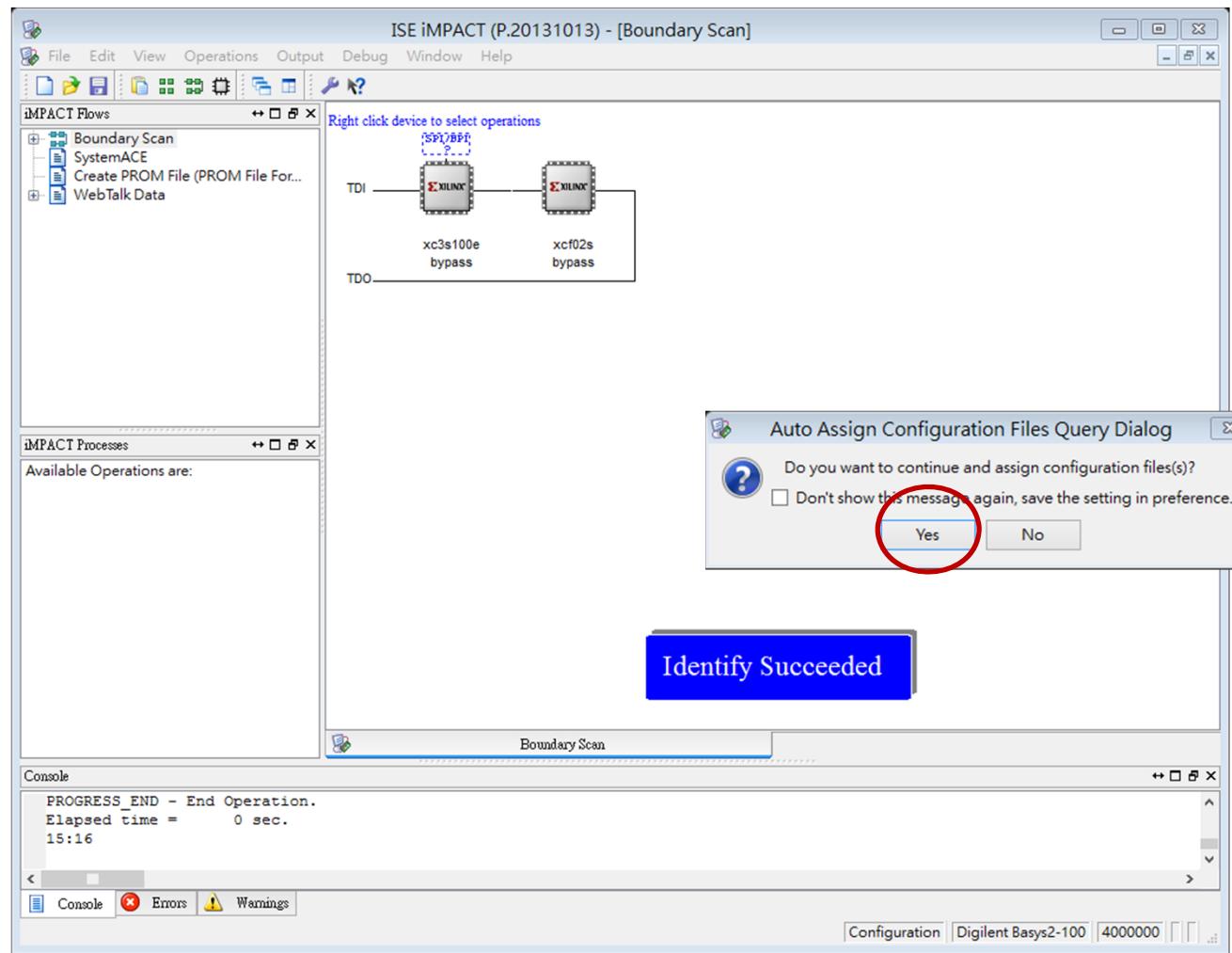
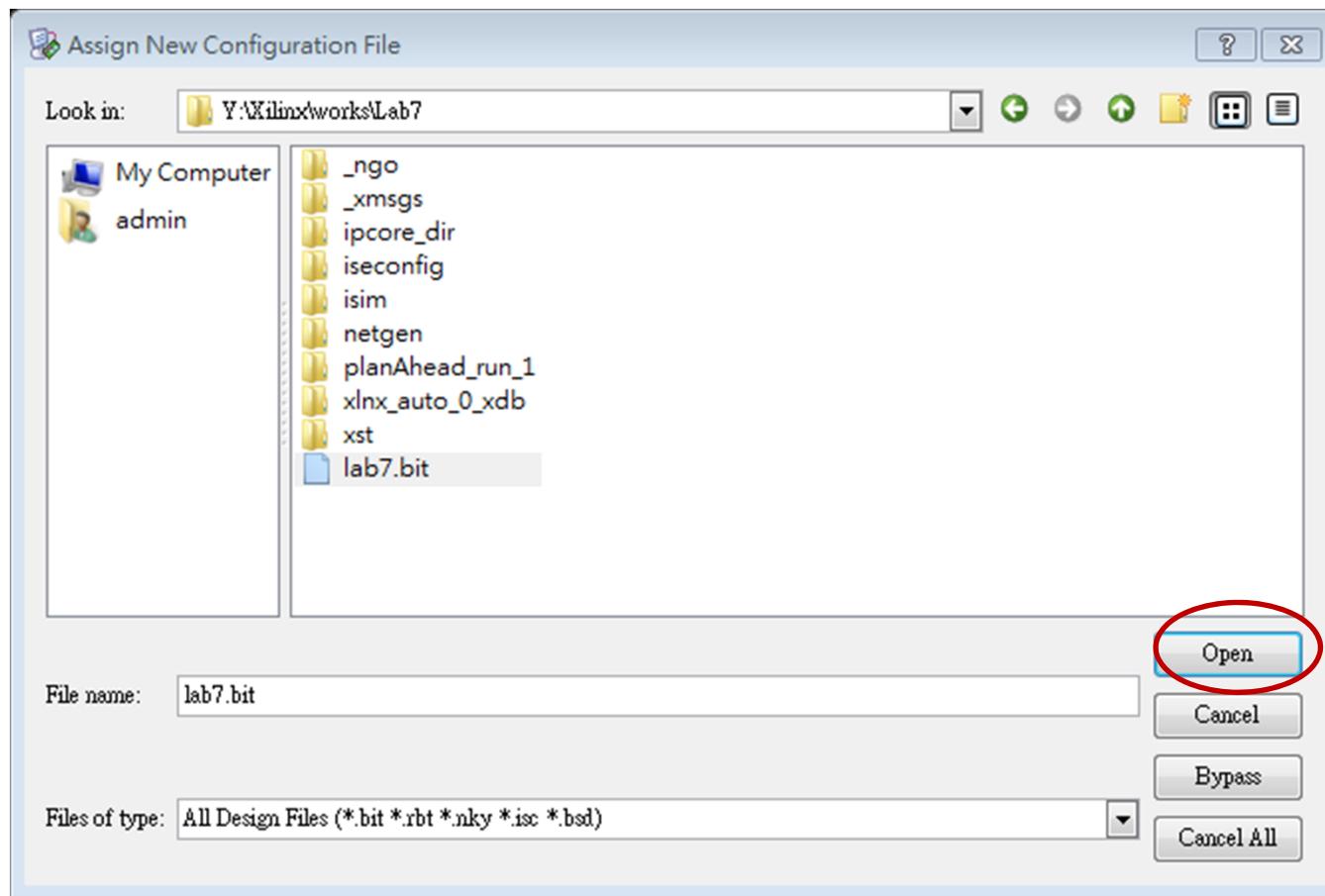


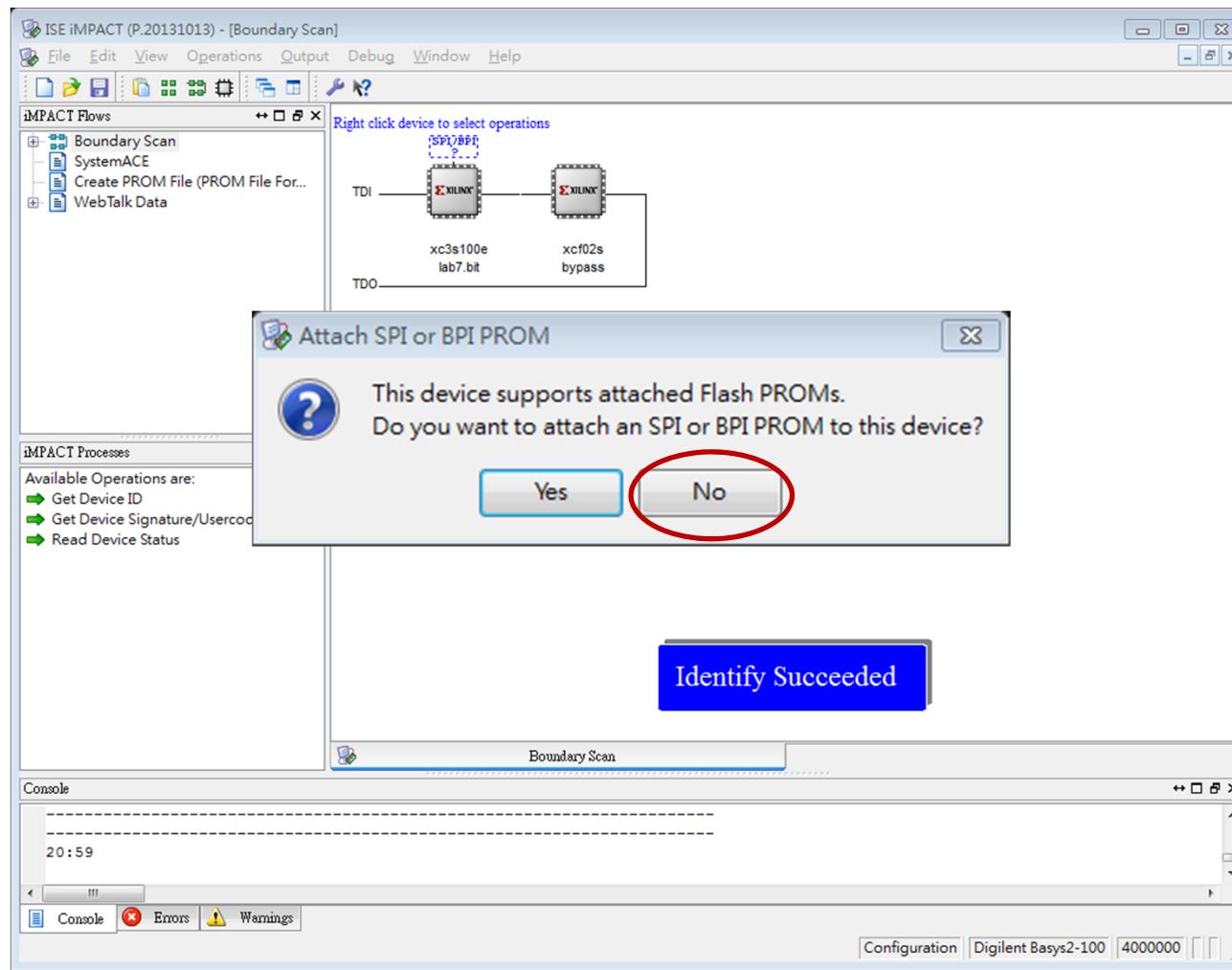
Figure 2. Basys2 power circuits

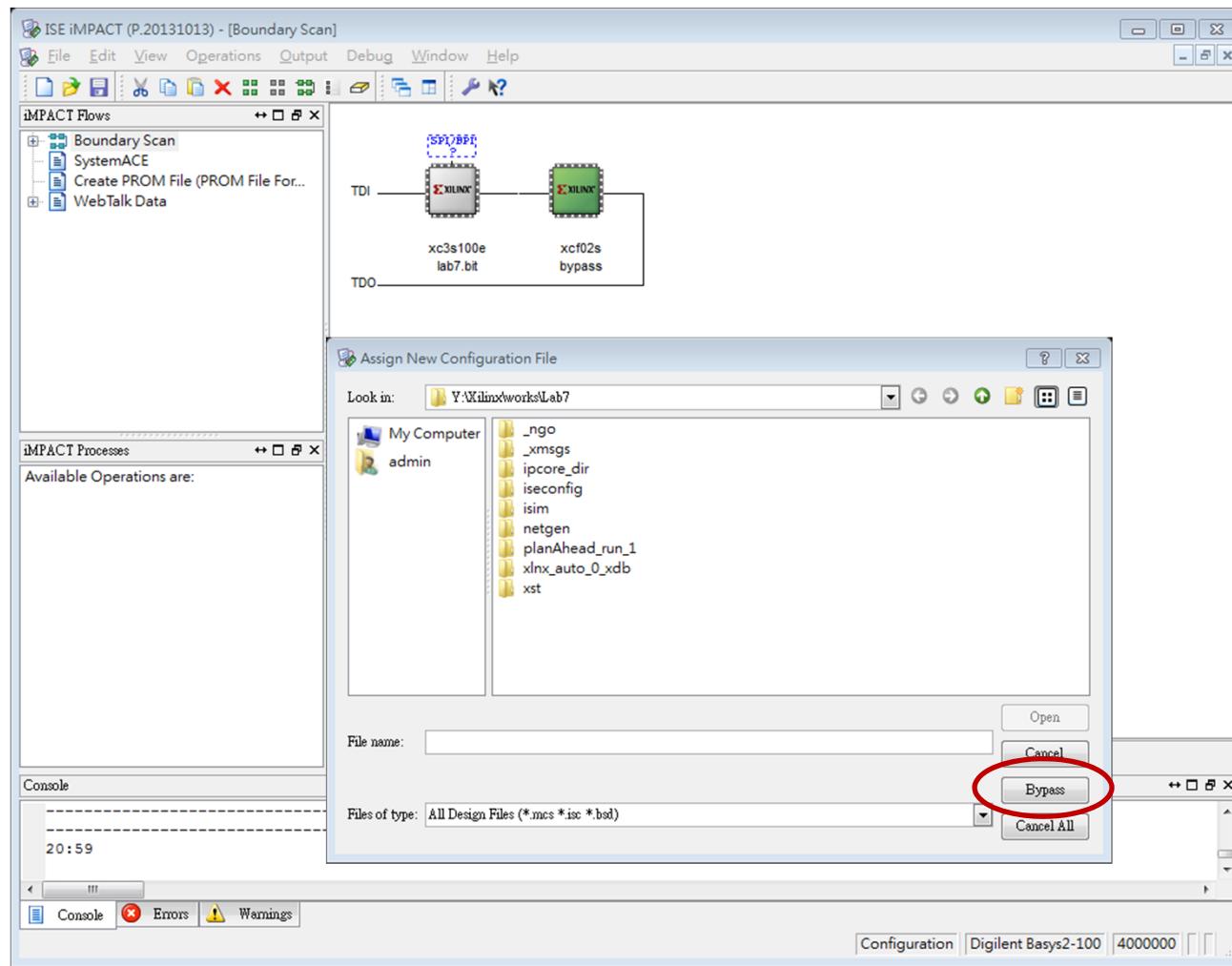
Download Bit-Stream

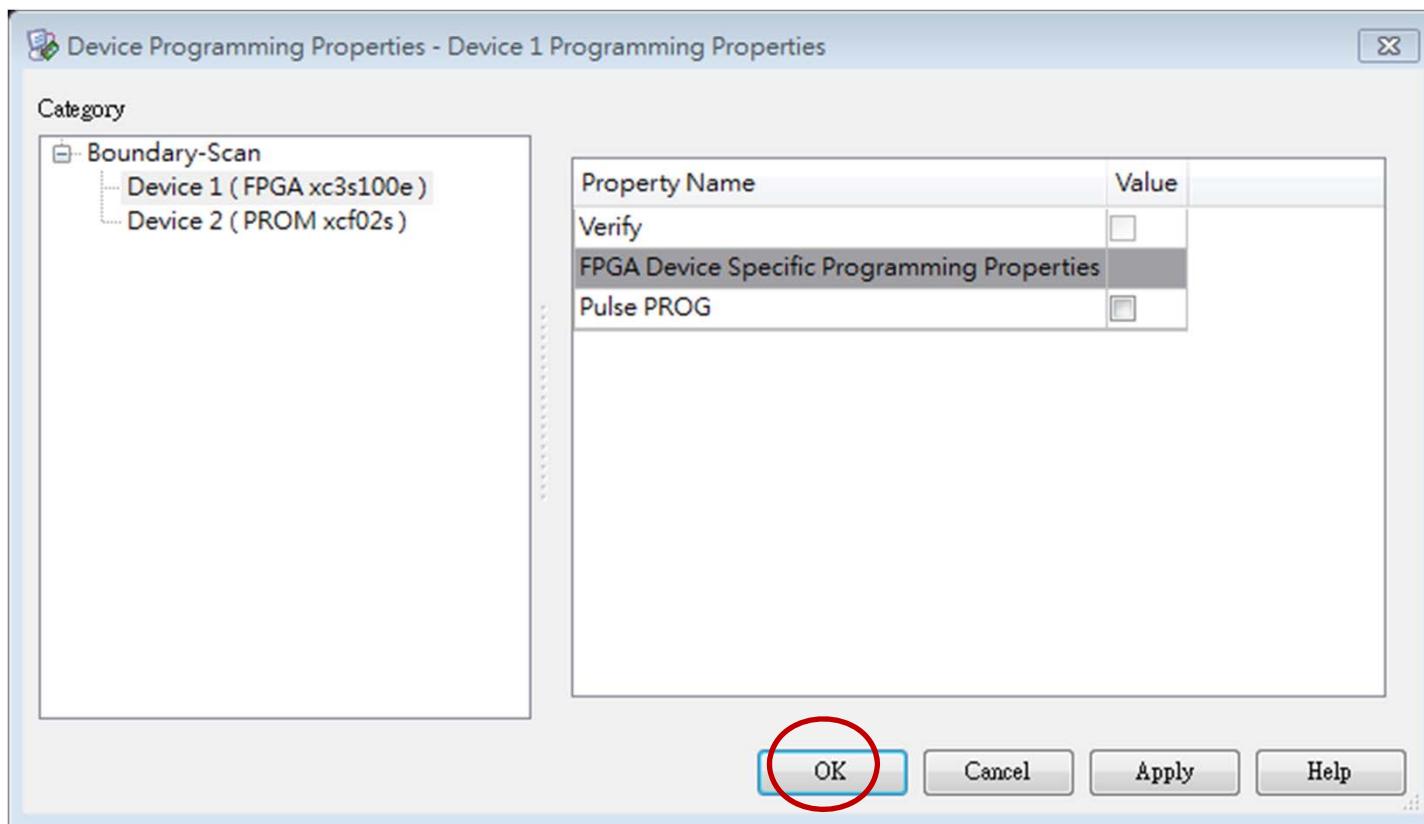


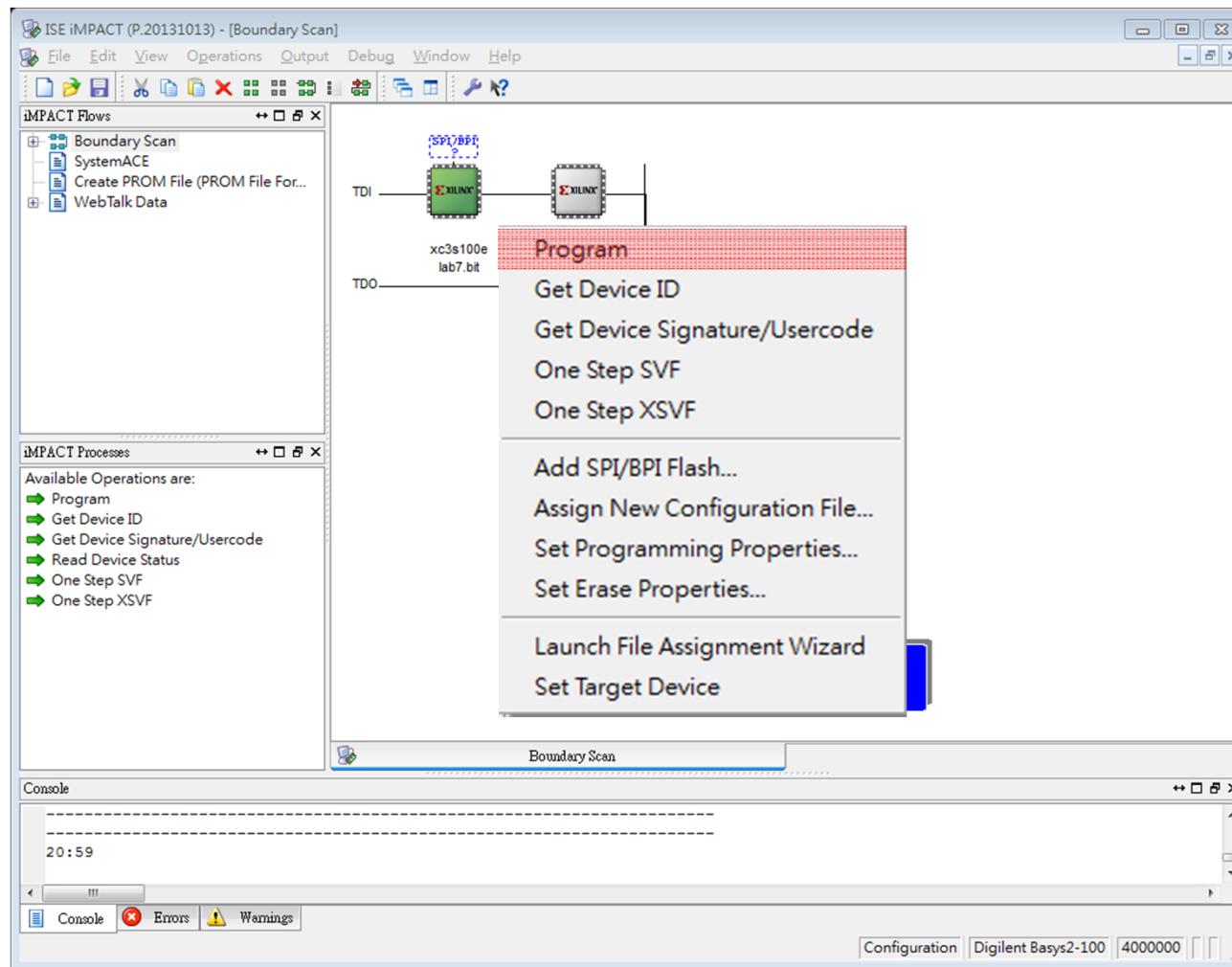




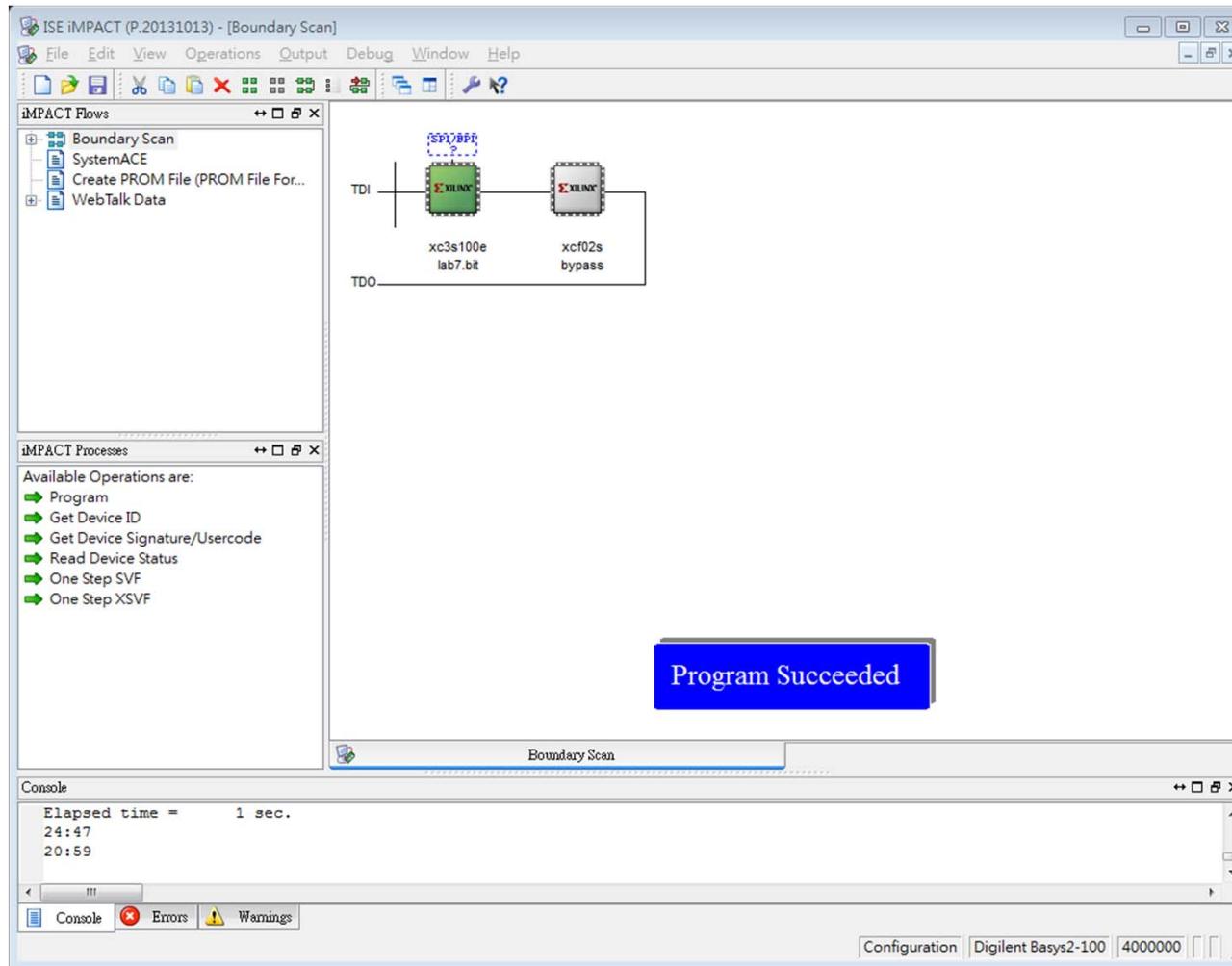






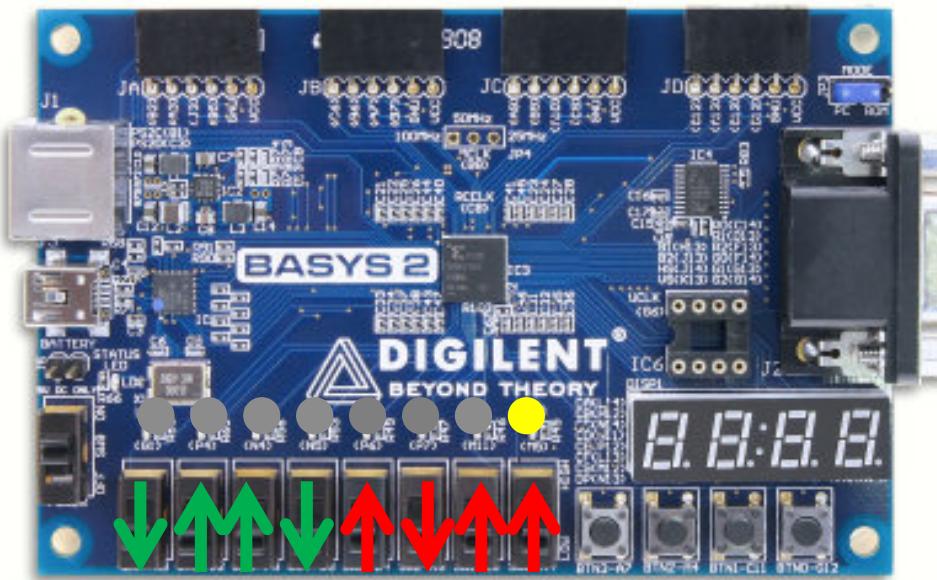


Download Bit-stream



Physical Verification

- **Inputs**
 - $a = 1011$
 - $b = 0110$
- **Output**
 - $dout = 0001$



Be careful

- 關掉電源再移動或拆解**FPGA**板。
- **FPGA**板附近請淨空，避免電路板短路。
- 請勿開著電移動**FPGA**板。