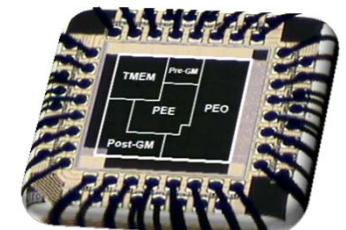


ChipScope Pro Design

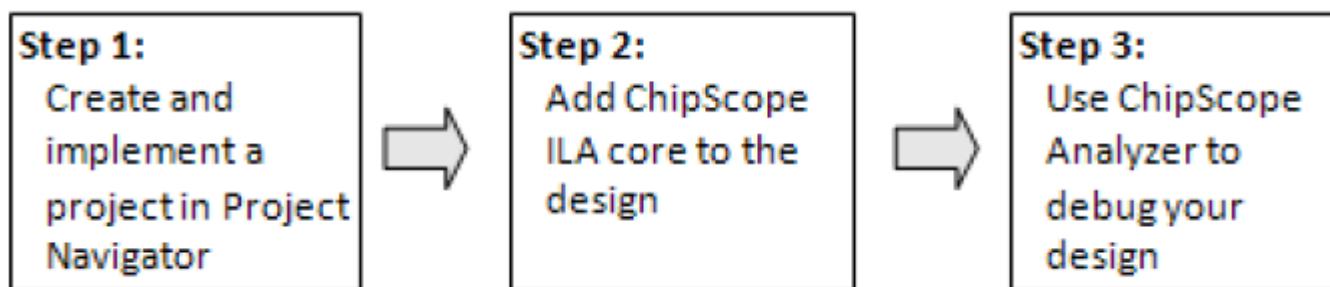
Yuan-Ho Chen

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Chung Yuan Christian University
yhchen@ice.cycu.edu.tw



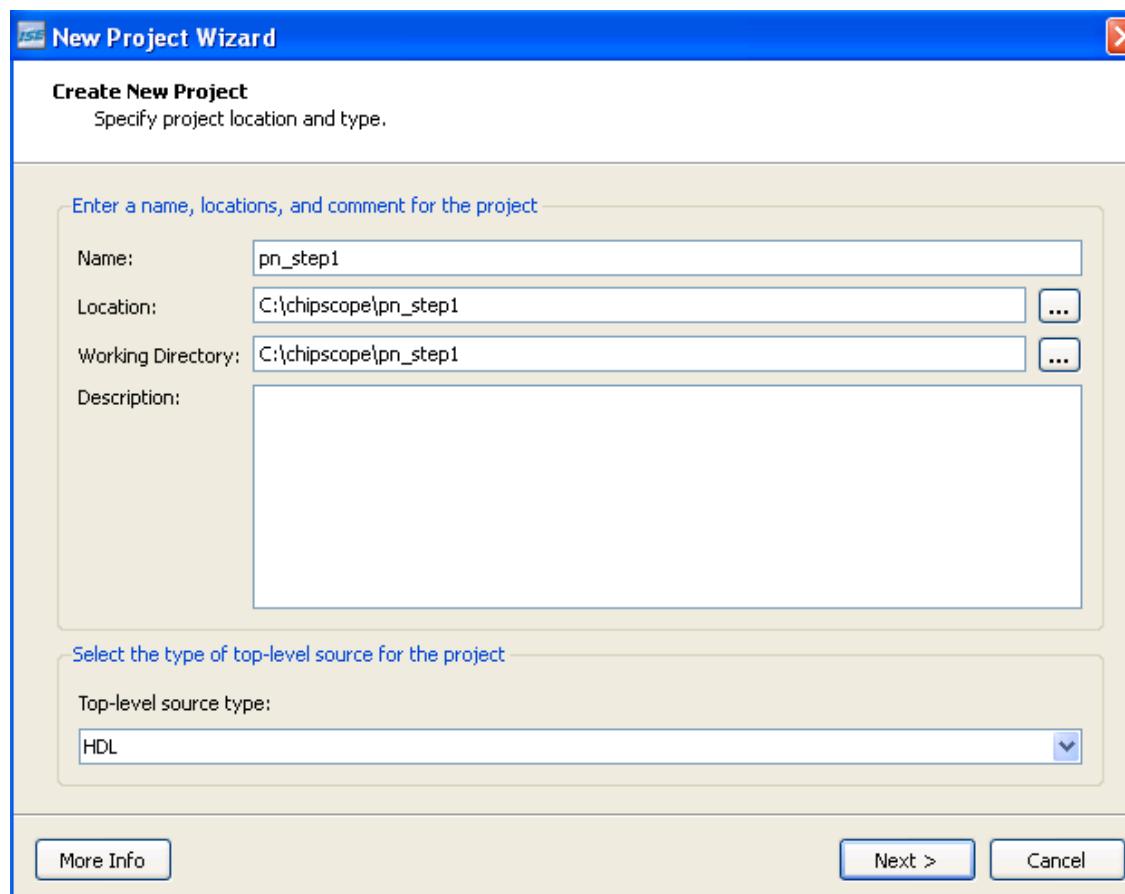
Design Procedure

1. Creating and Implementing a Project in Project Navigator
2. Adding a ChipScope ILA Core to Your Design
3. Debugging Your Design using ChipScope Pro Analyzer



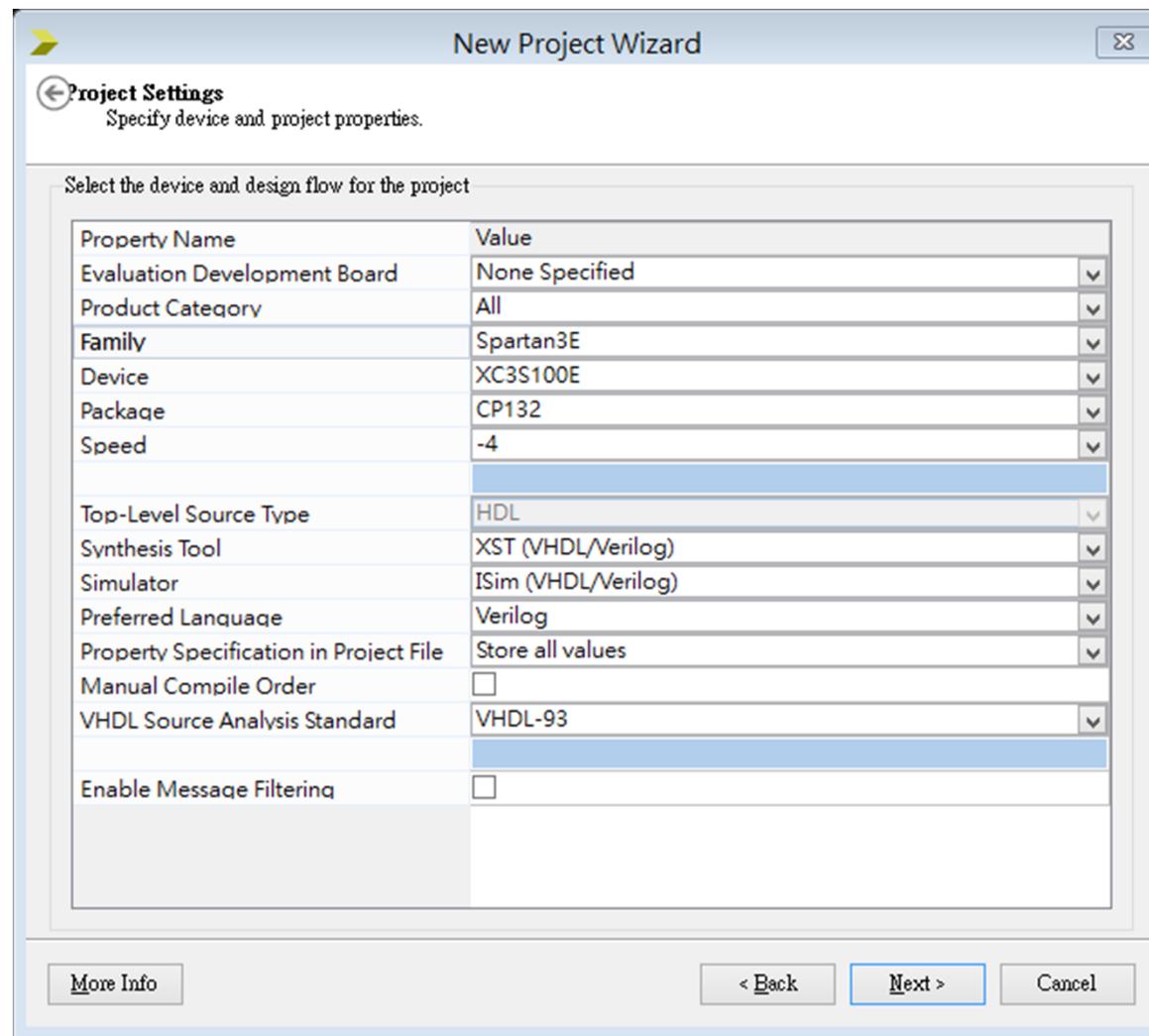
Creating and Implementing a Project in Project Navigator

- Start Project Navigator and select **File > New Project** to create a new project. Provide the name, location, and project type, and then click **Next**



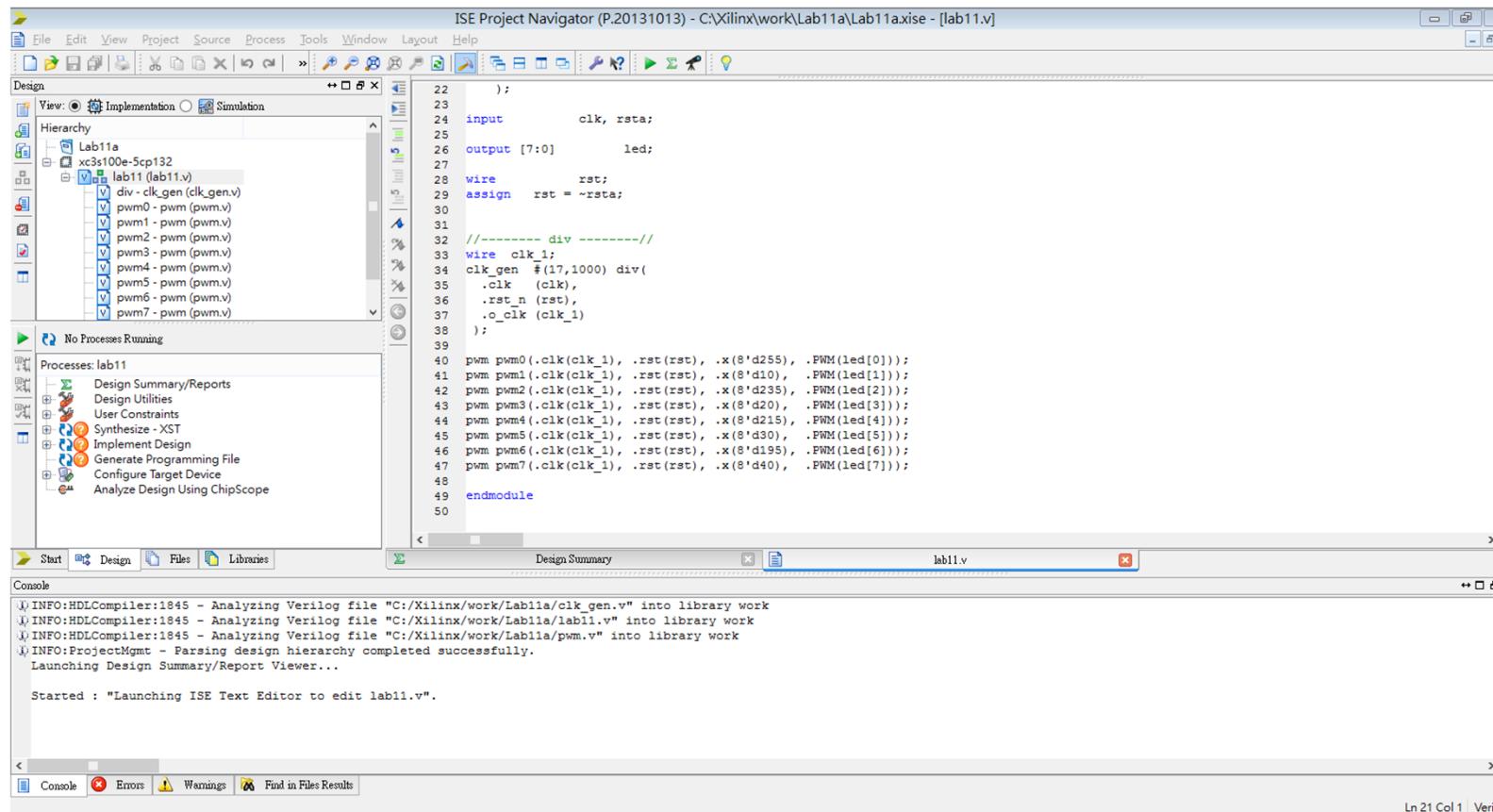
Creating and Implementing a Project in Project Navigator

- Specify device and project properties as shown here, and click **Next**

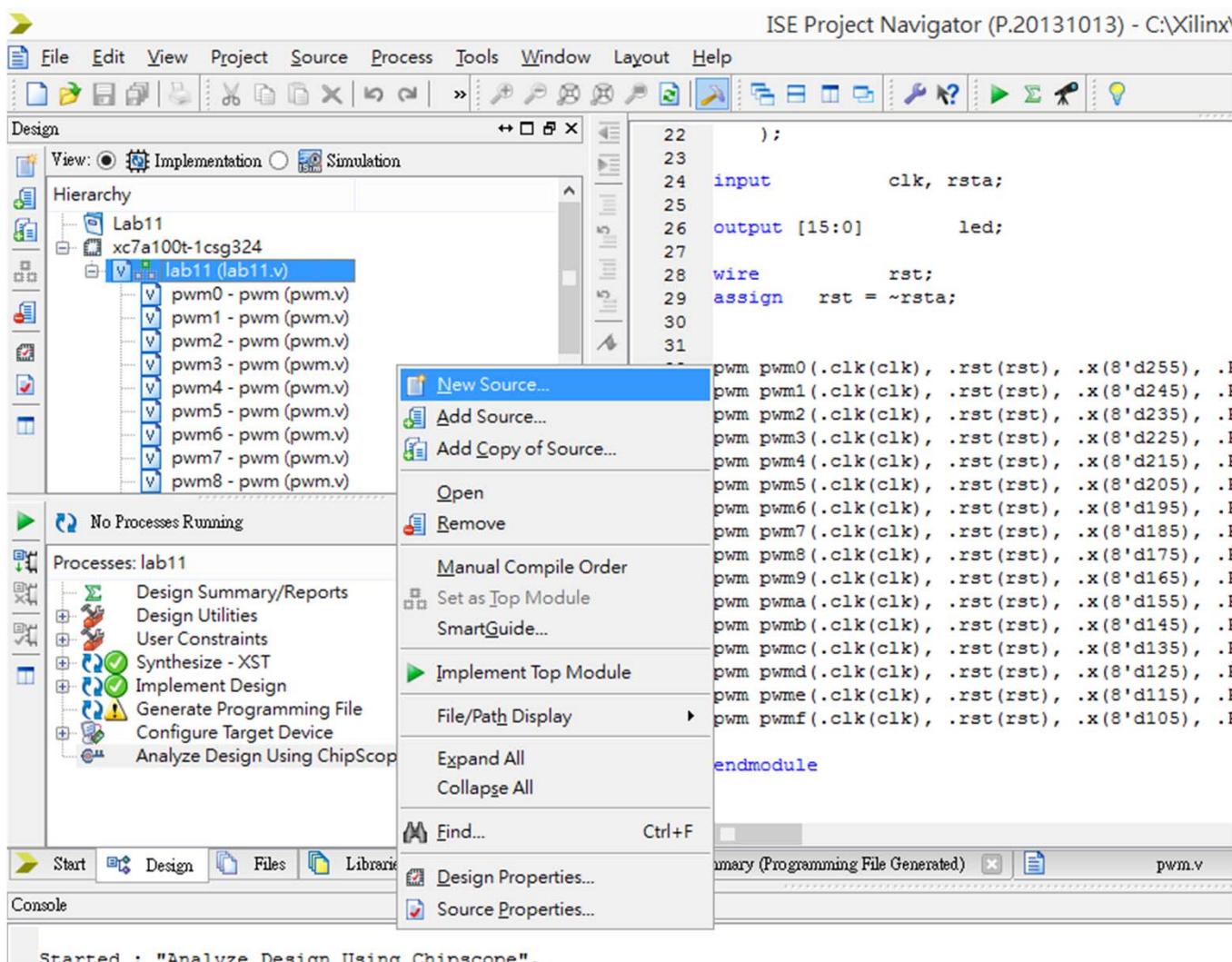


Creating and Implementing a Project in Project Navigator

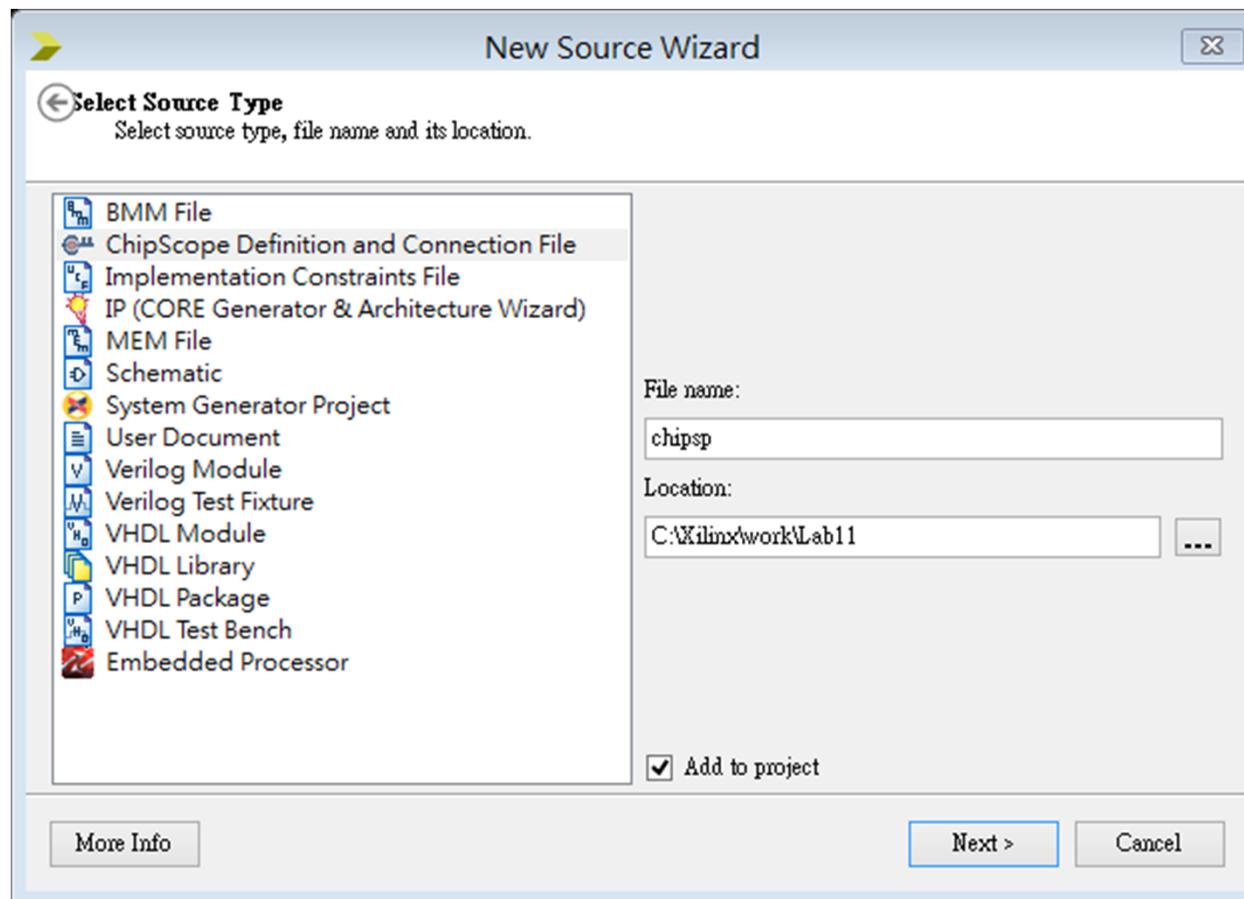
- Complete your design, and run synthesis.



Adding a ChipScope ILA Core to Your Design



Create Files



ISE Project Navigator (P.20131013) - C:\Xilinx\work\Lab11a\Lab11a.xise - [lab11.v]

```

Design View: Implementation Simulation
Hierarchy
lab11 (lab11.v)
  - div - clk_gen(clk_gen.v)
    - pwm0 - pwm(pwm.v)
    - pwm1 - pwm(pwm.v)
    - pwm2 - pwm(pwm.v)
    - pwm3 - pwm(pwm.v)
    - pwm4 - pwm(pwm.v)
    - pwm5 - pwm(pwm.v)
    - pwm6 - pwm(pwm.v)
    - pwm7 - pwm(pwm.v)
  - chipsps.cdc
  - lab11.ucf

No Processes Running
Processes: lab11
  - Design Summary/Reports
  - Design Utilities
  - User Constraints
  - Synthesize - XST
  - Implement Design
  - Generate Programming File
  - Configure Target Device
  - Analyze Design Using ChipScope

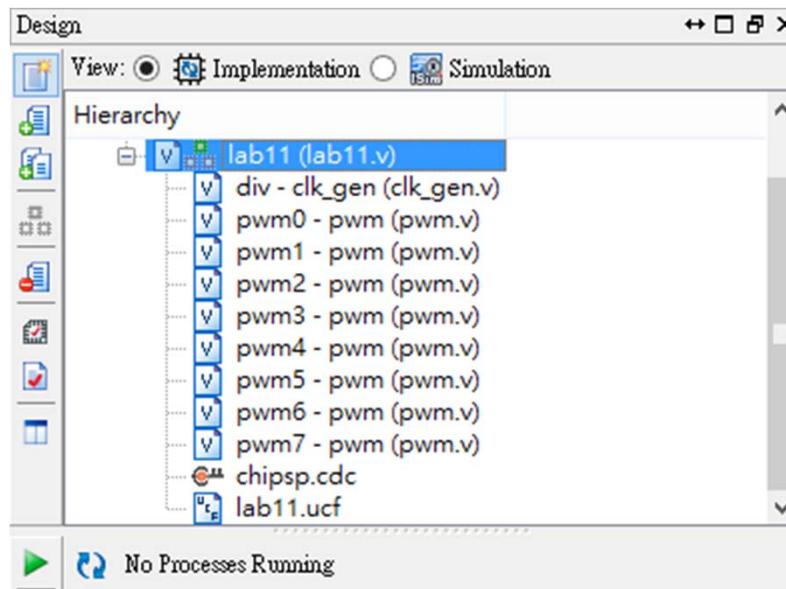
Start Design Files Libraries
Design Summary lab11.v
Console
INFO:HDLCompiler:1845 - Analyzing Verilog file "C:/Xilinx/work/Lab11a/clk_gen.v" into library work
INFO:HDLCompiler:1845 - Analyzing Verilog file "C:/Xilinx/work/Lab11a/lab11.v" into library work
INFO:HDLCompiler:1845 - Analyzing Verilog file "C:/Xilinx/work/Lab11a/pwm.v" into library work
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Launching Design Summary/Report Viewer...
Started : "Launching ISE Text Editor to edit lab11.v".

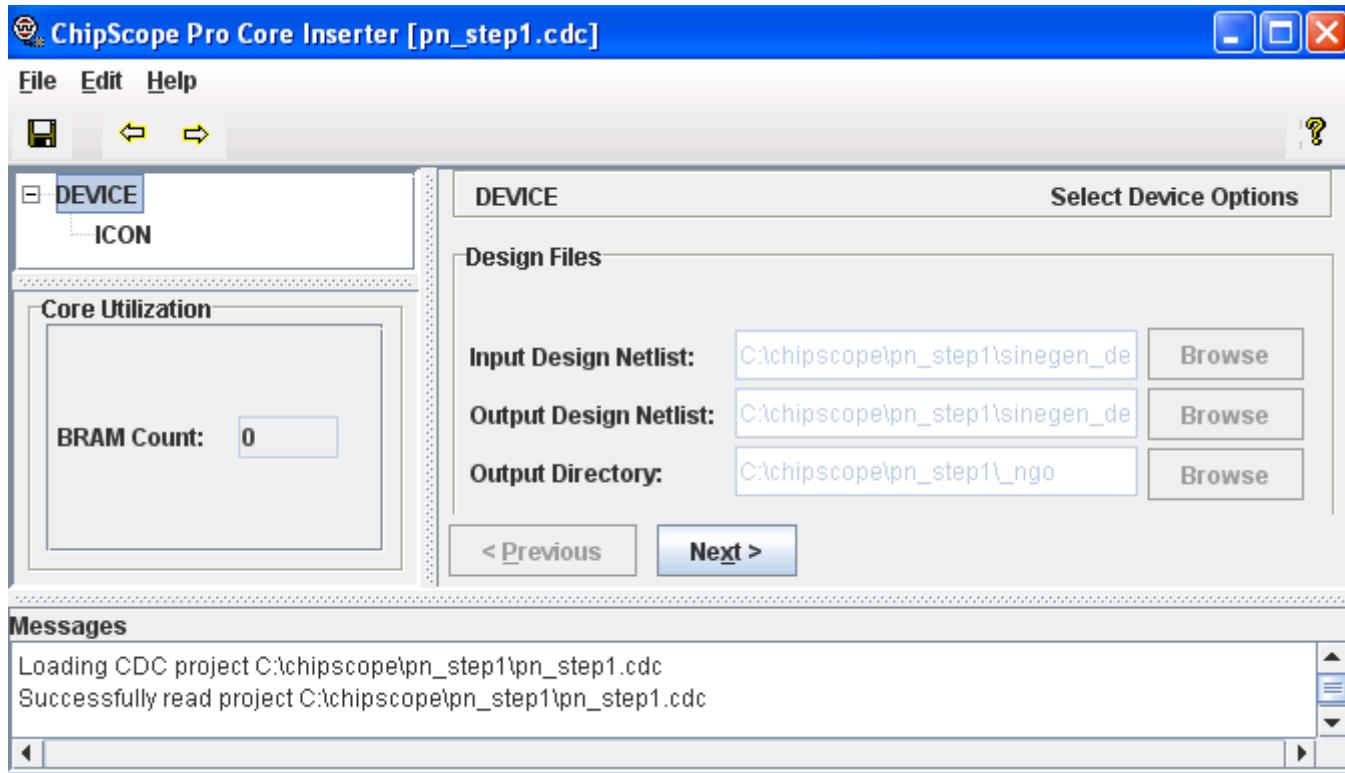
```

Console Errors Warnings Find in Files Results

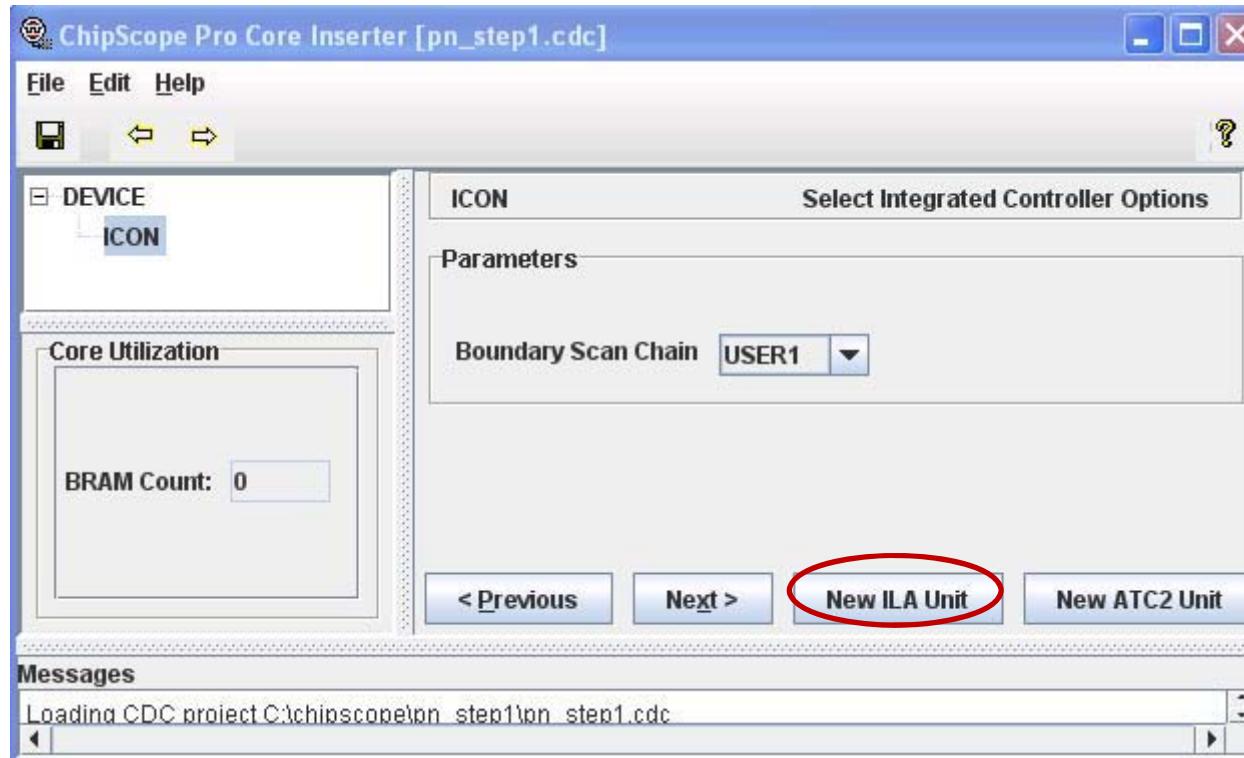
Ln 21 Col 1 Verilog

Double click

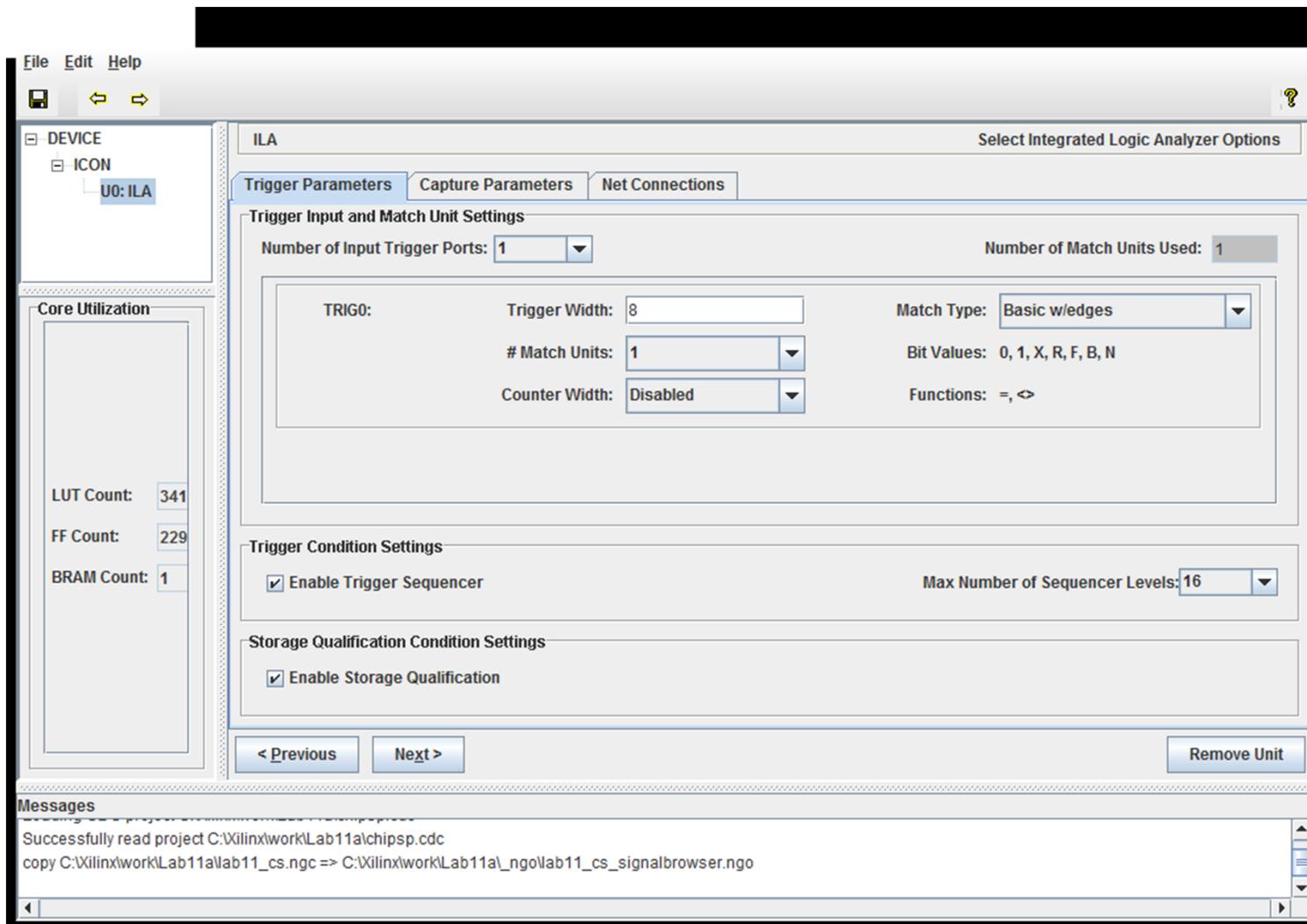




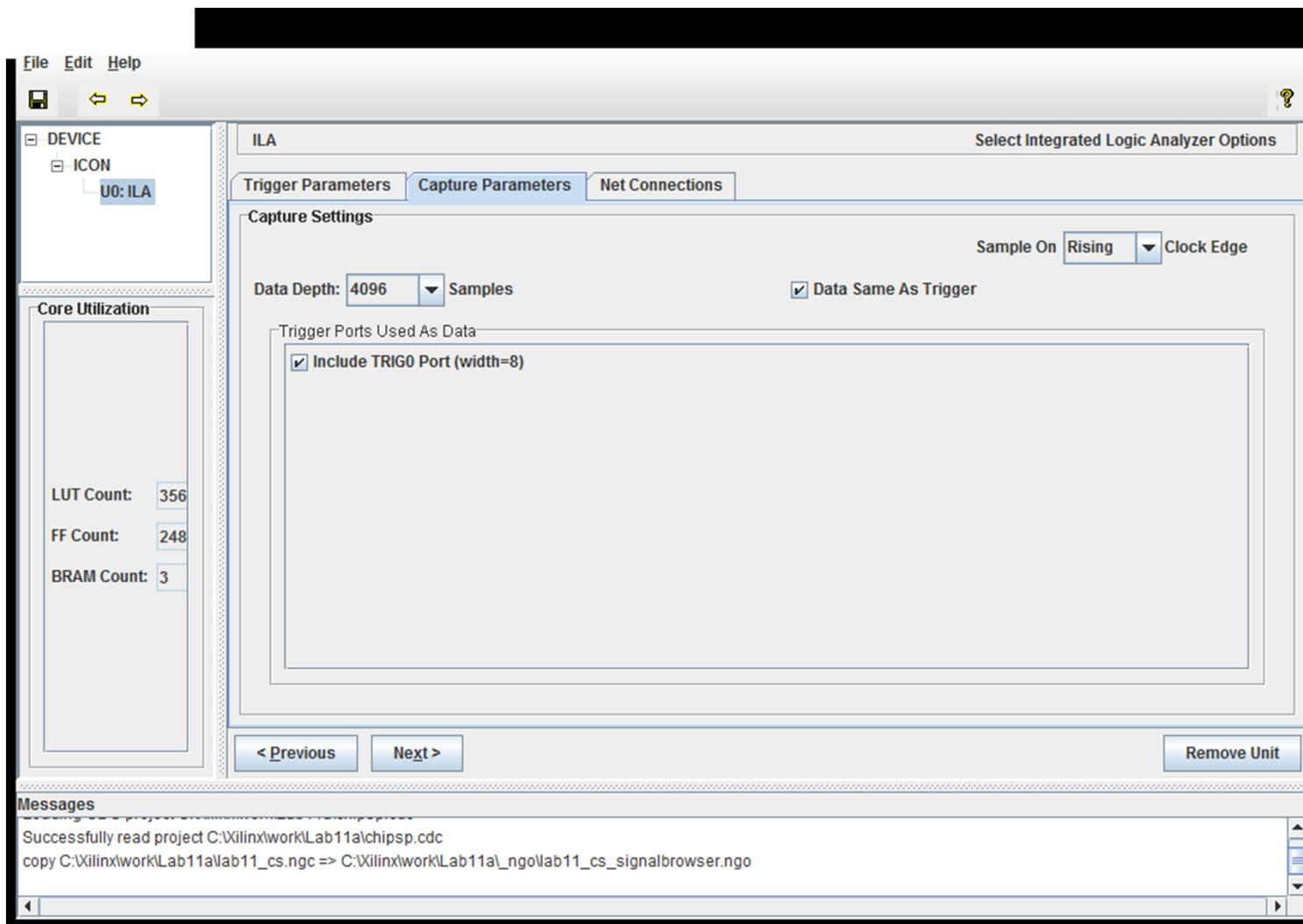
New ILA



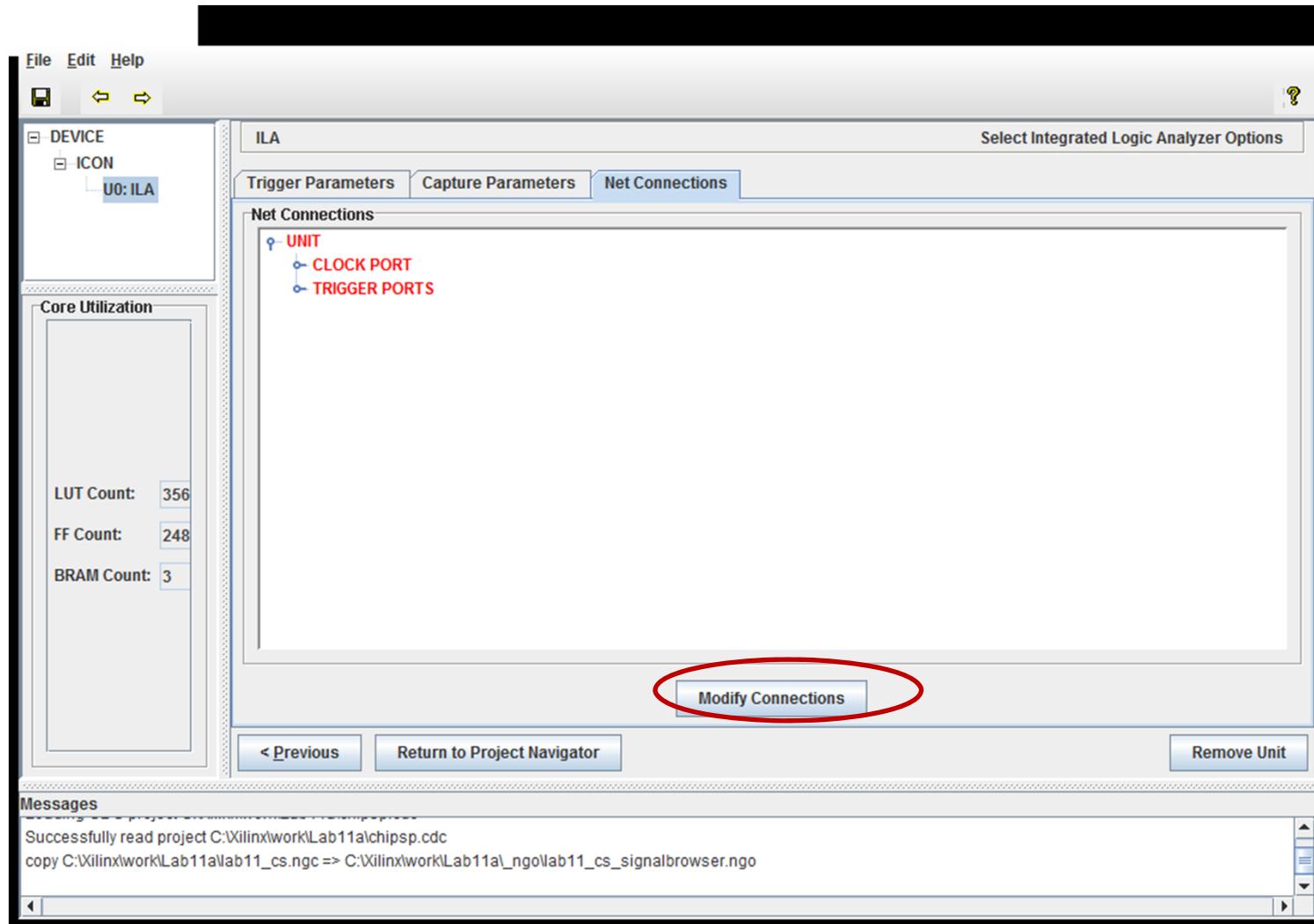
Watch signal



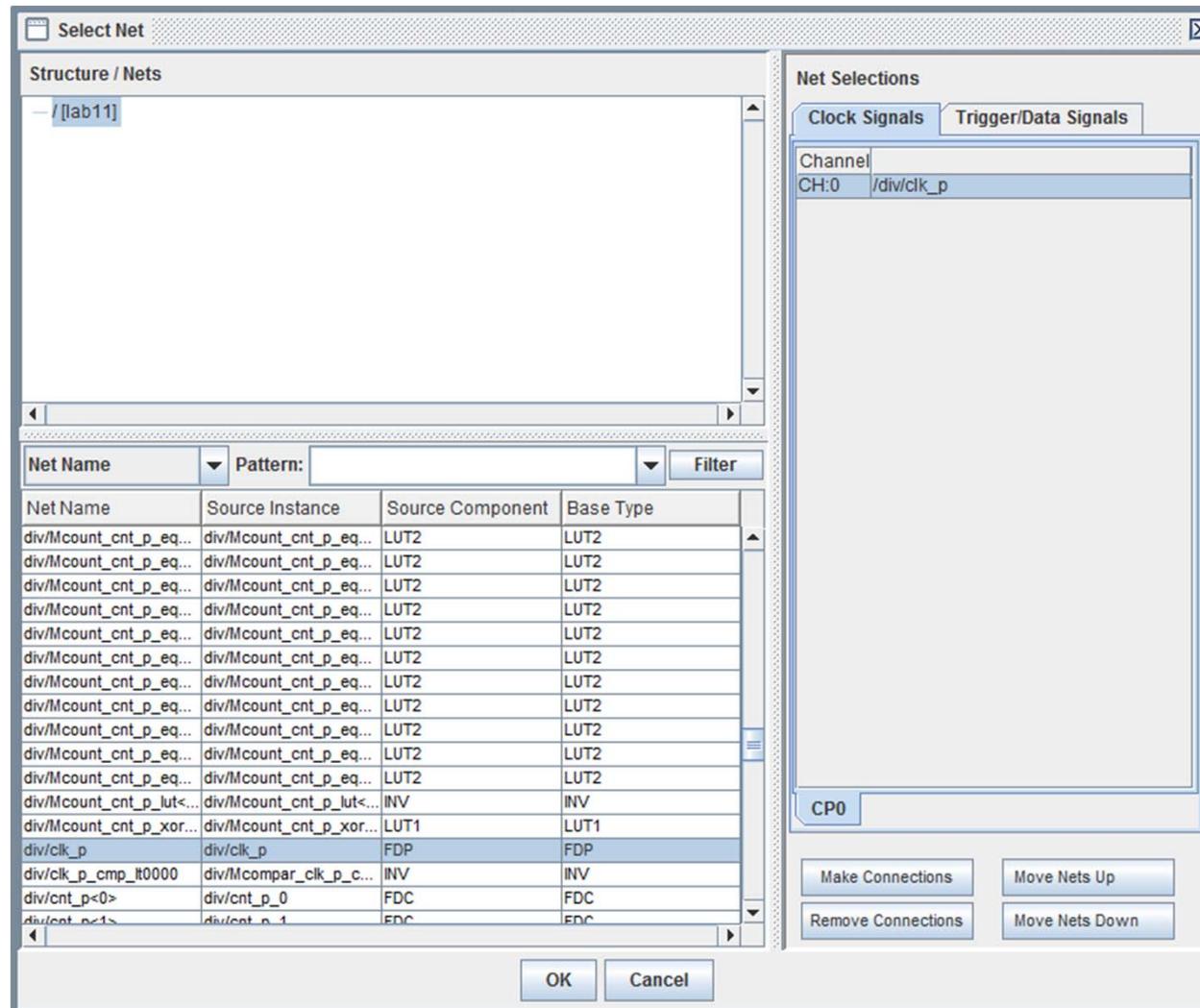
Sample Depth



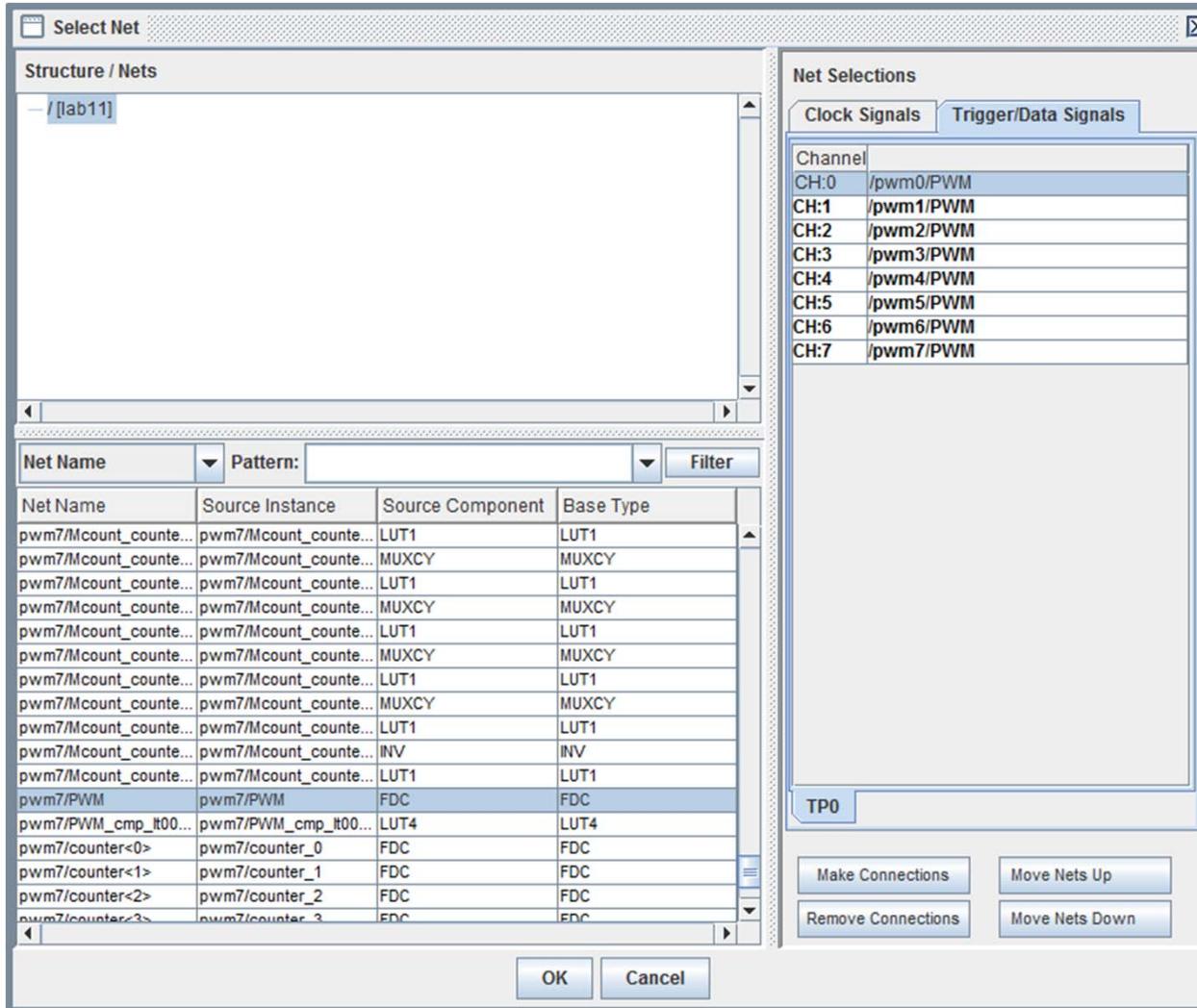
Connections



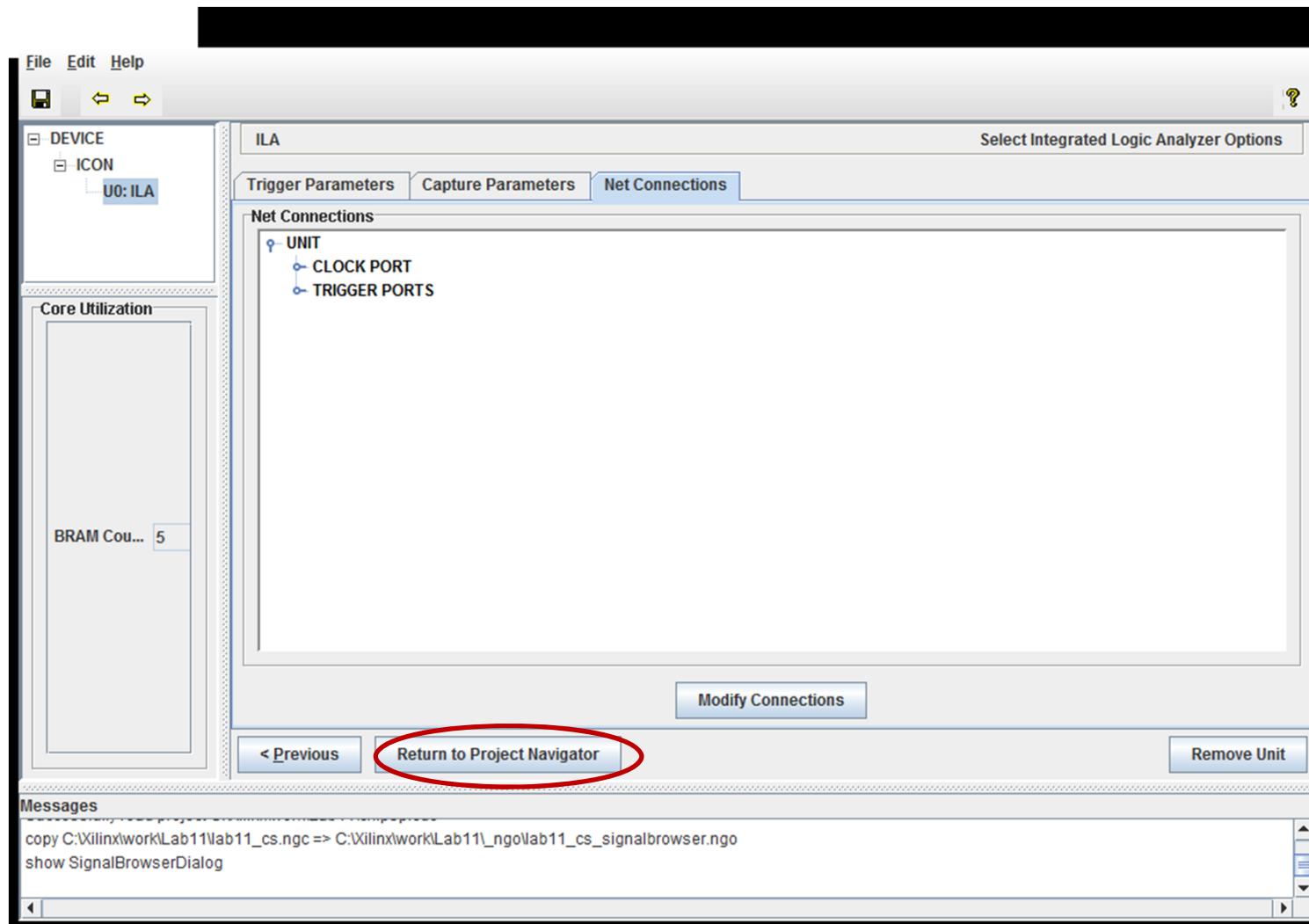
Trigger clock



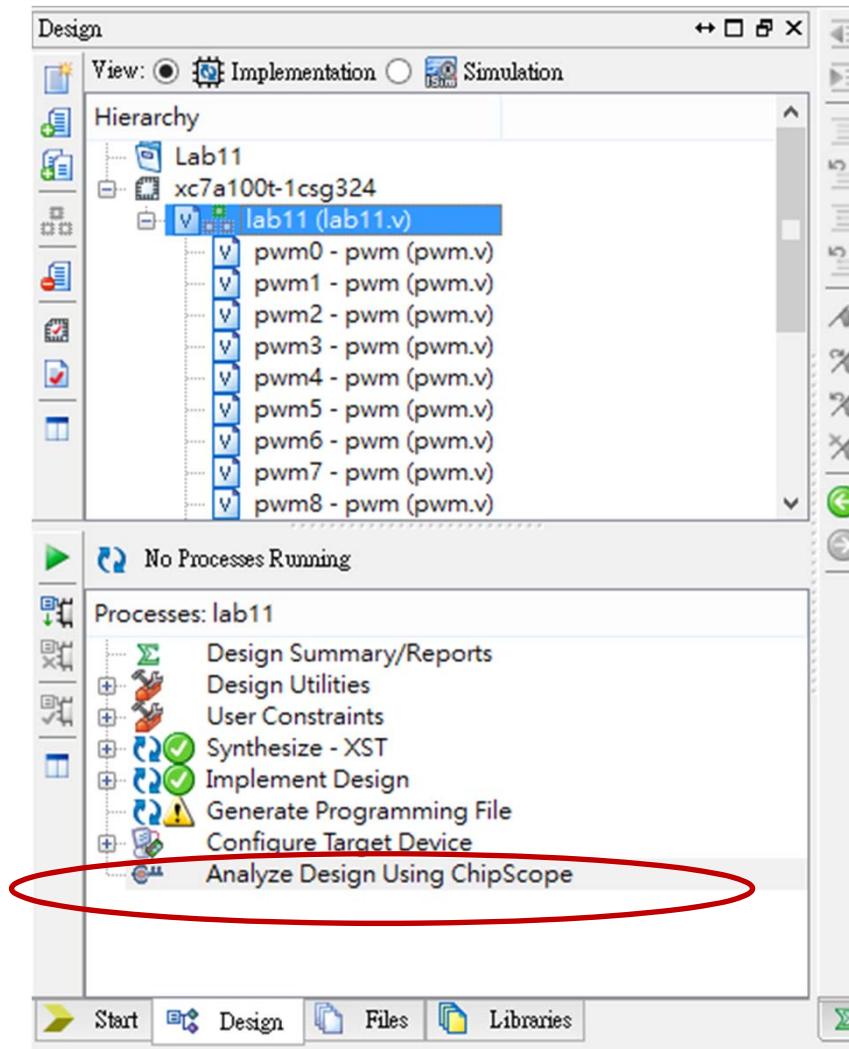
Signal



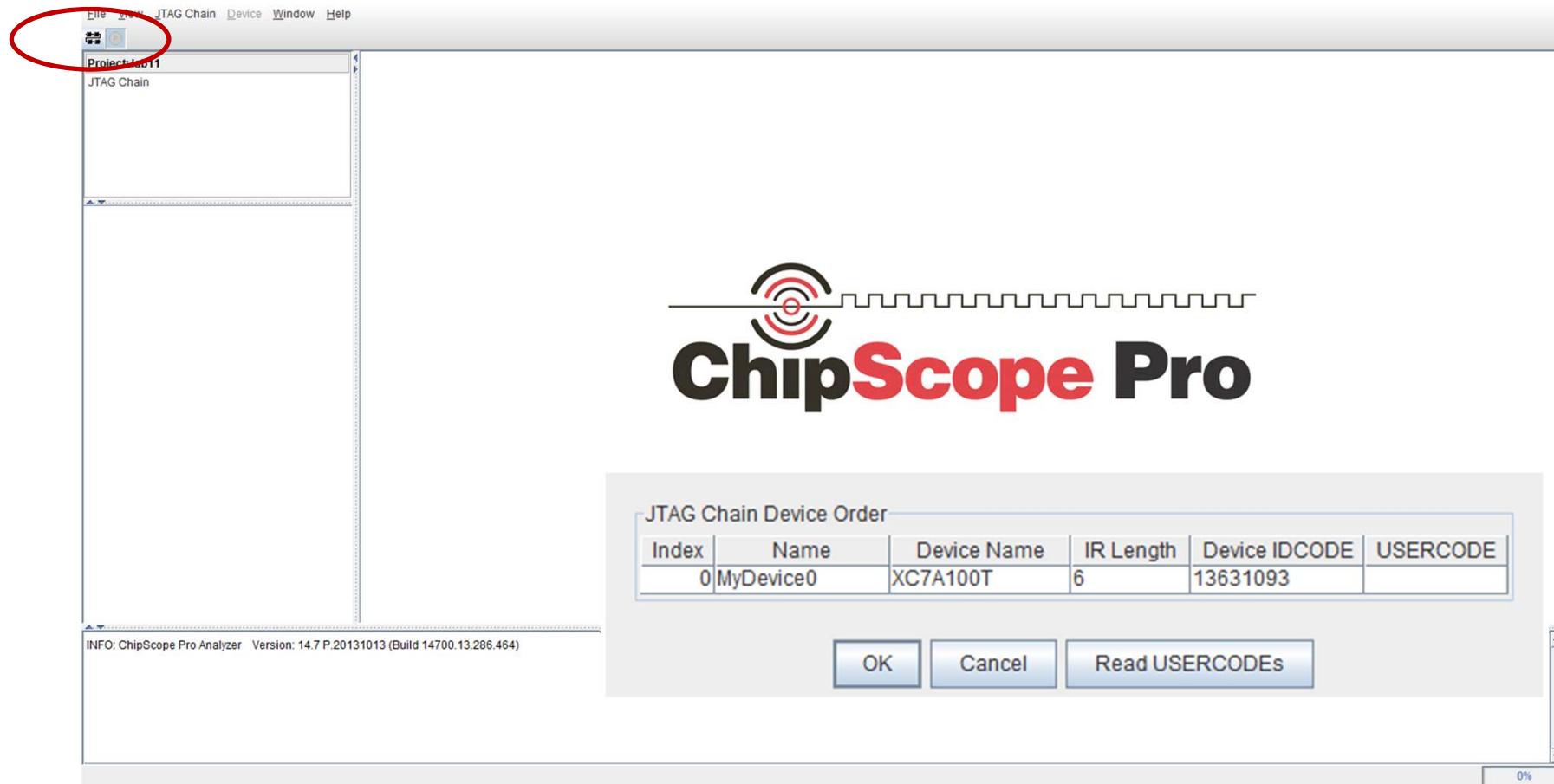
Complete setting

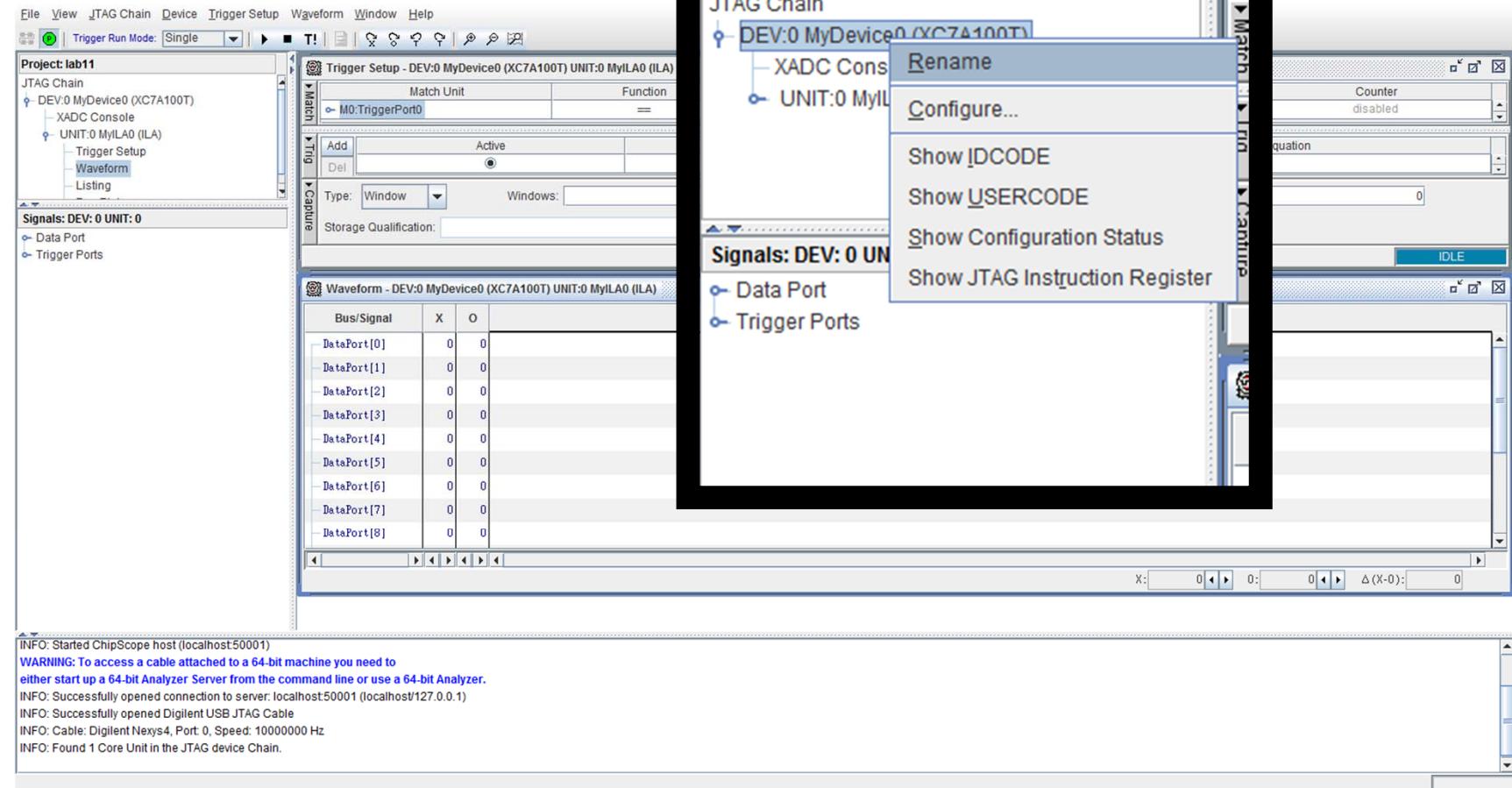


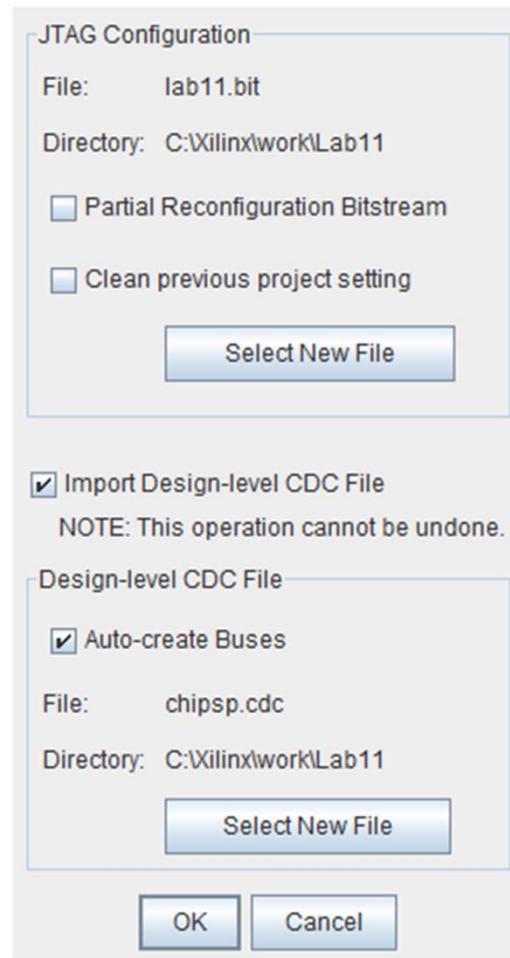
Analyze Design ChipScope

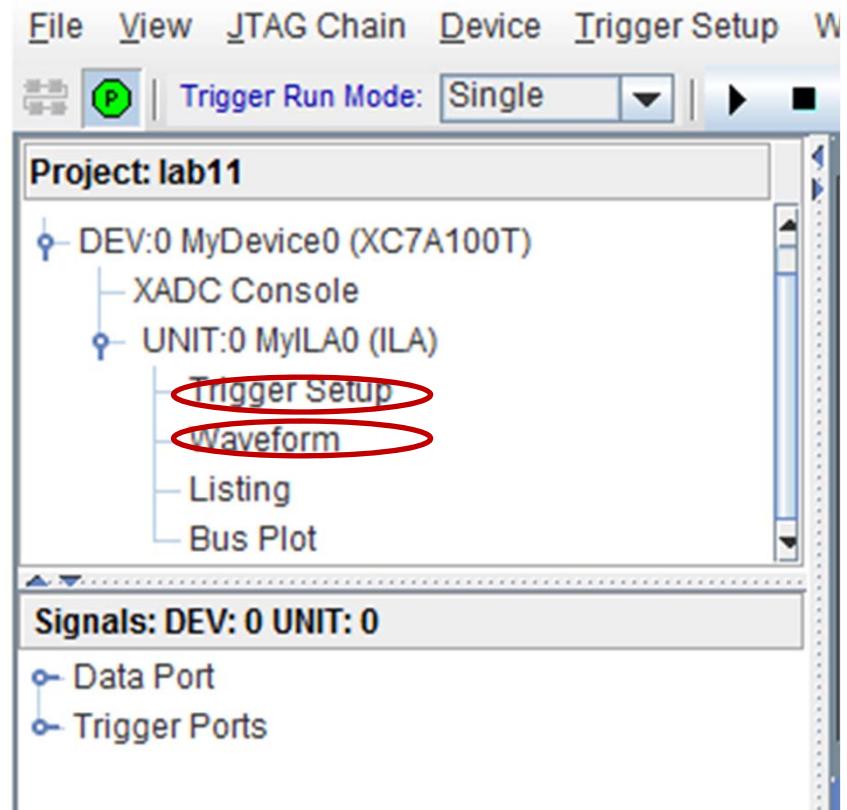


Open cable

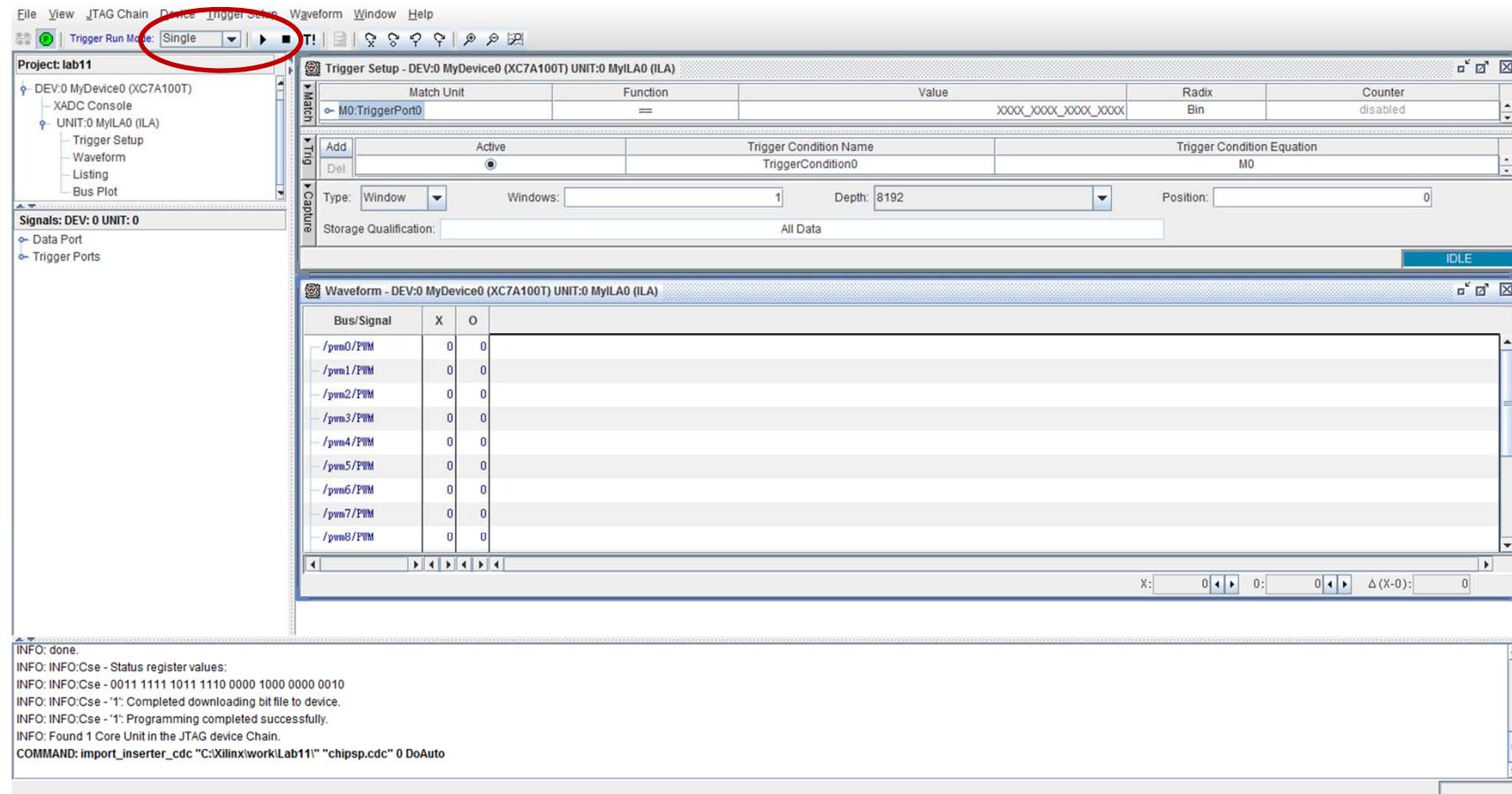








Run



Run

