Introduction to EDA Final Project

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December 25, 2015

1 Topic Chosen

Fixed-outline Chip Floorplanning

2 Instructor

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3 Problem Statement

This programming assignment asks you to write a fixed-outline chip floorplanner that can handle hard macros. Given a set of rectangular macros and a set of nets, the floorplanner places all macros within a rectangular chip without any overlaps. We assume that the lower-left corner of this chip is the origin (0,0), and no space (channel) is needed between two macros. The objective is to minimize the area of the chip bounding box and the total net wirelength. The total wirelength W of a set N can be computed by

$$W = \sum_{n_i \in N} HPWL(n_i)$$

where n_i denotes a net in N, and $HPWL(n_i)$ denotes the half-perimeter wirelength of n_i. The objective for this problem is to minimize

$$Cost = \alpha A + (1 - \alpha)W$$

where A denotes the bounding-box area of the floorplan, and $\alpha, 0 \leq \alpha \leq 1$, is a user-defined ratio to balance the final area and wirelength. Note that a floorplan that cannot fit into the given outline is not accepted.

4 Algorithm

詳細情形要寫了才知道，但是應該會採取 dynammic programming 和 maximum flow 的演算法。

5 Time Schedule

Week 15 選定題目、完成 proposal

Week 16 將資料結構寫好，如有需要會去找張耀文老師討論想法、解法

Week 17 把整個 project 完成，通過範例測資

2016.1.12 製作隔天報告的投影片

2016.1.13 繳交 project 並完成報告