Adam Frazee
CSE 278
Jianhui Yue
11/2/2015

Project 2

1 How do you design the circuit?

The design of the Fibonacci circuit is relatively simple. The base circuit consists of 2 registers and an adder. They of course are all 20 bits. We will respectively call register 1 (reg1), register 2 (reg 2) , and the adder (add). Starting with reg1 it is wired up to add, and reg2. While reg2 is wired to add. It is important to note that reg2 is fed to my output not the result after addition. Then add is wired to reg1. When reg1 is set to be one, and the clock starts to run then Fibonacci numbers are produced.

Dealing with the overflow of the 20 bits was the hardest part of the entire project. Since my output wasn't coming after the adder I couldn't use the overflow of add to signal that everything should restart. So instead I used a compararator, and compared my output to the biggest possible Fibonacci number I could generate. The compararator then switched two multiplexers to constant values that updated the registers.

2 What's the maximal Fibonacci number generated by your circuit?

The biggest number that my circuit can generate is 832040. Any number greater overflows.