# AD7367 HDL Driver

**Revision history**

| Date | Rev | Description |
|---|---|---|
| 11.20.2012 | 0.1 | Document creation |
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# 1. Introduction

This document describes the HDL driver for the AD7367 part. The driver is written in Verilog and can be integrated in designs with or without softcores.

# 2. Architecture

Fig. 1 presents the block diagram of the AD7367 IP.

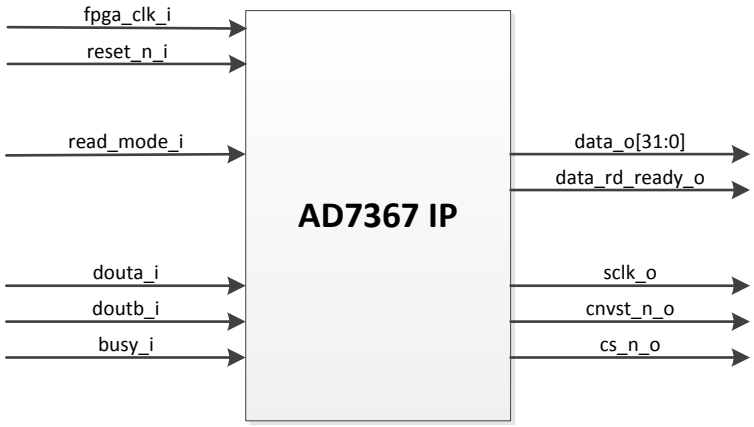


Fig. 1 AD7367 IP

Table 2 presents a description of the IP's IO ports.

| Port | Direction | Width | Description |
|---|---|---|---|
| *Clock and reset ports* | | | |
| FPGA_CLK_I | IN | 1 | Main clock input. 100 MHz |
| RESET_N_I | IN | 1 | Active low reset signal. |
| *IP control and data ports* | | | |
| READ_MODE_I | IN | 1 | Signal used to select between single line read mode(HIGH) or dual read mode(LOW). |
| DATA_O | OUT | 32 | Outputs the data read from the ADC. The most significant two bytes store the data from channel A, and the least significant two bytes store data from channel B. |
| DATA_RD_READY_O | OUT | 1 | Active high signal to indicate the status of a read operation from the AD7367. The IP continuously reads the conversion results from the AD7367 and outputs them on the DATA_O bus. When this signal is high data can be read from the DATA_O bus. |
| *Ad7367 control and data ports* | | | |
| DOUTA_I | IN | 1 | The data output is supplied to each pin as a serial data stream. The bits are clocked out on the falling edge of the |

| | | | |
|---|---|---|---|
| | | | SCLK input. The data simultaneously appears on both pins from the simultaneous conversions of both ADCs |
| DOUTB_I | IN | 1 | The data output is supplied to each pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data simultaneously appears on both pins from the simultaneous conversions of both ADCs |
| BUSY_I | OUT | 1 | Busy transitions high when a conversion is started and remains high until the conversion is complete. It is not used by the current driver. |
| SCLK_O | OUT | 1 | This pin provides the SCLK for accessing the data from AD7367. |
| CNVST_N_O | OUT | 1 | This pin is edge triggered. On the falling edge of this input, the track/hold goes into hold mode and the conversion is initiated. |
| CS_N_O | OUT | 1 | This signal frames the serial data transfer. |

Table 1. IO ports

Fig. 2 presents the timing diagram for read operations.

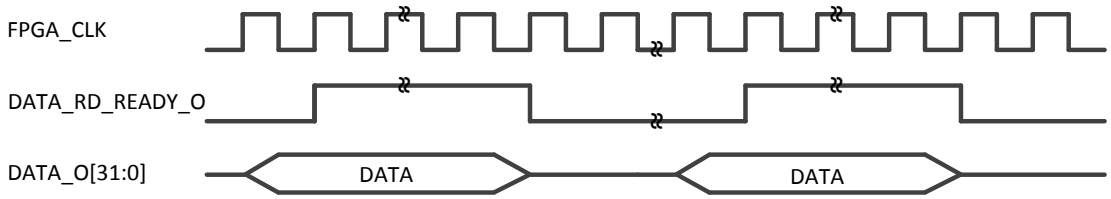


Fig. 2. Read operations timing diagram