Table 9. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name		specified in brackets below the pin name, the pin function during and after as the actual pin name
	S	Supply pin
Pin type	I	Input only pin
	I/O	Input / output pin
	FT	5 V tolerant I/O
I/O structure	TTa	3.3 V tolerant I/O directly connected to ADC
1/O structure	В	Dedicated BOOT pin
	RST	Bidirectional reset pin with weak pull-up resistor
Notes	Unless otherwise	specified by a note, all I/Os are set as floating inputs during and after reset
Alternate functions	Functions selected	d through GPIOx_AFR registers
Additional functions	Functions directly	selected/enabled through peripheral registers

Table 10. STM32F745xx and STM32F746xx pin and ball definition

		ı	Pin Nı	umbei	r								
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
1	А3	D8	1	A2	1	1	A3	PE2	I/O	FT	-	TRACECLK, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, ETH_MII_TXD3, FMC_A23, EVENTOUT	-
2	В3	C10	2	A1	2	2	A2	PE3	I/O	FT	-	TRACEDO, SAI1_SD_B, FMC_A19, EVENTOUT	-
3	СЗ	B11	3	B1	3	3	A1	PE4	I/O	FT	-	TRACED1, SPI4_NSS, SAI1_FS_A, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT	-



Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

				umbei								ban deminion (continu	
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
4	D3	D9	4	B2	4	4	B1	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT	-
5	E3	E8	5	В3	5	5	B2	PE6	I/O	FT	-	TRACED3, TIM1_BKIN2, TIM9_CH2, SPI4_MOSI, SAI1_SD_A, SAI2_MCK_B, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT	-
-	-	-	-	-	-	-	G6	VSS	S	-	-	-	-
-	ı	-	ı	-	-	-	F5	VDD	S	-	-	-	-
6	B2	C11	6	C1	6	6	C1	VBAT	S	ı	-	-	-
-	1	1	ı	D2	7	7	C2	PI8	I/O	FT	(2)	EVENTOUT	RTC_TAMP2/ RTC_TS,WK UP5
7	A2	D10	7	D1	8	8	D1	PC13	I/O	FT	(2)	EVENTOUT	RTC_TAMP1/ RTC_TS/RTC _OUT,WKUP 4
8	A1	D11	8	E1	9	9	E1	PC14- OSC32_I N(PC14)	I/O	FT	(2) (3)	EVENTOUT	OSC32_IN
9	B1	E11	9	F1	10	10	F1	PC15- OSC32_ OUT(PC 15)	I/O	FT	(2)	EVENTOUT	OSC32_OUT
-	-	-	-	-	-	-	G5	VDD	S	-	-	-	-
-	ı	1	ı	D3	11	11	E4	PI9	I/O	FT	-	CAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT	-
-	-	-	-	E3	12	12	D5	PI10	I/O	FT	-	ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT	-

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

		ı	Pin N	umbei	r								
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
-	-	-	-	E4	13	13	F3	PI11	I/O	FT	-	OTG_HS_ULPI_DIR, EVENTOUT	WKUP6
-	-	E7	-	F2	14	14	F2	VSS	S	-	-	-	-
-	-	E10	-	F3	15	15	F4	VDD	S	-	-	-	-
-	-	F11	10	E2	16	16	D2	PF0	I/O	FT	-	I2C2_SDA, FMC_A0, EVENTOUT	-
-	-	E9	11	НЗ	17	17	E2	PF1	I/O	FT	_	I2C2_SCL, FMC_A1, EVENTOUT	-
-	-	F10	12	H2	18	18	G2	PF2	I/O	FT	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	-	-	-	-	19	E3	PI12	I/O	FT	-	LCD_HSYNC, EVENTOUT	-
-	-	-	-	-	-	20	G3	PI13	I/O	FT	-	LCD_VSYNC, EVENTOUT	-
-	-	-	-	-	-	21	НЗ	PI14	I/O	FT	-	LCD_CLK, EVENTOUT	-
-	-	G11	13	J2	19	22	H2	PF3	I/O	FT	-	FMC_A3, EVENTOUT	ADC3_IN9
-	ı	F9	14	J3	20	23	J2	PF4	I/O	FT	-	FMC_A4, EVENTOUT	ADC3_IN14
-	ı	F8	15	K3	21	24	K3	PF5	I/O	FT	-	FMC_A5, EVENTOUT	ADC3_IN15
10	C2	H7	16	G2	22	25	H6	VSS	S	-	-	-	-
11	D2	-	17	G3	23	26	H5	VDD	S	-	-	-	-
-	-	G10	18	K2	24	27	K2	PF6	I/O	FT	-	TIM10_CH1, SPI5_NSS, SAI1_SD_B, UART7_Rx, QUADSPI_BK1_IO3, EVENTOUT	ADC3_IN4
-	1	F7	19	K1	25	28	K1	PF7	I/O	FT	-	TIM11_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_Tx, QUADSPI_BK1_IO2, EVENTOUT	ADC3_IN5



Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

				umbei								ball definition (continu	
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
-	-	H11	20	L3	26	29	L3	PF8	I/O	FT	-	SPI5_MISO, SAI1_SCK_B, UART7_RTS, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	ADC3_IN6
-	-	G8	21	L2	27	30	L2	PF9	I/O	FT	-	SPI5_MOSI, SAI1_FS_B, UART7_CTS, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	ADC3_IN7
-	-	G9	22	L1	28	31	L1	PF10	I/O	FT	-	DCMI_D11, LCD_DE, EVENTOUT	ADC3_IN8
12	C1	J11	23	G1	29	32	G1	PH0- OSC_IN( PH0)	I/O	FT	-	EVENTOUT	OSC_IN <sup>(4)</sup>
13	D1	H10	24	H1	30	33	H1	PH1- OSC_OU T(PH1)	I/O	FT	-	EVENTOUT	OSC_OUT <sup>(4)</sup>
14	E1	H9	25	J1	31	34	J1	NRST	I/O	RS T	-	-	-
15	F1	Н8	26	M2	32	35	M2	PC0	I/O	FT	(4)	SAI2_FS_B, OTG_HS_ULPI_STP, FMC_SDNWE, LCD_R5, EVENTOUT	ADC123_IN1 0
16	F2	K11	27	M3	33	36	M3	PC1	I/O	FT	(4)	TRACED0, SPI2_MOSI/I2S2_SD, SAI1_SD_A, ETH_MDC, EVENTOUT	ADC123_IN1 1, RTC_TAMP3, WKUP3
17	E2	J10	28	M4	34	37	M4	PC2	I/O	FT	(4)	SPI2_MISO, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT	ADC123_IN1 2

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

		ı	Pin N	umbei	r					-		,	
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
18	F3	J9	29	M5	35	38	L4	PC3	I/O	FT	(4)	SPI2_MOSI/I2S2_SD, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, FMC_SDCKE0, EVENTOUT	ADC123_IN1 3
-	-	G7	30	G3	36	39	J5	VDD	S	-	-	-	-
-	-	-	-	-	-	-	J6	VSS	S	-	-	-	-
19	G1	K10	31	M1	37	40	M1	VSSA	S	-	-	-	-
-	-	-	-	N1	-	-	N1	VREF-	S	-	-	-	-
20	-	L11	32	P1	38	41	P1	VREF+	S	-	-	-	-
21	H1	L10	33	R1	39	42	R1	VDDA	S	-	-	-	-
22	G2	K9	34	N3	40	43	N3	PA0- WKUP(P A0)	I/O	FT	(5)	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, SAI2_SD_B, ETH_MII_CRS, EVENTOUT	ADC123_IN0, WKUP1 <sup>(4)</sup>
23	H2	K8	35	N2	41	44	N2	PA1	I/O	FT	(4)	TIM2_CH2, TIM5_CH2, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCK_B, ETH_MII_RX_CLK/ETH_ RMII_REF_CLK, LCD_R2, EVENTOUT	ADC123_IN1
24	J2	L9	36	P2	42	45	P2	PA2	I/O	FT	(4)	TIM2_CH3, TIM5_CH3, TIM9_CH1, USART2_TX, SAI2_SCK_B, ETH_MDIO, LCD_R1, EVENTOUT	ADC123_IN2, WKUP2
-	-	-	-	F4	43	46	K4	PH2	I/O	FT		LPTIM1_IN2, QUADSPI_BK2_IO0, SAI2_SCK_B, ETH_MII_CRS, FMC_SDCKE0, LCD_R0, EVENTOUT	-



Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

				umbei				111102111				ball definition (continue	
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
-	-	-	-	G4	44	47	J4	PH3	I/O	FT	-	QUADSPI_BK2_IO1, SAI2_MCK_B, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	-
-	-	-	-	H4	45	48	H4	PH4	I/O	FT	-	I2C2_SCL, OTG_HS_ULPI_NXT, EVENTOUT	-
-	-	-	-	J4	46	49	J3	PH5	I/O	FT	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	-
25	K2	M11	37	R2	47	50	R2	PA3	I/O	FT	(4)	TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC123_IN3
26	J1	-	38	-	-	51	K6	VSS	S	-	-	-	-
-	E6	N11	ı	L4	48	ı	L5	BYPASS _REG	I	FT	-	-	-
27	K1	J8	39	K4	49	52	K5	VDD	S	-	-	-	-
28	G3	M10	40	N4	50	53	N4	PA4	I/O	TT a	(4)	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC12_IN4, DAC_OUT1
29	НЗ	M9	41	P4	51	54	P4	PA5	I/O	TT a	(4)	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT	ADC12_IN5, DAC_OUT2
30	J3	N10	42	P3	52	55	P3	PA6	I/O	FT	(4)	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, TIM13_CH1, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC12_IN6

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

		i	Pin Nu	umbei	r								
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
31	<b>K</b> 3	L8	43	R3	53	56	R3	PA7	I/O	FT	(4)	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, TIM14_CH1, ETH_MII_RX_DV/ETH_R MII_CRS_DV, FMC_SDNWE, EVENTOUT	ADC12_IN7
32	G4	M8	44	N5	54	57	N5	PC4	I/O	FT	(4)	I2S1_MCK, SPDIFRX_IN2, ETH_MII_RXD0/ETH_RM II_RXD0, FMC_SDNE0, EVENTOUT	ADC12_IN14
33	H4	N9	45	P5	55	58	P5	PC5	I/O	FT	(4)	SPDIFRX_IN3, ETH_MII_RXD1/ETH_RM II_RXD1, FMC_SDCKE0, EVENTOUT	ADC12_IN15
-	-	J7	-	-	-	59	L7	VDD	S	-	-	-	-
-	-	ı	ı	-	-	60	L6	VSS	S	ı	-	-	-
34	J4	N8	46	R5	56	61	R5	PB0	I/O	FT	(4)	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, EVENTOUT	ADC12_IN8
35	K4	K7	47	R4	57	62	R4	PB1	I/O	FT	(4)	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, EVENTOUT	ADC12_IN9
36	G5	L7	48	M6	58	63	M5	PB2	I/O	FT	-	SAI1_SD_A, SPI3_MOSI/I2S3_SD, QUADSPI_CLK, EVENTOUT	-
-	-	-	-	-	-	64	G4	PI15	I/O	FT	-	LCD_R0, EVENTOUT	-
-	1	-	-	-	-	65	R6	PJ0	I/O	FT	-	LCD_R1, EVENTOUT	-
-	-	-	-	-	-	66	R7	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	-



Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

				umbei		. 37171						ball definition (continue	,
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
-	-	-	-	-	-	67	P7	PJ2	I/O	FT	-	LCD_R3, EVENTOUT	-
-	-	-	-	-	-	68	N8	PJ3	I/O	FT	-	LCD_R4, EVENTOUT	-
-	-	-	-	-	-	69	М9	PJ4	I/O	FT	-	LCD_R5, EVENTOUT	-
-	-	M7	49	R6	59	70	P8	PF11	I/O	FT	-	SPI5_MOSI, SAI2_SD_B, FMC_SDNRAS, DCMI_D12, EVENTOUT	-
-	ı	N7	50	P6	60	71	M6	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-
-	ı	-	51	M8	61	72	K7	VSS	S	-	-	-	-
-	ı	-	52	N8	62	73	L8	VDD	S	-	-	-	-
-	-	K6	53	N6	63	74	N6	PF13	I/O	FT	-	I2C4_SMBA, FMC_A7, EVENTOUT	-
-	-	L6	54	R7	64	75	P6	PF14	I/O	FT	-	I2C4_SCL, FMC_A8, EVENTOUT	-
-	-	M6	55	P7	65	76	M8	PF15	I/O	FT	-	I2C4_SDA, FMC_A9, EVENTOUT	-
-	-	N6	56	N7	66	77	N7	PG0	I/O	FT	-	FMC_A10, EVENTOUT	-
-	-	K5	57	M7	67	78	M7	PG1	I/O	FT	-	FMC_A11, EVENTOUT	-
37	H5	L5	58	R8	68	79	R8	PE7	I/O	FT	-	TIM1_ETR, UART7_Rx, QUADSPI_BK2_IO0, FMC_D4, EVENTOUT	-
38	J5	M5	59	P8	69	80	N9	PE8	I/O	FT	-	TIM1_CH1N, UART7_Tx, QUADSPI_BK2_IO1, FMC_D5, EVENTOUT	-
39	K5	N5	60	P9	70	81	P9	PE9	I/O	FT	-	TIM1_CH1, UART7_RTS, QUADSPI_BK2_IO2, FMC_D6, EVENTOUT	-
-	-	НЗ	61	M9	71	82	K8	VSS	S	-	-	-	-
-	-	J5	62	N9	72	83	L9	VDD	S	-	-	-	-
40	G6	J4	63	R9	73	84	R9	PE10	I/O	FT	_	TIM1_CH2N, UART7_CTS, QUADSPI_BK2_IO3, FMC_D7, EVENTOUT	-

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

				umber								ban deminion (continue	
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
41	H6	K4	64	P10	74	85	P10	PE11	I/O	FT	-	TIM1_CH2, SPI4_NSS, SAI2_SD_B, FMC_D8, LCD_G3, EVENTOUT	-
42	J6	L4	65	R10	75	86	R10	PE12	I/O	FT	1	TIM1_CH3N, SPI4_SCK, SAI2_SCK_B, FMC_D9, LCD_B4, EVENTOUT	-
43	K6	N4	66	N11	76	87	R12	PE13	I/O	FT	1	TIM1_CH3, SPI4_MISO, SAI2_FS_B, FMC_D10, LCD_DE, EVENTOUT	-
44	G7	M4	67	P11	77	88	P11	PE14	I/O	FT	-	TIM1_CH4, SPI4_MOSI, SAI2_MCK_B, FMC_D11, LCD_CLK, EVENTOUT	-
45	H7	L3	68	R11	78	89	R11	PE15	I/O	FT	1	TIM1_BKIN, FMC_D12, LCD_R7, EVENTOUT	-
46	J7	M3	69	R12	79	90	P12	PB10	I/O	FT	-	TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, USART3_TX, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT	-
47	K7	N3	70	R13	80	91	R13	PB11	I/O	FT	1	TIM2_CH4, I2C2_SDA,	-
48	F8	N2	71	M10	81	92	L11	VCAP_1	S	-	-	-	-
49	-	H2	-	-	1	93	K9	VSS	S	-	_	-	-
50	-	J6	72	N10	82	94	L10	VDD	S	-	-	-	-
-	-	-	-	-	-	95	M14	PJ5	I/O	FT	-	LCD_R6, EVENTOUT	-
-	-	-	-	M11	83	96	P13	PH6	I/O	FT	-	I2C2_SMBA, SPI5_SCK, TIM12_CH1, ETH_MII_RXD2, FMC_SDNE1, DCMI_D8, EVENTOUT	-



Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

				umber						•		ban deminion (continue	
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
-	ı	-	-	N12	84	97	N13	PH7	I/O	FT	-	I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, DCMI_D9, EVENTOUT	-
-	-	-	-	M12	85	98	P14	PH8	I/O	FT	-	I2C3_SDA, FMC_D16, DCMI_HSYNC, LCD_R2, EVENTOUT	-
-	1	-	-	M13	86	99	N14	PH9	I/O	FT	-	I2C3_SMBA, TIM12_CH2, FMC_D17, DCMI_D0, LCD_R3, EVENTOUT	-
-	-	-	-	L13	87	100	P15	PH10	I/O	FT	-	TIM5_CH1, I2C4_SMBA, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT	-
-	1	-	-	L12	88	101	N15	PH11	I/O	FT	-	TIM5_CH2, I2C4_SCL, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT	-
-	ı	-	-	K12	89	102	M15	PH12	I/O	FT	-	TIM5_CH3, I2C4_SDA, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT	-
-	-	-	-	H12	90	-	K10	VSS	S	-	-	-	-
-	-	-	-	J12	91	103	K11	VDD	S	-	-	-	-
51	K8	M2	73	P12	92	104	L13	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, USART3_CK, CAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RM II_TXD0, OTG_HS_ID, EVENTOUT	-
52	J8	N1	74	P13	93	105	K14	PB13	I/O	FT	-	TIM1_CH1N, SPI2_SCK/I2S2_CK, USART3_CTS, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RM II_TXD1, EVENTOUT	OTG_HS_VB US

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

		ı	Pin N	umbei	,							·	
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
53	H10	K3	75	R14	94	106	R14	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, SPI2_MISO, USART3_RTS, TIM12_CH1, OTG_HS_DM, EVENTOUT	-
54	G10	J3	76	R15	95	107	R15	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI/I2S2_SD, TIM12_CH2, OTG_HS_DP, EVENTOUT	-
55	K9	L2	77	P15	96	108	L15	PD8	I/O	FT	-	USART3_TX, SPDIFRX_IN11, FMC_D13, EVENTOUT	-
56	J9	M1	78	P14	97	109	L14	PD9	I/O	FT	-	USART3_RX, FMC_D14, EVENTOUT	-
57	H9	H4	79	N15	98	110	K15	PD10	I/O	FT	-	USART3_CK, FMC_D15, LCD_B3, EVENTOUT	-
58	G9	K2	80	N14	99	111	N10	PD11	I/O	FT	-	I2C4_SMBA, USART3_CTS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16/FMC_CLE, EVENTOUT	-
59	K10	Н6	81	N13	100	112	M10	PD12	I/O	FT	-	TIM4_CH1, LPTIM1_IN1, I2C4_SCL, USART3_RTS, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17/FMC_ALE, EVENTOUT	-
60	J10	H5	82	M15	101	113	M11	PD13	I/O	FT	-	TIM4_CH2, LPTIM1_OUT, I2C4_SDA, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT	-



Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

				umbei		IOXX (		1111021114		<b>P</b> (		ball definition (continue	
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
-	-	-	83	-	102	114	J10	VSS	S	-	-	-	-
-	-	L1	84	J13	103	115	J11	VDD	S	-	-	-	-
61	H8	J2	85	M14	104	116	L12	PD14	I/O	FT	-	TIM4_CH3, UART8_CTS, FMC_D0, EVENTOUT	-
62	G8	K1	86	L14	105	117	K13	PD15	I/O	FT	-	TIM4_CH4, UART8_RTS, FMC_D1, EVENTOUT	-
-	-	-	-	-	-	118	K12	PJ6	I/O	FT	-	LCD_R7, EVENTOUT	-
-	-	-	-	-	-	119	J12	PJ7	I/O	FT	-	LCD_G0, EVENTOUT	-
-	-	-	-	-	-	120	H12	PJ8	I/O	FT	-	LCD_G1, EVENTOUT	-
-	-	-	-	-	-	121	J13	PJ9	I/O	FT	-	LCD_G2, EVENTOUT	-
-	-	-	-	-	-	122	H13	PJ10	I/O	FT	-	LCD_G3, EVENTOUT	-
-	-	-	-	-	-	123	G12	PJ11	I/O	FT	-	LCD_G4, EVENTOUT	-
-	-	-	-	-	-	124	H11	VDD	S	-	-	-	-
-	-	-	-	-	-	125	H10	VSS	S	-	-	-	-
-	-	-	-	-	-	126	G13	PK0	I/O	FT	-	LCD_G5, EVENTOUT	-
-	-	-	-	-	-	127	F12	PK1	I/O	FT	-	LCD_G6, EVENTOUT	-
-	-	-	-	-	-	128	F13	PK2	I/O	FT	-	LCD_G7, EVENTOUT	-
-	ı	J1	87	L15	106	129	M13	PG2	I/O	FT	-	FMC_A12, EVENTOUT	-
-	ı	G3	88	K15	107	130	M12	PG3	I/O	FT	-	FMC_A13, EVENTOUT	-
-	ı	G5	89	K14	108	131	N12	PG4	I/O	FT	-	FMC_A14/FMC_BA0, EVENTOUT	-
-	ı	G6	90	K13	109	132	N11	PG5	I/O	FT	-	FMC_A15/FMC_BA1, EVENTOUT	-
-	ı	G4	91	J15	110	133	J15	PG6	I/O	FT	-	DCMI_D12, LCD_R7, EVENTOUT	-
-	-	H1	92	J14	111	134	J14	PG7	I/O	FT	-	USART6_CK, FMC_INT, DCMI_D13, LCD_CLK, EVENTOUT	-

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

				umbei				_				ban deminion (continue	
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
-	-	G2	93	H14	112	135	H14	PG8	I/O	FT	-	SPI6_NSS, SPDIFRX_IN2, USART6_RTS, ETH_PPS_OUT, FMC_SDCLK, EVENTOUT	-
-	-	D2	94	G12	113	136	G10	VSS	S	-	-	-	-
-	F6	G1	95	H13	114	137	G11	VDDUSB	S	-	-	-	-
63	F10	F2	96	H15	115	138	H15	PC6	I/O	FT	1	TIM3_CH1, TIM8_CH1, I2S2_MCK, USART6_TX, SDMMC1_D6, DCMI_D0, LCD_HSYNC, EVENTOUT	-
64	E10	F3	97	G15	116	139	G15	PC7	I/O	FT	1	TIM3_CH2, TIM8_CH2, I2S3_MCK, USART6_RX, SDMMC1_D7, DCMI_D1, LCD_G6, EVENTOUT	-
65	F9	E4	98	G14	117	140	G14	PC8	I/O	FT	ı	TRACED1, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, SDMMC1_D0, DCMI_D2, EVENTOUT	-
66	E9	E3	99	F14	118	141	F14	PC9	I/O	FT	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, SDMMC1_D1, DCMI_D3, EVENTOUT	-
67	D9	F1	100	F15	119	142	F15	PA8	I/O	FT	1	MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, LCD_R6, EVENTOUT	-
68	C9	E2	101	E15	120	143	E15	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, DCMI_D0, EVENTOUT	OTG_FS_VB US



Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

				umbei						•		ban deminion (continue	,
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
69	D10	D5	102	D15	121	144	D15	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, OTG_FS_ID, DCMI_D1, EVENTOUT	-
70	C10	D4	103	C15	122	145	C15	PA11	I/O	FT	-	TIM1_CH4, USART1_CTS, CAN1_RX,OTG_FS_DM, LCD_R4, EVENTOUT	-
71	B10	E1	104	B15	123	146	B15	PA12	I/O	FT	-	TIM1_ETR, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT	-
72	A10	D3	105	A15	124	147	A15	PA13(JT MS- SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
73	E7	D1	106	F13	125	148	E11	VCAP_2	S	-	-	-	-
74	E5	D2	107	F12	126	149	F10	VSS	S	-	-	-	-
75	F5	C1	108	G13	127	150	F11	VDD	S	-	-	-	-
-	-	-	-	E12	128	151	E12	PH13	I/O	FT	-	TIM8_CH1N, CAN1_TX, FMC_D21, LCD_G2, EVENTOUT	-
-	1	-	-	E13	129	152	E13	PH14	I/O	FT	-	TIM8_CH2N, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT	-
-	-	-	-	D13	130	153	D13	PH15	I/O	FT	-	TIM8_CH3N, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT	-
-	-	-	-	E14	131	154	E14	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS/I2S2_WS, FMC_D24, DCMI_D13, LCD_G5, EVENTOUT	-
-	-	ı	-	D14	132	155	D14	PI1	I/O	FT	-	TIM8_BKIN2, SPI2_SCK/I2S2_CK, FMC_D25, DCMI_D8, LCD_G6, EVENTOUT	-

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

		ı	Pin N	umbei	7							,	·
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
-	-	-	-	C14	133	156	C14	PI2	I/O	FT	-	TIM8_CH4, SPI2_MISO, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT	-
1	1	1	-	C13	134	157	C13	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, DCMI_D10, EVENTOUT	-
-	-	F5	-	D9	135	-	F9	VSS	S	-	-	-	-
-	-	A1	-	C9	136	158	E10	VDD	S	-	-	-	-
76	A9	B1	109	A14	137	159	A14	PA14(JT CK- SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
77	A8	C2	110	A13	138	160	A13	PA15(JT DI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, HDMI-CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, UART4_RTS, EVENTOUT	-
78	В9	A2	111	B14	139	161	B14	PC10	I/O	FT	-	SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDMMC1_D2, DCMI_D8, LCD_R2, EVENTOUT	-
79	B8	B2	112	B13	140	162	B13	PC11	I/O	FT	-	SPI3_MISO, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDMMC1_D3, DCMI_D4, EVENTOUT	-
80	C8	C3	113	A12	141	163	A12	PC12	I/O	FT	-	TRACED3, SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, SDMMC1_CK, DCMI_D9, EVENTOUT	-



Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

				umbei								ban deminion (continue	,
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
81	D8	В3	114	B12	142	164	B12	PD0	I/O	FT	-	CAN1_RX, FMC_D2, EVENTOUT	-
82	E8	C4	115	C12	143	165	C12	PD1	I/O	FT	-	CAN1_TX, FMC_D3, EVENTOUT	-
83	В7	A3	116	D12	144	166	D12	PD2	I/O	FT	-	TRACED2, TIM3_ETR, UART5_RX, SDMMC1_CMD, DCMI_D11, EVENTOUT	-
84	C7	B4	117	D11	145	167	C11	PD3	I/O	FT	-	SPI2_SCK/I2S2_CK, USART2_CTS, FMC_CLK, DCMI_D5, LCD_G7, EVENTOUT	-
85	D7	B5	118	D10	146	168	D11	PD4	I/O	FT	-	USART2_RTS, FMC_NOE, EVENTOUT	-
86	В6	A4	119	C11	147	169	C10	PD5	I/O	FT	-	USART2_TX,FMC_NWE, EVENTOUT	-
-	-	-	120	D8	148	170	F8	VSS	S	-	-	-	-
-	-	C5	121	C8	149	171	E9	VDD	S	-	-	-	-
87	C6	F4	122	B11	150	172	B11	PD6	I/O	FT	-	SPI3_MOSI/I2S3_SD, SAI1_SD_A, USART2_RX, FMC_NWAIT, DCMI_D10, LCD_B2, EVENTOUT	-
88	D6	A5	123	A11	151	173	A11	PD7	I/O	FT	-	USART2_CK, SPDIFRX_IN0, FMC_NE1, EVENTOUT	-
-	-	-	-	-	-	174	B10	PJ12	I/O	FT	-	LCD_B0, EVENTOUT	-
-	-	ı	-	-	ı	175	В9	PJ13	I/O	FT	-	LCD_B1, EVENTOUT	-
-	-	-	-	-	-	176	C9	PJ14	I/O	FT	-	LCD_B2, EVENTOUT	-
-	-	-	-	-	-	177	D10	PJ15	I/O	FT	-	LCD_B3, EVENTOUT	-

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

		i	Pin N	umbei	r								
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
-	-	E5	124	C10	152	178	D9	PG9	I/O	FT	-	SPDIFRX_IN3, USART6_RX, QUADSPI_BK2_IO2, SAI2_FS_B, FMC_NE2/FMC_NCE, DCMI_VSYNC, EVENTOUT	-
-	1	C6	125	B10	153	179	C8	PG10	I/O	FT	-	LCD_G3, SAI2_SD_B, FMC_NE3, DCMI_D2, LCD_B2, EVENTOUT	-
-		В6	126	В9	154	180	В8	PG11	I/O	FT	-	SPDIFRX_IN0, ETH_MII_TX_EN/ETH_R MII_TX_EN, DCMI_D3, LCD_B3, EVENTOUT	-
-	-	A6	127	В8	155	181	C7	PG12	I/O	FT	-	LPTIM1_IN1, SPI6_MISO, SPDIFRX_IN1, USART6_RTS, LCD_B4, FMC_NE4, LCD_B1, EVENTOUT	-
-	-	D6	128	A8	156	182	В3	PG13	I/O	FT	-	TRACED0, LPTIM1_OUT, SPI6_SCK, USART6_CTS, ETH_MII_TXD0/ETH_RM II_TXD0, FMC_A24, LCD_R0, EVENTOUT	-
-	-	F6	129	A7	157	183	A4	PG14	I/O	FT	-	TRACED1, LPTIM1_ETR, SPI6_MOSI, USART6_TX, QUADSPI_BK2_IO3, ETH_MII_TXD1/ETH_RM II_TXD1, FMC_A25, LCD_B0, EVENTOUT	-
-	-	-	130	D7	158	184	F7	VSS	S	-	-	-	-
-	ı	E6	131	C7	159	185	E8	VDD	S	-	-	-	-



Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

				ımbeı								ban deminion (continue	,
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
-	-	-	-	-	-	186	D8	PK3	I/O	FT	-	LCD_B4, EVENTOUT	-
-	-	-	-	-	-	187	D7	PK4	I/O	FT	-	LCD_B5, EVENTOUT	-
-	-	-	-	-	-	188	C6	PK5	I/O	FT	-	LCD_B6, EVENTOUT	-
-	-	-	-	-	-	189	C5	PK6	I/O	FT	-	LCD_B7, EVENTOUT	-
-	-	-	-	-	-	190	C4	PK7	I/O	FT	-	LCD_DE, EVENTOUT	-
-	-	A7	132	В7	160	191	В7	PG15	I/O	FT	1	USART6_CTS, FMC_SDNCAS, DCMI_D13, EVENTOUT	-
89	A7	В7	133	A10	161	192	A10	PB3(JTD O/TRAC ESWO)	I/O	FT	1	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, EVENTOUT	-
90	A6	C7	134	A9	162	193	A9	PB4(NJT RST)	I/O	FT	i	NJTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, SPI2_NSS/I2S2_WS, EVENTOUT	-
91	C5	C8	135	A6	163	194	A8	PB5	I/O	FT	-	TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, FMC_SDCKE1, DCMI_D10, EVENTOUT	-
92	B5	A8	136	В6	164	195	В6	PB6	I/O	FT	-	TIM4_CH1, HDMI-CEC, I2C1_SCL, USART1_TX, CAN2_TX, QUADSPI_BK1_NCS, FMC_SDNE1, DCMI_D5, EVENTOUT	-
93	A5	В8	137	B5	165	196	B5	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, USART1_RX, FMC_NL, DCMI_VSYNC, EVENTOUT	-
94	D5	C9	138	D6	166	197	E6	воот	ı	В	-	-	VPP

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

		ı	Pin Nu	ımbeı	r								•
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
95	B4	A9	139	A5	167	198	A7	PB8	I/O	FT	1	TIM4_CH3, TIM10_CH1, I2C1_SCL, CAN1_RX, ETH_MII_TXD3, SDMMC1_D4, DCMI_D6, LCD_B6, EVENTOUT	-
96	A4	В9	140	B4	168	199	B4	PB9	I/O	FT	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, SDMMC1_D5, DCMI_D7, LCD_B7, EVENTOUT	-
97	D4	B10	141	A4	169	200	A6	PE0	I/O	FT	1	TIM4_ETR, LPTIM1_ETR, UART8_Rx, SAI2_MCK_A, FMC_NBL0, DCMI_D2, EVENTOUT	-
98	C4	A10	142	A3	170	201	A5	PE1	I/O	FT	1	LPTIM1_IN2, UART8_Tx, FMC_NBL1, DCMI_D3, EVENTOUT	-
99	E4	-	-	D5	-	202	F6	VSS	S	-	-	-	-
-	F7	A11	143	C6	171	203	E5	PDR_ON	S	-	-	-	-
100	F4	D7	144	C5	172	204	E7	VDD	S	-	-	-	-
-	-	-	-	D4	173	205	C3	PI4	I/O	FT	-	TIM8_BKIN, SAI2_MCK_A, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	-	-	C4	174	206	D3	PI5	I/O	FT	-	TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-



Pin Number Pin structure name Pin type Notes WLCSP143 **UFBGA176** FFBGA216 FFBGA100 Additional LQFP176 LQFP100 LQFP144 LQFP208 (function **Alternate functions functions** after reset)<sup>(1)</sup> 9 TIM8\_CH2, SAI2\_SD\_A, C3 175 207 D6 PI6 I/O FT FMC\_D28, DCMI\_D6, LCD\_B6, EVENTOUT TIM8 CH3, SAI2 FS A, FT FMC\_D29, DCMI\_D7, C2 176 208 D4 PI7 I/O LCD\_B7, EVENTOUT

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

- 1. Function availability depends on the chosen device.
- 2. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:
  - The speed should not exceed 2 MHz with a maximum load of 30 pF.
  - These I/Os must not be used as a current source (e.g. to drive an LED).
- Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F75xxx and STM32F74xxx reference manual.
- 4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
- If the device is delivered in an WLCSP143, UFBGA176, LQFP176, TFBGA100 or TFBGA216 package, and the BYPASS\_REG pin is set to VDD (Regulator OFF/internal reset ON mode), then PA0 is used as an internal Reset (active low).

	AF15	SYS	EVEN	EVEN	EVEN	EVEN	EVEN TOUT	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN
	AF14	LCD	LCD_R5	-	1	-	1	-	1	-	1	-	1	1	LCD_B6
	AF13	DСМІ	-	-	1	-	1	-	1	-	1	DCMI_D 10	DCMI_D 5	DCMI_V SYNC	DCMI_D 6
ed)	AF12	FMC/SD MMC1/O TG2_FS	1	-	-	-	-	-	-	-	-	FMC_SD CKE1	FMC_SD NE1	FMC_NL	SDMMC 1_D4
continu	AF11	ETH/ OTG1_FS	1	-			ETH_MII_ RXD2	ETH_MII_ RXD3	1	-		ETH_PPS _OUT		1	ETH_MII_ TXD3
Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)	AF10	SAIZ/QU ADSPI/O TG2_HS/ OTG1_FS	OTG_FS_ DP	-	-	-	OTG_HS_ ULPI_D1	OTG_HS_ ULPI_D2	-	-	-	OTG_HS_ ULPI_D7	QUADSPI _BK1_NC S	1	
nction m	AF9	CAN1/2/T IM12/13/ 14/QUAD SPI/LCD	CAN1_T	-	-	-	LCD_R3	PS_CD_R6	QUADSP I_CLK	-	-	CAN2_R X	CAN2_T X	1	CAN1_R X
nate fur	AF8	SAIZ/US ART6/UA RT4/5/7/8 /SPDIFR	SAIZ_FS _B	-		UART4_ RTS	UART4_ CTS	-						1	
3xx alter	AF7	SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX	USART1 _RTS	-		-	-	-	SPI3_MO SI/I2S3_ SD	-	SPI2_NS S/I2S2_ WS	-	USART1 _TX	USART1 _RX	-
<b>N32F74</b>	AF6	SPI3/ SAI1	1	-	-	SP13_NS S/12S3_ WS	-	-	SAI1_SD _A	SP13_SC K/12S3_ CK	SPI3_MI SO_	SPI3_M OSI/I2S3 _SD	-	-	-
and STI	AF5	SP11/2/3/ 4/5/6	ı	ı	ı	SPI1_NS S/I2S1_ WS	ı	-	ı	SP11_SC K/12S1_ CK	SPI1_MI SO	SPI1_M OSI/I2S1 _SD	ı	ı	1
F745xx	AF4	12C1/2/3/ 4/CEC	1	-		HDMI- CEC		-				I2C1_SM BA	12C1_SC	I2C1_SD A	I2C1_SC
. STM32	AF3	TIM8/9/10/ 11/LPTIM 1/CEC		-	1	-	TIM8_CH 2N	TIM8_CH 3N	1	-	1	-	HDMI- CEC	1	TIM10_C H1
rable 12	AF2	TIM3/4/5	1	-	-	-	TIM3_C H3	TIM3_C H4	-	-	TIM3_C H1	TIM3_C H2	TIM4_C H1	TIM4_C H2	TIM4_C H3
	AF1	TIM1/2	TIM1_ET R	-	1	TIM2_C H1/TIM2 _ETR	TIM1_C H2N	TIM1_C H3N	1	TIM2_C H2_	1	-	-	1	-
	AF0	SYS	,	JTMS- SWDIO	JTCK- SWCLK	JTDI	ı	1	1	JTDO/T RACES WO	NJTRST	1	1	1	1
		Port	PA12	PA13	PA14	PA15	PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB7	PB8
		Ğ			Port A			_			Port B			_	



AF15 EVEN TOUT SYS LCD\_R5 8 G5 B7 **AF14** CO CD CO CO DCMI\_D AF13 DCMI FMC/SD MMC1/O TG2 FS OTG\_HS \_ID\_ OTG\_HS\_DP FMC\_SD NE0 FMC\_SD CKE0 SDMMC 1\_D5 OTG\_HS \_DM FMC\_SD NWE AF12 Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued) ETH/ OTG1\_FS ETH MII TX\_EN/E TH\_RMII\_ TX\_EN ETH\_MII\_ TXD0/ET H\_RMII\_T XD0 ETH\_MII\_ TXD1/ET H\_RMII\_T XD1 ETH\_MII\_ TX\_CLK ETH\_MD C ETH\_MII\_ TXD2 ETH\_MII\_ RX\_ER\_ **AF11** OTG\_HS\_ ULPI\_NX\_ SAIZ/QU ADSPI/O TG2\_HS/ OTG1\_FS OTG\_HS\_ ULPI\_DIR OTG\_HS\_ ULPI\_D3 OTG\_HS\_ ULPI\_D4 OTG\_HS\_ ULPI\_D5 OTG\_HS\_ ULPI\_D6 OTG\_HS\_ ULPI\_ST\_ P AF10 CAN1/2/T IM12/13/ 14/QUAD SPI/LCD CAN2\_R X CAN2\_T X TIM12\_C H2\_ TIM12\_C H1 CAN1\_T AF9 SAIZ/US ART6/UA RT4/5/7/8 /SPDIFR X SAIZ\_FS \_B AF8 SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX USART3 \_CTS USART3 \_TX USART3 \_RX USART3 \_CK USART3 \_RTS SAI1\_SD \_A SPI3/ SAI1 AF6 SPI2\_NS S/I2S2\_ WS SPI2\_NS S/I2S2\_ WS SPI2\_M OSI/I2S2 \_SD SPI2\_M OSI/I2S2 \_SD SPI2\_SC K/I2S2\_ CK SPI2\_SC K/I2S2\_ CK SPI2\_M OSI/I2S2 \_SD SPI1/2/3/ 4/5/6 SPI2\_MI SO SPI2\_MI SO AF5 I2C2\_SM BA 12C1/2/3/ 4/CEC I2C2\_SC L I2C1\_SD A I2C2\_SD A\_ AF4 TIM8/9/10/ 11/LPTIM 1/CEC TIM11\_CH TIM8\_CH 3N TIM8\_CH 2N AF3 TIM3/4/5 TIM4\_C H4\_C AF2 TIM2\_C H3 TIM2\_C H4\_ TIM1\_C H1N TIM1\_C H2N TIM1\_C H3N TIM1 KIN\_B TIM1/2 AF1 RTC\_R EFIN TRACE D0 PB10 PB13 PB12 PB14 2 PB11 PC2 PB9 PC0 PC РСЗ PB1 Port Port B Port C

	AF15	SYS	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN
	AF14	LCD	1	-	LCD_HS YNC	PO_GC	-	-	LCD_R2	-	-	-	-	-
	AF13	DCMI	1	1	DCMI_D 0	DCMI_D	DCMI_D	DCMI_D	DCMI_D 8	DCMI_D	DCMI_D	1	1	-
ed)	AF12	FMC/SD MMC1/O TG2_FS	FMC_SD NE0	FMC_SD CKE0	SDMMC 1_D6	SDMMC 1_D7	SDMMC 1_D0	SDMMC 1_D1	SDMMC 1_D2	SDMMC 1_D3	SDMMC 1_CK	1	1	-
continu	AF11	ETH/ OTG1_FS	ETH_MII_ RXD0/ET_ H_RMII_ RXD0	ETH_MII_ RXD1/ET_ H_RMII_ RXD1	-	-	-	-	-	-	-	-	-	-
M32F745xx and STM32F746xx alternate function mapping (continued)	AF10	SAIZ/QU ADSPI/O TG2_HS/ OTG1_FS		-	-	-	-	-	-	-	-	-	-	-
nction m	AF9	CAN1/2/T IM12/13/ 14/QUAD SPI/LCD	-	-	-	-	-	QUADSP I_BK1_IO 0	QUADSP I_BK1_IO 1	QUADSP I_BK2_N CS	-	-	-	-
nate fur	AF8	SAIZ/US ART6/UA RT4/5/7/8 /SPDIFR X	SPDIFRX _IN2	SPDIFRX _IN3	USART6 _TX	USART6 _RX	USART6 _CK	-	UART4_T X	UART4_ RX	UART5_T X	-	-	-
6xx alter	AF7	SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX	-	-	-	-	UART5_ RTS	UART5_ CTS	USART3 _TX	USART3 _RX	USART3 _CK	-	-	-
<b>132F74</b> (	AF6	SPI3/ SAI1	-	-	-	12S3_M CK	-	-	SP13_SC K/12S3_ CK	SPI3_MI	SPI3_M OSI/I2S3 _SD	-	-	-
and STI	AF5	SP11/2/3/ 4/5/6	12S1_M CK	ı	12S2_M CK	ı	ı	I2S_CKI	ı	ı	ı	1	ı	1
F745xx	AF4	12C1/2/3/ 4/CEC	1	-	-	-	ı	I2C3_SD A	-	1	-	-	1	-
. STM32	AF3	TIM8/9/10/ 11/LPTIM 1/CEC			TIM8_CH	TIM8_ CH2_	TIM8_ CH3_	TIM8_ CH4						
Table 12. ST	AF2	TIM3/4/5			TIM3_C H1	TIM3_C H2	TIM3_C H3	TIM3_C H4		1		-	-	1
•	AF1	TIM1/2		-	-	ı	ı	1	1	1	1	-	1	-
	AF0	SYS	ı	ı	ı	1	TRACE D1	MCO2	1	1	TRACE D3	-	ı	1
		Port	PC4	PC5	PC6	PC7	PC8	PC9	PC10	PC11	PC12	PC13	PC14	PC15
		<u>.</u>						Port C						



AF15 EVEN TOUT EVEN EVEN TOUT EVEN TOUT EVEN TOUT EVEN TOUT EVEN TOUT EVEN TOUT EVEN EVEN TOUT EVEN TOUT EVEN TOUT EVEN TOUT EVEN TOUT SYS G7 B2 83 **AF14** CO LCD\_I CCD 0 DCMI\_D DCMI\_D DCMI\_D AF13 DCMI FMC/SD MMC1/O TG2 FS FMC\_CL K\_CL SDMMC 1\_CMD FMC\_N WAIT FMC\_D3 FMC\_N OE FMC\_N WE\_N FMC\_D1 FMC\_D1 FMC\_D1 FMC\_A1 6/FMC\_ CLE FMC\_A1 7/FMC\_ ALE FMC\_A1 FMC\_NE FMC\_D2 AF12 Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued) ETH/ OTG1\_FS **AF11** SAIZ/QU ADSPI/O TG2\_HS/ OTG1\_FS SAI2\_SD\_ A SAIZ\_FS\_ A SAI2\_SC K\_A AF10 CAN1/2/T IM12/13/ 14/QUAD SPI/LCD QUADSP I\_BK1\_IO 0 QUADSP I\_BK1\_IO QUADSP I\_BK1\_IO 3 CAN1\_R X CAN1\_T X AF9 SAIZ/US ART6/UA RT4/5/7/8 /SPDIFR X SPDIFRX \_IN0 SPDIFRX \_IN1 UART5\_ RX AF8 SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX USART2 \_RTS USART2 \_TX USART2 \_RX USART2 \_CK USART3 \_TX USART3 \_RX USART3 \_CK USART3 \_CTS USART3 \_RTS USART2 \_CTS SAI1\_SD \_A SPI3/ SAI1 AF6 SPI3\_M OSI/I2S3 \_SD SPI2\_SC K/I2S2\_ CK SPI1/2/3/ 4/5/6 AF5 12C1/2/3/ 4/CEC I2C4\_SM BA I2C4\_SD A I2C4\_SC L AF4 TIM8/9/10/ 11/LPTIM 1/CEC LPTIM1\_I N1 LPTIM1\_ OUT AF3 TIM3\_ET R TIM3/4/5 AF2 TIM4 TIM4 HZ TIM1/2 AF1 TRACE D2 PD10 PD13 PD12 PD11 PD2 PD0 PD1 PD3 PD4 PD5 PD7 PD8 PD9 Port Port D

	AF15	SYS	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN
	AF14	LCD	-	1	1	1	1	1	LCD_B0	LCD_G0	LCD_G1	1	-	-	-	rop_G3	LCD_B4	TCD_DE
•	AF13	DCMI	1	1	DCMI_D	DCMI_D	1	1	DCMI_D	DCMI_D 6	DCMI_D	1	1	1	1	1	1	ı
(pe	AF12	FMC/SD MMC1/O TG2_FS	FMC_D0	FMC_D1	FMC_NB L0	FMC_NB L1	FMC_A2	FMC_A1	FMC_A2	FMC_A2	FMC_A2	FMC_D4	FMC_D5	FMC_D6	FMC_D7	FMC_D8	FMC_D9	FMC_D1
continu	AF11	ETH/ OTG1_FS		ı	ı	1	ETH_MII_ TXD3	1	ı	1	ı	ı	ı	ı	ı	1	ı	1
M32F745xx and STM32F746xx alternate function mapping (continued)	AF10	SAIZ/QU ADSPI/O TG2_HS/ OTG1_FS	1	1	SAIZ_MC K_A	1	1	1	ı	1	SAIZ_MC K_B	QUADSPI _BK2_IO0	QUADSPI _BK2_I01	QUADSPI _BK2_102	QUADSPI _BK2_IO3	SAIZ_SD_	SAIZ_SC K_B	SAI2_FS_ B
nction m	AF9	CAN1/2/T IM12/13/ 14/QUAD SPI/LCD	•	ı	ı	1	QUADSP I_BK1_IO 2	1	ı	1	•	ı	ı	•	ı		ı	1
nate fur	AF8	SAIZ/US ART6/UA RT4/5/7/8 /SPDIFR X	UART8_ CTS	UART8_ RTS	UART8_ Rx	UART8_T x	1	1	1	1	1	UART7_ Rx	UART7_T x	UART7_ RTS	UART7_ CTS	1	1	1
3xx alter	AF7	SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX	-	-	1	1	1	1	1	1	-	1	-	-	-	-	-	-
<b>132F74</b> (	AF6	SPI3/ SAI1	-	1	1	1	SAI1_M CLK_A	SAI1_SD _B	SAI1_FS	SAI1_SC K_A	SAI1_SD	1	-	-	-	-	1	-
and STI	AF5	SP11/2/3/ 4/5/6	-	-	-	-	SPI4_SC K	-	SPI4_NS	SPI4_MI SO	SPI4_M OSI	-	-	-	-	SP14_NS S	SPI4_SC K	SPI4_MI SO
F745xx	AF4	12C1/2/3/ 4/CEC	1	1	1	1	1	1	,	1	1	1	1	1	1	1	1	,
. STM32	AF3	TIM8/9/10/ 11/LPTIM 1/CEC	,	1	LPTIM1_E TR	LPTIM1_I N2	1	1	ı	TIM9_CH	TIM9_CH	1	1		ı		1	1
Table 12. STI	AF2	TIM3/4/5	TIM4_C H3	TIM4_C H4	TIM4_ET	1	1	1	1	1	1	1	1	1	1	-	1	1
	AF1	TIM1/2	-	1	1	1	1	1	1	1	TIM1_B KINZ	TIM1_ET	TIM1_C H1N	TIM1_C H1	TIM1_C H2N	TIM1_C H2	TIM1_C H3N	TIM1_C H3
•	AF0	SYS	1	1			TRACE	TRACE D0	TRACE D1	TRACE D2	TRACE D3		1	1	1	1	1	
•		Port	PD14	PD15	PE0	PE1	PE2	PE3	PE4	PE5	PE6	PE7	PE8	PE9	PE10	PE11	PE12	PE13
		<u>a</u>	1	<u> </u>							Port E							



AF15 EVEN TOUT EVEN EVEN TOUT EVEN TOUT EVEN TOUT EVEN TOUT EVEN TOUT EVEN TOUT EVEN EVEN TOUT EVEN EVEN TOUT EVEN TOUT EVEN EVEN TOUT SYS LCD\_CL K LCD\_R7 핌 **AF14** CO CCD DCMI\_D DCMI\_D 12 DCMI FMC/SD MMC1/O TG2 FS FMC\_SD NRAS FMC\_A5 FMC\_A0 FMC\_D1 FMC\_D1 FMC\_A1 FMC\_A6 FMC\_A3 FMC\_A4 AF12 Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued) ETH/ OTG1\_FS **AF11** SAIZ/QU ADSPI/O TG2\_HS/ OTG1\_FS QUADSPI \_BK1\_I00  $\begin{array}{c} \text{SAI2\_SD\_} \\ \overline{\text{B}} \end{array}$ SAIZ\_MC K\_B QUADSPI \_BK1\_I01 AF10 CAN1/2/T IM12/13/ 14/QUAD SPI/LCD QUADSP I\_BK1\_IO 3 QUADSP I\_BK1\_IO 2 TIM13\_C H1 TIM14\_C H1 AF9 SAI2/US ART6/UA RT4/5/7/8 /SPDIFR X UART7\_ UART7\_T X UART7\_ RTS UART7\_ CTS AF8 SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX SAI1\_SD \_B SAI1\_SC K\_B SAI1\_M CLK\_B SAI1\_FS \_B SPI3/ SAI1 AF6 SPI5\_NS S SPI5\_SC K SPI5\_MI SO SPI1/2/3/ 4/5/6 SPI4\_M OSI SPI5\_M OSI SPI5\_M OSI AF5 12C1/2/3/ 4/CEC I2C2\_SM BA SD 12C2\_SC AF4 12C2\_ A\_ TIM8/9/10/ 11/LPTIM 1/CEC TIM11\_CH TIM10\_C H1 TIM3/4/5 AF2 TIM1\_C H4\_ TIM1\_B KIN\_B TIM1/2 AF1 PE14 PF12 PF10 PF11 PF5 PF6 PF8 PF9 PF0 PF2 PF3 PF4 PF7 F <u>H</u> Port Port F Port E

	AF15	SYS	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN
	AF14	ГСБ	1	1	1	1	1	1	1	1	1	LCD_R7	K LCD_CL	1	1	LCD_B2
	AF13	DCMI	-	-	1	-	-	-	-	-	1	DCMI_D 12	DCMI_D	-	DCMI_V SYNC	DCMI_D 2
ed)	AF12	FMC/SD MMC1/O TG2_FS	FMC_A7	FMC_A8	FMC_A9	FMC_A1	FMC_A1	FMC_A1	FMC_A1	FMC_A1 4/FMC_ BA0_	FMC_A1 5/FMC_ BA1	1	FMC_IN T	FMC_SD CLK	FMC_NE 2/FMC_ NCE	FMC_NE
continu	AF11	ETH/ OTG1_FS	1			-			-			1		ETH_PPS _OUT		
M32F745xx and STM32F746xx alternate function mapping (continued)	AF10	SAIZ/QU ADSPI/O TG2_HS/ OTG1_FS	-	-	-	-	-	-	-	-		1	-	-	SAI2_FS_ B	SAIZ_SD_
nction m	AF9	CAN1/2/T IM12/13/ 14/QUAD SPI/LCD	1	-	-	-	-	-	-	-	-	1	-	-	QUADSP I_BK2_IO 2	LCD_G3
nate fur	AF8	SAI2/US ART6/UA RT4/5/7/8 /SPDIFR X	-	-	-	-	-	-	-	-		1	USART6 _CK	USART6 _RTS	USART6 _RX	1
6xx alter	AF7	SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX	-	-	-	-	-	-	-			1	-	SPDIFRX _IN2	SPDIFRX _IN3	1
132F74	AF6	SPI3/ SAI1		1	1	-	1	1	•	1	1		1		ı	
and STN	AF5	SP11/2/3/ 4/5/6	1	-	1	-	-	-	-	-	1	1	-	SPI6_NS	1	1
F745xx	AF4	12C1/2/3/ 4/CEC	I2C4_SM BA	12C4_SC L	12C4_SD A	-	-	-	-	-	-	1	-	-	-	1
ST	AF3	TIM8/9/10/ 11/LPTIM 1/CEC	1	-	-	-	-	-	-	-	-	1	-	-	1	1
Table 12.	AF2	TIM3/4/5	1	1	1	-	1	1	-	1	1	1	1	-	1	1
	AF1	TIM1/2	ı	-	-	-	-	-	-	-	-	ı	-	-	-	1
	AF0	SYS	-	-	-	-	-	-	-	-	-	1	-	-	-	
•		Port	PF13	PF14	PF15	PG0	PG1	PG2	PG3	PG4	PG5	PG6	PG7	PG8	PG9	PG10
		<b>₫</b>		Port F							Port G					



AF15 EVEN TOUT EVEN EVEN EVEN EVEN TOUT EVEN TOUT EVEN TOUT SYS R0 R0 LCD\_R1 B3 В LCD B0 **AF14** CO CD CD CD CD DCMI\_D 8 DCMI\_D DCMI\_D 13 DCMI\_D AF13 DCMI FMC/SD MMC1/O TG2 FS FMC\_SD NE1 FMC\_SD CKE1 FMC\_A2 FMC\_A2 5 FMC\_SD NCAS FMC\_SD CKE0 FMC\_SD NE0 FMC\_SD NWE FMC\_NE AF12 Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued) ETH/ OTG1\_FS ETH MII TX\_EN/E TH\_RMII TX\_EN ETH\_MII\_ TXD0/ET H\_RMII\_T XD0 ETH\_MII\_ TXD1/ET H\_RMII\_T XD1 ETH\_MII\_ CRS\_ ETH\_MII\_ COL ETH\_MII\_ RXD3\_ ETH\_MII\_ RXD2 **AF11** SAIZ/QU ADSPI/O TG2\_HS/ OTG1\_FS SAIZ\_MC K\_B SAIZ\_SC K\_B OTG\_HS\_ ULPI\_NX\_ AF10 CAN1/2/T IM12/13/ 14/QUAD SPI/LCD QUADSP I\_BK2\_IO 3 QUADSP I\_BK2\_IO 0 QUADSP I\_BK2\_IO TIM12\_C H1 B4 AF9 2 SAI2/US ART6/UA RT4/5/7/8 /SPDIFR X USART6 \_RTS USART6 \_CTS USART6 \_TX USART6 \_CTS AF8 SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX SPDIFRX \_IN1 SPDIFRX \_IN0 SPI3/ SAI1 AF6 SPI6\_SC K SPI5\_NS S SPI1/2/3/ 4/5/6 SPI5\_SC K SPI6\_M OSI SPI6\_MI SO SPI5\_MI SO AF5 I2C2\_SM BA 12C1/2/3/ 4/CEC I2C2\_SD A 12C3\_SC L ISC2\_SC AF4 TIM8/9/10/ 11/LPTIM 1/CEC LPTIM1\_E TR LPTIM1\_I N2 LPTIM1\_I N1 LPTIM1\_ OUT TIM3/4/5 AF2 TIM1/2 AF1 TRACE D0 TRACE D1 PG12 PG13 PG15 PG11 H PH1 PH2 PH3 PH5 PH6 PH7 PT4 Port Port G Port H

	AF15	SYS	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN
	AF14	LCD	LCD_R2	LCD_R3	LCD_R4	LCD_R5	LCD_R6	LCD_G2	LCD_G3	LCD_G4	LCD_G5	PD_GG	LCD_G7	1	LCD_B4	LCD_B5	PG_B6
-	AF13	рсмі	DCMI_H SYNC	DCMI_D 0	DCMI_D	DCMI_D	DCMI_D	ı	DCMI_D	DCMI_D 11	DCMI_D 13	DCMI_D 8	DCMI_D	DCMI_D 10	DCMI_D	DCMI_V SYNC	DCMI_D 6
(pa	AF12	FMC/SD MMC1/O TG2_FS	FMC_D1	FMC_D1	FMC_D1	FMC_D1	FMC_D2	FMC_D2	FMC_D2	FMC_D2	FMC_D2	FMC_D2	FMC_D2	FMC_D2	FMC_NB L2	FMC_NB L3	FMC_D2
continu	AF11	ETH/ OTG1_FS	ı	ı	1	1	ı	ı	1	-	-	1	-	1	1	ı	-
M32F745xx and STM32F746xx alternate function mapping (continued)	AF10	SAIZ/QU ADSPI/O TG2_HS/ OTG1_FS	1	1	,	1	1	1	1	-	-	1	-	1	SAI2_MC K_A	SAIZ_SC K_A	SAIZ_SD_
nction m	AF9	CAN1/2/T IM12/13/ 14/QUAD SPI/LCD	-	TIM12_C H2	1	1	-	CAN1_T	-	-	-	1	-	-	-	-	-
nate fur	AF8	SAIZ/US ART6/UA RT4/5/7/8 /SPDIFR X	-	-	1	1	-	-	-	-	-		-	-	-	-	-
oxx alter	AF7	SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX	-	-	-	1	-	-	-	-	-		-	-	-	-	-
<b>1</b> 32F74	AF6	SPI3/ SAI1	1	1	1	1		-		-			-			1	1
and STI	AF5	SP11/2/3/ 4/5/6	-	-	-	-	-	-	-	-	SPI2_NS S/12S2_ WS	SPI2_SC KI2S2_ CK	SPI2_MI SO	SPI2_M OSI/I2S2 _SD	-	-	-
F745xx	AF4	12C1/2/3/ 4/CEC	12C3_SD A	I2C3_SM BA	I2C4_SM BA	12C4_SC L	12C4_SD A	-	-	-	-	1	-	-	-	-	-
. STM32	AF3	TIM8/9/10/ 11/LPTIM 1/CEC	1	ı	ı	1	ı	TIM8_CH 1N	TIM8_CH 2N	TIM8_CH 3N	-	TIM8_BKI N2	TIM8_CH	TIM8_ET R	TIM8_BKI	TIM8_CH	TIM8_CH
Table 12. ST	AF2	TIM3/4/5	ı	ı	TIM5_C H1	TIM5_C H2	TIM5_C H3_	ı	1	1	TIM5_C H4	1	-	1	1	ı	-
	AF1	TIM1/2	-	-	1	-	-	-	-	-	-	1	-	-	-	-	-
	AF0	SYS	ı	ı	ı	ı	-	-	1	-	1	1	1	ı	1	-	-
		Port	PH8	РН9	PH10	PH11	PH12	PH13	PH14	PH15	PIO	PI L	PI2	PI3	PI4	PI5	PI6
	<u> </u>		Port H								Port						



AF15 EVEN TOUT EVEN EVEN TOUT EVEN EVEN EVEN TOUT EVEN EVEN TOUT EVEN EVEN TOUT EVEN EVEN EVEN TOUT EVEN EVEN EVEN SYS LCD\_HS YNC LCD\_HS YNC LCD\_VS YNC LCD\_VS YNC LCD\_CL K LCD\_R2 LCD\_R3 LCD\_R6 LCD\_R0 LCD\_R1 <sub>7</sub> R5 R7 B7 **AF14** 5 LCD\_E LCD CD CD DCMI\_D DCMI FMC/SD MMC1/O TG2 FS FMC\_D2 FMC\_D3 FMC\_D3 AF12 Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued) ETH/ OTG1\_FS ETH\_MII\_ RX\_ER\_ **AF11** SAIZ/QU ADSPI/O TG2\_HS/ OTG1\_FS SAIZ\_FS\_ A OTG\_HS\_ ULPI\_DIR AF10 CAN1/2/T IM12/13/ 14/QUAD SPI/LCD CAN1\_R X AF9 SAI2/US ART6/UA RT4/5/7/8 /SPDIFR X AF8 SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX AF6 SPI3/ SAI1 SP11/2/3/ 4/5/6 AF5 12C1/2/3/ 4/CEC AF4 TIM8/9/10/ 11/LPTIM 1/CEC TIM8\_CH TIM3/4/5 AF2 TIM1/2 AF1 P110 P113 P114 P115 P112 5 PJ2 PJ3 PJ6 <u>B</u> PI9 P11 PI7 Port Port J Port

**577** 

AF15 EVEN TOUT EVEN EVEN EVEN EVEN EVEN EVEN EVEN TOUT EVEN SYS LCD\_G0 9 G2 63 B2 83 ٦ 8 8 AF14 CO LCD CO CD LCD CCD CCD LCD\_ CD DCMI FMC/SD MMC1/O TG2 FS AF12 Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued) ETH/ OTG1\_FS **AF11** SAIZ/QU ADSPI/O TG2\_HS/ OTG1\_FS CAN1/2/T IM12/13/ 14/QUAD SPI/LCD AF9 SAIZ/US ART6/UA RT4/5/7/8 /SPDIFR X AF8 SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX AF6 SPI3/ SAI1 SP11/2/3/ 4/5/6 AF5 12C1/2/3/ 4/CEC AF4 TIM8/9/10/ 11/LPTIM 1/CEC TIM3/4/5 AF2 TIM1/2 AF1 PJ14 P.11 PJ7 Port Port J



	AF15	SYS	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	EVEN	
	AF14	ГСБ	59_G51	95 <sup>-</sup> G27	LCD_G7	LCD_B4	LCD_B5	PB_DCD_B6	LCD_B7	LCD_DE	
	AF13	рсмі	-	-	-	-	-	-	-	-	
ed)	AF12	L ≥ ⊢		ı	-	-	-	-	-	1	
continu	AF11	ETH/ OTG1_FS	,		-	-	-	-	-		
M32F745xx and STM32F746xx alternate function mapping (continued)	AF10	SAI2/QU ADSPI/O TG2_HS/ OTG1_FS	ı	ı	-	-	-	-	-	-	
nction m	AF9	CAN1/2/T IM12/13/ 14/QUAD SPI/LCD	-	-	-	-	-	-	-	-	
nate fur	AF8	SAIZ/US ART6/UA RT4/5/7/8 /SPDIFR X	ı	1	-	-	-	-	-	-	
3xx alter	AF7	SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX		1	-	-	-	-	-	-	
<b>132F74</b> (	AF6	SPI3/ SAI1	-	-	-	-	-	-	-	-	
and STI	AF5	SP11/2/3/ 4/5/6	ı	ı	1	-	-	-	-	1	
F745xx	AF4	12C1/2/3/ 4/CEC			-	-	-	-	-		
	AF3	TIM8/9/10/ 11/LPTIM 1/CEC		1	-	-	-	-	-	-	
Table 12. STI	AF2	TIM3/4/5	-	-	-	-	-	-	-		
•	AF1	TIM1/2	ı	1	1	-	1	-	1	•	
	AF0	SYS	ı	1	1	1	1	1	-	1	
		Port	PK0	PK1	PK2	PK3	PK4	PK5	PK6	PK7	
		ď	Port K								

The 8 requests from the peripherals (such as TIM, ADC, SPI, I2C) are independently connected to each channel and their connection depends on the product implementation.

Table 24 and Table 25 give examples of DMA request mappings.

Table 24. DMA1 request mapping

				•	- 11 5			
Peripheral requests	Stream 0	Stream 1	Stream 2	Stream 3	Stream 4	Stream 5	Stream 6	Stream 7
Channel 0	SPI3_RX	SPDIFRX_DT	SPI3_RX	SPI2_RX	SPI2_TX	SPI3_TX	SPDIFRX_CS	SPI3_TX
Channel 1	I2C1_RX	I2C3_RX	TIM7_UP	-	TIM7_UP	I2C1_RX	I2C1_TX	I2C1_TX
Channel 2	TIM4_CH1	-	I2C4_RX	TIM4_CH2	-	I2C4_RX	TIM4_UP	TIM4_CH3
Channel 3	-	TIM2_UP TIM2_CH3	I2C3_RX	-	I2C3_TX	TIM2_CH1	TIM2_CH2 TIM2_CH4	TIM2_UP TIM2_CH4
Channel 4	UART5_RX	USART3_RX	UART4_RX	USART3_TX	UART4_TX	USART2_RX	USART2_TX	UART5_TX
Channel 5	UART8_TX	UART7_TX	TIM3_CH4 TIM3_UP	UART7_RX	TIM3_CH1 TIM3_TRIG	TIM3_CH2	UART8_RX	TIM3_CH3
Channel 6	TIM5_CH3 TIM5_UP	TIM5_CH4 TIM5_TRIG	TIM5_CH1	TIM5_CH4 TIM5_TRIG	TIM5_CH2	-	TIM5_UP	-
Channel 7		TIM6_UP	I2C2_RX	I2C2_RX	USART3_TX	DAC1	DAC2	I2C2_TX

## Table 25. DMA2 request mapping

Peripheral requests	Stream 0	Stream 1	Stream 2	Stream 3	Stream 4	Stream 5	Stream 6	Stream 7		
Channel 0	ADC1	SAI1_A	TIM8_CH1 TIM8_CH2 TIM8_CH3	SAI1_A	ADC1	SAI1_B	TIM1_CH1 TIM1_CH2 TIM1_CH3	SAI2_B		
Channel 1	=	DCMI	ADC2	ADC2	SAI1_B	SPI6_TX	SPI6_RX	DCMI		
Channel 2	ADC3	ADC3	-	SPI5_RX	SPI5_TX	CRYP_OUT	CRYP_IN	HASH_IN		
Channel 3	SPI1_RX	-	SPI1_RX	SPI1_TX	SAI2_A	SPI1_TX	SAI2_B	QUADSPI		
Channel 4	SPI4_RX	SPI4_TX	USART1_RX	SDMMC1	-	USART1_RX	SDMMC1	USART1_TX		
Channel 5	-	USART6_RX	USART6_RX	SPI4_RX	SPI4_TX	-	USART6_TX	USART6_TX		
Channel 6	TIM1_TRIG	TIM1_CH1	TIM1_CH2	TIM1_CH1	TIM1_CH4 TIM1_TRIG TIM1_COM	TIM1_UP	TIM1_CH3	-		
Channel 7	-	TIM8_UP	TIM8_CH1	TIM8_CH2	TIM8_CH3	SPI5_RX	SPI5_TX	TIM8_CH4 TIM8_TRIG TIM8_COM		

