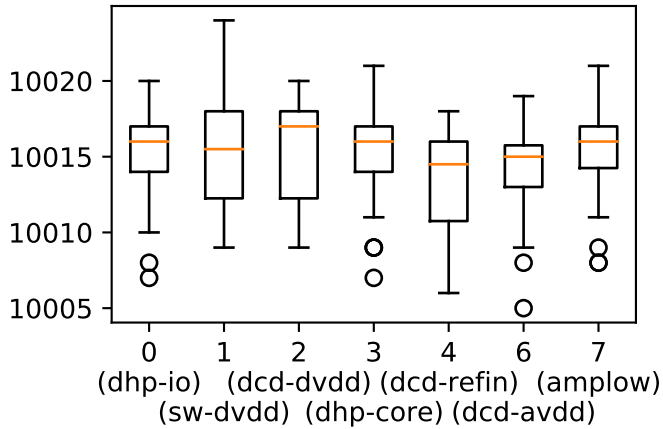
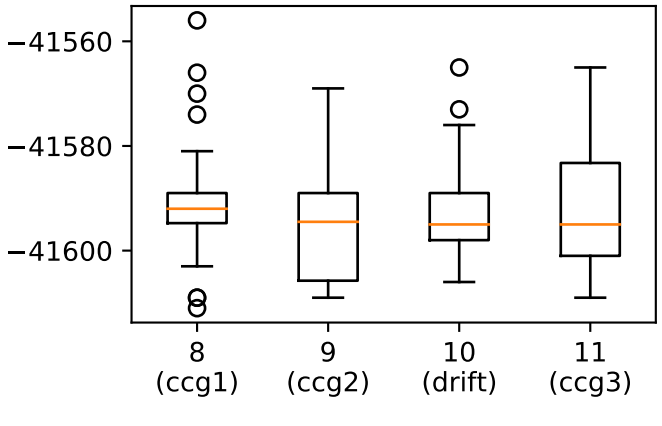
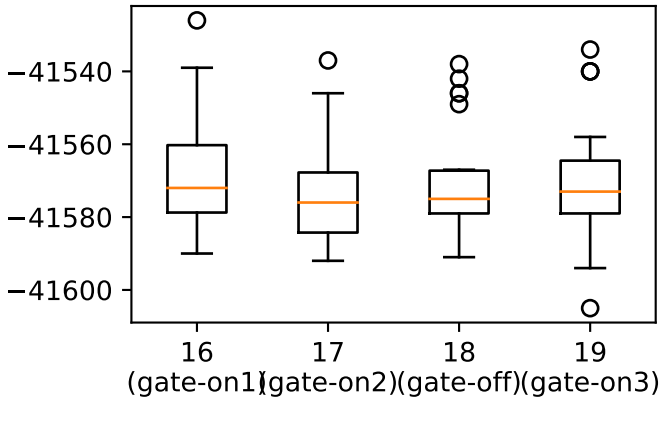
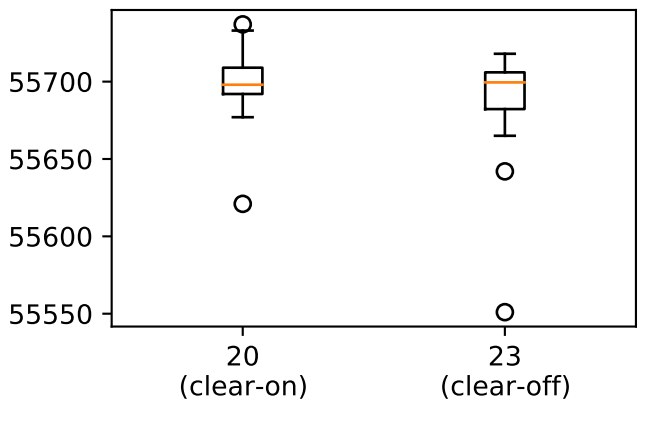
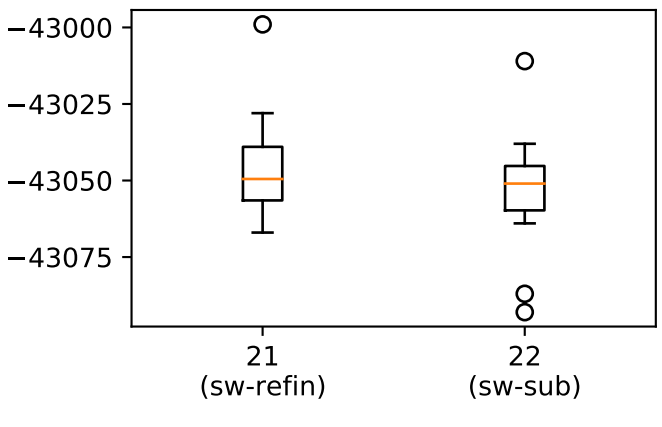
DAC VOLTAGE GAIN

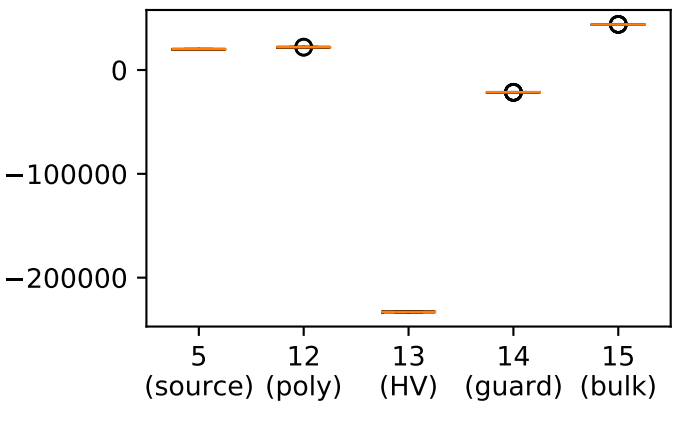




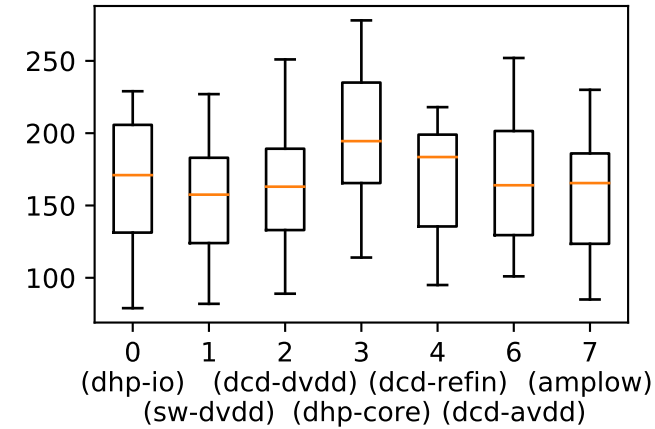


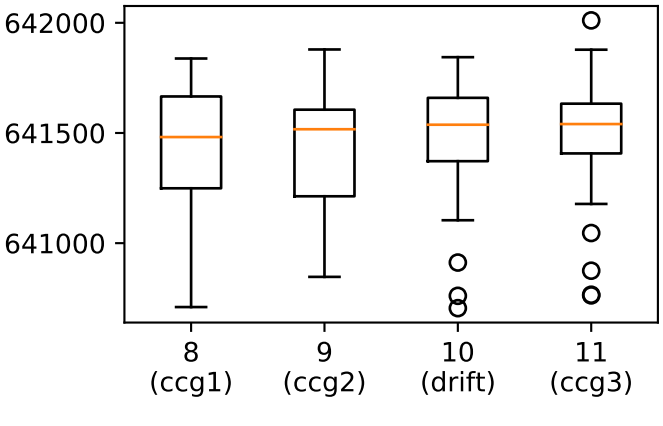


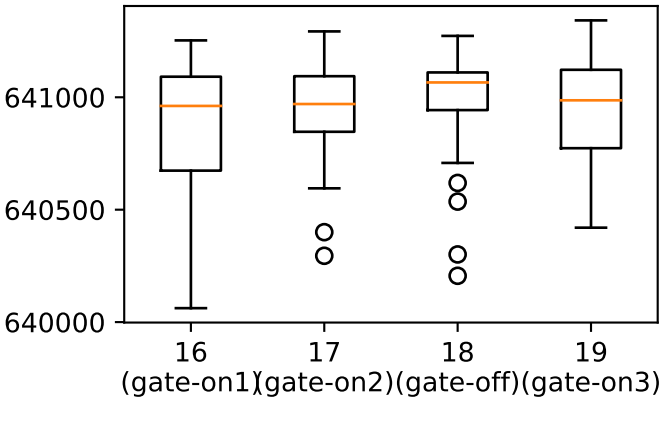


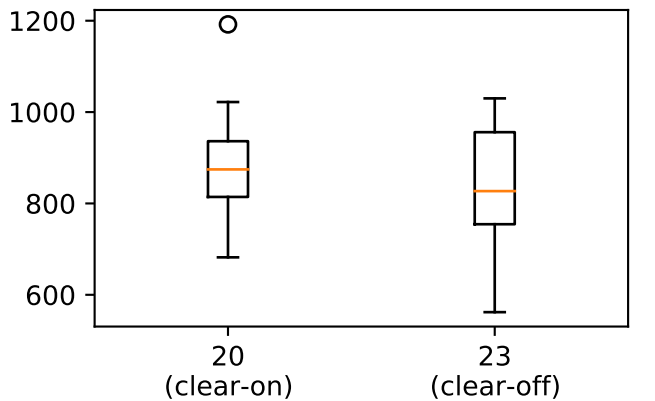


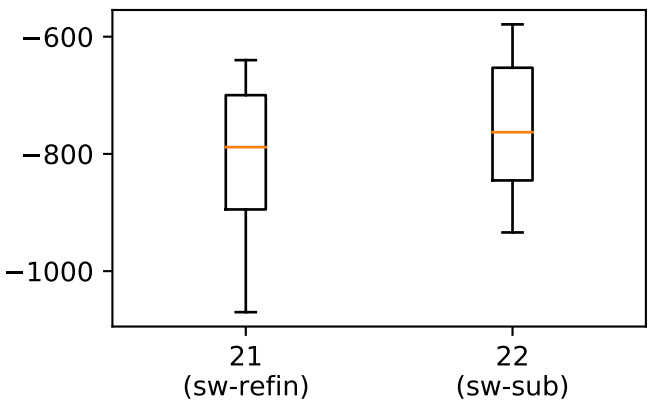
DAC VOLTAGE OFFSET

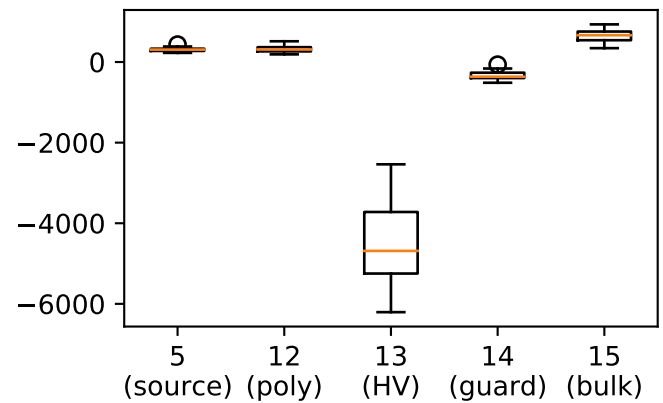


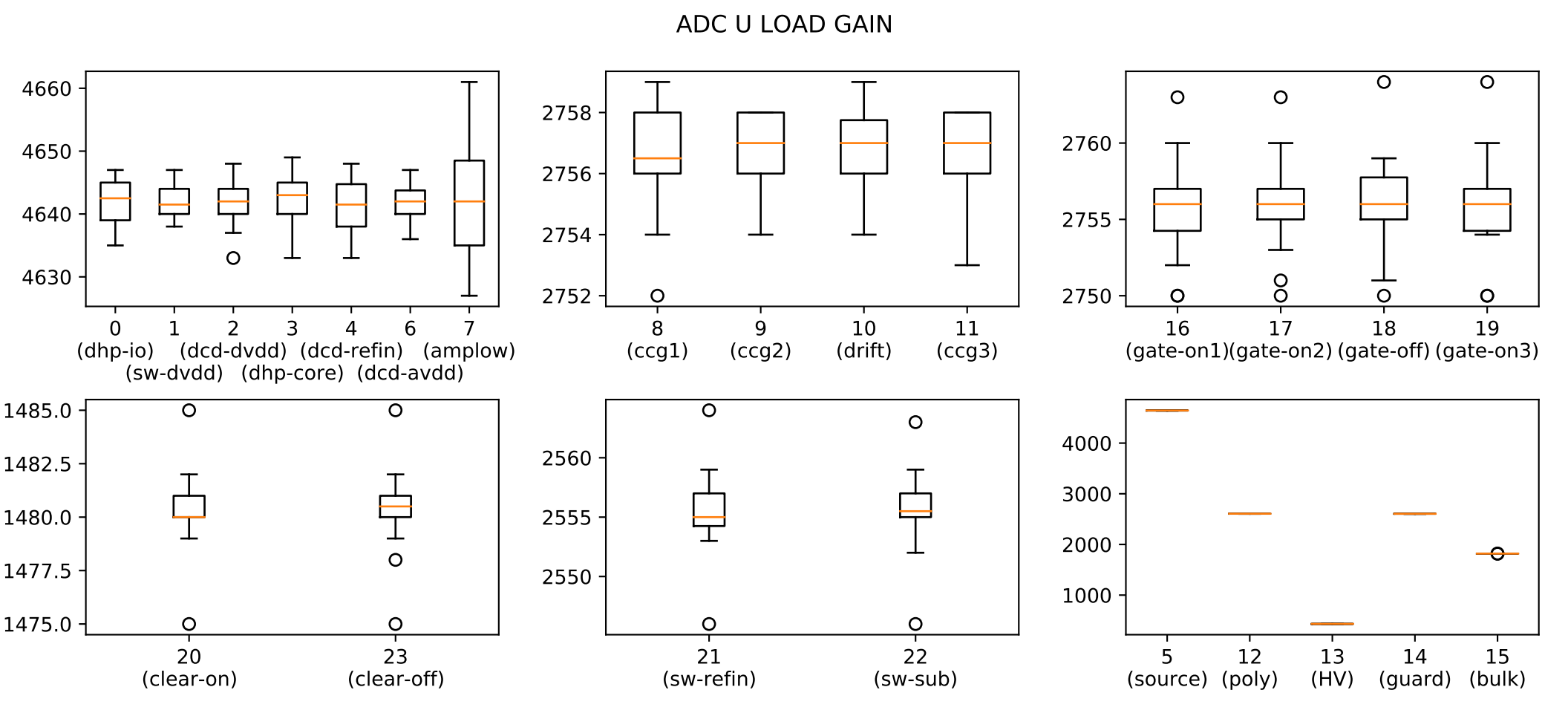


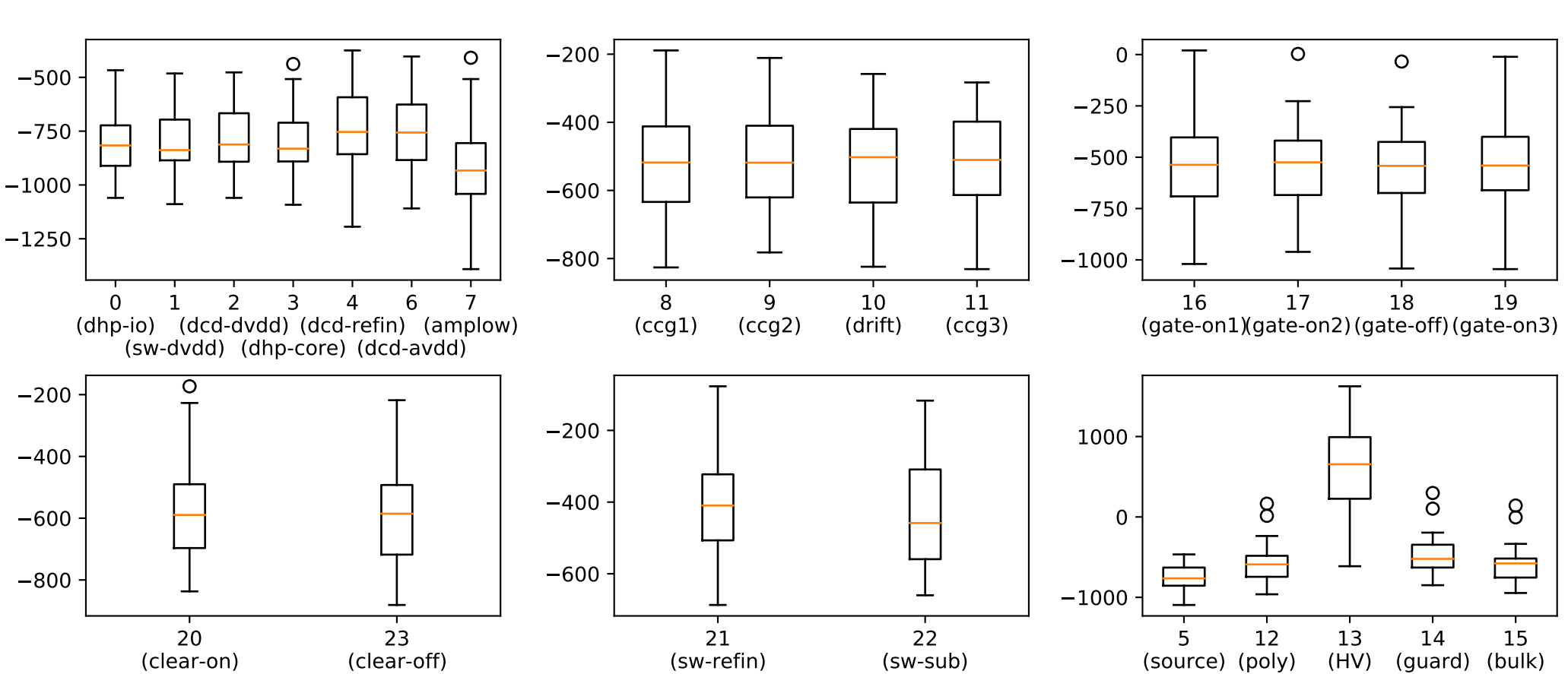




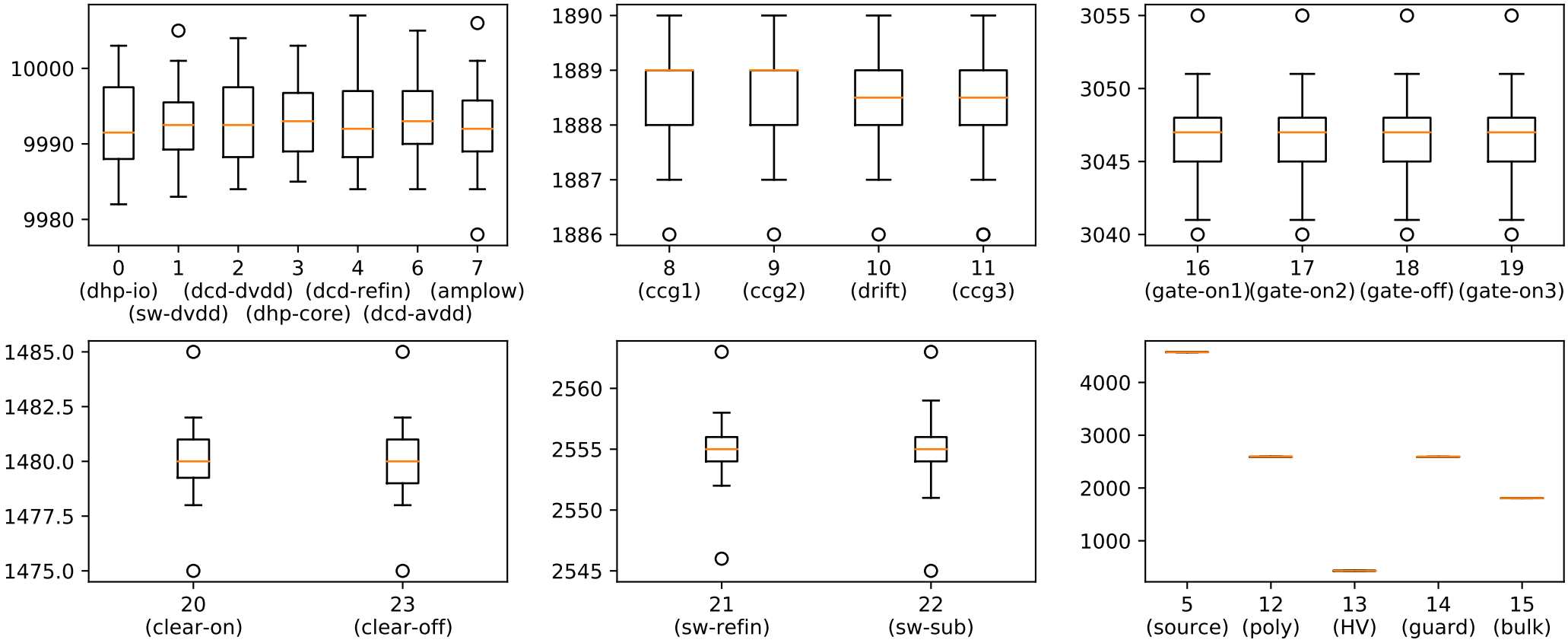


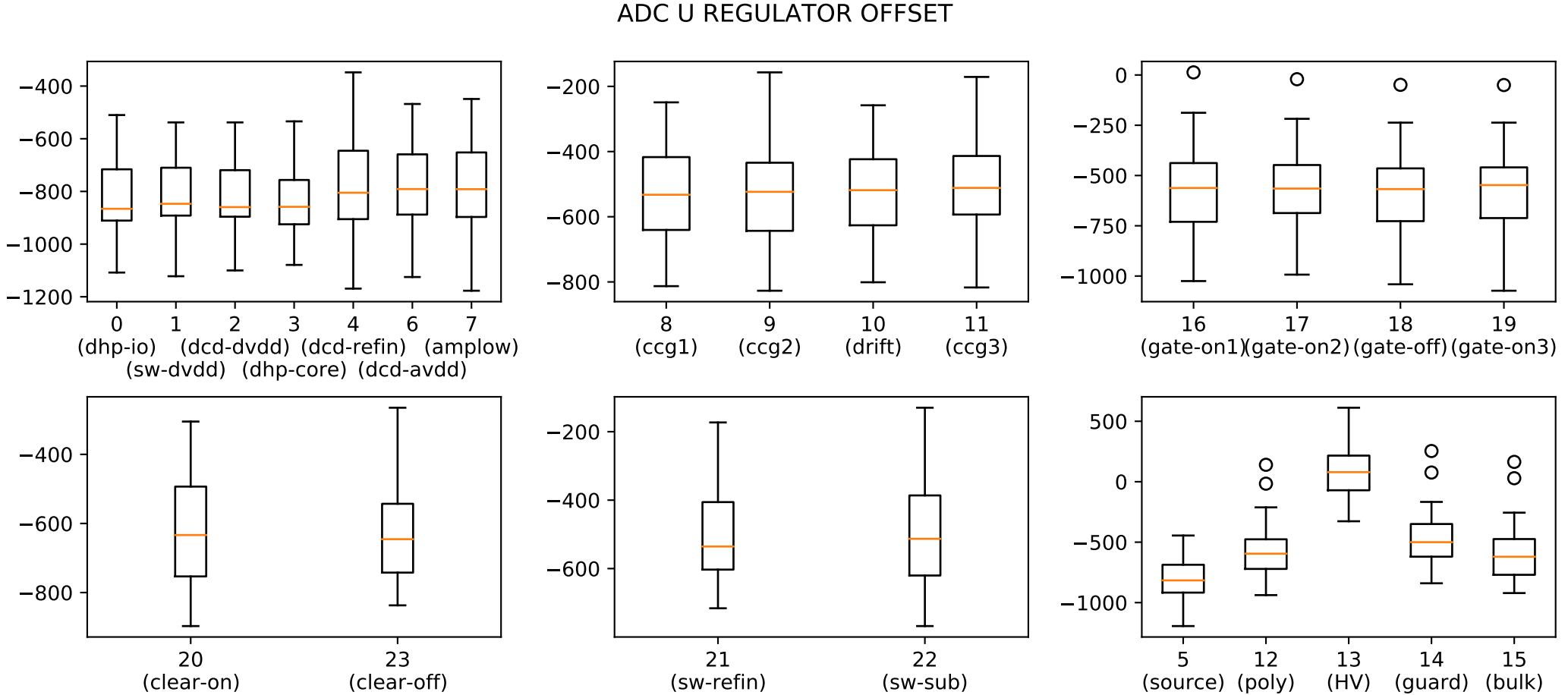


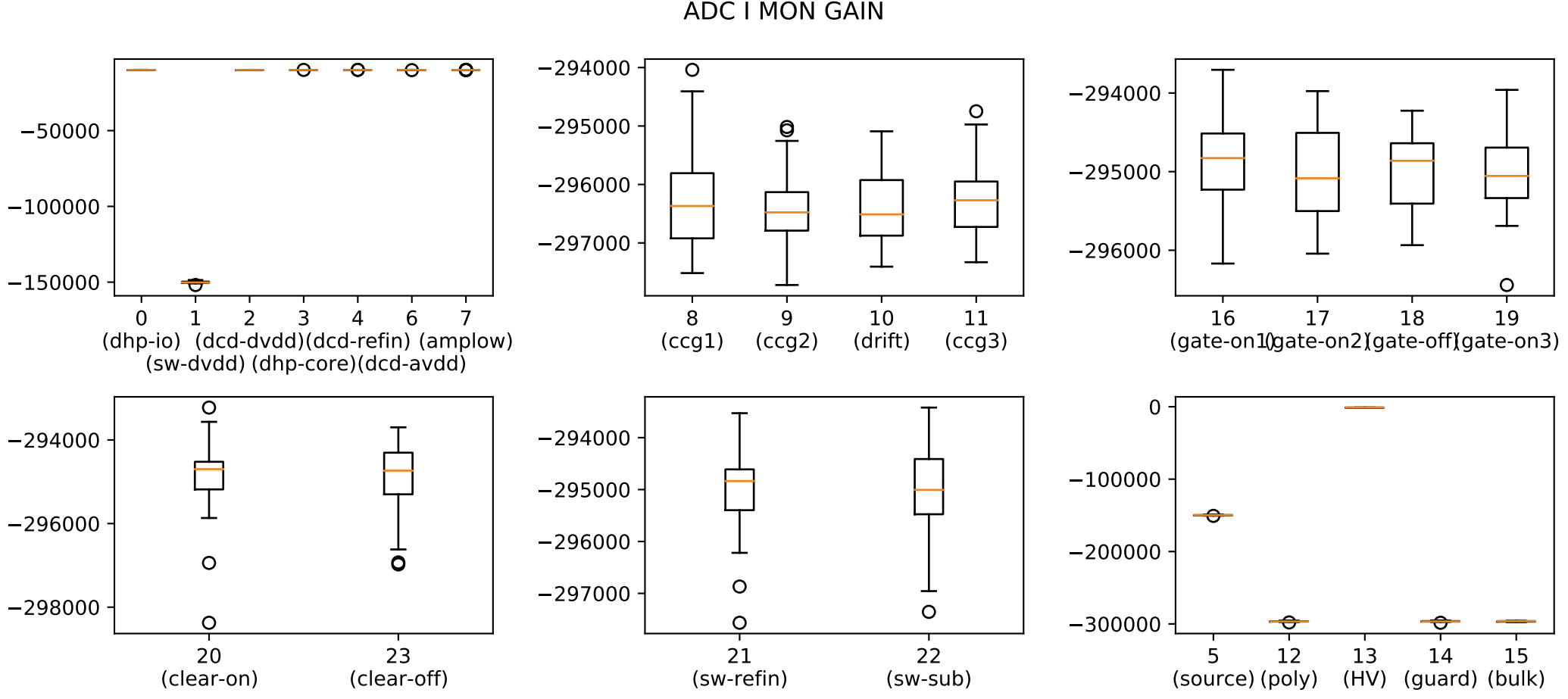

ADC U LOAD GAIN
4660
4650
4640
4630
0
(dhp-io)
1
(sw-dvdd)
2
(dcd-dvdd)
3
(dhp-core)
4
(dcd-refin)
6
(dcd-avdd)
7
(amplow)
2758
2756
2754
2752
8
(ccg1)
9
(ccg2)
10
(drift)
11
(ccg3)
2760
2755
2750
16
(gate-on1)
17
(gate-on2)
18
(gate-off)
19
(gate-on3)
1485.0
1482.5
1480.0
1477.5
1475.0
20
(clear-on)
23
(clear-off)
2560
2555
2550
21
(sw-refin)
22
(sw-sub)
4000
3000
2000
1000
5
(source)
12
(poly)
13
(HV)
14
(guard)
15
(bulk)

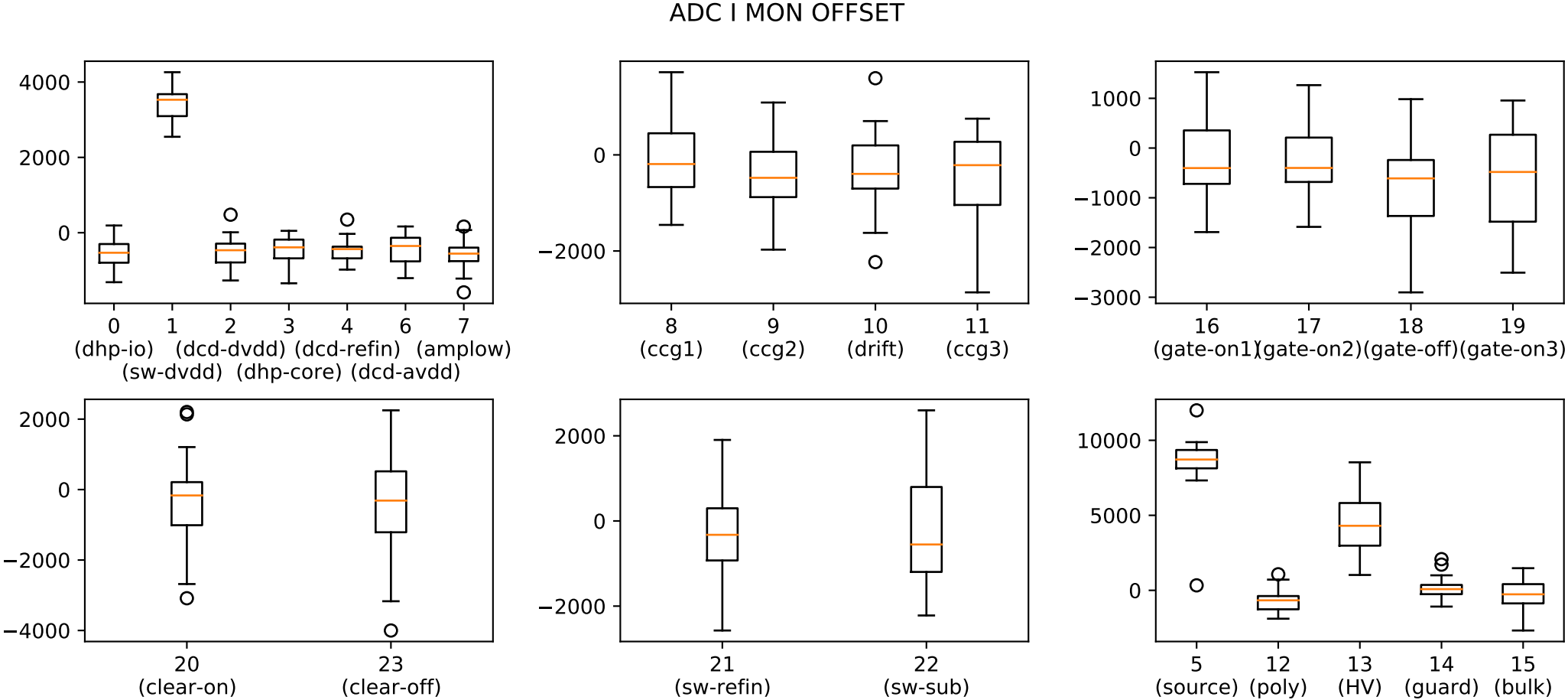

ADC U LOAD OFFSET
−500
−750
−1000
−1250
0 (dhp-io)
1 (sw-dvdd)
2 (dcd-dvdd)
3 (dhp-core)
4 (dcd-refin)
6 (dcd-avdd)
7 (amplow)
−200
−400
−600
−800
8 (ccg1)
9 (ccg2)
10 (drift)
11 (ccg3)
0
−250
−500
−750
−1000
16 (gate-on1)
17 (gate-on2)
18 (gate-off)
19 (gate-on3)
−200
−400
−600
−800
20 (clear-on)
23 (clear-off)
−200
−400
−600
21 (sw-refin)
22 (sw-sub)
1000
0
−1000
5 (source)
12 (poly)
13 (HV)
14 (guard)
15 (bulk)

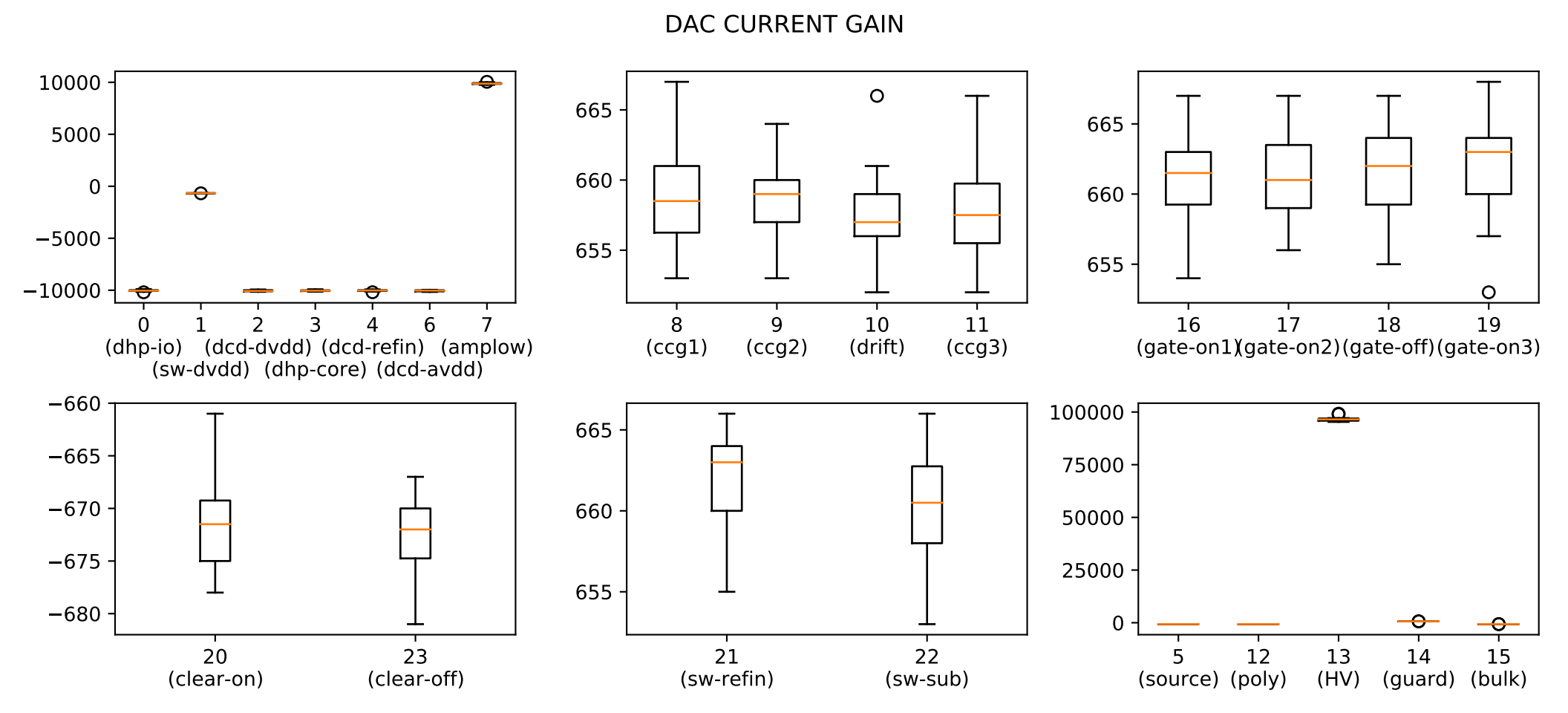
ADC U REGULATOR GAIN

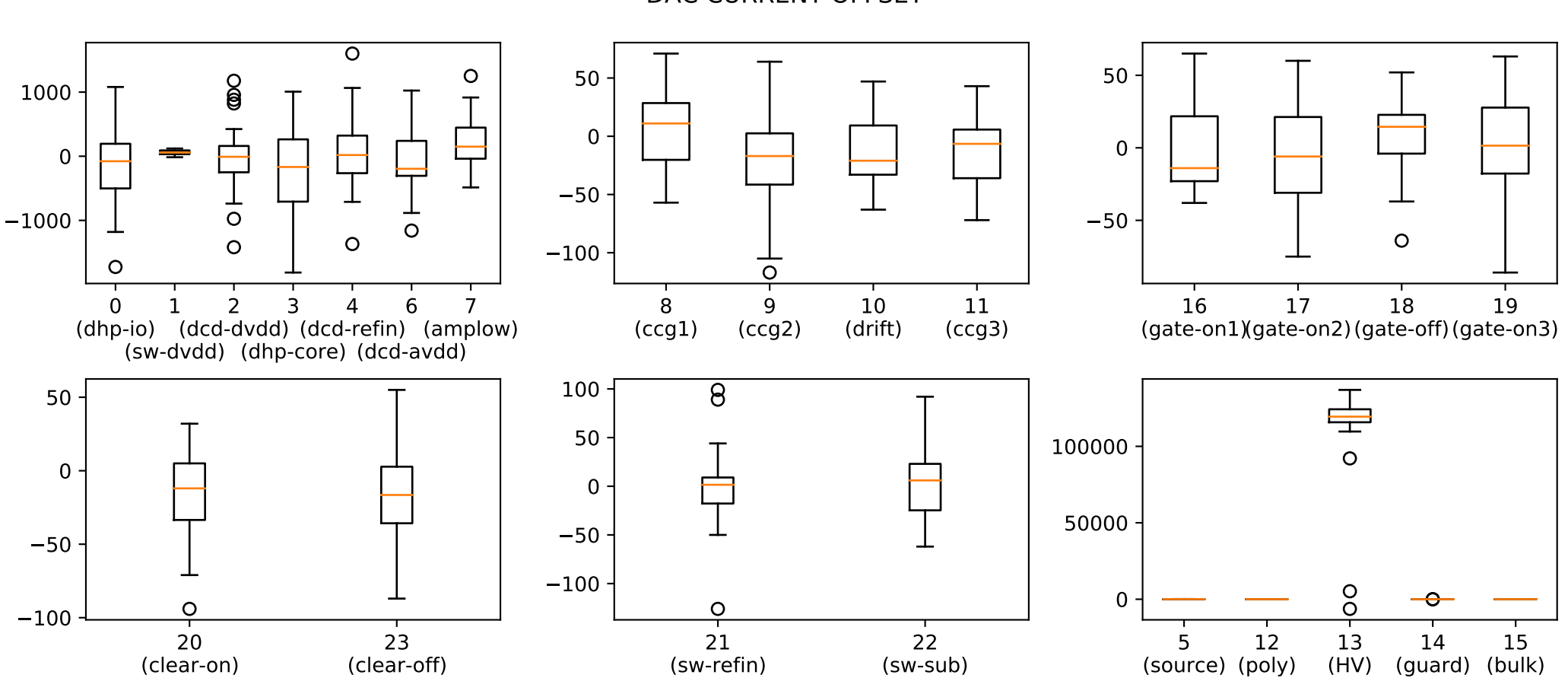



ADC U REGULATOR OFFSET
−400
−600
−800
−1000
−1200
0
(dhp-io)
(sw-dvdd)
1
(dcd-dvdd)
2
(dhp-core)
3
4
(dcd-refin)
6
(dcd-avdd)
7
(amplow)
−200
−400
−600
−800
8
(ccg1)
9
(ccg2)
10
(drift)
11
(ccg3)
0
−250
−500
−750
−1000
16
(gate-on1)
17
(gate-on2)
18
(gate-off)
19
(gate-on3)
−400
−600
−800
20
(clear-on)
23
(clear-off)
−200
−400
−600
21
(sw-refin)
22
(sw-sub)
500
0
−500
−1000
5
(source)
12
(poly)
13
(HV)
14
(guard)
15
(bulk)


ADC I MON GAIN
−50000
−100000
−150000
0
(dhp-io)
(sw-dvdd)
1
(dcd-dvdd)
2
(dhp-core)
3
(dcd-refin)
4
(dcd-avdd)
6
(amplow)
7
−294000
−295000
−296000
−297000
8
(ccg1)
9
(ccg2)
10
(drift)
11
(ccg3)
−294000
−295000
−296000
16
(gate-on1)
17
(gate-on2)
18
(gate-off)
19
(gate-on3)
−294000
−296000
−298000
20
(clear-on)
23
(clear-off)
−294000
−295000
−296000
−297000
21
(sw-refin)
22
(sw-sub)
0
−100000
−200000
−300000
5
(source)
12
(poly)
13
(HV)
14
(guard)
15
(bulk)


ADC I MON OFFSET
4000
2000
0
0
(dhp-io)
1
(dcd-dvdd)
(sw-dvdd)
2
3
(dcd-refin)
(dhp-core)
4
6
(amplow)
(dcd-avdd)
7
0
−2000
8
(ccg1)
9
(ccg2)
10
(drift)
11
(ccg3)
1000
0
−1000
−2000
−3000
16
(gate-on1)
17
(gate-on2)
18
(gate-off)
19
(gate-on3)
2000
0
−2000
−4000
20
(clear-on)
23
(clear-off)
2000
0
−2000
21
(sw-refin)
22
(sw-sub)
10000
5000
0
5
(source)
12
(poly)
13
(HV)
14
(guard)
15
(bulk)


DAC CURRENT GAIN
10000
5000
0
−5000
−10000
0 (dhp-io)
1 (dcd-dvdd) (sw-dvdd)
2 (dcd-refin) (dhp-core)
3
4 (amplow) (dcd-avdd)
6
7
665
660
655
8 (ccg1)
9 (ccg2)
10 (drift)
11 (ccg3)
16 (gate-on1)
17 (gate-on2)
18 (gate-off)
19 (gate-on3)
−660
−665
−670
−675
−680
20 (clear-on)
23 (clear-off)
21 (sw-refin)
22 (sw-sub)
100000
75000
50000
25000
0
5 (source)
12 (poly)
13 (HV)
14 (guard)
15 (bulk)


DAC CURRENT OFFSET
1000
0
−1000
0
(dhp-io)
(sw-dvdd)
1
2
(dcd-dvdd)
3
(dhp-core)
4
(dcd-refin)
6
(dcd-avdd)
7
(amplow)
50
0
−50
−100
8
(ccg1)
9
(ccg2)
10
(drift)
11
(ccg3)
50
0
−50
16
(gate-on1)
17
(gate-on2)
18
(gate-off)
19
(gate-on3)
50
0
−50
−100
20
(clear-on)
23
(clear-off)
100
50
0
−50
−100
21
(sw-refin)
22
(sw-sub)
100000
50000
0
5
(source)
12
(poly)
13
(HV)
14
(guard)
15
(bulk)