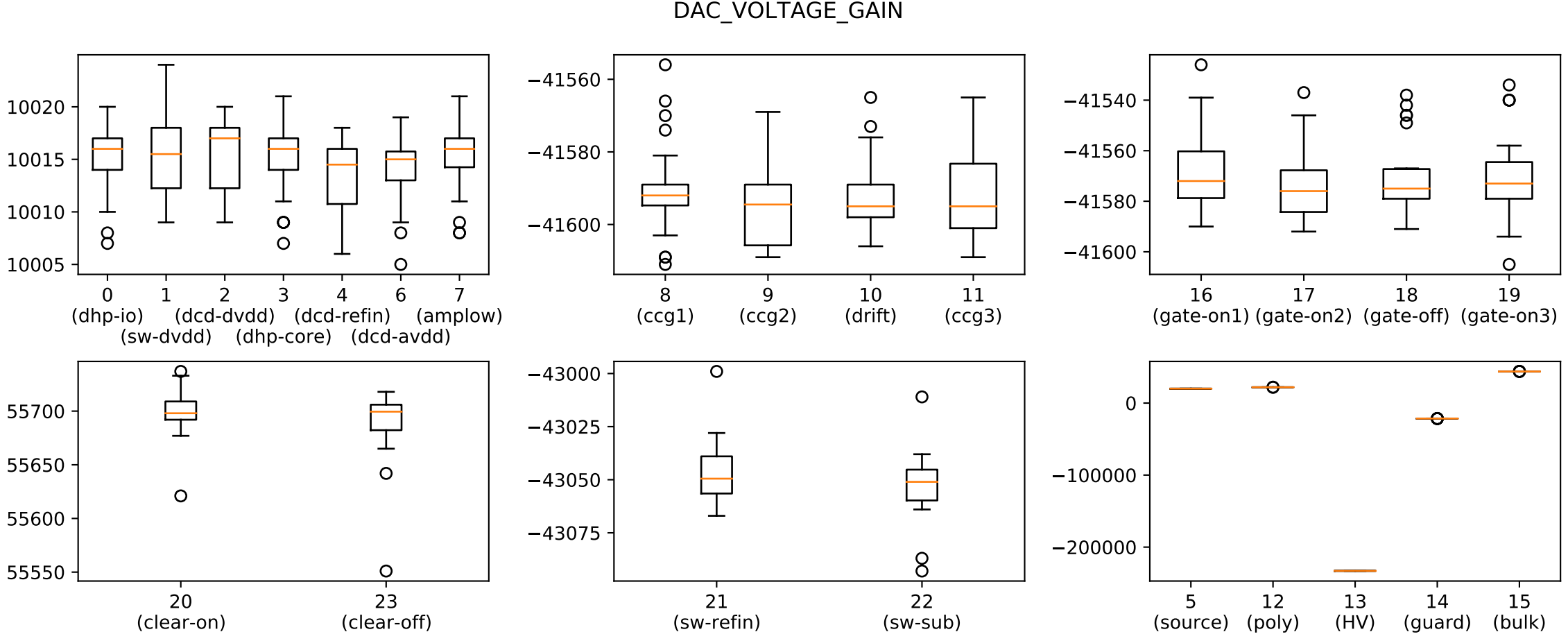
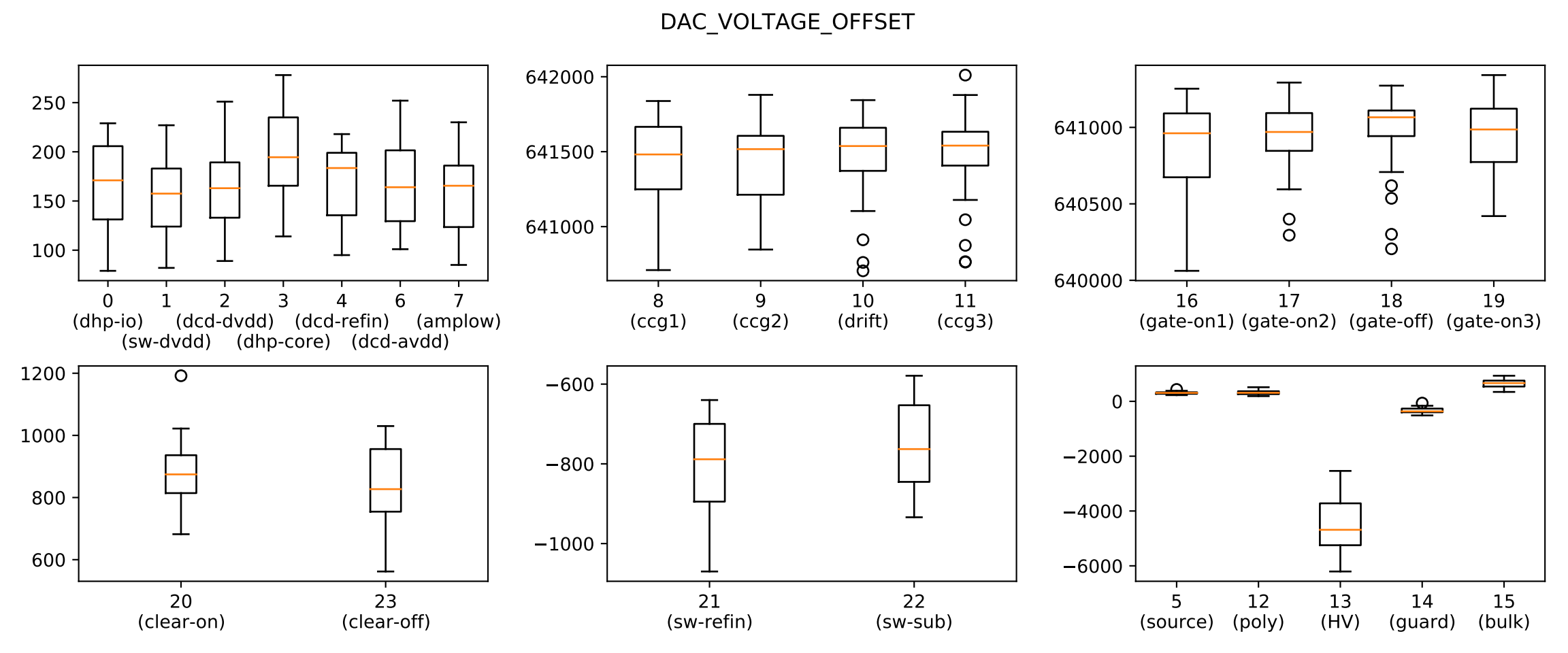
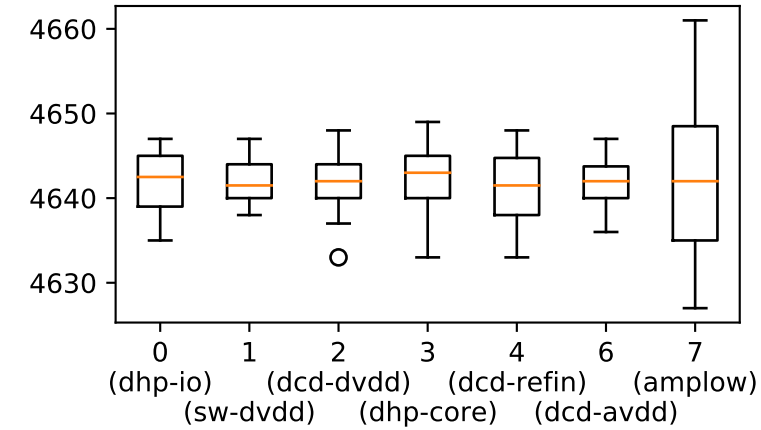
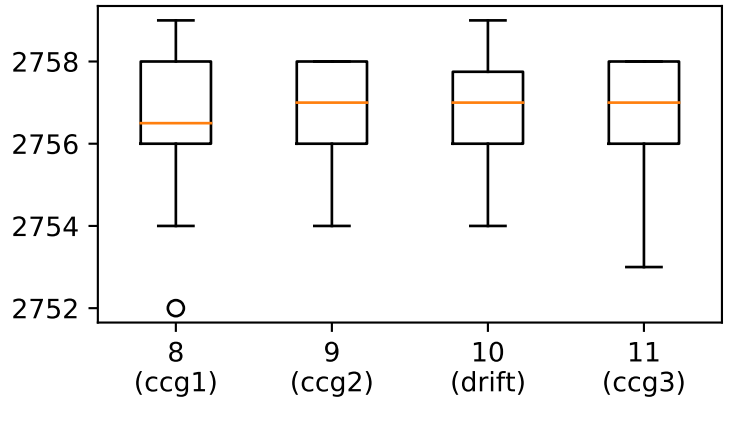
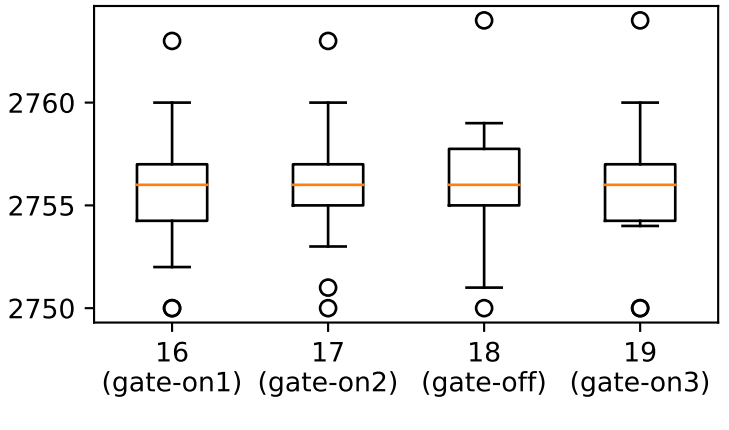

DAC_VOLTAGE_GAIN
10020
10015
10010
10005
0
(dhp-io)
(sw-dvdd)
1
(dcd-dvdd)
(dhp-core)
2
3
(dcd-refin)
(dcd-avdd)
4
6
(amplow)
7
−41560
−41580
−41600
8
(ccg1)
9
(ccg2)
10
(drift)
11
(ccg3)
−41540
−41560
−41580
−41600
16
(gate-on1)
17
(gate-on2)
18
(gate-off)
19
(gate-on3)
55700
55650
55600
55550
20
(clear-on)
23
(clear-off)
−43000
−43025
−43050
−43075
21
(sw-refin)
22
(sw-sub)
0
−100000
−200000
5
(source)
12
(poly)
13
(HV)
14
(guard)
15
(bulk)

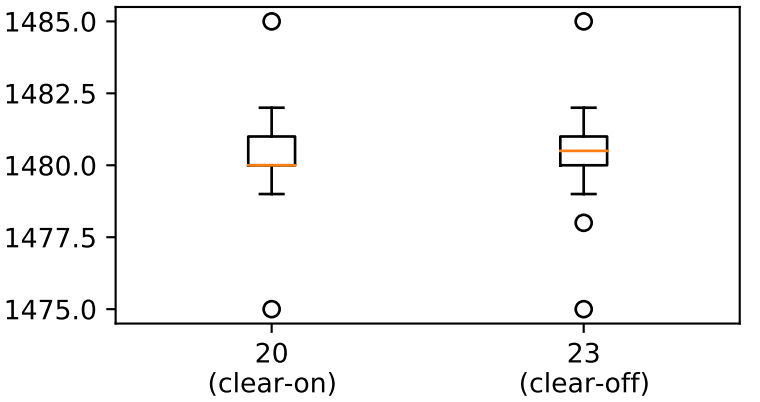

DAC_VOLTAGE_OFFSET
250
200
150
100
0
(dhp-io)
1
(sw-dvdd)
2
(dcd-dvdd)
3
(dhp-core)
4
(dcd-refin)
6
(dcd-avdd)
7
(amplow)
642000
641500
641000
8
(ccg1)
9
(ccg2)
10
(drift)
11
(ccg3)
641000
640500
640000
16
(gate-on1)
17
(gate-on2)
18
(gate-off)
19
(gate-on3)
1200
1000
800
600
20
(clear-on)
23
(clear-off)
−600
−800
−1000
21
(sw-refin)
22
(sw-sub)
0
−2000
−4000
−6000
5
(source)
12
(poly)
13
(HV)
14
(guard)
15
(bulk)

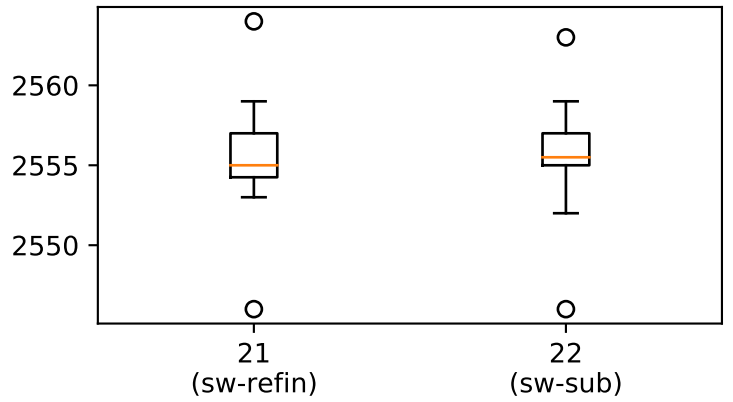
ADC_U_LOAD_GAIN

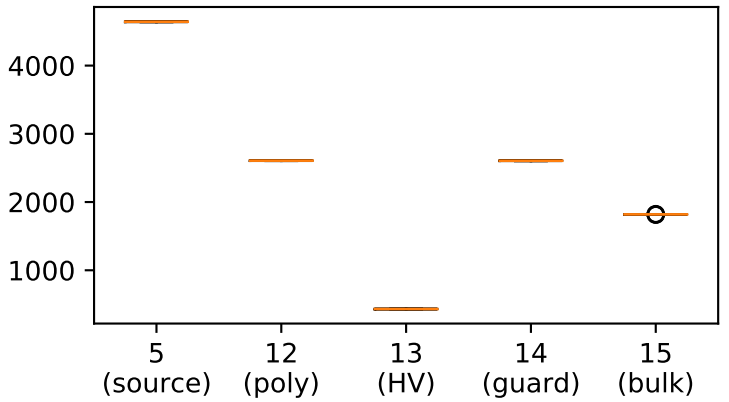


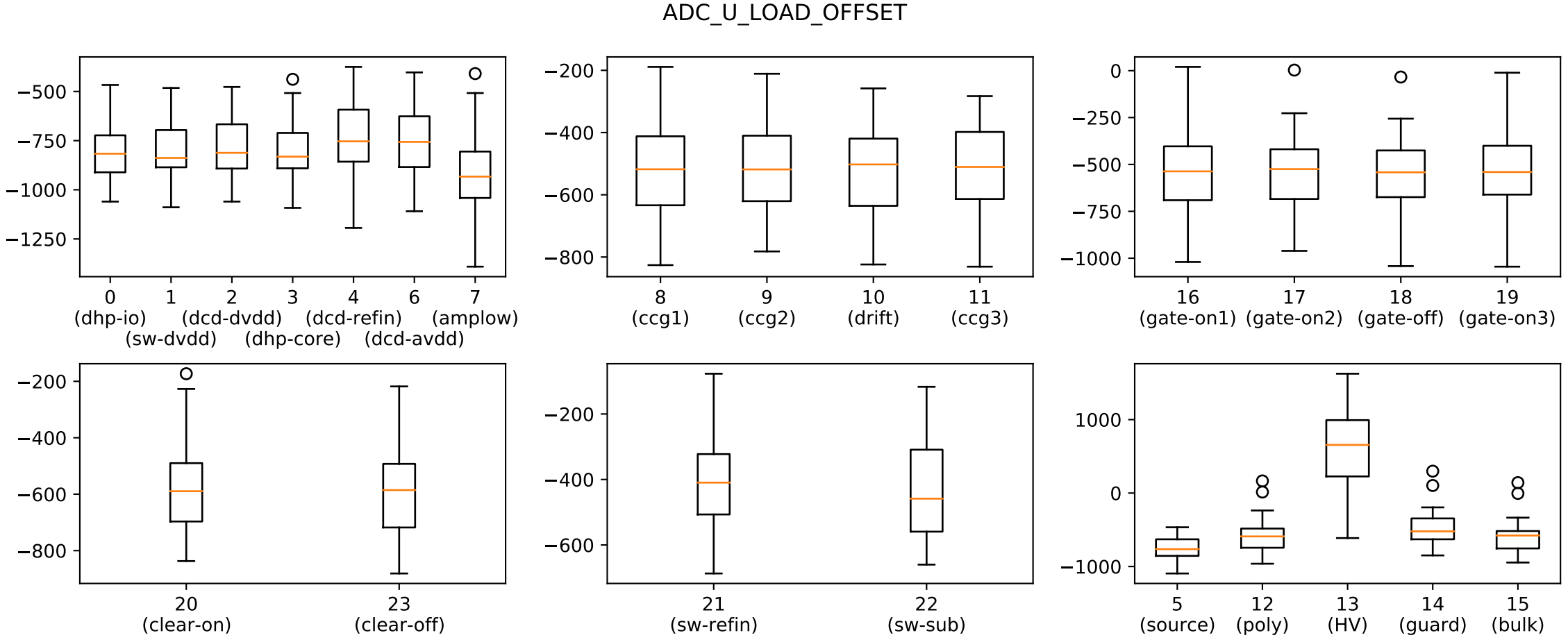


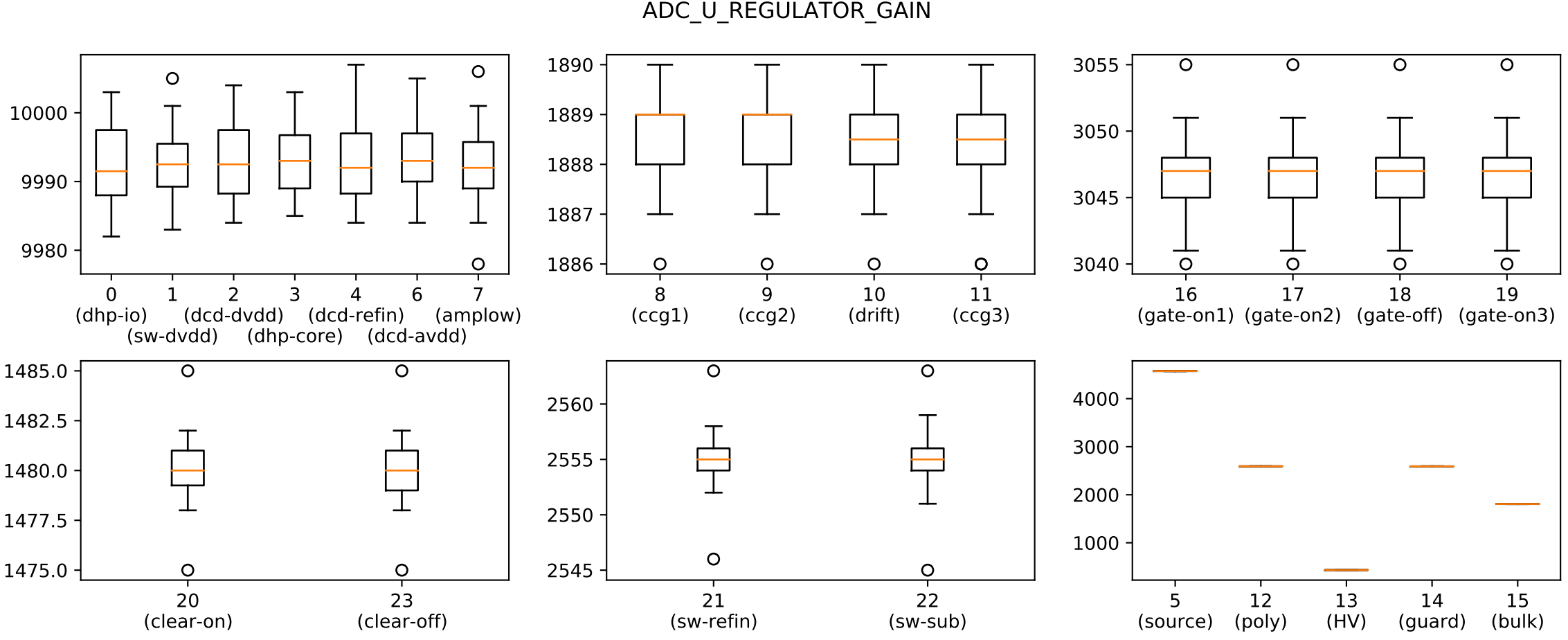


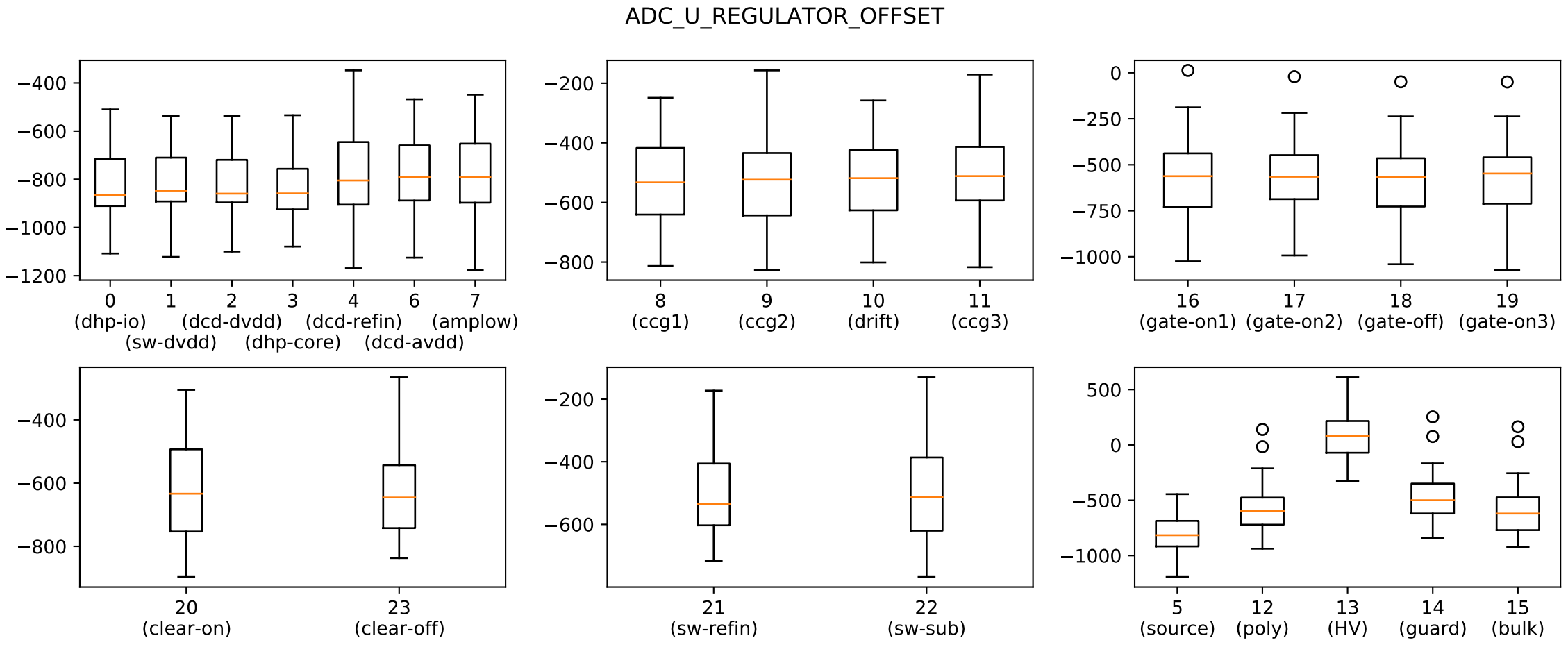


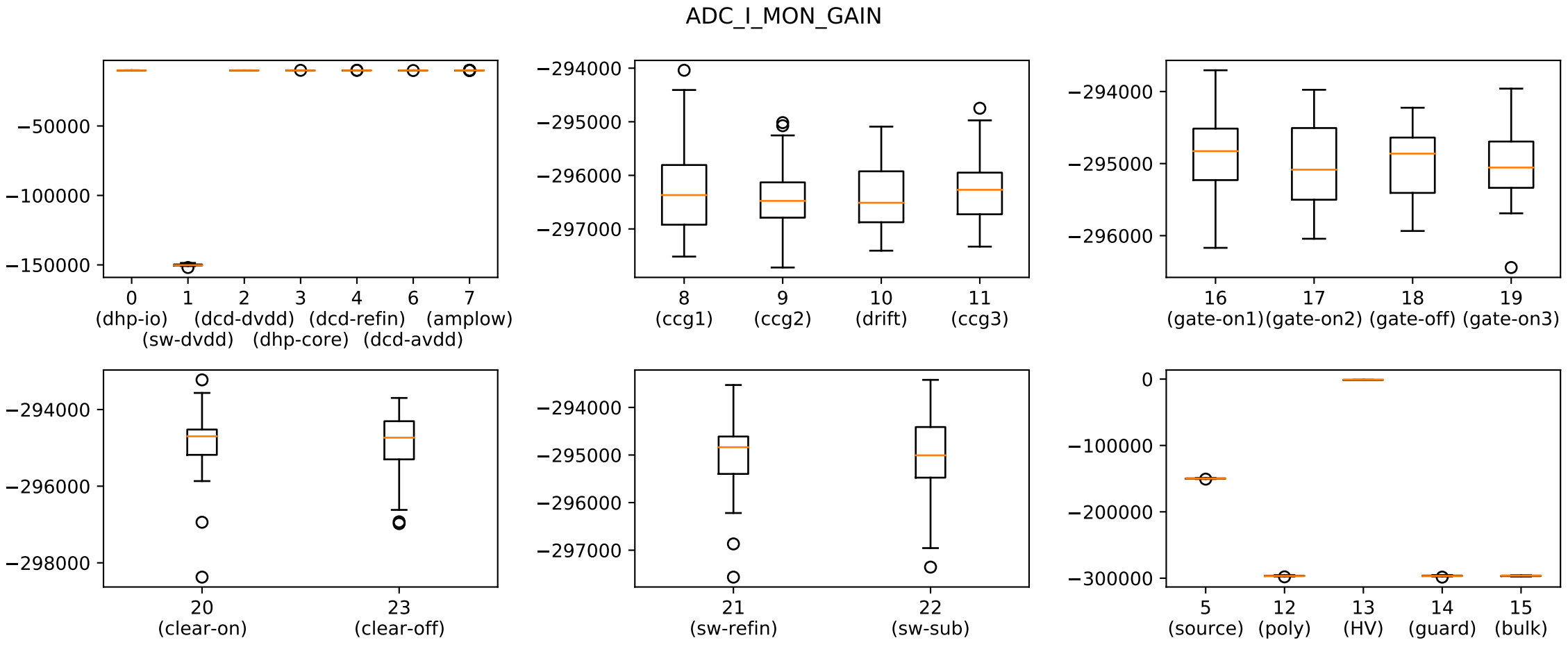


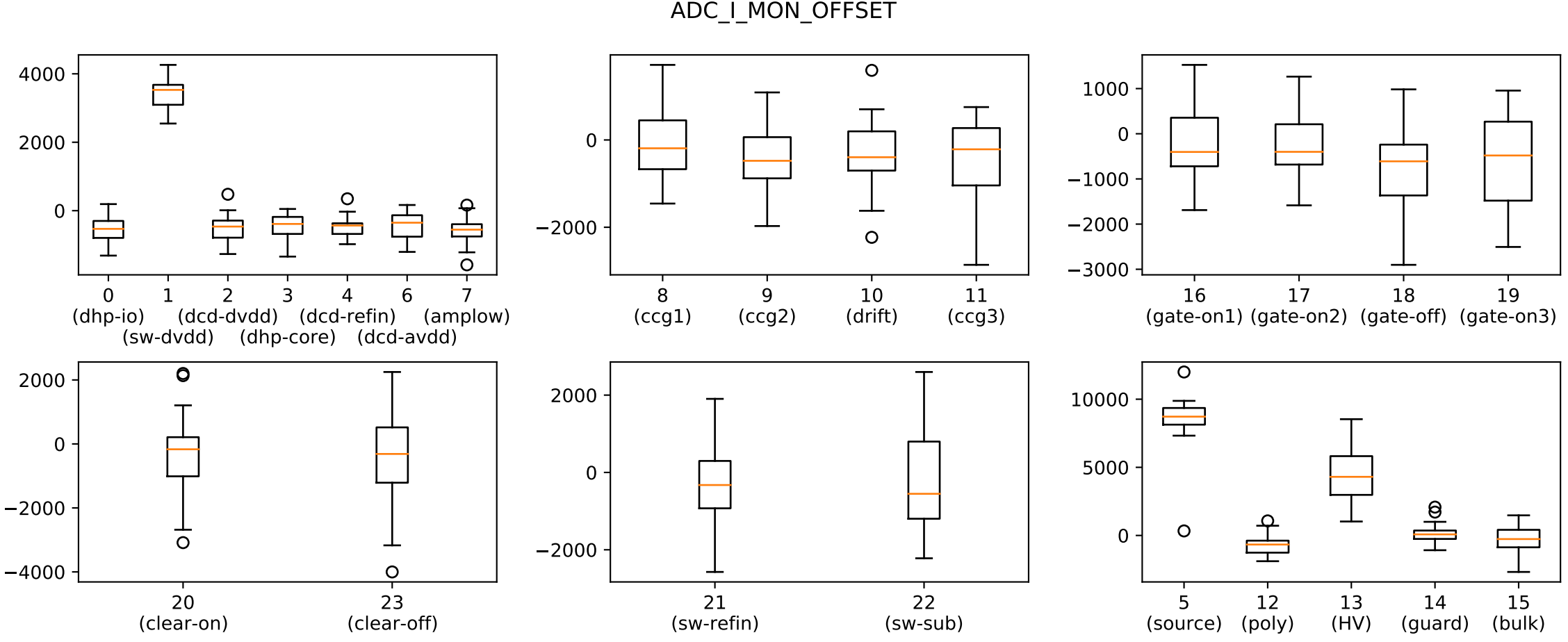


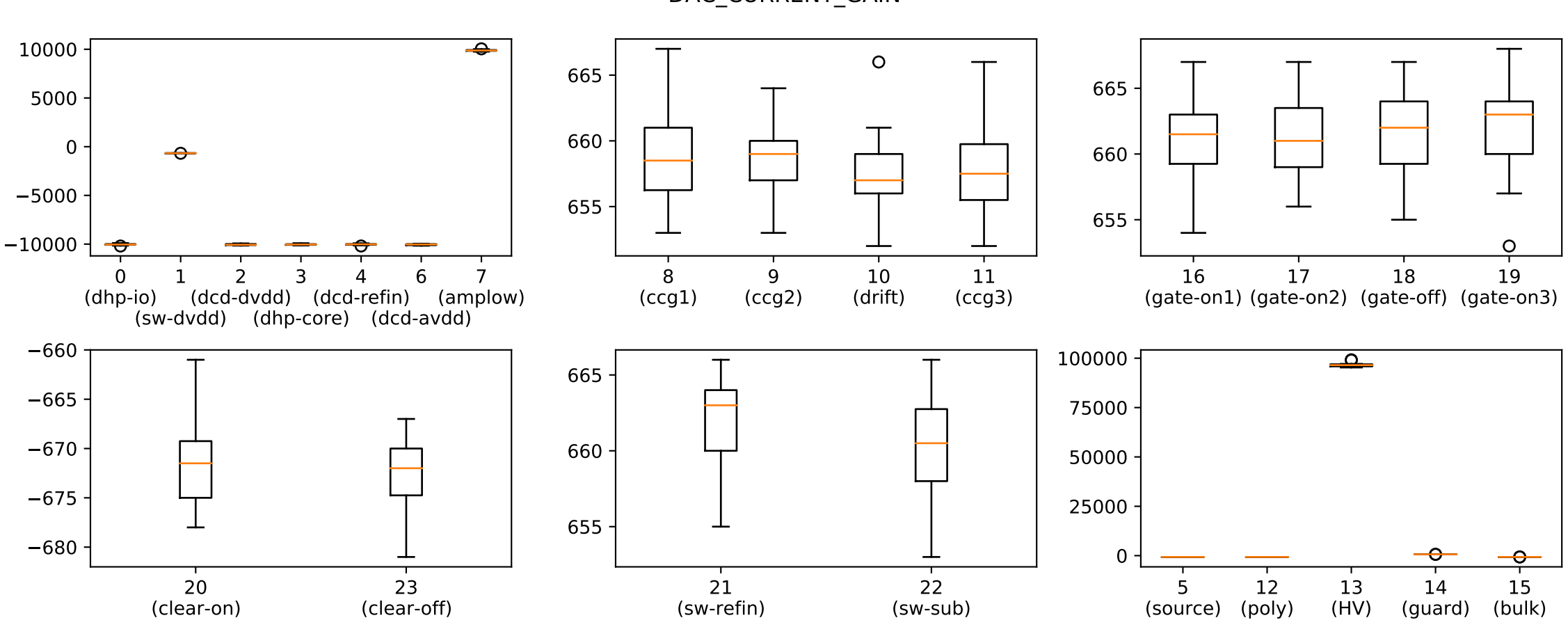

ADC_U_LOAD_OFFSET
−500
−750
−1000
−1250
0 (dhp-io)
1 (sw-dvdd)
2 (dcd-dvdd)
3 (dhp-core)
4 (dcd-refin)
6 (dcd-avdd)
7 (amplow)
−200
−400
−600
−800
8 (ccg1)
9 (ccg2)
10 (drift)
11 (ccg3)
0
−250
−500
−750
−1000
16 (gate-on1)
17 (gate-on2)
18 (gate-off)
19 (gate-on3)
−200
−400
−600
−800
20 (clear-on)
23 (clear-off)
−200
−400
−600
21 (sw-refin)
22 (sw-sub)
1000
0
−1000
5 (source)
12 (poly)
13 (HV)
14 (guard)
15 (bulk)

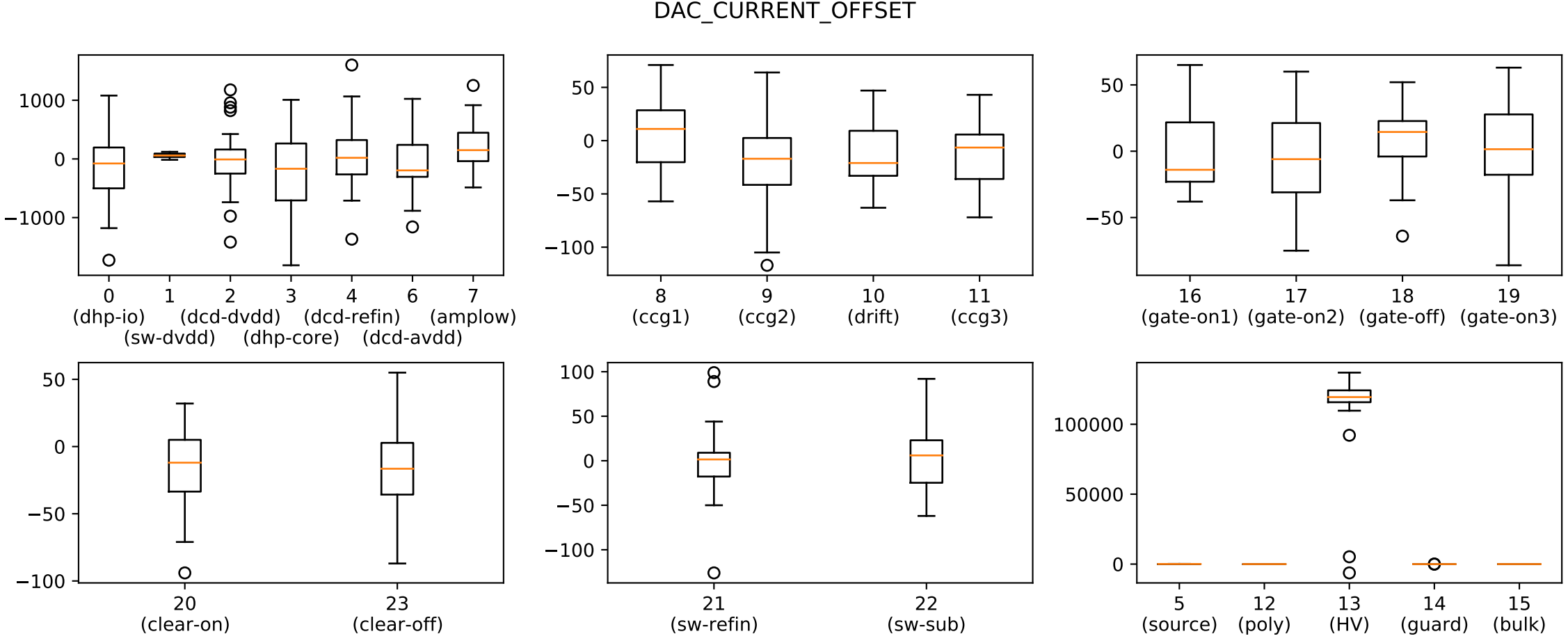

ADC_U_REGULATOR_GAIN
10000
9990
9980
0
(dhp-io)
1
(sw-dvdd)
2
(dcd-dvdd)
3
(dhp-core)
4
(dcd-refin)
6
(dcd-avdd)
7
(amplow)
1890
1889
1888
1887
1886
8
(ccg1)
9
(ccg2)
10
(drift)
11
(ccg3)
3055
3050
3045
3040
16
(gate-on1)
17
(gate-on2)
18
(gate-off)
19
(gate-on3)
1485.0
1482.5
1480.0
1477.5
1475.0
20
(clear-on)
23
(clear-off)
2560
2555
2550
2545
21
(sw-refin)
22
(sw-sub)
4000
3000
2000
1000
5
(source)
12
(poly)
13
(HV)
14
(guard)
15
(bulk)


ADC_U_REGULATOR_OFFSET
−400
−600
−800
−1000
−1200
0
(dhp-io)
1
(sw-dvdd)
2
(dcd-dvdd)
3
(dhp-core)
4
(dcd-refin)
6
(dcd-avdd)
7
(amplow)
−200
−400
−600
−800
8
(ccg1)
9
(ccg2)
10
(drift)
11
(ccg3)
0
−250
−500
−750
−1000
16
(gate-on1)
17
(gate-on2)
18
(gate-off)
19
(gate-on3)
−400
−600
−800
20
(clear-on)
23
(clear-off)
−200
−400
−600
21
(sw-refin)
22
(sw-sub)
500
0
−500
−1000
5
(source)
12
(poly)
13
(HV)
14
(guard)
15
(bulk)


ADC_I_MON_GAIN
−50000
−100000
−150000
0 (dhp-io)
1 (dcd-dvdd) (sw-dvdd)
2
3 (dcd-refin) (dhp-core)
4
6 (amplow) (dcd-avdd)
7
−294000
−295000
−296000
−297000
8 (ccg1)
9 (ccg2)
10 (drift)
11 (ccg3)
−294000
−295000
−296000
16 (gate-on1)
17 (gate-on2)
18 (gate-off)
19 (gate-on3)
−294000
−296000
−298000
20 (clear-on)
23 (clear-off)
−294000
−295000
−296000
−297000
21 (sw-refin)
22 (sw-sub)
0
−100000
−200000
−300000
5 (source)
12 (poly)
13 (HV)
14 (guard)
15 (bulk)


ADC_I_MON_OFFSET
4000
2000
0
0
(dhp-io)
1
(sw-dvdd)
2
(dcd-dvdd)
3
(dhp-core)
4
(dcd-refin)
6
(dcd-avdd)
7
(amplow)
0
−2000
8
(ccg1)
9
(ccg2)
10
(drift)
11
(ccg3)
1000
0
−1000
−2000
−3000
16
(gate-on1)
17
(gate-on2)
18
(gate-off)
19
(gate-on3)
2000
0
−2000
−4000
20
(clear-on)
23
(clear-off)
2000
0
−2000
21
(sw-refin)
22
(sw-sub)
10000
5000
0
5
(source)
12
(poly)
13
(HV)
14
(guard)
15
(bulk)


DAC_CURRENT_GAIN
10000
5000
0
−5000
−10000
0
(dhp-io)
1
(sw-dvdd)
2
(dcd-dvdd)
3
(dhp-core)
4
(dcd-refin)
6
(dcd-avdd)
7
(amplow)
665
660
655
8
(ccg1)
9
(ccg2)
10
(drift)
11
(ccg3)
665
660
655
16
(gate-on1)
17
(gate-on2)
18
(gate-off)
19
(gate-on3)
−660
−665
−670
−675
−680
20
(clear-on)
23
(clear-off)
665
660
655
21
(sw-refin)
22
(sw-sub)
100000
75000
50000
25000
0
5
(source)
12
(poly)
13
(HV)
14
(guard)
15
(bulk)


DAC_CURRENT_OFFSET
1000
0
−1000
0
(dhp-io)
1
(sw-dvdd)
2
(dcd-dvdd)
3
(dhp-core)
4
(dcd-refin)
6
(dcd-avdd)
7
(amplow)
50
0
−50
−100
8
(ccg1)
9
(ccg2)
10
(drift)
11
(ccg3)
50
0
−50
16
(gate-on1)
17
(gate-on2)
18
(gate-off)
19
(gate-on3)
50
0
−50
−100
20
(clear-on)
23
(clear-off)
100
50
0
−50
−100
21
(sw-refin)
22
(sw-sub)
100000
50000
0
5
(source)
12
(poly)
13
(HV)
14
(guard)
15
(bulk)