Cache Memory

- EXERCISE
  - Assume there are three different cache memories with an address bus of 8 bits (2 of them are used for byte selection). Each cache memory has 8 blocks; each block has 2 words (1 word = 2 bytes). The first cache memory uses Direct Mapping; the second is a 2-way Set Associative; the last one is Fully Associative. Given the sequence of references 0, 8, 0, 40, 8, 12, 40, 24, 28, 48, 24, 56, 60,26,112,58,63,127,201,73,27 and using LRU as the replacement policy, find the number of misses for each cache memory.