CAO Clock Cycles

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Mnemonic	Operands	Description	Clock Cycles
ADC	Rd, Rr	Add with Carry	1
ADD	Rd, Rr	Add without Carry	1
ADIW	Rd, K	Add Immediate to Word	2
AND	Rd, Rr	Logical AND	1
ANDI	Rd, K	Logical AND with Immediate	1
ASR	Rd	Arithmetic Shift Right	1
BCLR	s	Bit Clear in SREG	1
BLD	Rd, b	Bit Load from the T Bit in SREG to a Bit in Register	1
BRBC	s, k	Branch if Bit in SREG is Cleared	1 (false) / 2 (true)
BRBS	s, k	Branch if Bit in SREG is Set	1 (false) / 2 (true)
BRCC	k	Branch if Carry Cleared	1 (false) / 2 (true)
BRCS	k	Branch if Carry Set	1 (false) / 2 (true)
BREAK	None	Break	1
BREQ	k	Branch if Equal	1 (false) / 2 (true)
BRGE	k	Branch if Greater or Equal (Signed)	1 (false) / 2 (true)
BRHC	k	Branch if Half Carry Flag is Cleared	1 (false) / 2 (true)
BRHS	k	Branch if Half Carry Flag is Set	1 (false) / 2 (true)
BRID	k	Branch if Global Interrupt is Disabled	1 (false) / 2 (true)
BRIE	k	Branch if Global Interrupt is Enabled	1 (false) / 2 (true)
BRLO	k	Branch if Lower (Unsigned)	1 (false) / 2 (true)
BRLT	k	Branch if Less Than (Signed)	1 (false) / 2 (true)
BRMI	k	Branch if Minus	1 (false) / 2 (true)
BRNE	k	Branch if Not Equal	1 (false) / 2 (true)
BRPL	k	Branch if Plus	1 (false) / 2 (true)
BRSH	k	Branch if Same or Higher (Unsigned)	1 (false) / 2 (true)
BRTC	k	Branch if the T Bit is Cleared	1 (false) / 2 (true)
BRTS	k	Branch if the T Bit is Set	1 (false) / 2 (true)
BRVC	k	Branch if Overflow Cleared	1 (false) / 2 (true)
BRVS	k	Branch if Overflow Set	1 (false) / 2 (true)
BSET	s	Bit Set in SREG	1
BST	Rd, b	Bit Store from Bit in Register to T Bit in SREG	1
CALL	k	Long Call to a Subroutine	4
CBI	A, b	Clear Bit in I/O Register	2
CBR	Rd, K	Clear Bits in Register	1
CLC	None	Clear Carry Flag	1
CLH	None	Clear Half Carry Flag	1

Mnemonic	Operands	Description	Clock Cycles
CLI	None	Clear Global Interrupt Enable Bit	1
CLN	None	Clear Negative Flag	1
CLR	Rd	Clear Register	1
CLS	None	Clear Sign Flag	1
CLT	None	Clear T Bit	1
CLV	None	Clear Overflow Flag	1
CLZ	None	Clear Zero Flag	1
COM	Rd	One's Complement	1
CP	Rd, Rr	Compare	1
CPC	Rd, Rr	Compare with Carry	1
CPI	Rd, K	Compare with Immediate	1
CPSE	Rd, Rr	Compare Skip if Equal	1 (false) / 2 (true, 1 word) / 3 (true, 2 words)
DEC	Rd	Decrement	1
EICALL	None	Extended Indirect Call to Subroutine	4
EIJMP	None	Extended Indirect Jump	2
ELPM	None, Rd, Z+	Extended Load Program Memory	3
EOR	Rd, Rr	Exclusive OR	1
FMUL	Rd, Rr	Fractional Multiply Unsigned	2
FMULS	Rd, Rr	Fractional Multiply Signed	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	2
ICALL	None	Indirect Call to Subroutine	3
IJMP	None	Indirect Jump	2
IN	Rd, A	Load an I/O Location to Register	1
INC	Rd	Increment	1
JMP	k	Jump	3
LD	Rd, X	Load Indirect from Data Space to Register using X	2
LD	Rd, X+	Load Indirect using X (Post-increment)	2
LD	Rd, -X	Load Indirect using X (Pre-decrement)	2
LD	Rd, Y	Load Indirect from Data Space to Register using Y	2
LD	Rd, Y+	Load Indirect using Y (Post-increment)	2
LD	Rd, -Y	Load Indirect using Y (Pre-decrement)	2
LDD	Rd, Y+q	Load Indirect using Y with Displacement	2
LD	Rd, Z	Load Indirect from Data Space to Register using Z	2
LD	Rd, Z+	Load Indirect using Z (Post-increment)	2
LD	Rd, -Z	Load Indirect using Z (Pre-decrement)	2

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LDD	Rd, Z+q	Load Indirect using Z with Displacement	2
LDI	Rd, K	Load Immediate	1
LDS	Rd, k	Load Direct from Data Space	2
LPM	None, Rd, Z+	Load Program Memory	3
LSL	Rd	Logical Shift Left	1
LSR	Rd	Logical Shift Right	1
MOV	Rd, Rr	Copy Register	1
MOVW	Rd, Rr	Copy Register Word	1
MUL	Rd, Rr	Multiply Unsigned	2
MULS	Rd, Rr	Multiply Signed	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	2
NEG	Rd	Two's Complement	1
NOP	None	No Operation	1
OR	Rd, Rr	Logical OR	1
ORI	Rd, K	Logical OR with Immediate	1
OUT	A, Rr	Store Register to I/O Location	1
POP	Rd	Pop Register from Stack	2
PUSH	Rr	Push Register on Stack	2
RCALL	k	Relative Call to Subroutine	3
RET	None	Return from Subroutine	4
RETI	None	Return from Interrupt	4
RJMP	k	Relative Jump	2
ROL	Rd	Rotate Left through Carry	1
ROR	Rd	Rotate Right through Carry	1
SBC	Rd, Rr	Subtract with Carry	1
SBCI	Rd, K	Subtract Immediate with Carry	1
SBI	A, b	Set Bit in I/O Register	2
SBIC	A, b	Skip if Bit in I/O Register is Cleared	1 (false) / 2 (true, 1 word) / 3 (true, 2 words)
SBIS	A, b	Skip if Bit in I/O Register is Set	1 (false) / 2 (true, 1 word) / 3 (true, 2 words)
SBIW	Rd, K	Subtract Immediate from Word	2
SBR	Rd, K	Set Bits in Register	1
SBRC	Rr, b	Skip if Bit in Register is Cleared	1 (false) / 2 (true, 1 word) / 3 (true, 2 words)
SBRS	Rr, b	Skip if Bit in Register is Set	1 (false) / 2 (true, 1 word) / 3 (true, 2 words)
SEC	None	Set Carry Flag	1
SEH	None	Set Half Carry Flag	1
SEI	None	Set Global Interrupt Enable Bit	1
SEN	None	Set Negative Flag	1
SER	Rd	Set all Bits in Register	1

Mnemonic	Operands	Description	Clock Cycles
SES	None	Set Sign Flag	1
SET	None	Set T Bit	1
SEV	None	Set Overflow Flag	1
SEZ	None	Set Zero Flag	1
SLEEP	None	Enter Sleep Mode	1
SPM	None	Store Program Memory	- (Depends on operation)
ST	X, Rr	Store Indirect from Register to Data Space using X	2
ST	X+, Rr	Store Indirect using X (Post-increment)	2
ST	-X, Rr	Store Indirect using X (Pre-decrement)	2
ST	Y, Rr	Store Indirect from Register to Data Space using Y	2
ST	Y+, Rr	Store Indirect using Y (Post-increment)	2
ST	-Y, Rr	Store Indirect using Y (Pre-decrement)	2
STD	Y+q, Rr	Store Indirect using Y with Displacement	2
ST	Z, Rr	Store Indirect from Register to Data Space using Z	2
ST	Z+, Rr	Store Indirect using Z (Post-increment)	2
ST	-Z, Rr	Store Indirect using Z (Pre-decrement)	2
STD	Z+q, Rr	Store Indirect using Z with Displacement	2
STS	k, Rr	Store Direct to Data Space	2
SUB	Rd, Rr	Subtract Without Carry	1
SUBI	Rd, K	Subtract Immediate	1
SWAP	Rd	Swap Nibbles	1
TST	Rd	Test for Zero or Minus	1
WDR	None	Watchdog Reset	1