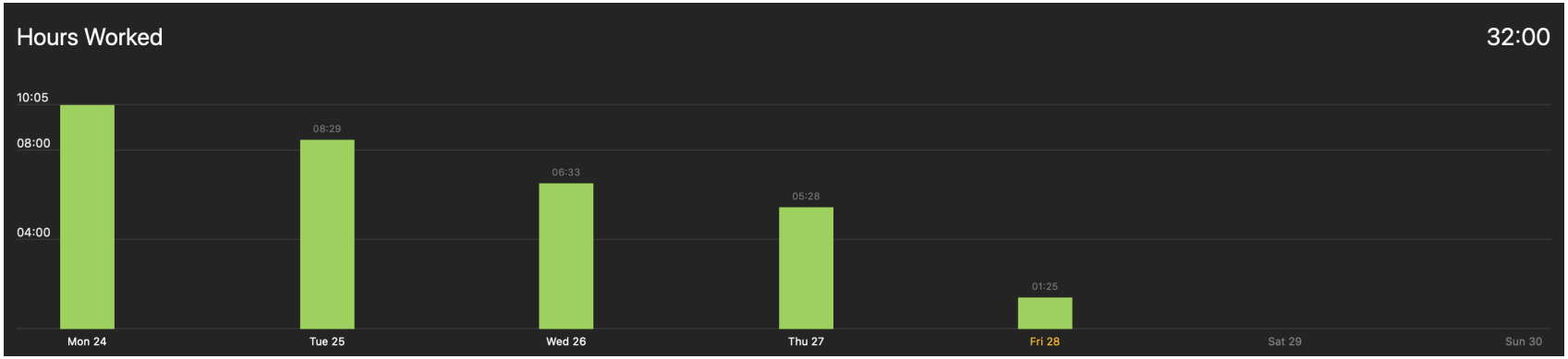
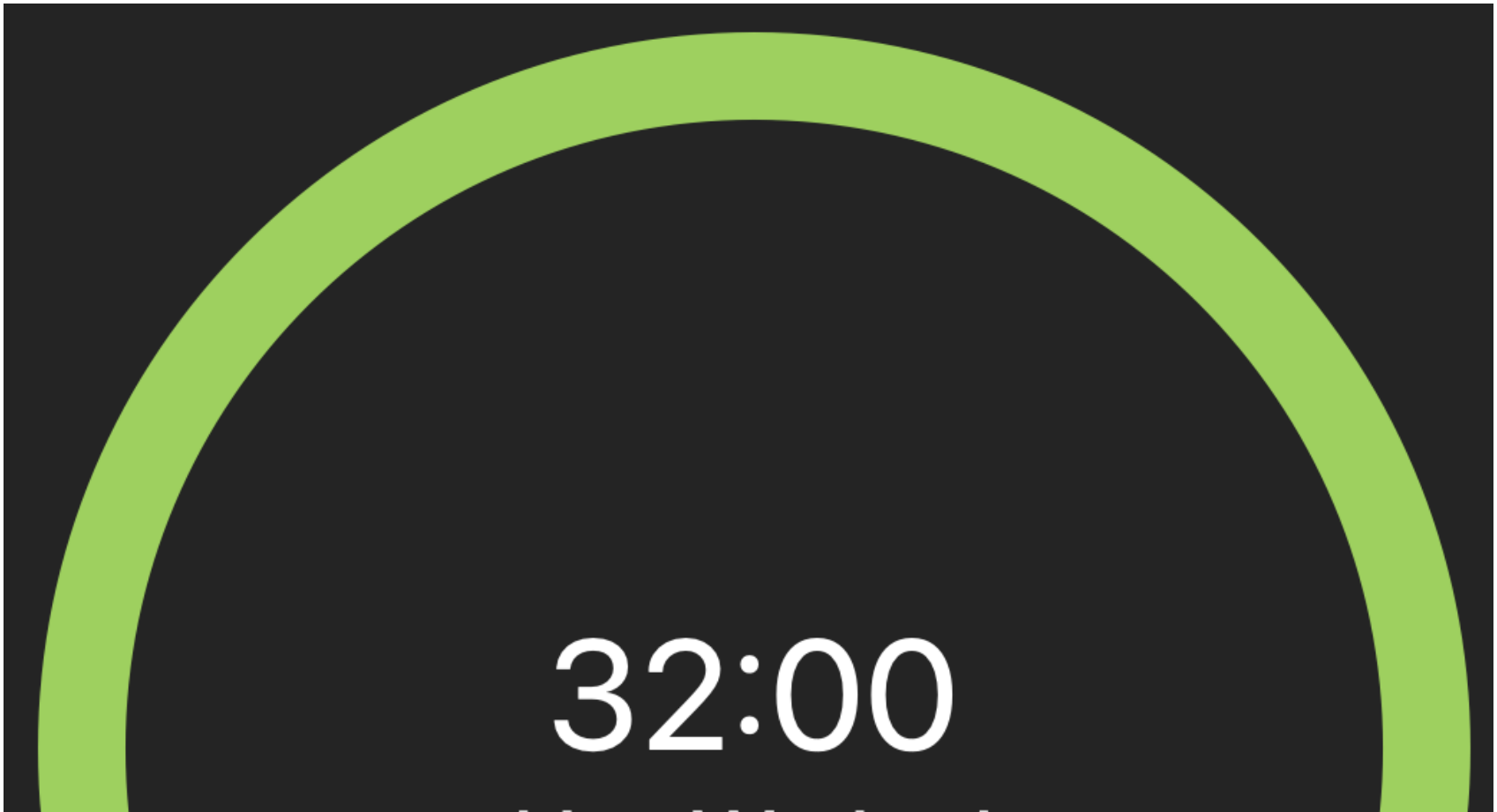
Specialization Project - Weekly meeting

Fredrik Feyling

August 28, 2020

Since last week



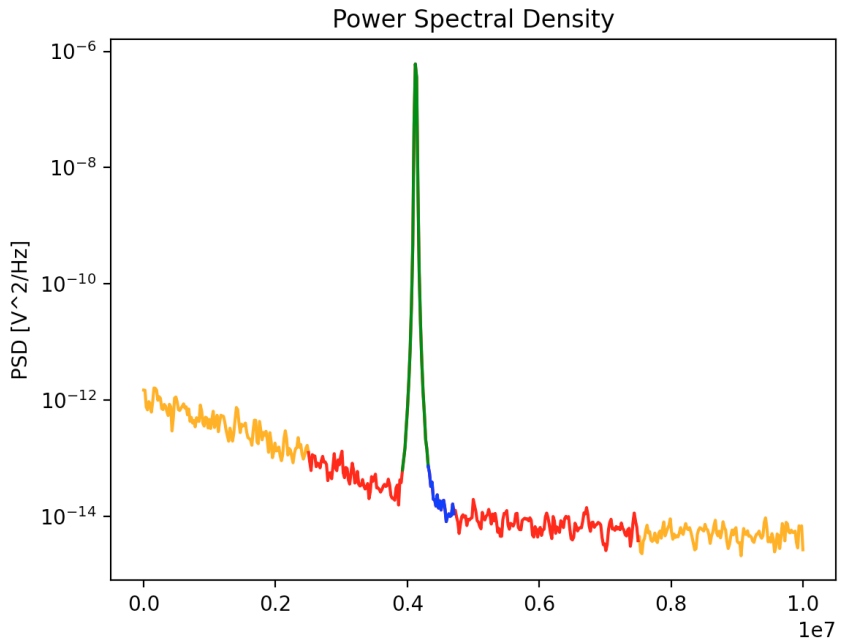


Since last week

Started writing script for simulating ADC and LNA

Written classes for ADC, LNA and Signal Generator

Function for



Timeline

Activity\Week	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	Comments
Understand behaviour Control-Bounded ADC																			
Python Simulation C-B ADC																			
First Python Sim Ready				X															
Optimize analog filter/digital control																			
Second Python Sim						X													
Implement building blocks in Cadence																			To obtain estimate for power consumption
Synthesize Verilog for digital estimation																			To obtain estimate for power consumption
First Power Estimate Ready								X											
Cadence implementation																			Full analog part and digital control
Final Simulation Results ready													X						
Report writing																			
Report deadline																		X	19.12.2020

Today

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Report deadline																		X	19.12.2020

Today

Specs

Table: ADC Specs

Parameter	Symbol	Value	Comment
Carrier Frequency	f_c	5 MHz	
Bandwidth	$\mathcal{B}$	5 MHz	$2.5 - 7.5$MHz
Effective number of bits	ENOB	> 10 bits	
Noise density	$\overline{V_n}$	$< 10\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$	NF=3 dB
Supply Voltage	V_{dd}	$< 0.8\,\mathrm{V}$	
Power Consumption	P_{tot}	$< 50\,\mu\mathrm{W}$	500 aJ/c.s[1][2]

[1] Walden FOM

[2] Hårete mål