**Memo: Current Status of Processor Milestone 5**

Section 1, Team 1a

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For this milestone, the group created the test benches for our integration tests and our unit tests. These had already been designed, but the verilog code had not been tested for syntax or correctness. Now all test benches are complete and fully functional.

A big part of this milestone was documenting how we are going to write system tests. We decided to use our snippets of code from the first milestone and Euclid’s algorithm to test sets of instructions, and we’ll use basic, one line instructions to test if the whole processor works at all. So far, only the cpi instruction has been tested, but it works.

We decided not to make a bubble state diagram despite being urged to do so. Instead, we updated the documentation for our current diagrams to make it more readable and easier to understand.

In addition, the assembler is now 100% complete.