

Voltage Division Rules

1. Voltage Division Rule

The **voltage** is divided between two series resistors in direct proportion to their resistance.

VOLTAGE DIVISION RULE :-

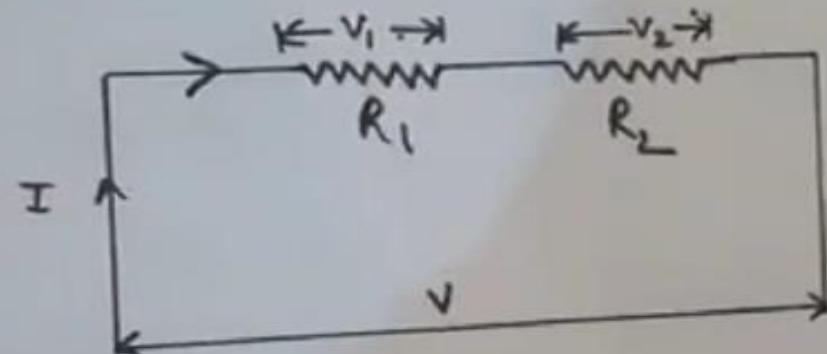
KVL

$$V = V_1 + V_2$$

$$V_1 = R_1 I$$

$$V_2 = R_2 I$$

$$I = V / (R_1 + R_2)$$



$$V = R_1 I + R_2 I$$

$$V = I (R_1 + R_2)$$

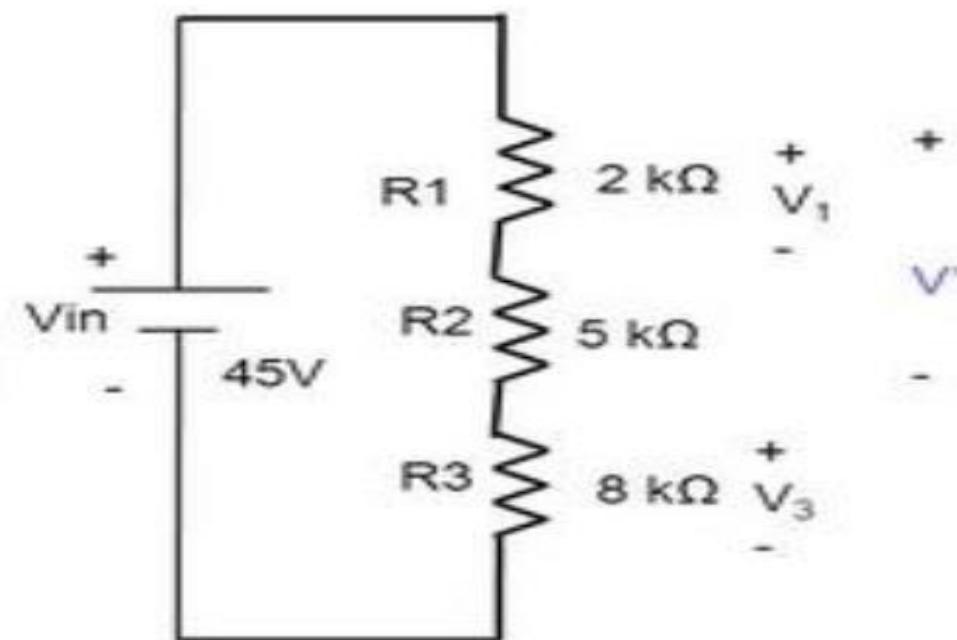
$$V_1 = V \times \frac{R_1}{R_1 + R_2}$$

$$V_2 = V \times \frac{R_2}{R_1 + R_2}$$

Voltage Division Rules

Voltage Divider Rule –Example 2

Using the voltage divider rule, determine the voltage V_1 and V_3 for the series circuit



Voltage Division Rules

Voltage Divider Rule –Example 2

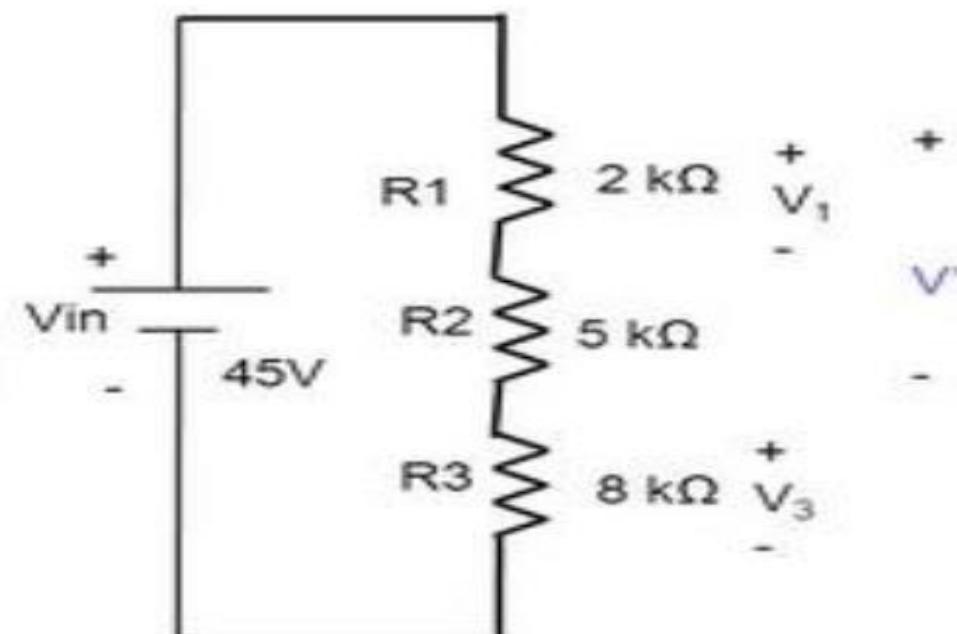
Using the voltage divider rule, determine the voltage V_1 and V_3 for the series circuit

$$V_1 = \frac{R_1 V_{in}}{R_T} = \frac{(2k\Omega)(45V)}{2k\Omega + 5k\Omega + 8k\Omega} = \frac{(2k\Omega)(45V)}{15k\Omega}$$

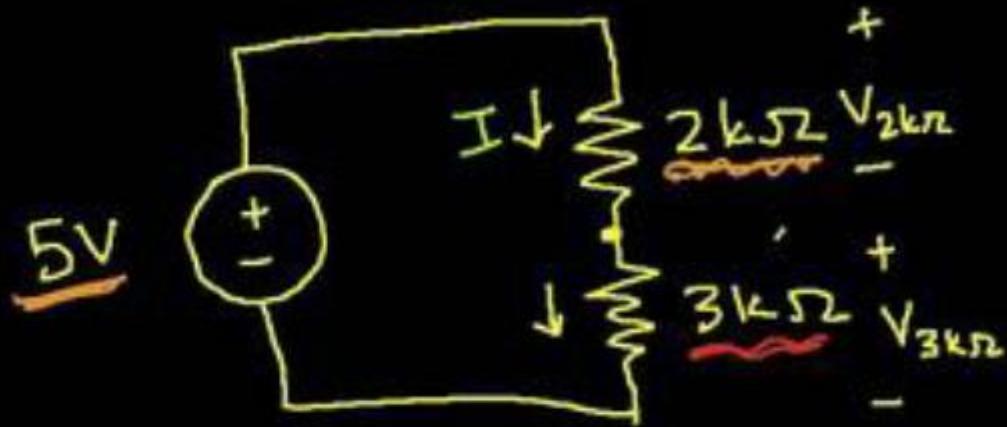
$$= \frac{(2 \times 10^3\Omega)(45V)}{15 \times 10^3\Omega} = \frac{90}{15} = 6V$$

$$V_3 = \frac{R_3 V_{in}}{R_T} = \frac{(8k\Omega)(45V)}{2k\Omega + 5k\Omega + 8k\Omega} = \frac{(8 \times 10^3\Omega)(45V)}{15 \times 10^3\Omega}$$

$$= \frac{360}{15} = 24V$$



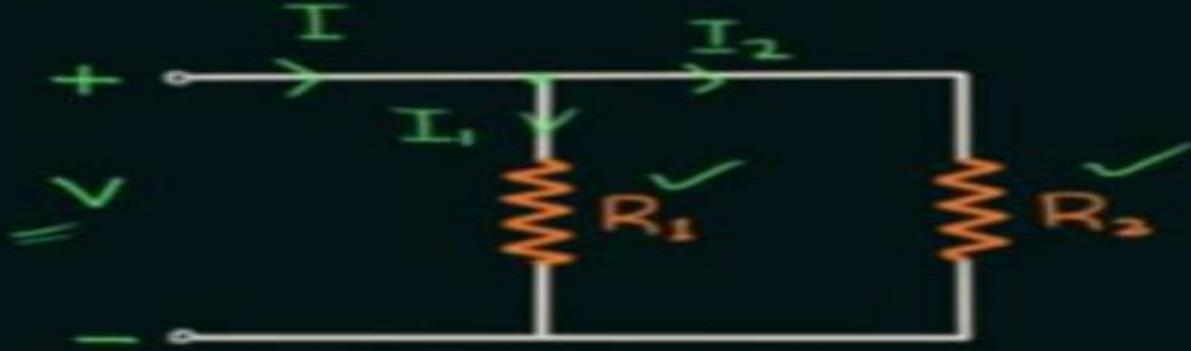
Voltage Division Rules



Current Division Rule

Current division refers to the splitting of **current** between the branches .

parallel $\rightarrow V \rightarrow$ same



$$R_{eq} = \frac{R_1 R_2}{R_1 + R_2}$$

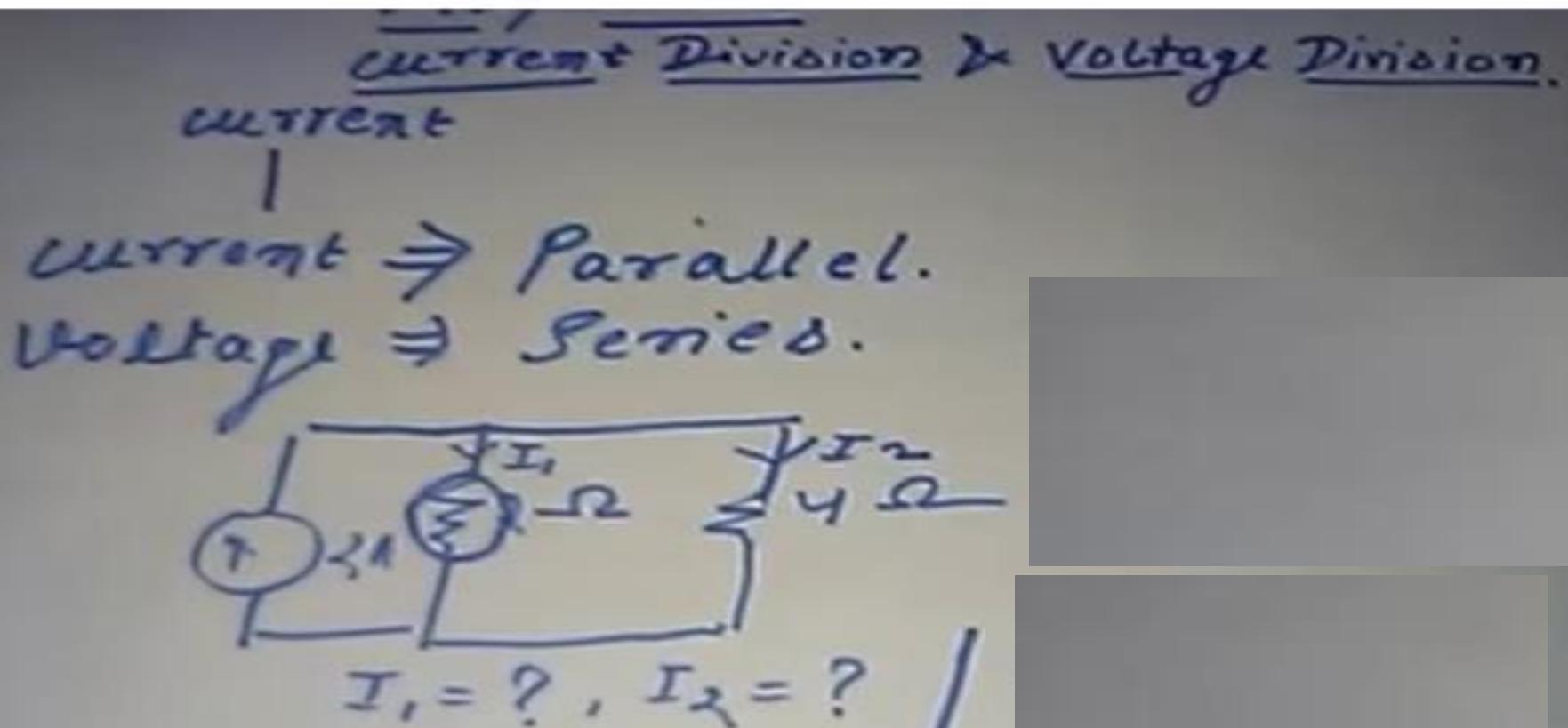
$$V = I R_{eq} \Rightarrow V = \frac{I R_1 R_2}{R_1 + R_2}$$

$$I_1 = \frac{V}{R_1} = \frac{I R_1 R_2}{(R_1 + R_2) R_1} = \frac{I}{R_1 + R_2} \cdot R_1$$

$$I_2 = \frac{V}{R_2} = \frac{I}{R_1 + R_2} \cdot R_2$$

Current Division Rule

Examples-1

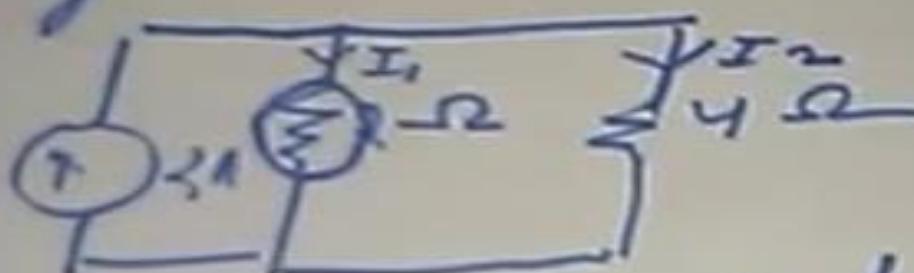


Current Division Rule

Examples-1

current Division & voltage Division.

current
|
current \Rightarrow Parallel.
Voltage \Rightarrow Series.



$$I_1 = ?, \quad I_2 = ?$$

$$I_1 = \left(\frac{4}{2+4} \right) \times 2$$

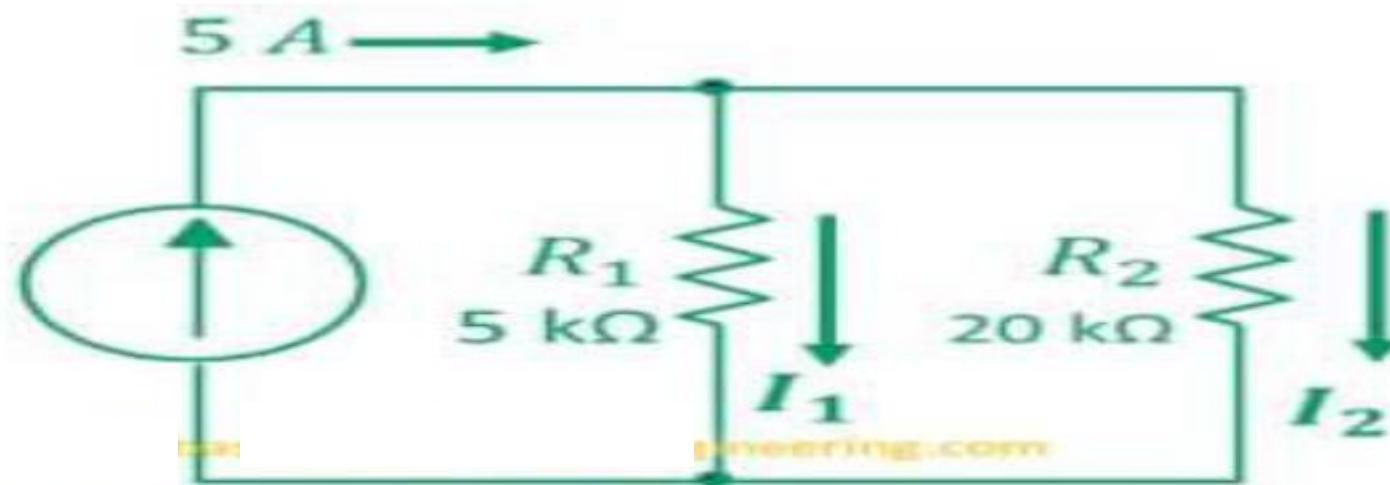
$$I_1 = \frac{4}{6} \times 2 = \frac{4}{3} \text{ Amp.}$$

$$\begin{aligned} I &= I_1 + I_2 \\ &= \frac{4}{3} + \frac{2}{3} = \frac{6}{3} = 2 \end{aligned}$$

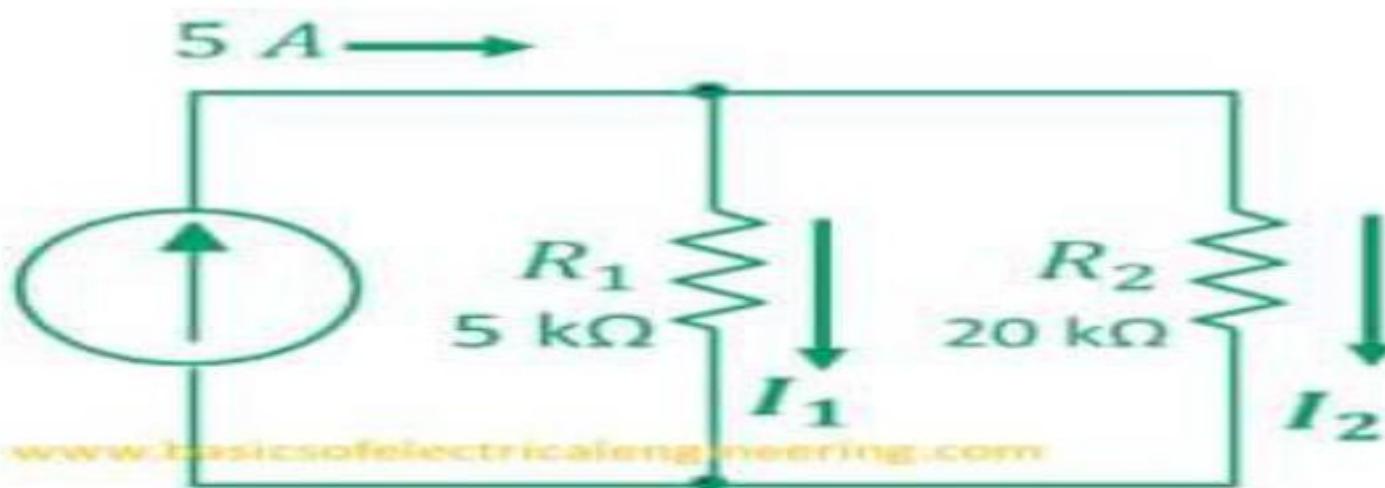
$$I_2 = \left(\frac{2}{6} \right) \times 2$$

$$I_2 = \frac{2}{3}$$

Current Division Rule



Current Division Rule



$$I_1 = \frac{R_2}{R_1 + R_2} * I_t$$

$$I_1 = \frac{20 \text{ k}\Omega}{25 \text{ k}\Omega} * 5 \text{ A}$$

$$I_1 = 4 \text{ A}$$

$$I_2 = \frac{R_1}{R_1 + R_2} * I_t$$

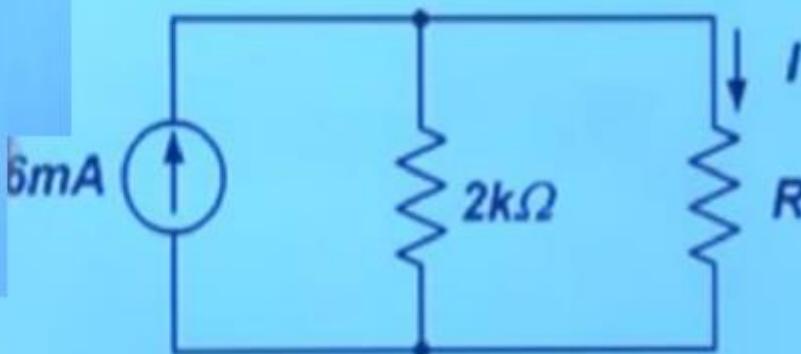
$$I_2 = \frac{5 \text{ k}\Omega}{25 \text{ k}\Omega} * 5 \text{ A}$$

$$I_2 = 1 \text{ A}$$

Current Division Rule

Current division – example 2

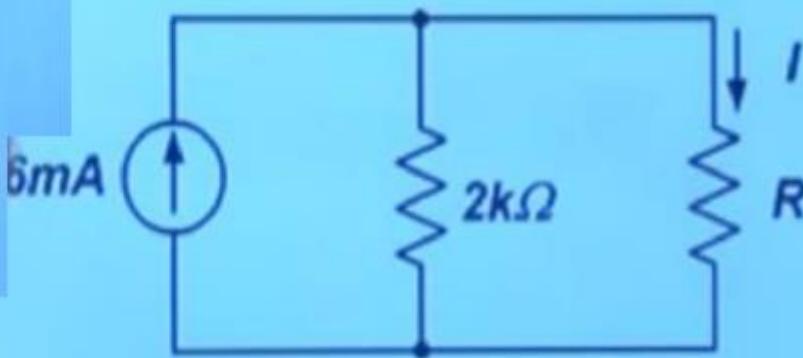
Determine the resistance, R , which makes $I = 2\text{mA}$.



Current Division Rule

Current division – example 2

Determine the resistance, R, which makes $I = 2\text{mA}$.



$$2(R+2\text{k}\Omega) = 12\text{k}\Omega$$

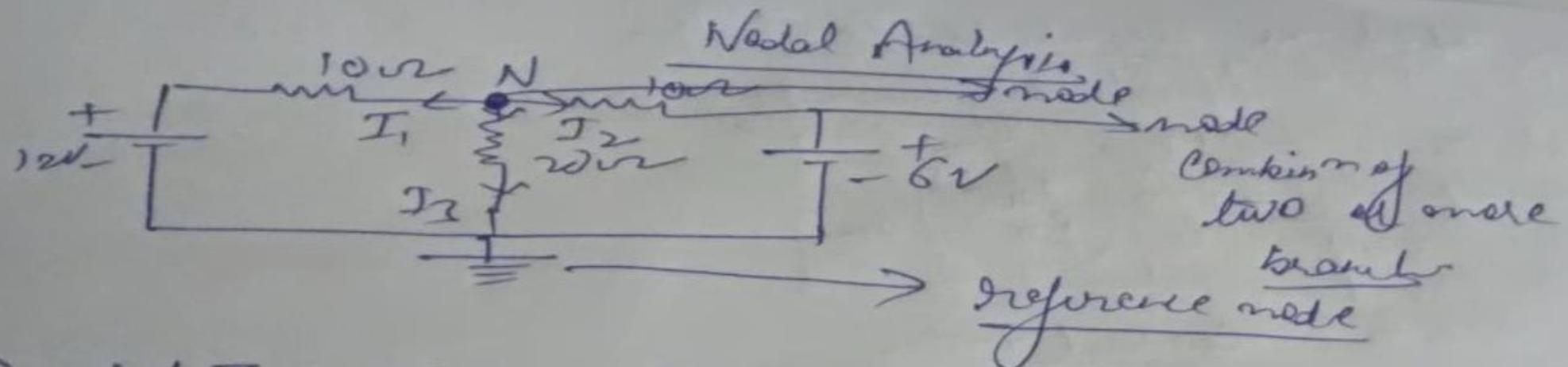
$$R+2\text{k}\Omega = 6\text{k}\Omega$$

$$2\text{mA} = 6\text{mA} \left(\frac{2\text{k}\Omega}{R+2\text{k}\Omega} \right)$$

$$\underline{\underline{R = 4\text{k}\Omega}}$$

Nodal Analysis

Nodal analysis is a method that provides a general procedure for analyzing circuits using node voltages as the circuit variables. **Nodal Analysis** is also called the **Node-Voltage Method**.



Sum of Incoming = Sum of outgoing

$$0 = I_1 + I_2 - I_3$$

$$I_1 + I_2 + I_3 = 0$$

Nodal Analysis

or

$$I_1 + I_2 + I_3 = 0$$
$$\left[\frac{N-12}{10} + \frac{N-0}{20} + \frac{N-6}{10} = 0 \right]$$

$$\frac{\cancel{2N}-24+\cancel{N}+2\cancel{N}+12}{20} = 0$$

$$5N - 36 = 0$$

$$N = \frac{36}{5} \Rightarrow 7.2V$$

$$I_1 = \frac{N-12}{10} \Rightarrow \frac{7.2-12}{10} \Rightarrow 1.2 - \frac{4.8}{10} = -0.48$$

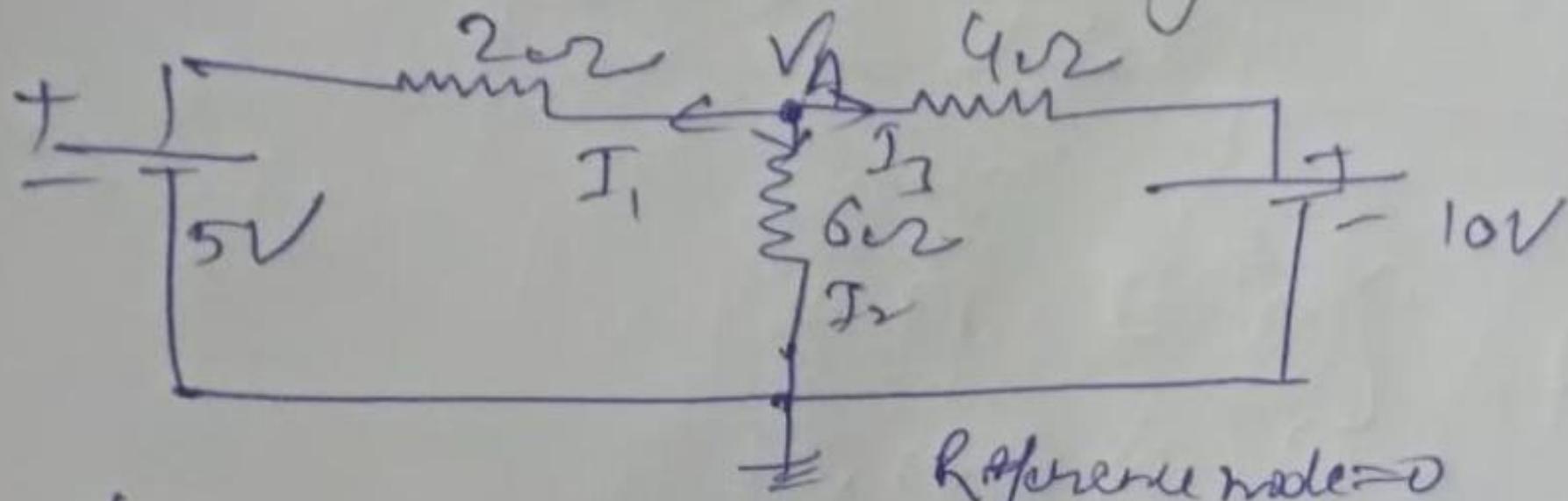
$$I_2 = \frac{N}{20} \Rightarrow \frac{7.2}{20} = 0.36A$$

$$I_3 = \frac{N-6}{10} \Rightarrow \frac{7.2-6}{10} \Rightarrow \frac{1.2}{10} = 0.12A$$

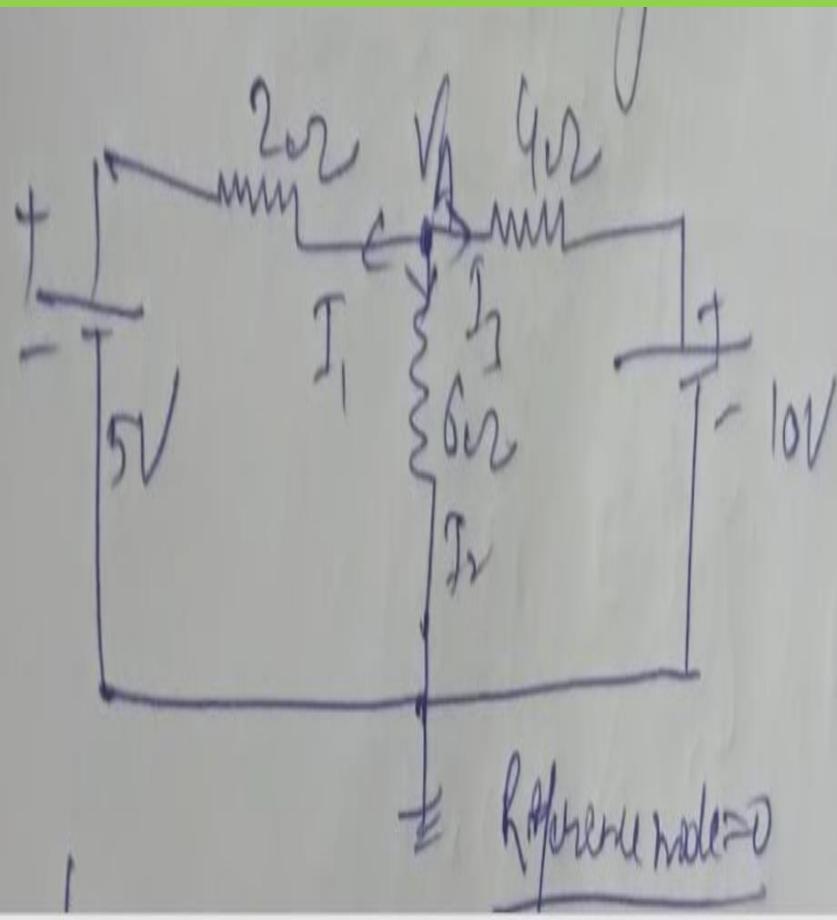
Nodal Analysis

②

Nodal Voltage Analysis
~~Nodal Analysis~~
Nodal Voltage



Nodal Analysis



(outgoing)

$$I_1 + I_2 + I_3 = 0 \quad \{ \text{Kirchhoff's Law} \}$$

$$\frac{V_A - 5}{2} + \frac{V_A}{6} + \frac{V_A - 10}{4} = 0$$

$$\cancel{\frac{6V_A - 30 + 2V_A + 3V_A - 30}{12} = 0}$$

$$11V_A - 60 = 0$$

$$V_A = \frac{60}{11} \rightarrow 5.45$$

$$I_1 = \frac{60 - 5}{2} \rightarrow \frac{45}{2} \rightarrow 22.5 \text{ A}$$

$$I_2 = \frac{60}{6} \rightarrow 10 \text{ A}$$

$$I_3 = \frac{60 - 10}{4} \rightarrow \frac{50}{4} \rightarrow 12.5 \text{ A}$$

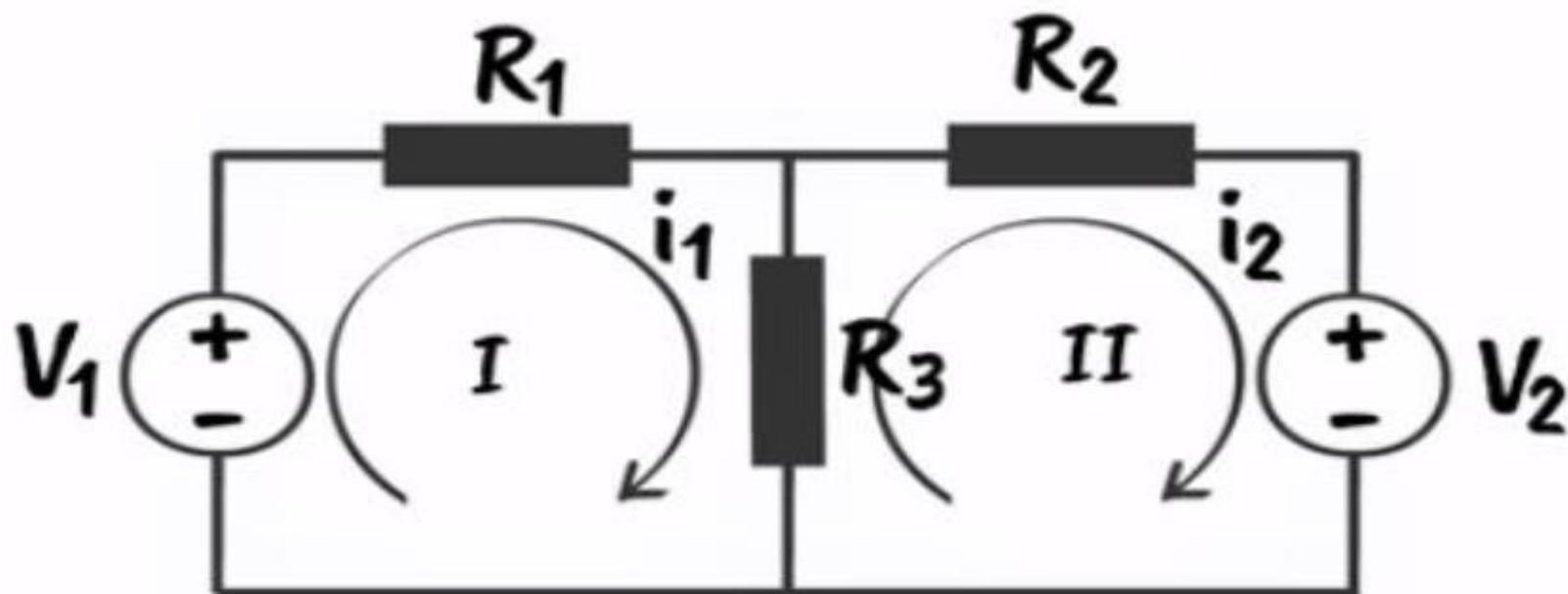
$$1.13$$

$$1.13$$

$$1.13$$

Mesh Analysis

Mesh analysis is a method that is used to solve circuits for the currents at any place in the electrical circuit.

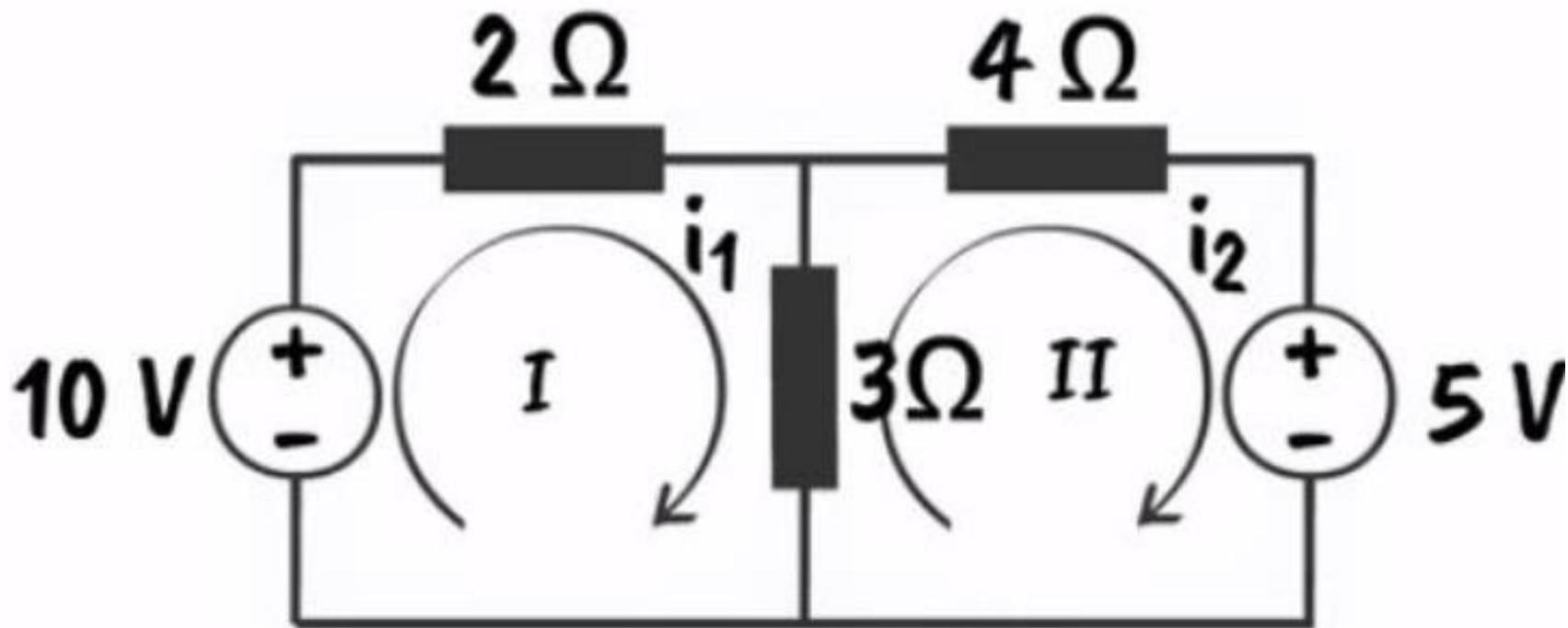


KVL

$$V_1 - i_1 R_1 - (i_1 - i_2) R_3 = 0 \quad \text{---(1)}$$

~~$$- (i_2 - i_1) R_3 - i_2 R_2 - V_2 = 0 \quad \text{---(2)}$$~~

Mesh Analysis

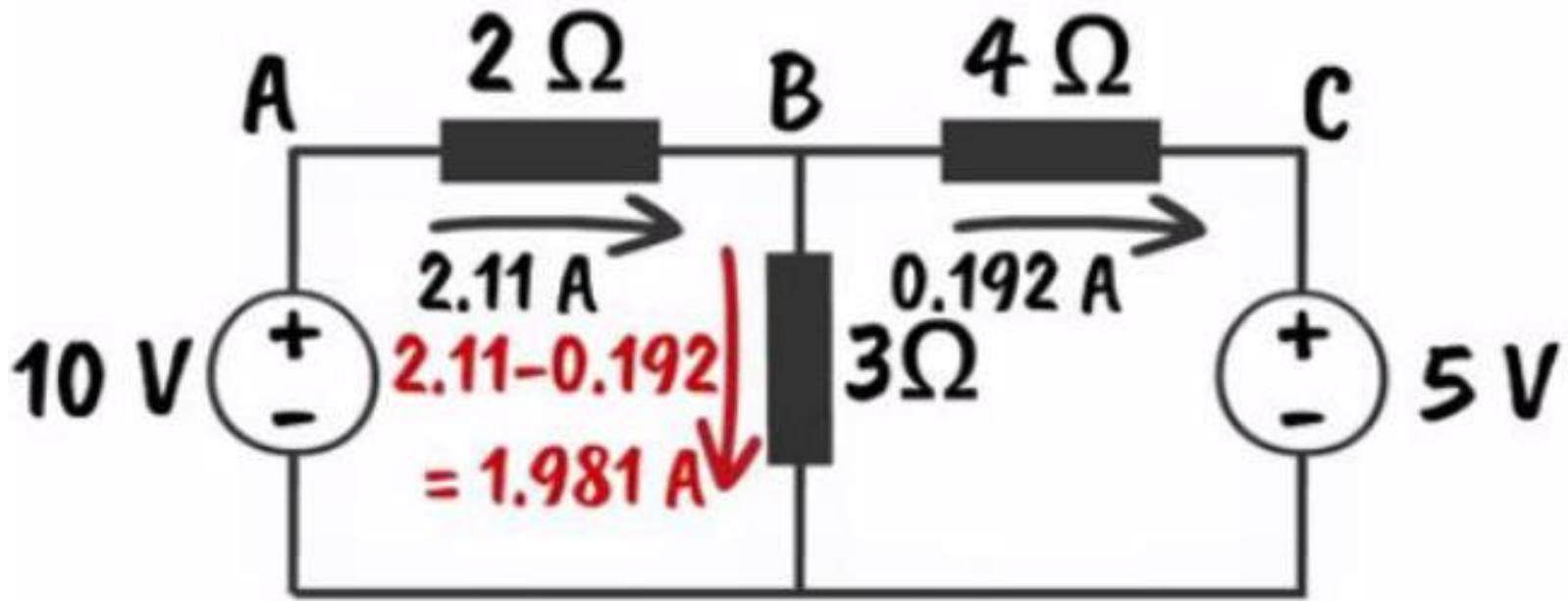


KVL

$$10 - i_1 2 - (i_1 - i_2) 3 = 0 \quad \text{---(3)}$$

$$-(i_2 - i_1) 3 - i_2 4 - 5 = 0 \quad \text{---(4)}$$

Mesh Analysis



KVL

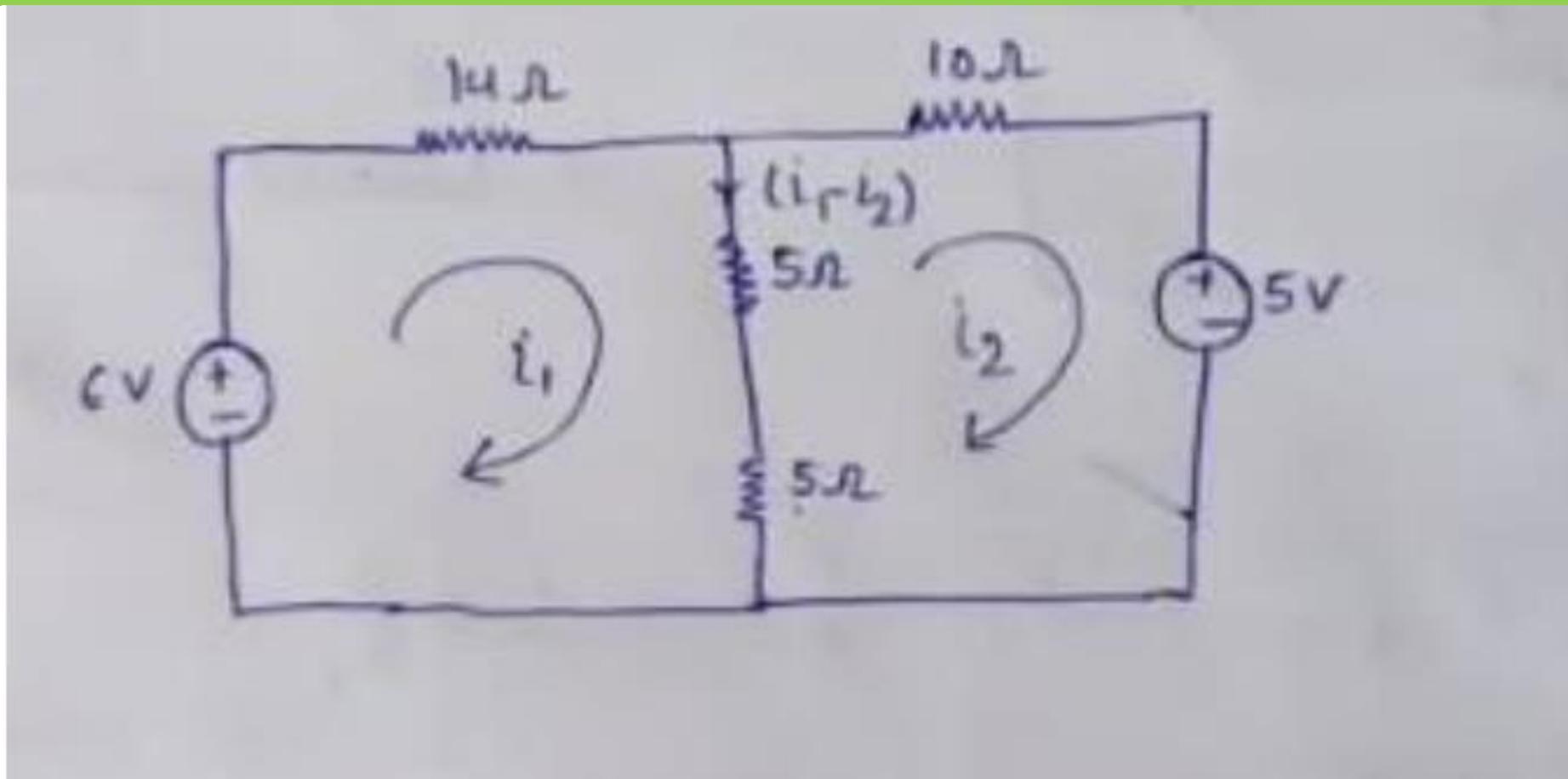
$$10 - i_1 2 - (i_1 - i_2) 3 = 0 \quad \dots (3)$$

$$-(i_2 - i_1) 3 - i_2 4 - 5 = 0 \quad \dots (4)$$

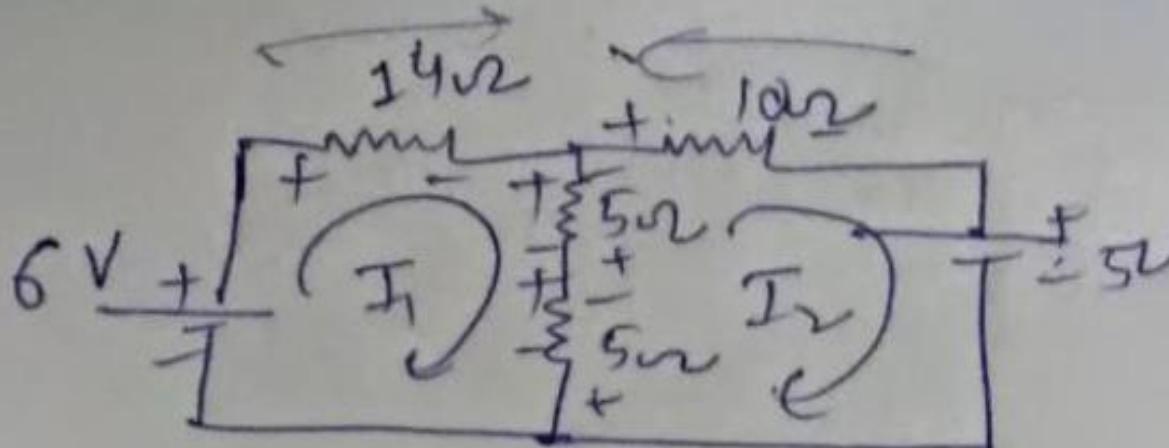
$$i_1 = 2.11 \text{ A}$$

$$i_2 = 0.192 \text{ A}$$

Mesh Analysis



Mesh Analysis



$$I_1 = 184.2 \text{ mA}$$

$$I_2 = -157.89 \text{ mA}$$

$$\begin{cases} +6 - 14I_1 - 5(I_1 - I_2) - 5(I_1 - I_2) = 0 \\ -10I_2 - 5 - 5(I_2 - I_1) - 5(I_2 - I_1) = 0 \end{cases}$$

$I_2 = 157.89 \text{ mA} \leftarrow$
 $I_1 + I_2 \Rightarrow 341.79 \text{ mA}$

Mesh Analysis

$$\begin{aligned}
 & \left. \begin{aligned}
 & -14I_1 - 5I_1 + 5I_2 - 5I_1 + 5I_2 = 0 \\
 & -24I_1 + 10I_2 = 0 \\
 & -24I_1 + 10I_2 = -6 \Rightarrow [24I_1 - 10I_2 = 6] \\
 & -10I_2 - 5 - 5I_2 + 5I_1 - 5I_2 + 5I_1 = 0 \\
 & -20I_2 + 10I_1 = 5 \\
 & [4I_2 + 2I_1 = 1]
 \end{aligned} \right\} \\
 & 12 \times [2I_1 + 4I_2 = 1] \\
 & \left. \begin{aligned}
 & 24I_1 - 48I_2 = 12 \\
 & 20I_1 - 10I_2 = 6 \\
 & \hline
 & -38I_2 = 18
 \end{aligned} \right\} \quad (1) \\
 & \frac{24I_1 - 10x6}{38} = 6 \\
 & I_2 = \frac{-6}{38} \\
 & I_2 = -0.1578A \\
 & I_2 = -0.1578A
 \end{aligned}$$

$$\begin{aligned}
 & \cancel{\rightarrow} \quad \rightarrow \\
 & I_1 = 184.2mA \\
 & I_2 = -157.89mA \\
 & I_2 = 157.89mA \leftarrow \\
 & I_1 + I_2 \Rightarrow 341.79mA
 \end{aligned}$$

Independent Source

Independent Source

The Source which does not depend on any other quantity (like voltage and current) in the circuit.



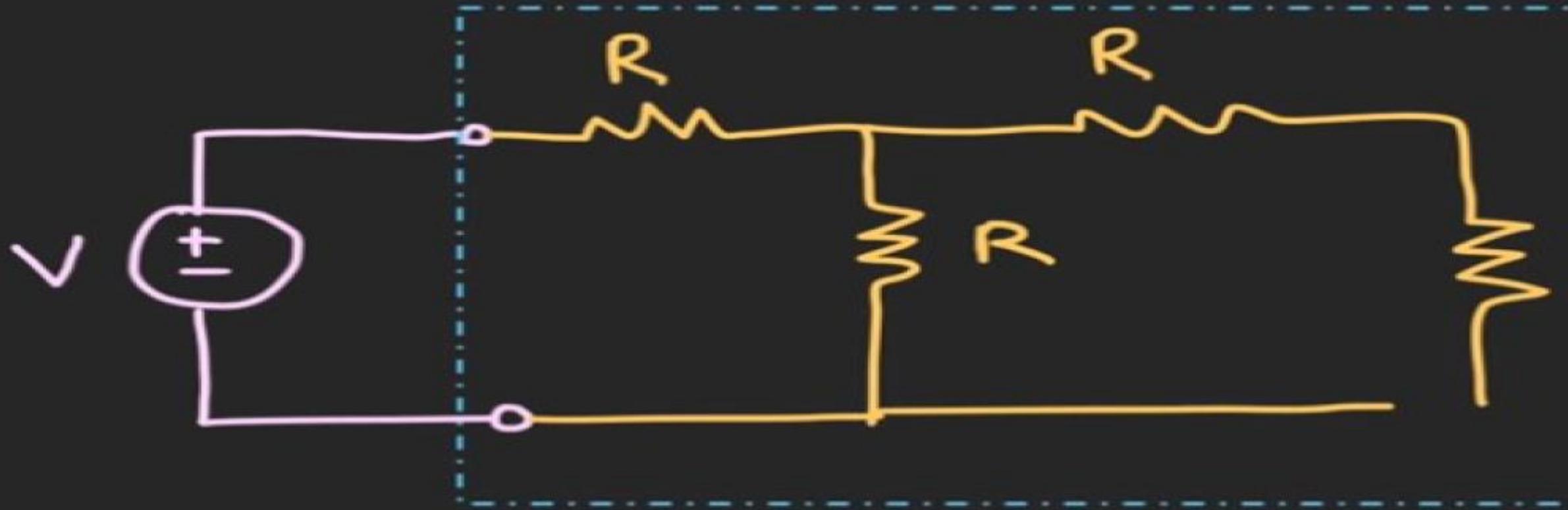
Voltage Source



Current Source

Independent Source

Independent Source



Dependent Source

Dependent Source

The Source whose output value depends upon the voltage or current at some other part of the circuit.



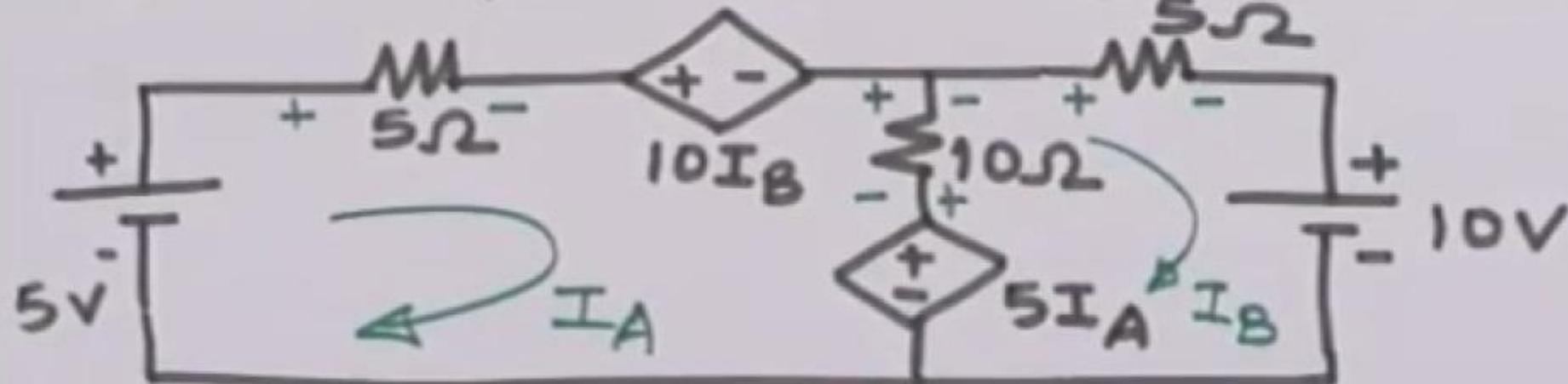
Dependent Voltage Source



Dependent Current Source

Discussions

Obtain I_A and I_B using Mesh Analysis



Apply KVL to mesh ①

$$5 - 5I_A - \cancel{10I_B} - 10I_A + \cancel{10I_B} - 5I_A = 0$$

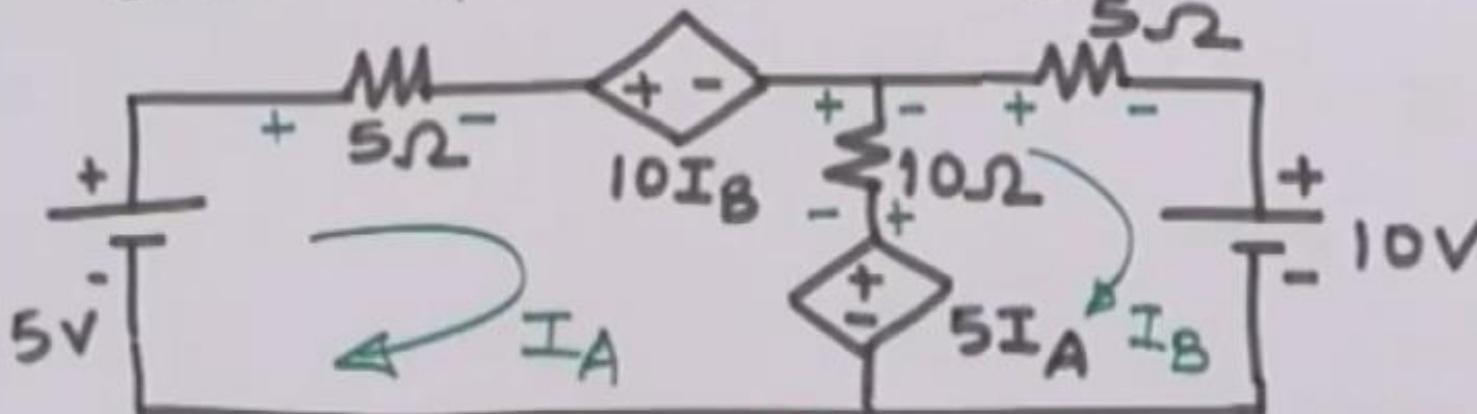
$$5 - 20I_A = 0$$

$$5 = 20I_A$$

$$\boxed{I_A = 0.25A}$$

Discussions

Obtain I_A and I_B using Mesh Analysis.



Apply KVL to mesh ①

$$5 - 5I_A - \cancel{10I_B} - 10I_A + \cancel{10I_B} - 5I_A = 0$$

$$5 - 20I_A = 0$$

$$5 = 20I_A$$

$$\boxed{I_A = 0.25A}$$

Apply KVL to mesh ②

$$-5I_B - 10 + 5I_A - \cancel{10I_B} + \cancel{10I_A} = 0$$

$$\therefore 15I_A - 15I_B = 10$$

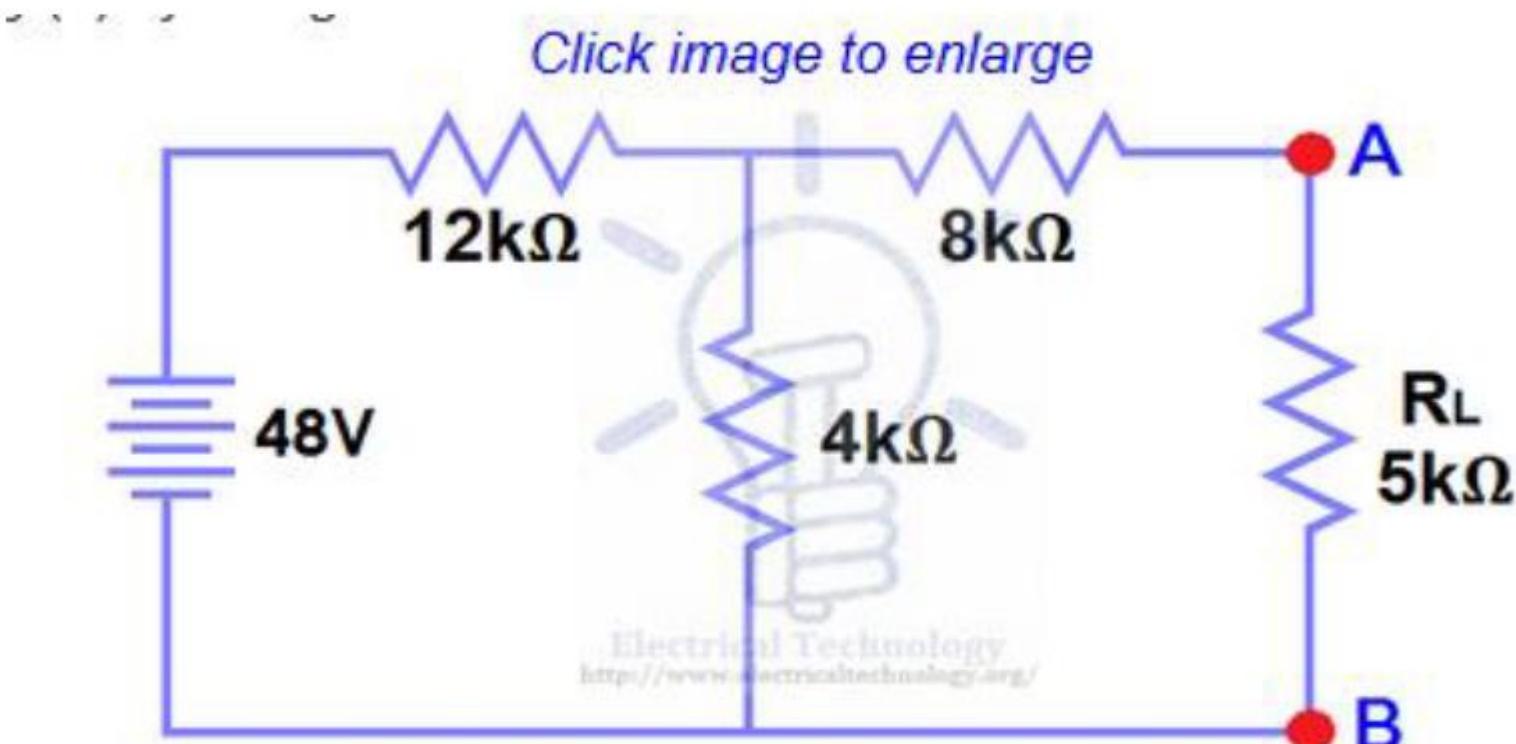
$$\therefore 15(0.25) - 15I_B = 10$$

$$3.75 - 10 = 15I_B$$

$$\therefore \boxed{I_B = -0.4167A}$$

Thevenin Theorem

Calculate current across 5Kohm using thevenin theorem



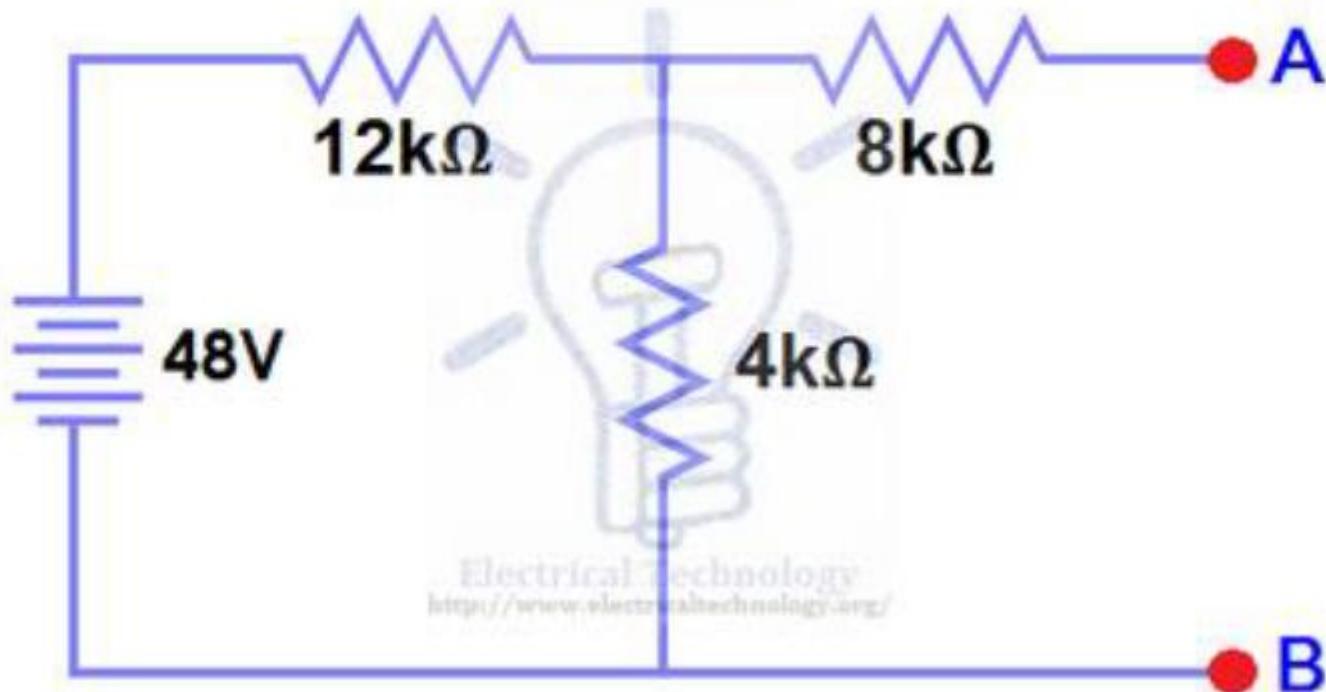
Thevenin's Theorem. Easy Step by Step Procedure with Example (Pictorial Views)

Thevenin Theorem

Step 1.

Open the **5kΩ load resistor** (Fig 2).

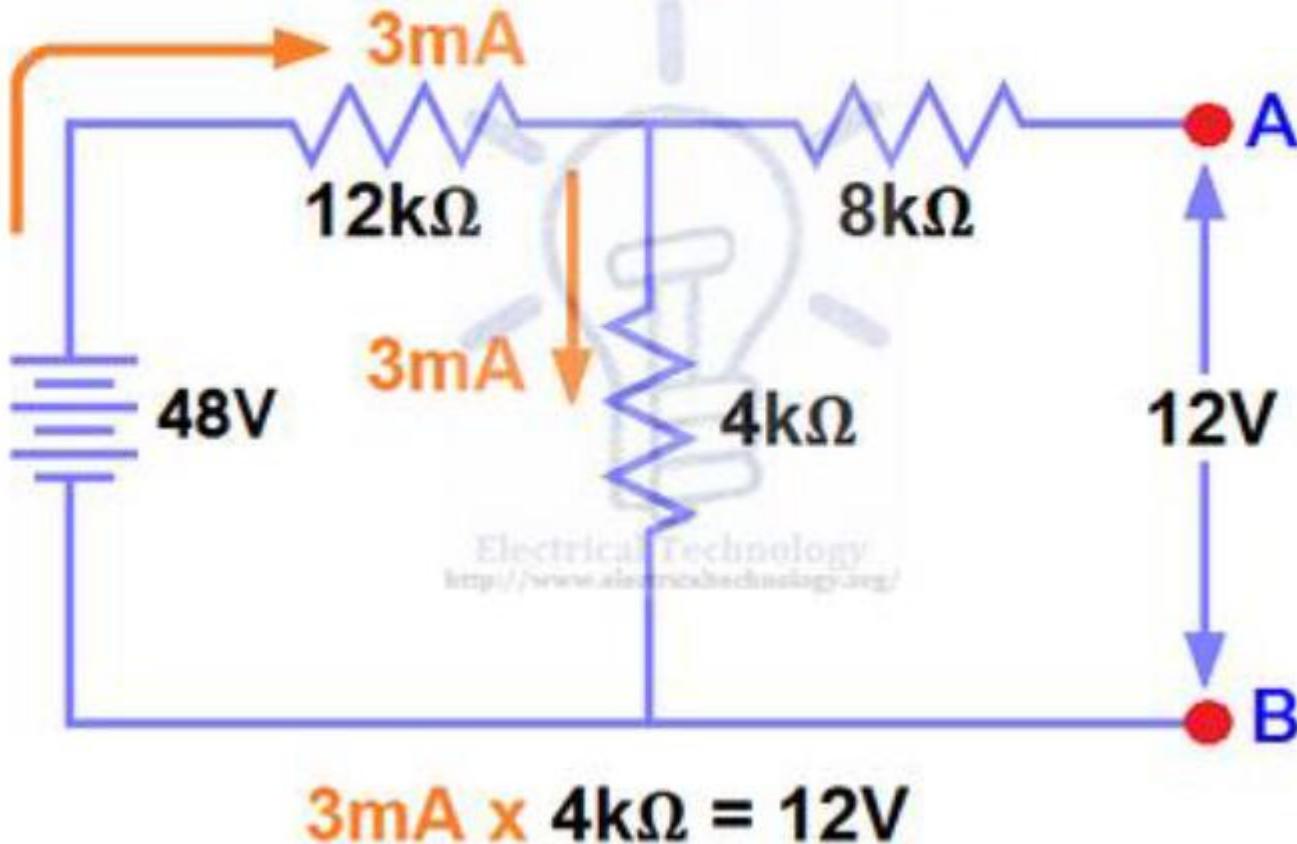
Click image to enlarge



Thevenin Theorem

$$V_{TH} = 12V$$

Click image to enlarge



Total Voltage/ Total Resistance= Total Current

*No Current flow through- 8kohm

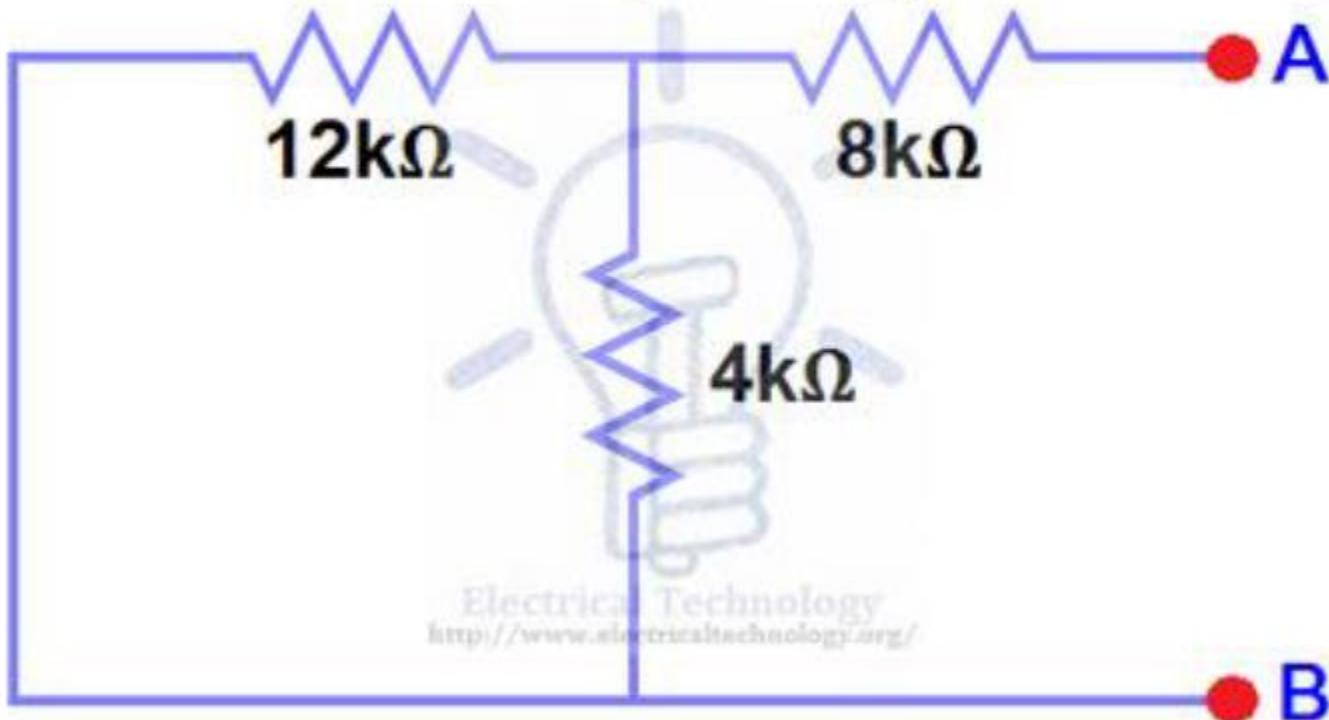
*Voltage Across 4kohm will be same- As Across A and B terminal

Thevenin Theorem

Step 3.

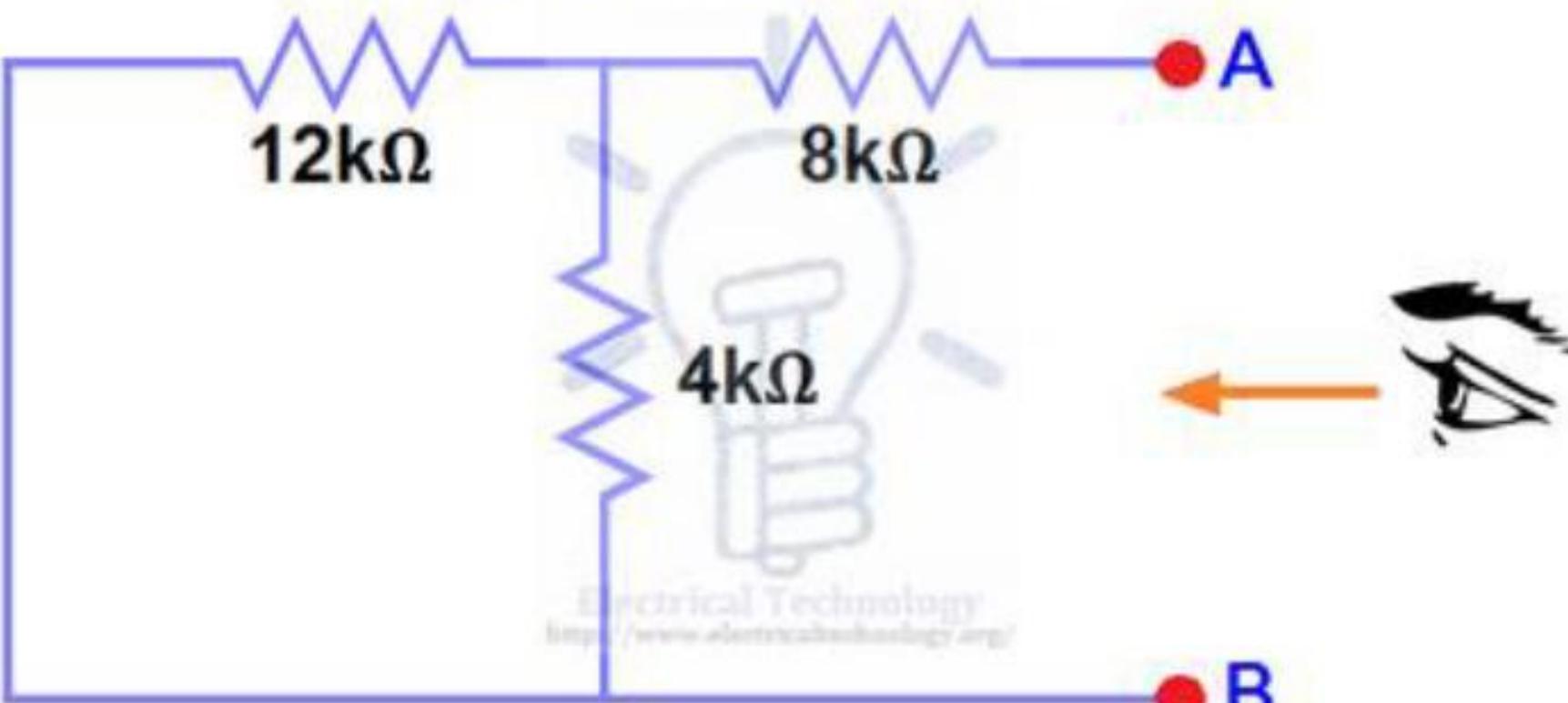
Open current sources and short voltage sources as shown below. Fig (4)

Click image to enlarge



Thevenin Theorem

Click image to enlarge



$$= 8\text{k}\Omega + (4\text{k}\Omega \parallel 12\text{k}\Omega) \rightarrow = 8\text{k}\Omega + 3\text{k}\Omega$$

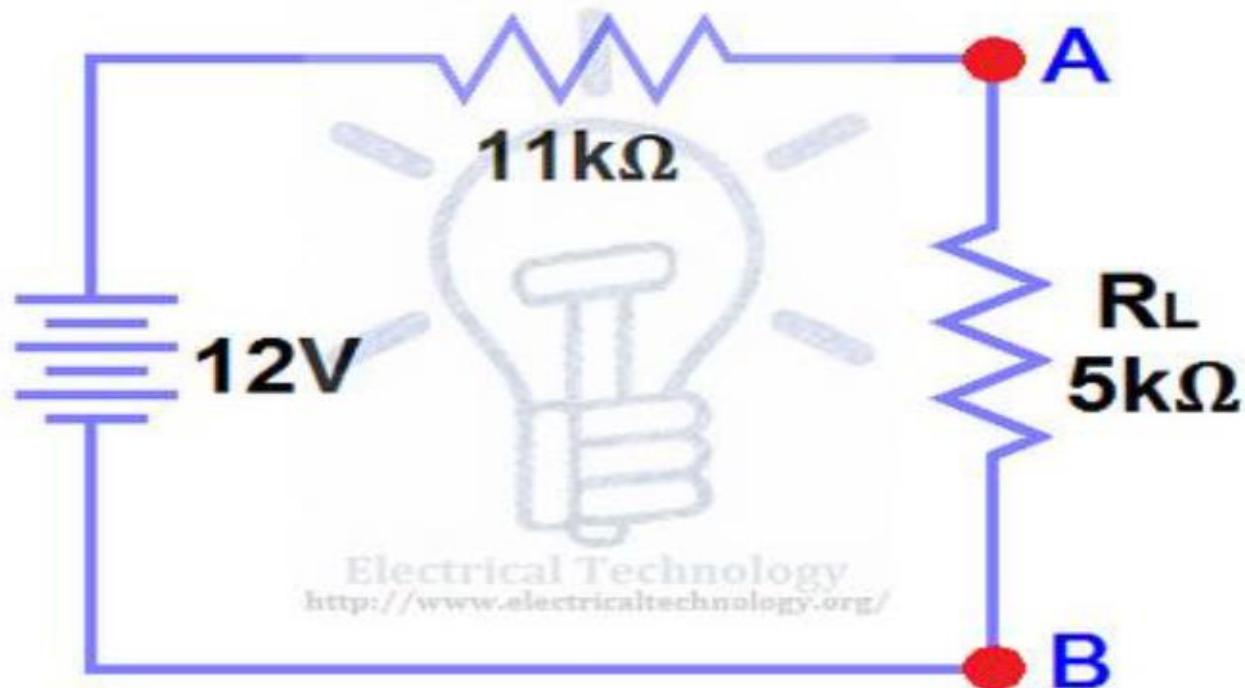
$$R_{TH} = 11\text{k}\Omega$$

Thevenin Theorem

Step 5.

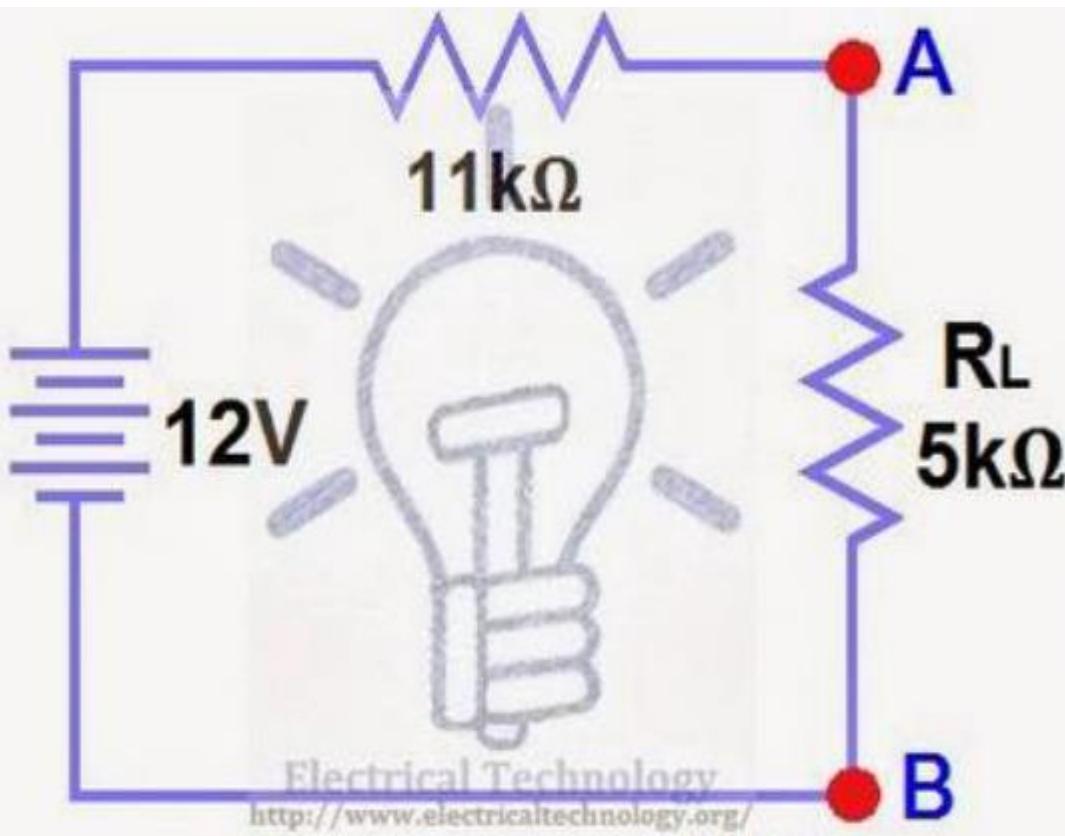
Connect the R_{TH} in series with Voltage Source V_{TH} and re-connect the load resistor. This is shown in fig (6) i.e. Thevenin circuit with load resistor. This is the Thevenin's equivalent circuit

Click image to enlarge



Thevenin's equivalent circuit

Thevenin Theorem



$$I_L = \frac{V_{TH}}{R_{TH} + R_L} = \frac{12V}{11k\Omega + 5k\Omega}$$

$$I_L = 0.75mA$$

$$V_L = I_L \times R_L$$

$$V_L = 0.75mA \times 5k\Omega$$

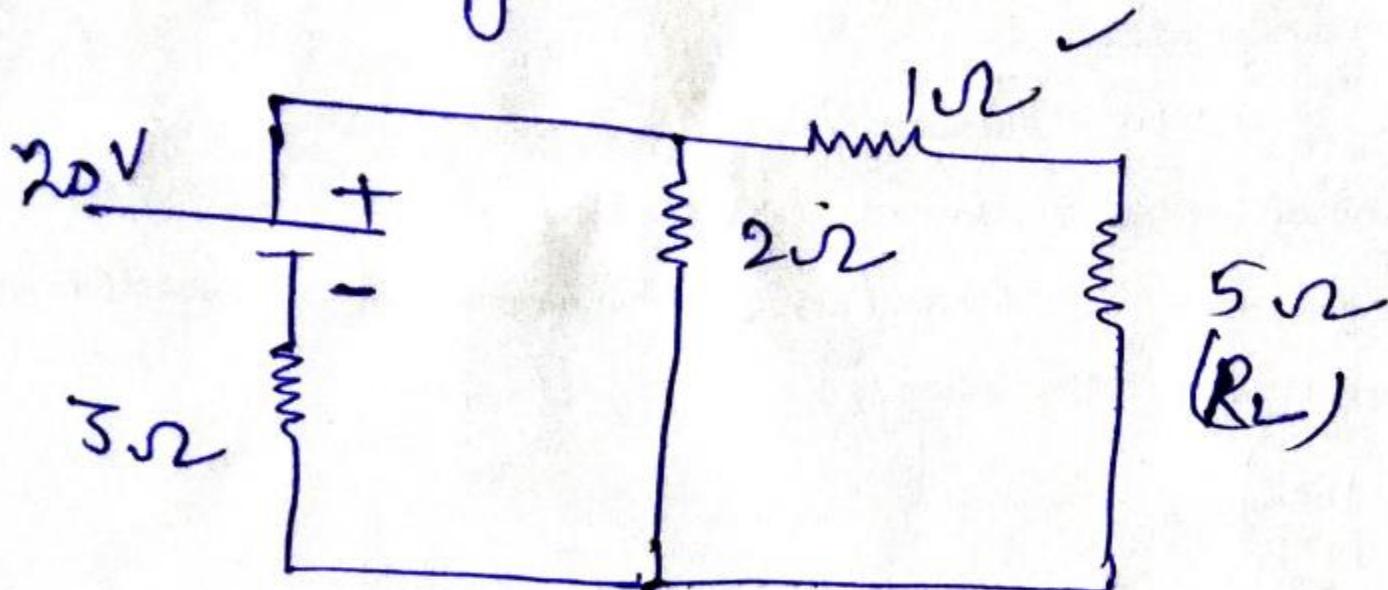
$$V_L = 3.75V$$

Norton Theorem



~~#### NORTON Theorem ####~~

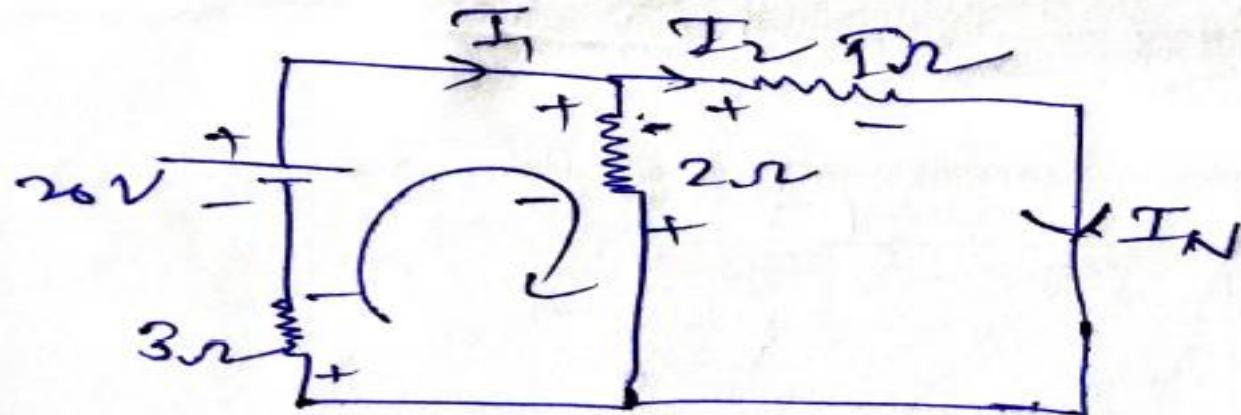
find the current through $5\ \Omega$
using norton's theorem?



Norton Theorem

bohr:

Remove load resistor shell the terminal



$$+20 - 2(I_1 - I_2) - 3I_1 = 0 \quad (1)$$

$$-1 \cdot I_2 - 2(I_2 - I_1) = 0 \quad (2)$$

$$\Rightarrow -I_2 - 2I_2 + 2I_1 = 0 \Rightarrow \frac{2I_1 = 3I_2}{I_1 = 1.5I_2}$$

put in ①

$$+20 - 2(1.5I_2 - I_2) - 3I_1 = 0 \quad (1)$$
$$+20 - 2(0.5I_2) - 3I_1 = 0 \quad (2)$$
$$+20 - I_2 - 3I_1 = 0 \quad (3)$$
$$+20 - I_2 - 4.5I_2 = 0$$

Norton Theorem

(2)

$$+20 - I_2 - 4.5I_2 = 0$$

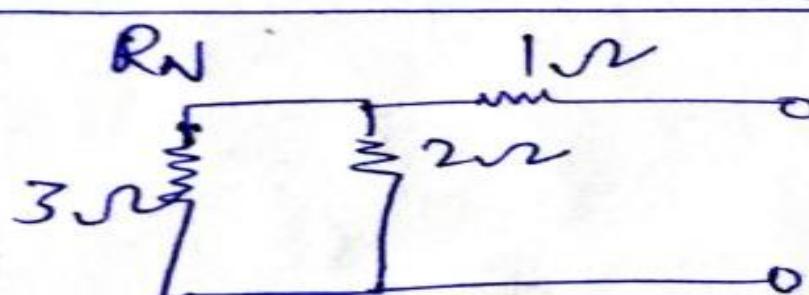
$$20 = 5.5I_2$$

$$\boxed{\frac{20}{5.5} = I_2} \Rightarrow \boxed{3.63 = I_2}$$

$$I_1 = 1.5 I_2$$

$$\boxed{I_1 \Rightarrow 1.5 \times 3.63 \Rightarrow 5.45A}$$

$$\boxed{I_N = I_2 = 3.63A}$$



Remove load

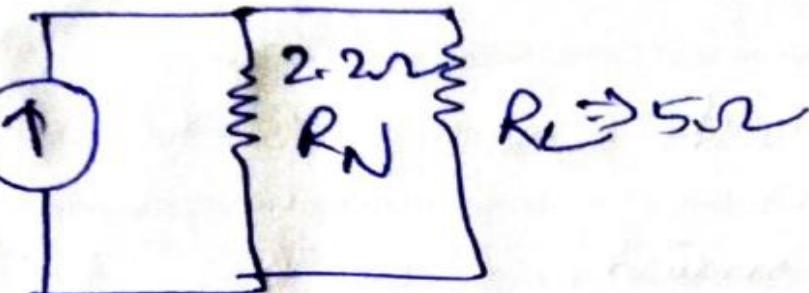
$$\Rightarrow \frac{3 \times 2}{3 + 2} + 1$$

$$\Rightarrow \frac{6}{5} + 1 \Rightarrow 2.2\Omega$$

Norton Theorem

③

3.63 A
(I_N)



③

$$I_{R_L} \Rightarrow \frac{I_N \cdot R_N}{R_N + R_L}$$

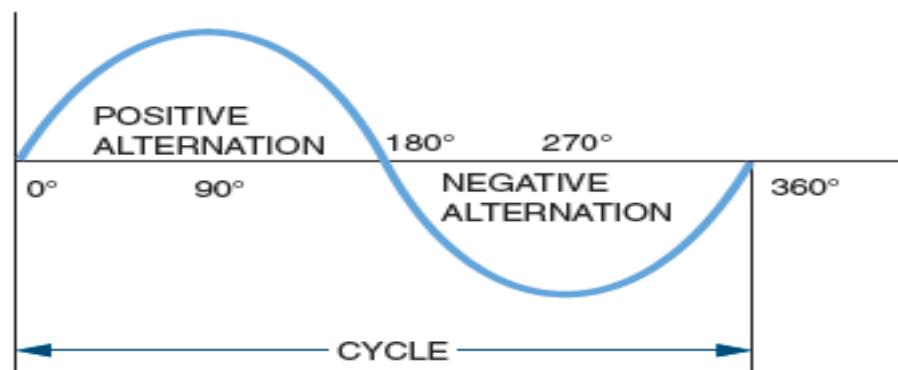
$$\Rightarrow \frac{3.63 \times 2.2}{2.2 + 5}$$

$$I_{R_L} \Rightarrow 1.109 \text{ A}$$

Fundamentals of A.C. circuits

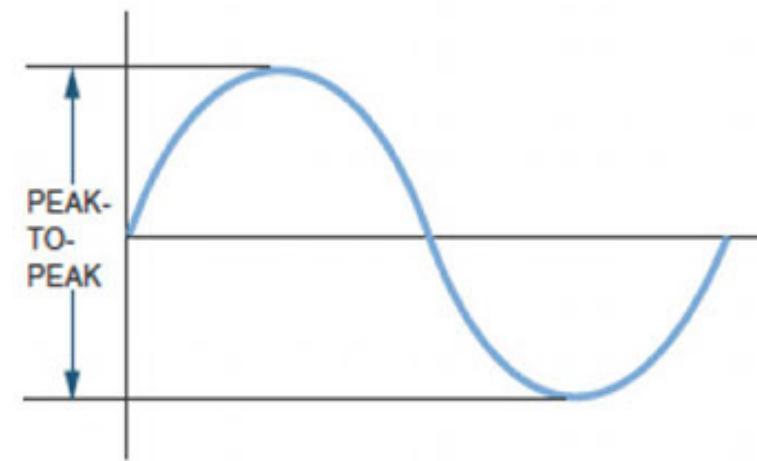
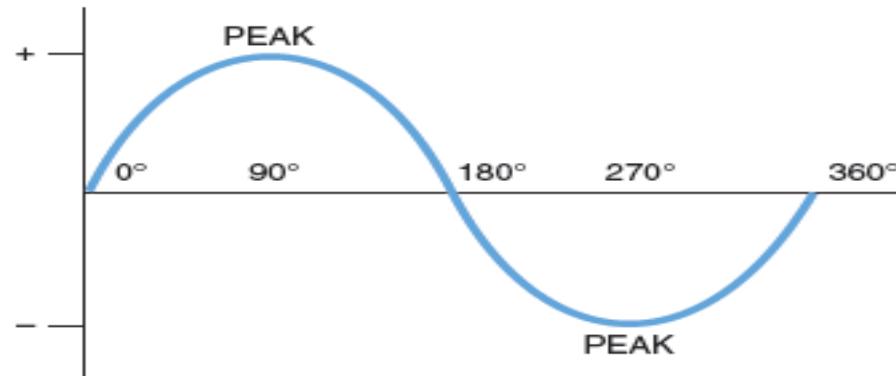
Fundamentals of A.C. circuits

1. Each time an AC generator moves through one complete revolution, it is said to complete **one cycle**.
2. The two half of a cycle are referred as **alternations**.
3. One complete cycle per second is defined as a **hertz**.



AC Values

- **Peak value:** Absolute value of the point with the greatest amplitude.
- **Peak to Peak value:** Vertical distance b/w 2 peaks.
- The amplitude of an AC waveform is its height as depicted on a graph over time. An amplitude measurement can take the form of peak, peak-to-peak.

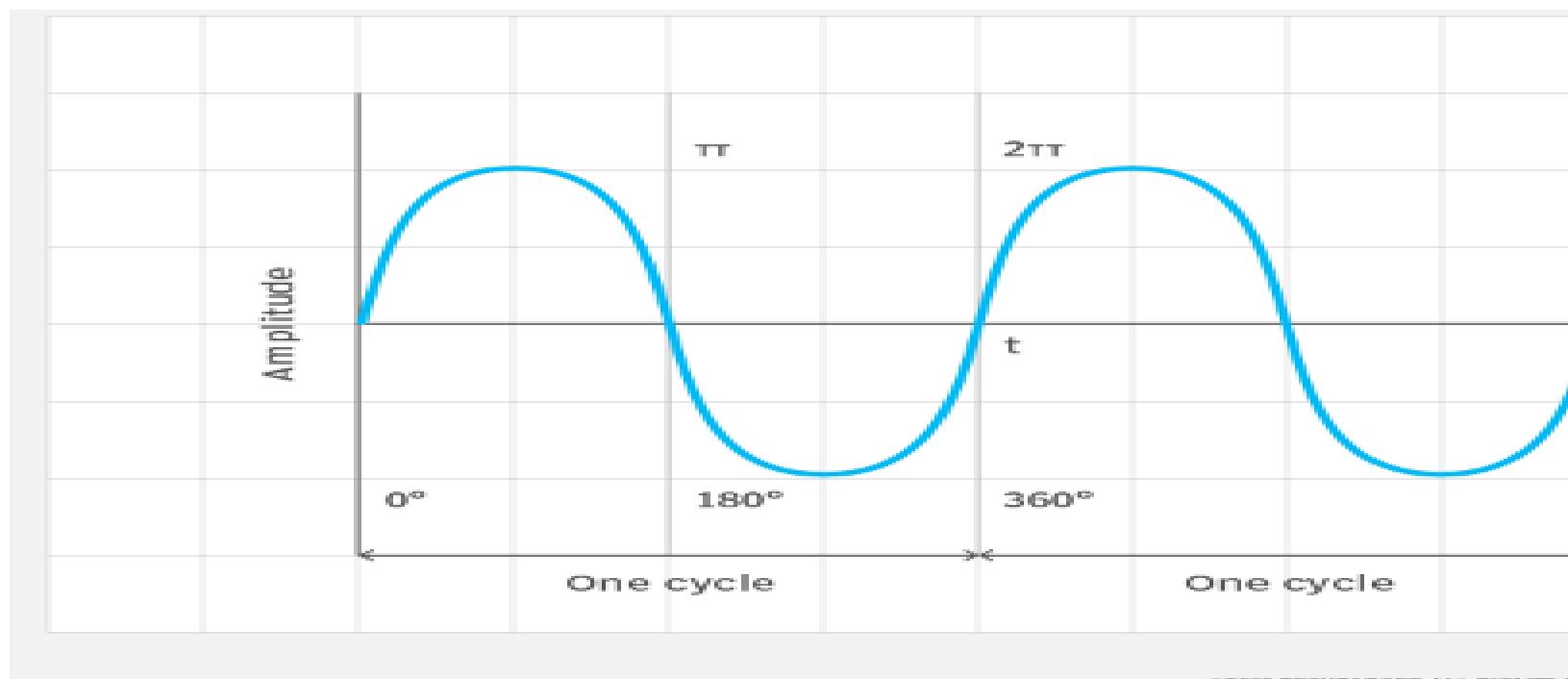


Fundamentals of A.C. circuits

- A phase is the position of a wave at a point in time (instant) on a waveform cycle.
- It provides a measurement of exactly where the wave is positioned within its cycle, using either degrees (0-360) or radians (0- 2π).

Fundamentals of A.C. circuits

- The wave starts at the 0-degree phase and has no amplitude.
- The wave reaches positive peak amplitude at the 90-degree phase.



AC Values (cont'd.)

- **Effective value of alternating current** is the amount that produces same degree of heat in a resistance as produced by direct current. It is also referred as rms value.

$$E_{\text{rms}} = 0.707 E_p$$

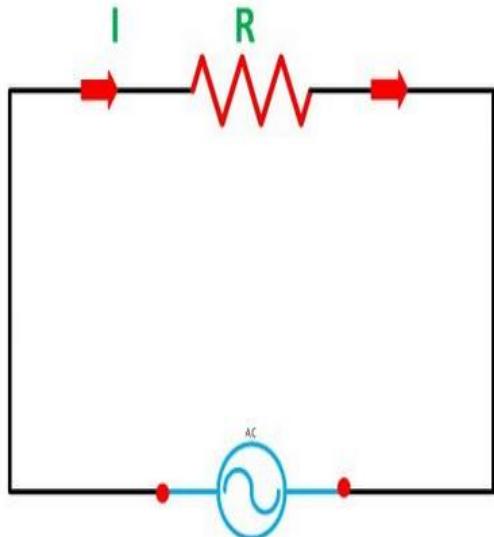
where: E_{rms} = rms or effective voltage value

Average Value of alternating current

$$I_{\text{av}} = 0.637 I_m$$

The average current of a sinusoidal waveform is determined by multiplying the peak voltage value by **0.637**.

Pure Resistive AC Circuit



$$v = V_m \sin\omega t$$

$$v = V_m \sin\omega t \dots \dots \dots (1)$$

$$i = \frac{v}{R} = \frac{V_m}{R} \sin\omega t \dots \dots \dots (2)$$

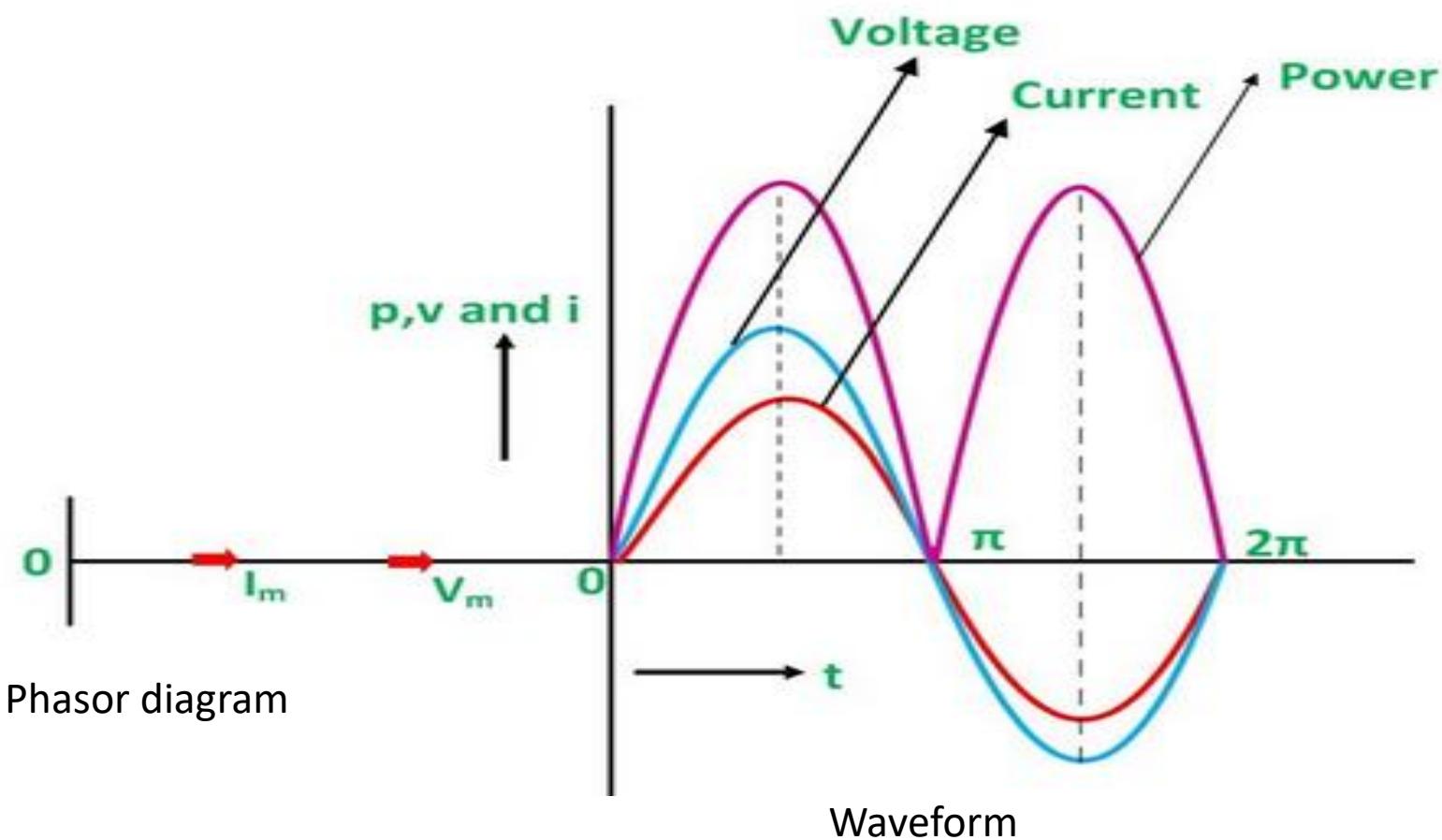
$$i = I_m \sin\omega t \dots \dots \dots (3)$$

$$v = V_m \sin \omega t \dots\dots\dots(1)$$

$$i = I_m \sin \omega t \dots \dots \dots (3)$$

Instantaneous power, $p = vi$

$$p = (V_m \sin \omega t)(I_m \sin \omega t)$$



PN Junction Diode

- **Semiconductor:** A semiconductor material has an electrical conductivity value falling between that of a conductor, such as metallic copper, and an insulator, such as glass.
- The semiconductor in its pure form is known as **intrinsic semiconductor**.
- When a chemical impurity is added to an intrinsic semiconductor, then the resulting semiconductor is known as **extrinsic semiconductor**.

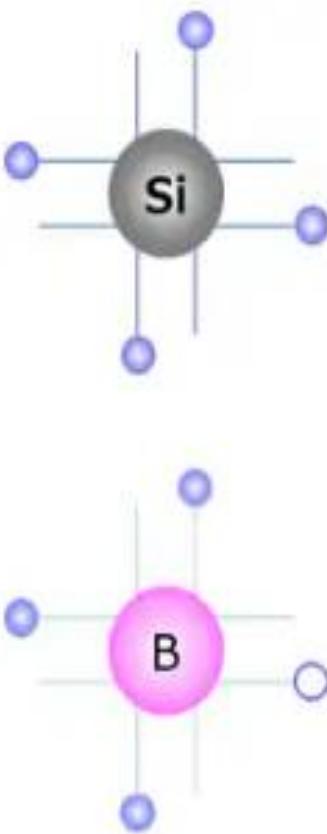
PN Junction Diode

- **P type SEMICONDUCTOR:**

- A p-type semiconductor is an intrinsic semiconductor doped with boron or indium.
- The majority of carriers in p-type semiconductors are holes.
- Electrons are minority carriers in a p-type semiconductor.
- In a p-type semiconductor, the hole density is much greater than the electron density.
- In an n-type semiconductor an intrinsic semiconductor doped with phosphorus or antimony as impurity.

PN Junction Diode

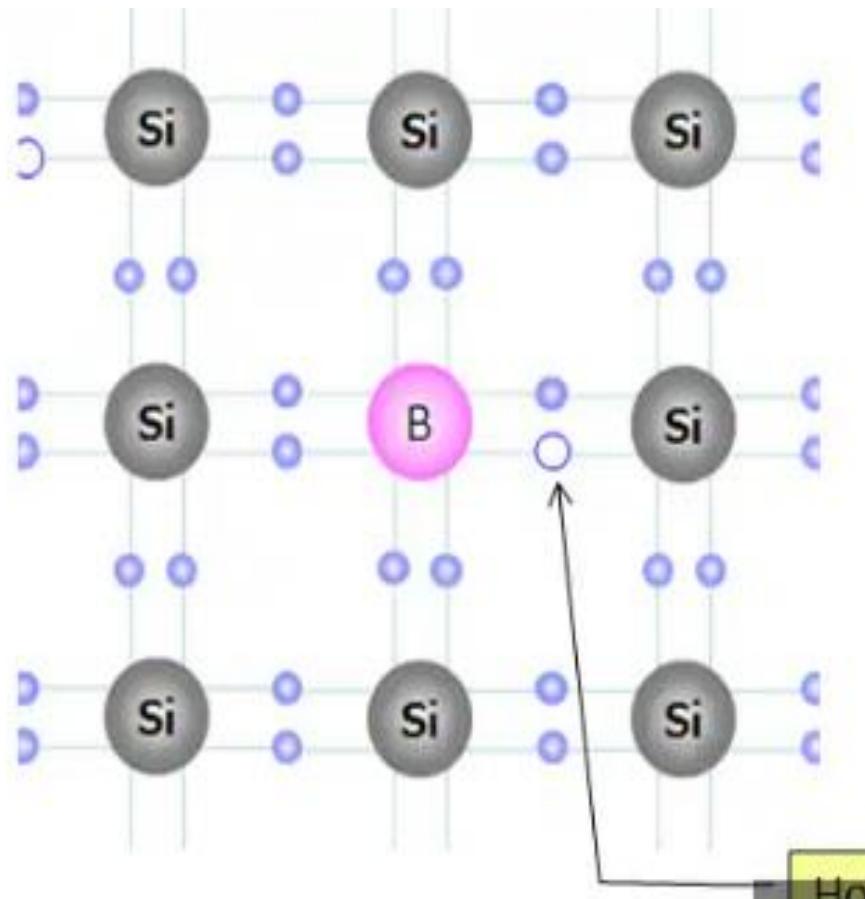
Silicon (Si):
Four valence
electrons



Boron (B):
Three valence
electrons



Adding boron to
pure silicon crystal
results in lack of an
electron. And it
becomes a hole.

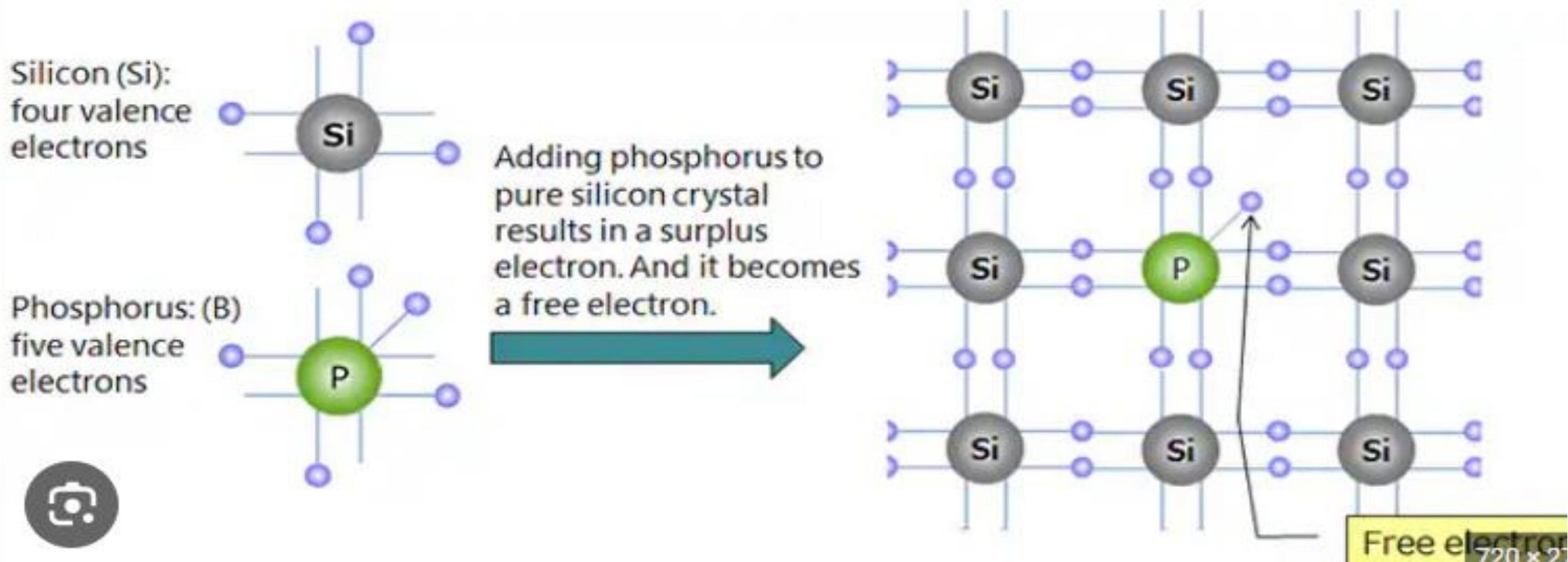


PN Junction Diode

- **N TYPE SEMICONDUCTOR:**

- The majority of charge carriers in n-type semiconductors are electrons.
- Holes are minority carriers in a n type semiconductor.
- In the n type of semiconductor, the electron density is much greater than the hole density.

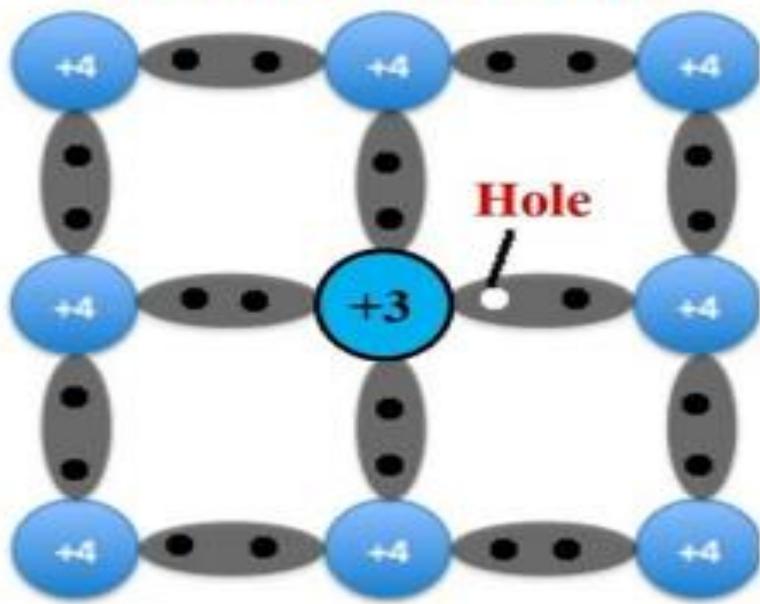
PN Junction Diode



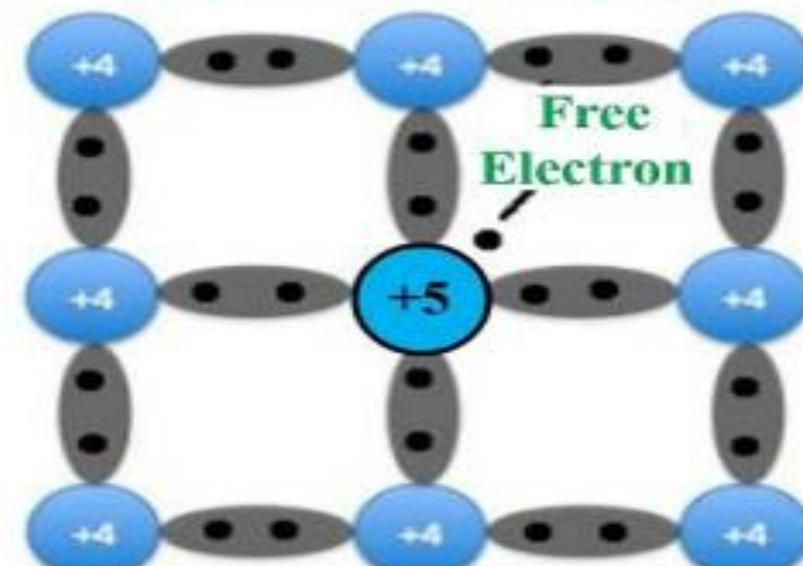
PN Junction Diode

Semiconductors

P-Type
Semiconductor

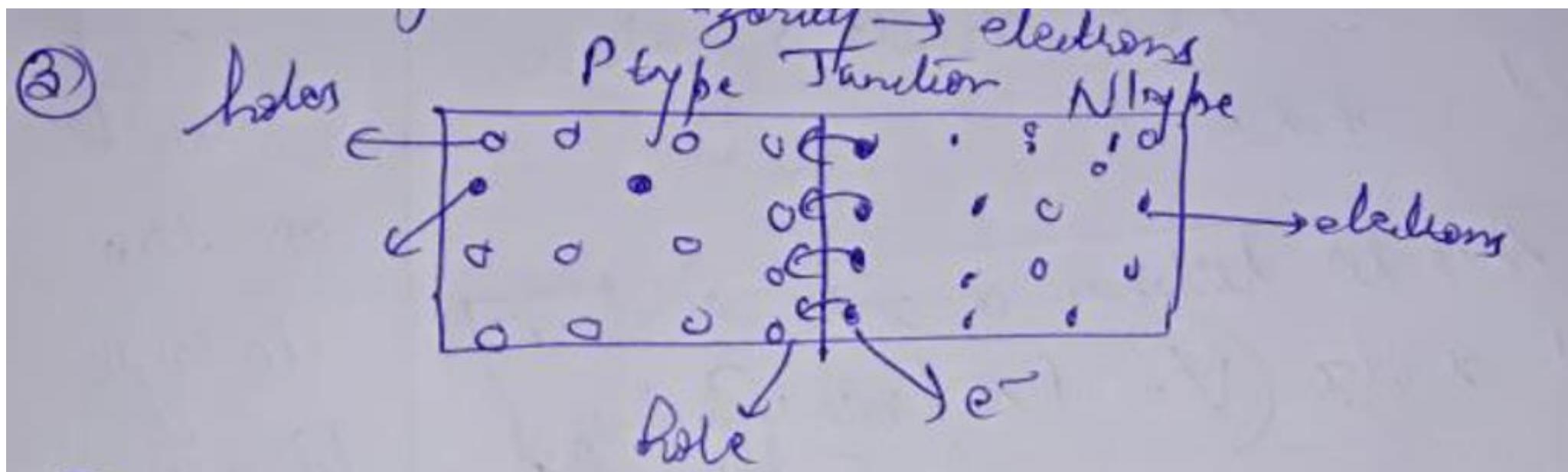


N-Type
Semiconductor



PN Junction Diode

- Joining P type and N Type semiconductor create a device is called P-N Junction diode.
- P type-- majority- Holes
- N Type- Majority- Electrons



PN Junction Diode

4. Electrons Move Towards holes
5. It moves itself & Diffuse. So, it neutralise holes.
6. Electrons move so there exist some current which is called as diffusion current. {moment current}
7. This process is called as diffusion & current is known as diffusion current.
8. In P Type holes vanish/ neutralise electrons near the junction which are not present now.

PN Junction Diode

9. Electrons move due to which positive ions are created.
10. Shortage of charges in layer is called Depletion layer.{Deplete}
11. Here + to - create an electric field.

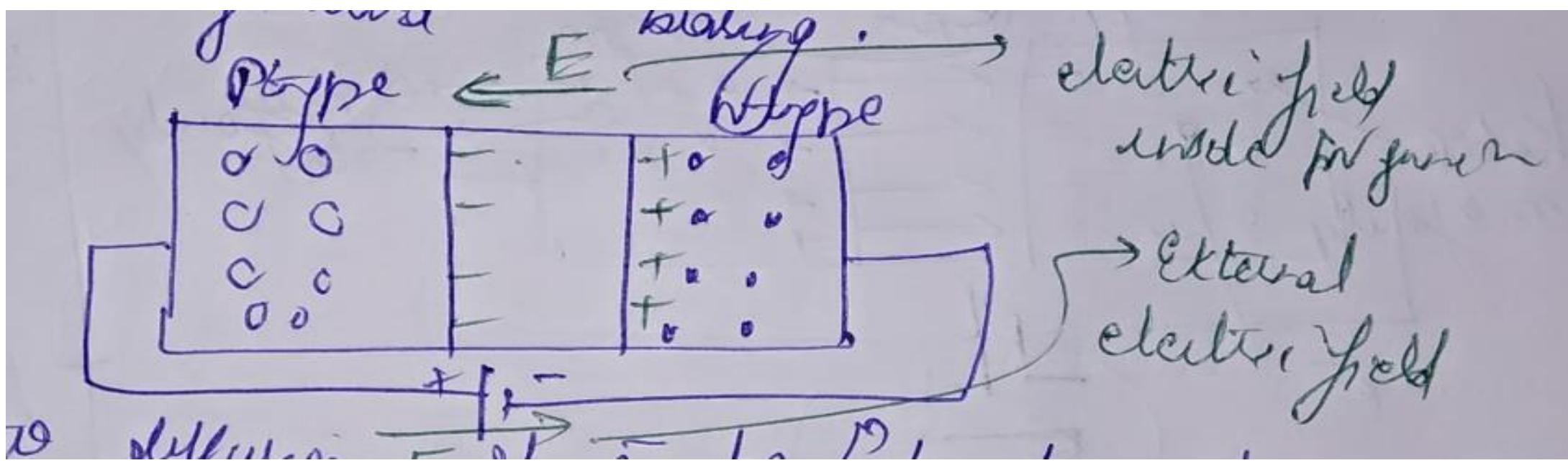
PN Junction Diode

12. Due to distance d with electric field creates $V=Ed$ (with the help of E and d , we will have V)
13. This potential difference is known as potential barrier.
14. Due to + higher potential and - lower potential
15. Remaining electrons can not go due to large distance.
16. They need more energy to do so.

Biasing of Diode

- Whenever PN Diode is connected with battery then this situation is called as biasing.
- **Forward Biasing**
- P with positive terminal and n section is connected with negative terminal. So, this is called as forward biasing.

Biasing of Diode



Biasing of Diode

- Due to Diffusion of electrons to holes so layer of N Type have positive ions and P Type have negative ions.
- Resultant electric field will be less because of opposite direction. So overall electric field decreases.
- Due to this potential barrier decrease & depletion layer becomes small.
- n section electrons will move easily due to battery when electrons diffuse into holes so current start flowing.

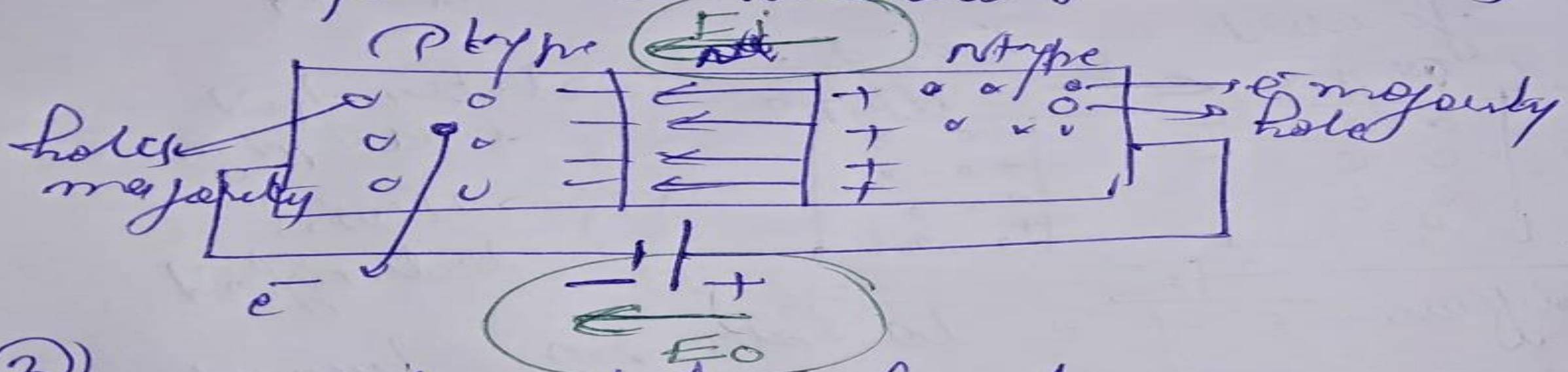
Biasing of Diode

- **Reverse Bias**
- p type-- connected---with-- negative Terminal
- n type-- connected-- with- positive terminal
- Inside electric field and outside electric field are in same direction. So net electric field will increase.
- Hence, depletion layer increases
- Need more voltage to jump the electrons. So, very small amount of current will flow.

Biasing of Diode

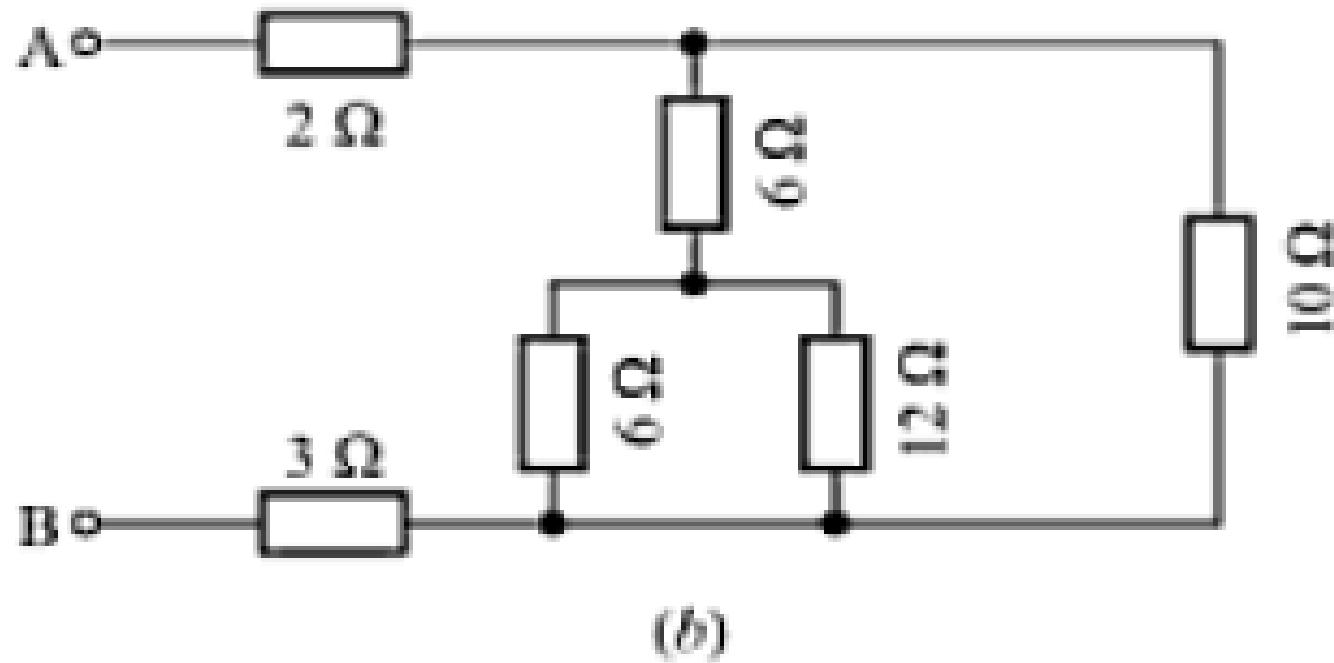
①

p type \rightarrow \ominus terminal
n type \rightarrow \oplus terminal } Reverse biasing



②

Discussions

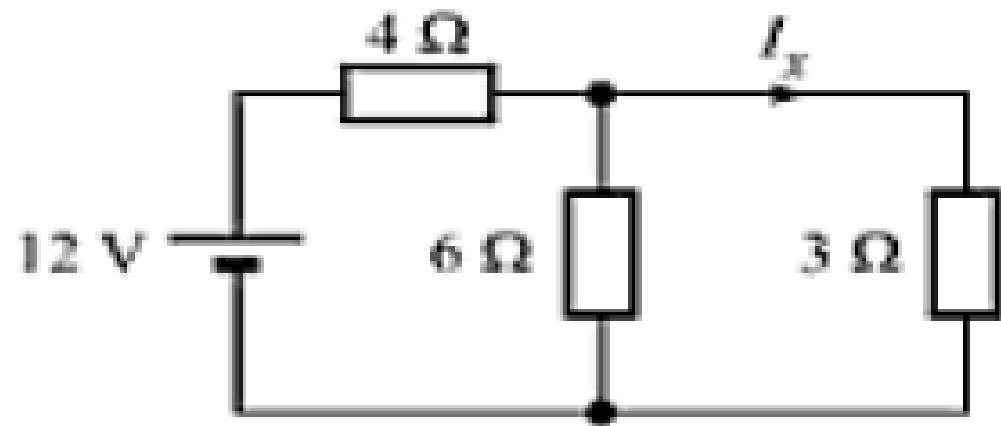


Discussions

(b) The resistance between terminals A and B is

$$\begin{aligned}R_{AB} &= 2 + [(6 + (6 \parallel 12)) \parallel 10] + 3 = 2 + [(6 + 4) \parallel 10] + 3 = 2 + [10 \parallel 10] + 3 \\&= 2 + 5 + 3 = 10 \Omega\end{aligned}$$

Discussions



Total resistance

Current across all resistors

Voltage across each resistors

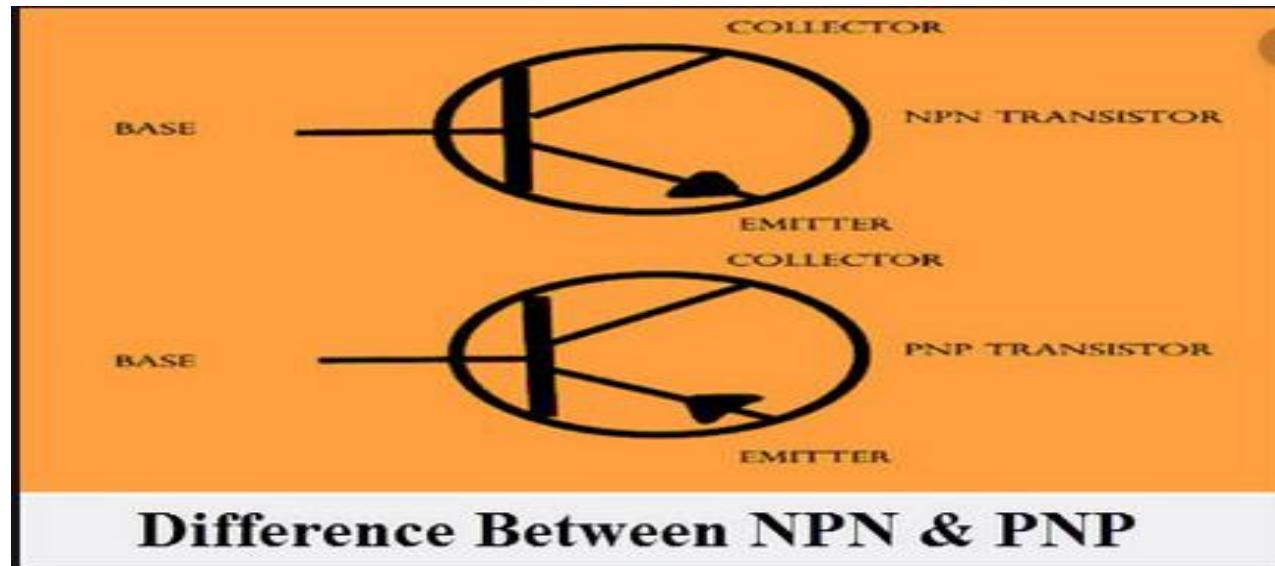
Bipolar Junction Transistor(BJT)

Bipolar Junction Transistor(BJT)

The transistor is made of two PN junction diode.

Types:

NPN and PNP



The transistor in which one p-type material is placed between two n-type materials is known as NPN transistor.

In NPN transistor, the direction of movement of an electron is from the emitter to collector region due to which the current constitutes in the transistor.

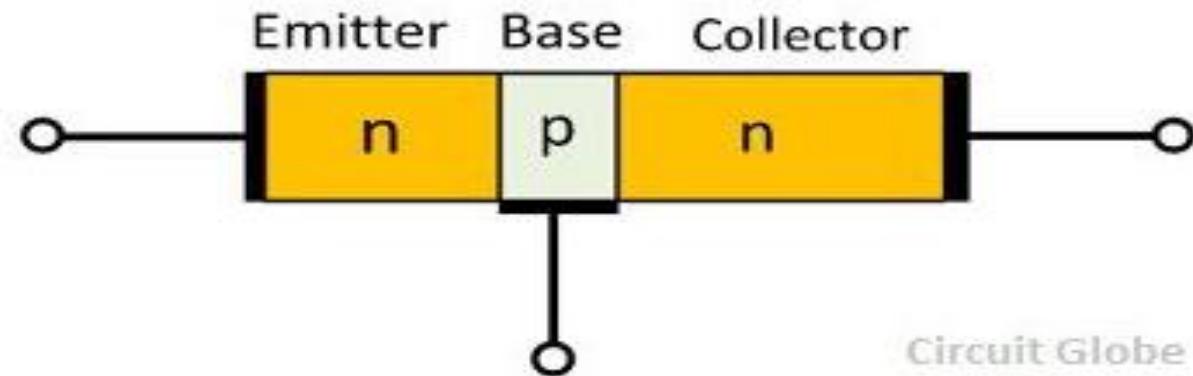
Such type of transistor is mostly used in the circuit because their majority charge carriers are electrons which have high mobility as compared to holes.

Name	Size	Doping
Emitter	Between Base and collector-	High
Base	less	less
Collector	Huge	Between Base and emitter

Construction of NPN Transistor

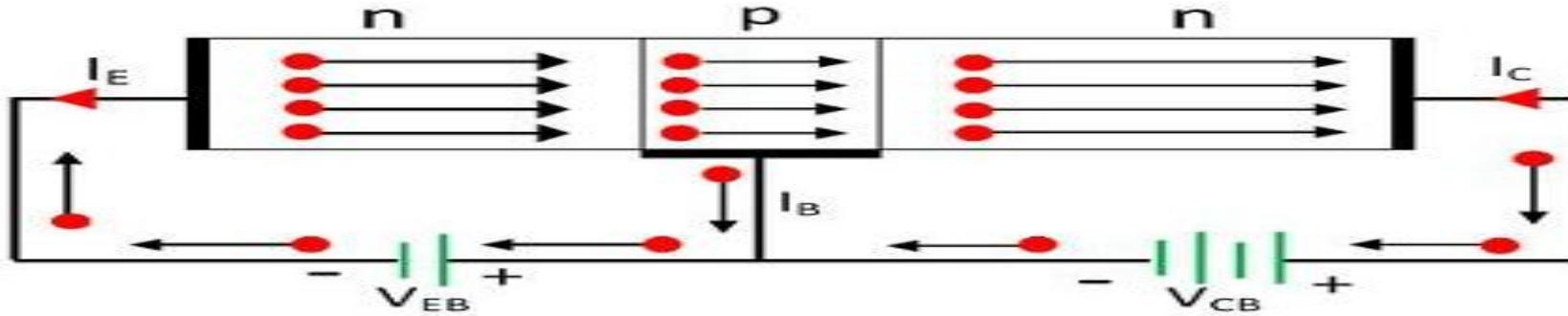
The NPN transistor has two diodes connected back to back.

The diode on the left side is called an emitter-base diode, and the diodes on the right side are called collector-base diode.



Working of NPN Transistor

The forward biased is applied across the emitter-base junction, and the reversed biased is applied across the collector-base junction.



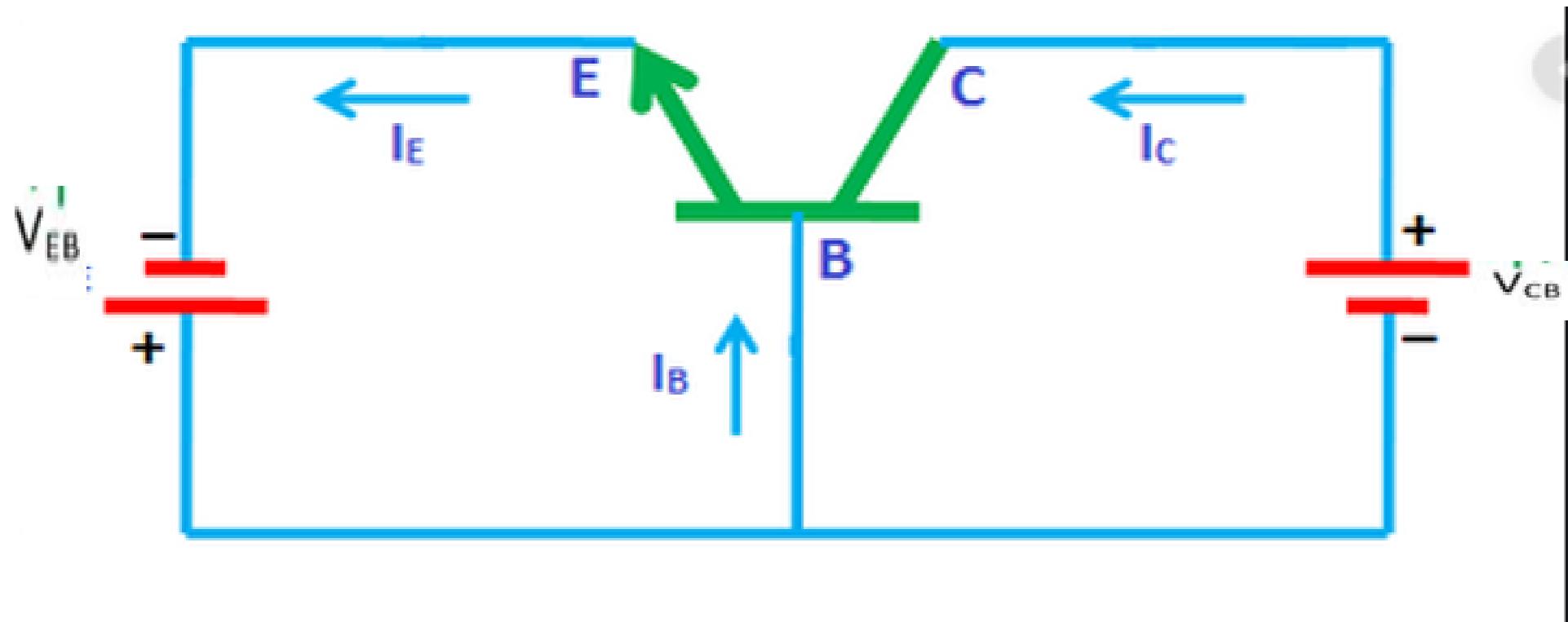
When the forward bias is applied across the emitter, the majority charge carriers move towards the base.

This causes the emitter current I_E . The electrons enter into the P-type material and combine with the holes.

The base of the NPN transistor is lightly doped. Due to which only a few electrons are combined and remaining constitutes the base current I_B .

The reversed bias potential of the collector region applies the high attractive force on the electrons reaching collector junction. Thus attract or collect the electrons at the collector.

Thus, we can say that the emitter current is the sum of the collector or the base current.



$$\boxed{I_E = I_B + I_C}$$

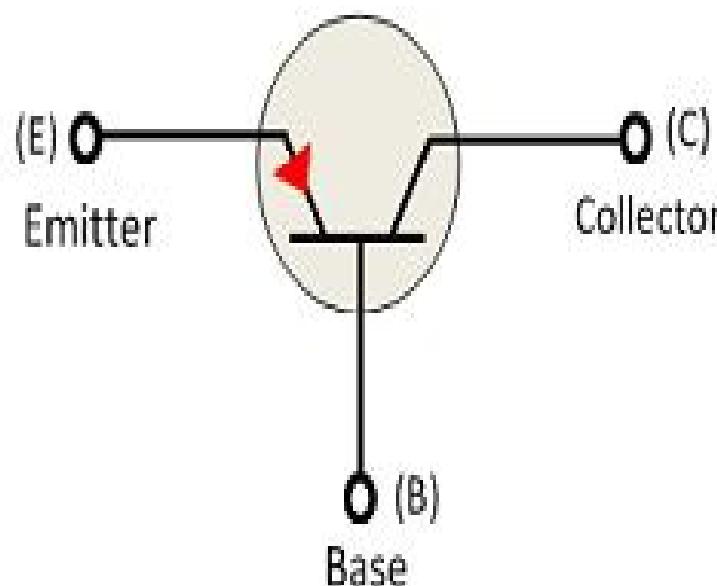
PNP Transistor

PNP Transistor

- The transistor in which one n-type material is doped with two p-type materials such type of transistor is known as **PNP transistor.**
- The PNP transistor has two crystal diodes connected back to back.
- The left side of the diode is known as the emitter-base diode and the right side of the diode is known as the collector-base diode.
- The hole is the majority carriers of the PNP transistors which constitute the current in it.

Symbol of PNP Transistor

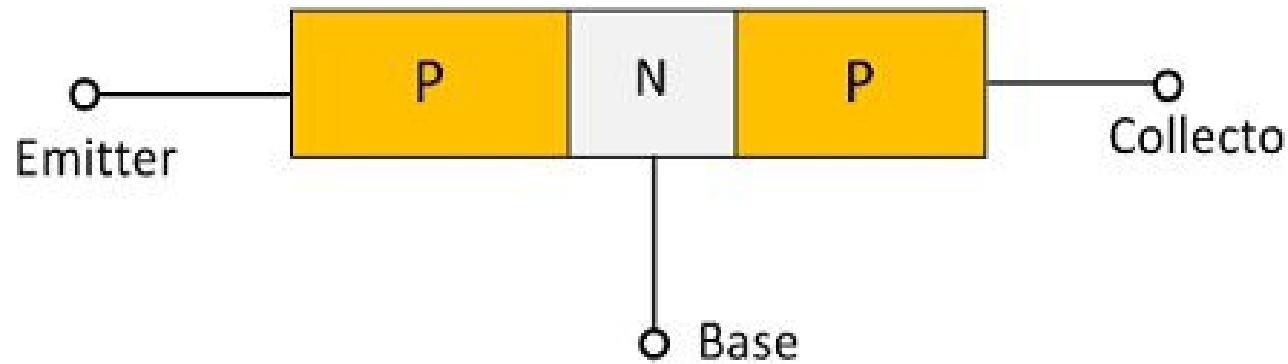
The symbol of PNP transistor is shown in the figure below. The inward arrow shows that the direction of current in PNP transistor is from the emitter to collector.



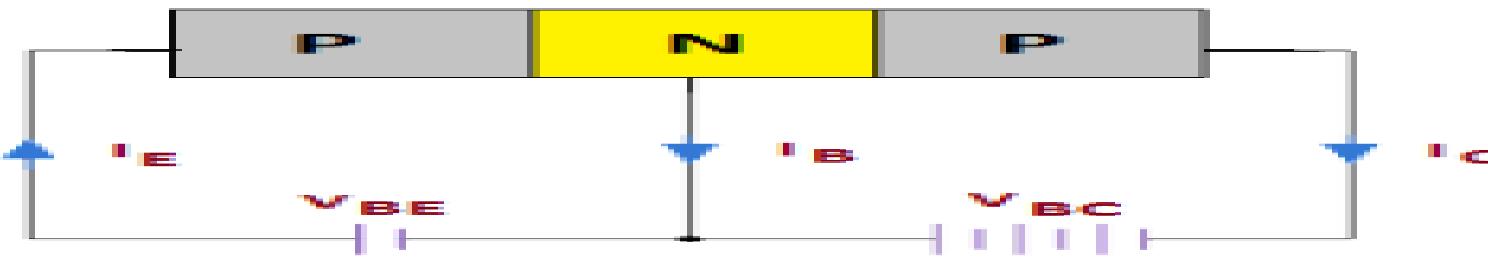
PNP Transistor

Construction of PNP Transistor

- The construction of PNP transistor is shown in the figure below.
- The emitter-base junction is connected in forward biased, and the collector-base junction is connected in reverse biased.



Working of PNP Transistor



Construction

The emitter-base junction is connected in forward biased due to which the emitter pushes the holes in the base region. These holes constitute the emitter current.

When these holes move into the N-type semiconductor material or base, they combine with the electrons.

The base of the transistor is thin and very lightly doped.

Hence only a few holes combined with the electrons and follow base path while remaining are moved towards the collector. Hence develops the base current.

The collector base region is connected in reverse biased.

The holes which collect around the depletion region when coming under the impact of negative polarity collected or attracted by the collector.

This develops the collector current.

Thus, we can say that the emitter current is the sum of the collector or the base current.

$$I_E = I_B + I_C$$

Discussions

Determine I_x in the circuit shown in Fig. 3.50

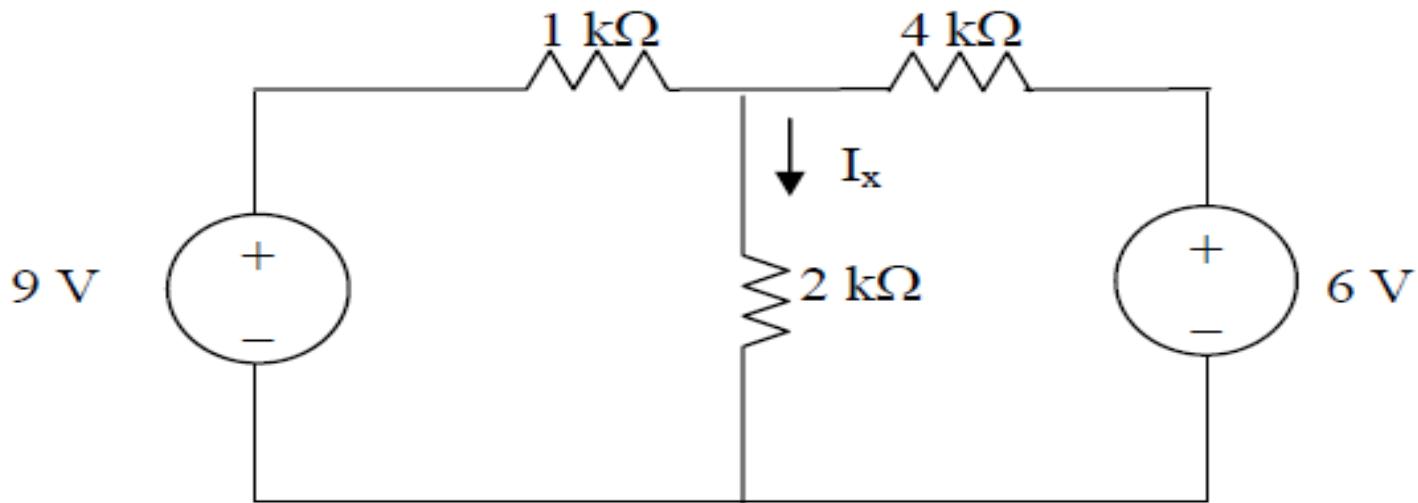


Figure 3.50 For Prob. 3.1.

Discussions

Determine I_x in the circuit shown in Fig. 3.50

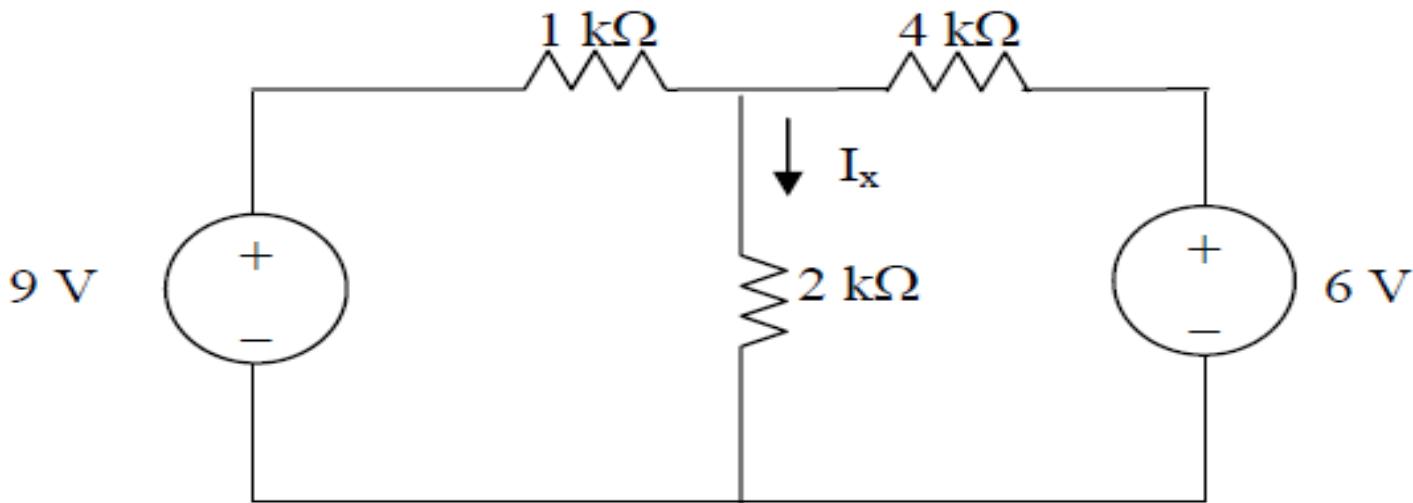


Figure 3.50 For Prob. 3.1.

$$\longrightarrow V_x = 6$$

$$I_x = \frac{V_x}{2k} = \underline{3 \text{ mA}}$$

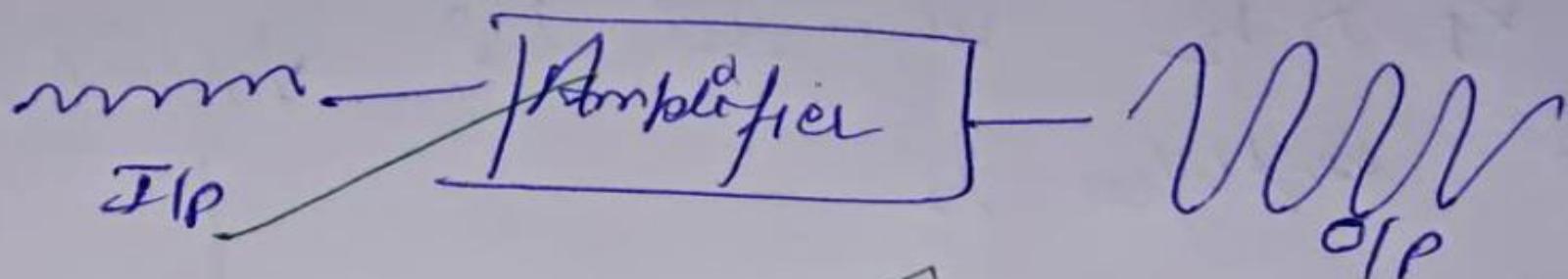
Operational Amplifier (OPAMP)

~~OP-AMP~~

①

Operational Amplifier { Op-amp in T41C }

① It is basically an amplifier [to amplify the input signal]



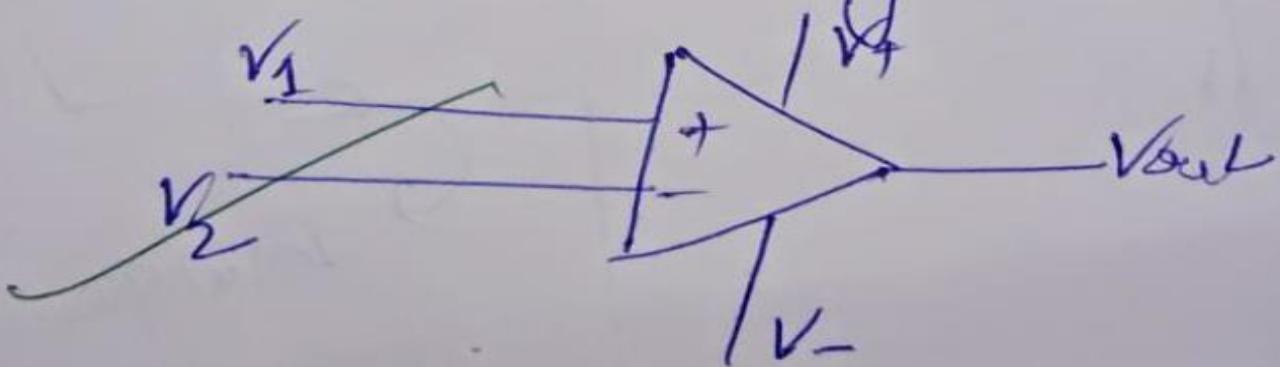
Operational Amplifier (OPAMP)

- ❖ We can perform addition, subtraction using amplifier.
- ❖ Just by connecting few resistors- It is possible to perform the mathematical operations.

Operational Amplifier (OPAMP)

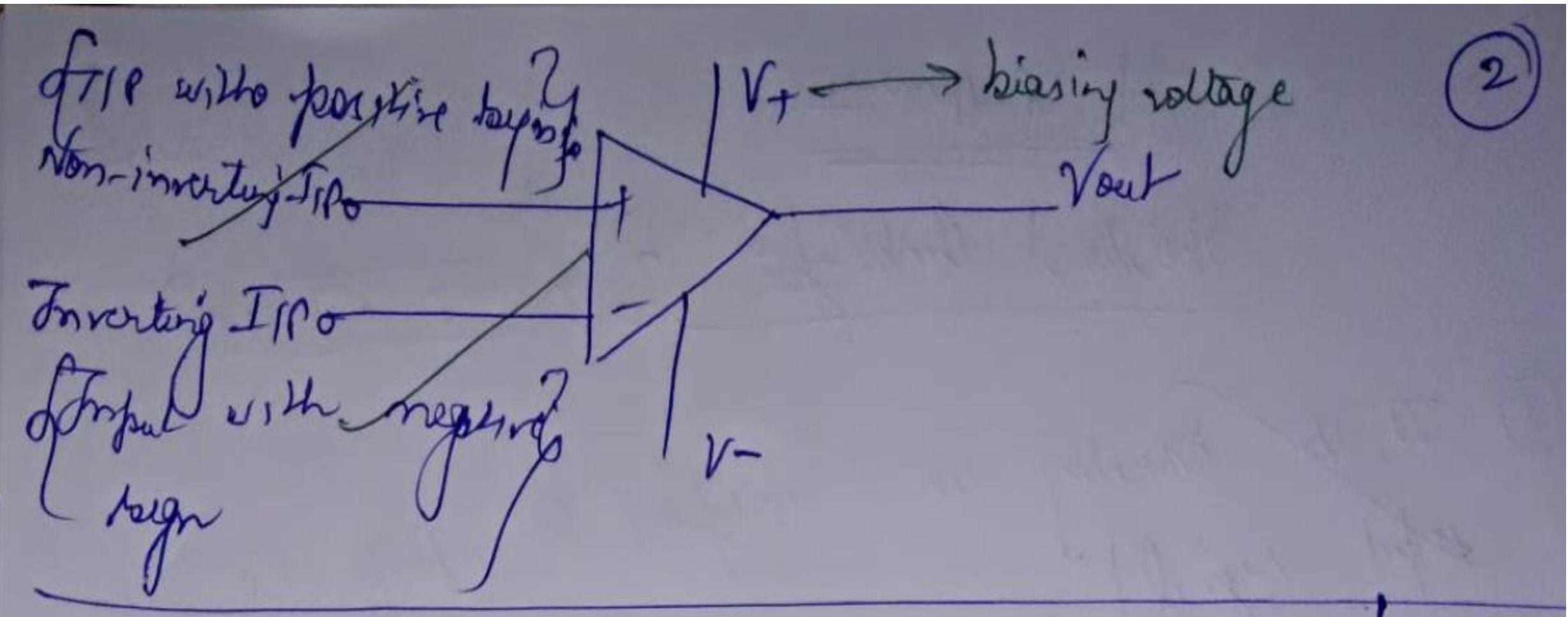
③ That's why it is called as operational amplifier.

④ Circuit symbol of OP-Amp



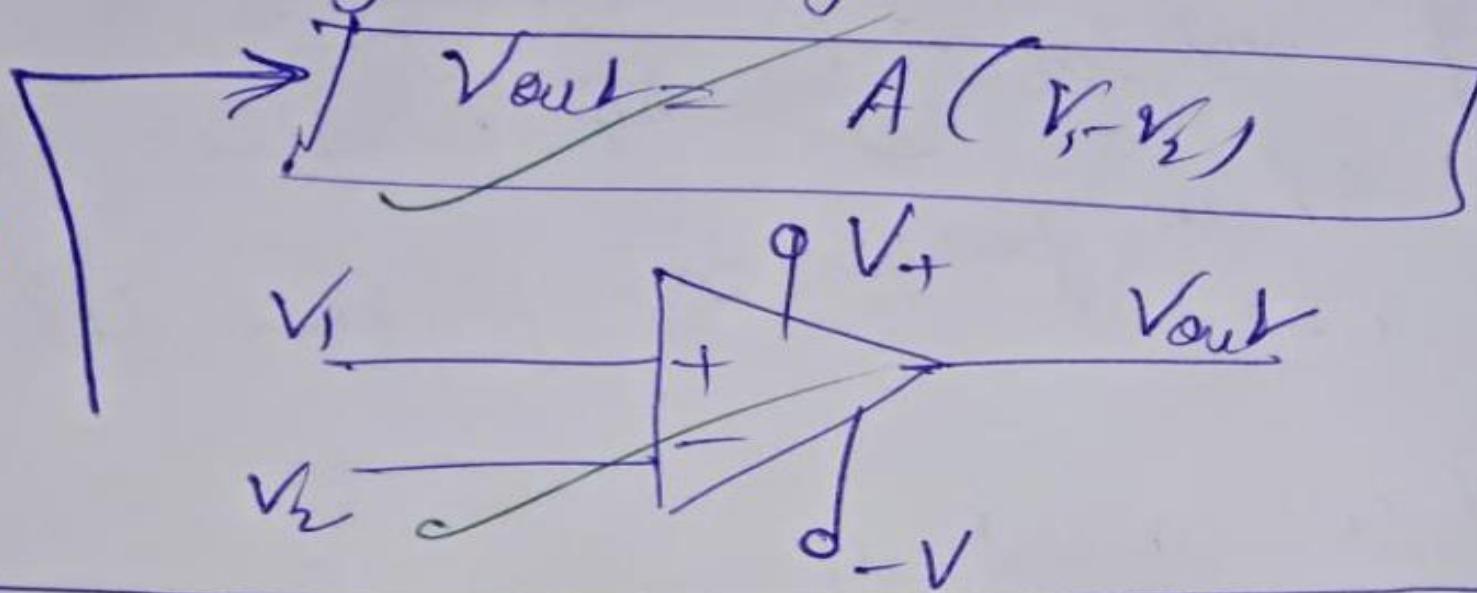
It consists of two inputs & one op.

Operational Amplifier (OPAMP)



Operational Amplifier (OPAMP)

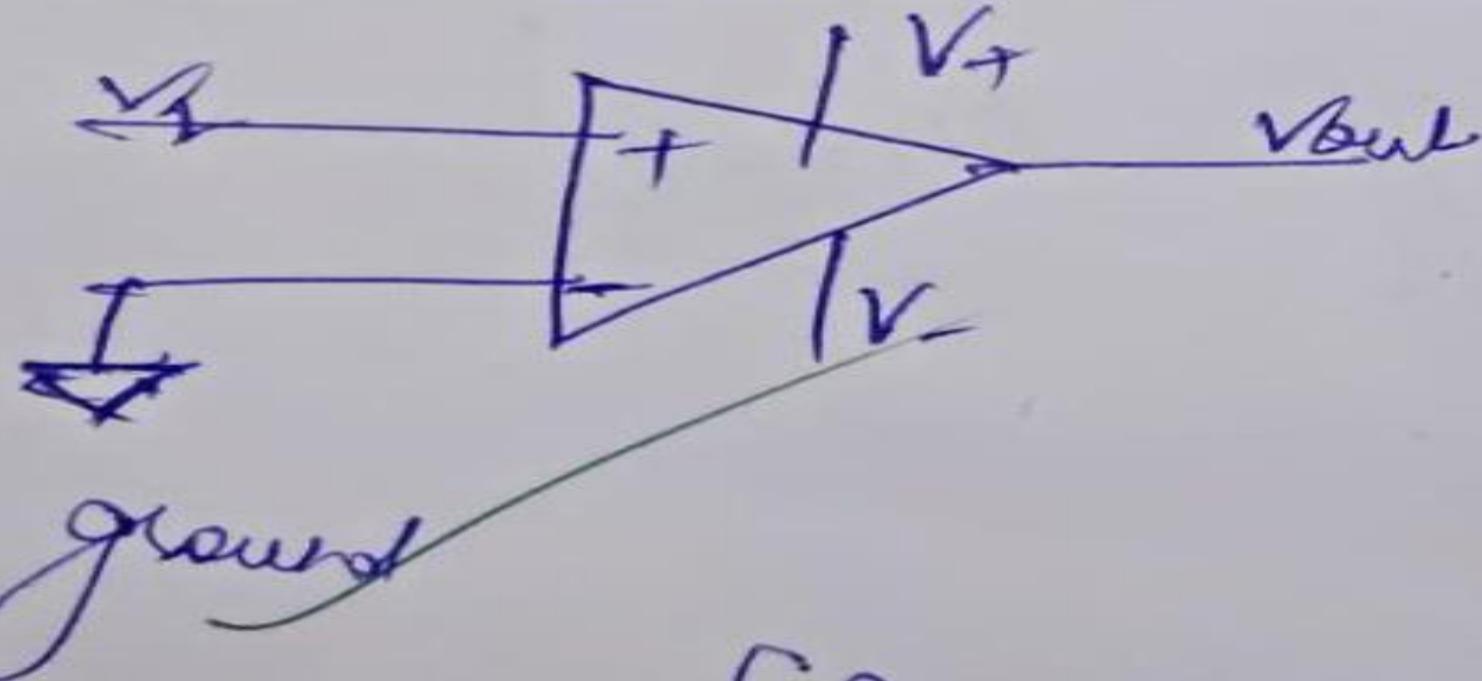
- 1) Suppose v_1 & v_2 are the I/P applied to the
operational amplifier is
- 2) Gain of amplifier is A then



$$V_{out} = A(v_1 - v_2)$$

Operational Amplifier (OPAMP)

Case 1:-

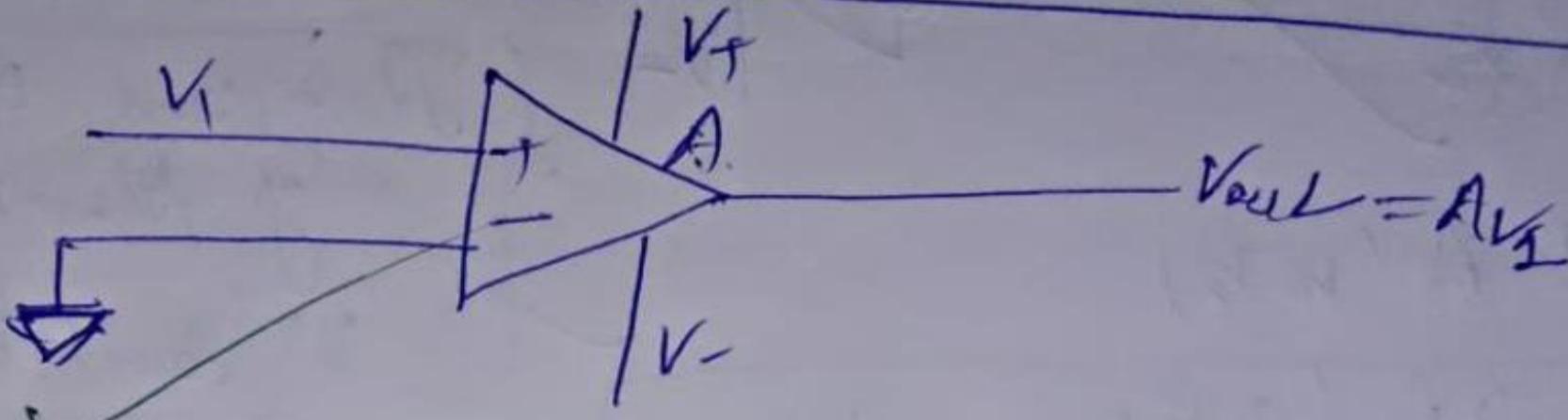


$$R_2 = 0$$

ground

$$v_{out} = A(v_+ - v_-) \quad \left\{ \text{here } v_+ = V_T \right.$$
$$\frac{v_{out}}{v_{out} - A(v_+)} \rightarrow A(v_+)$$

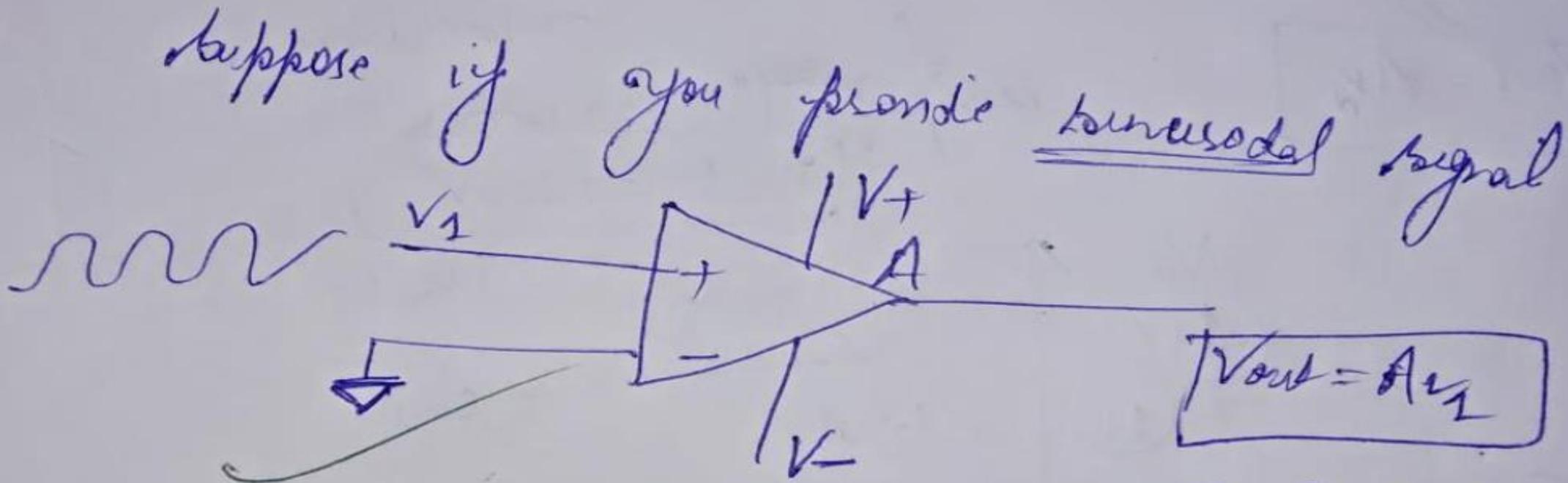
Operational Amplifier (OPAMP)



~~„A is known at open loop gain ∞ because there does not exist any feedback from output to the input.~~

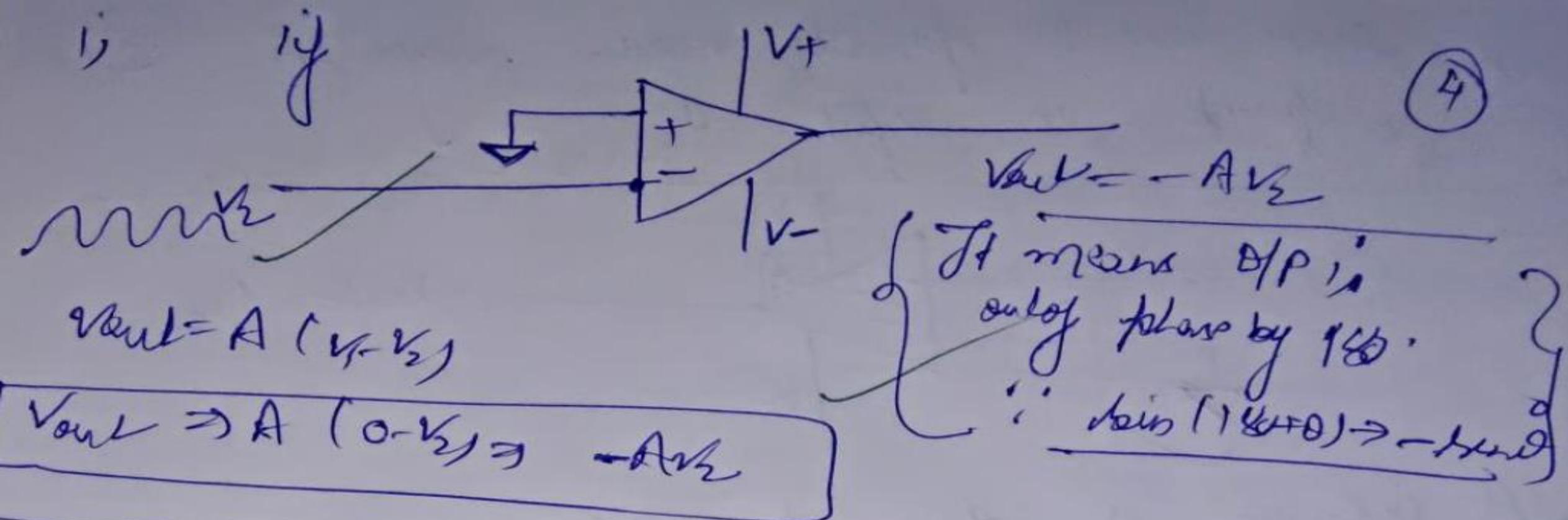
Operational Amplifier (OPAMP)

3

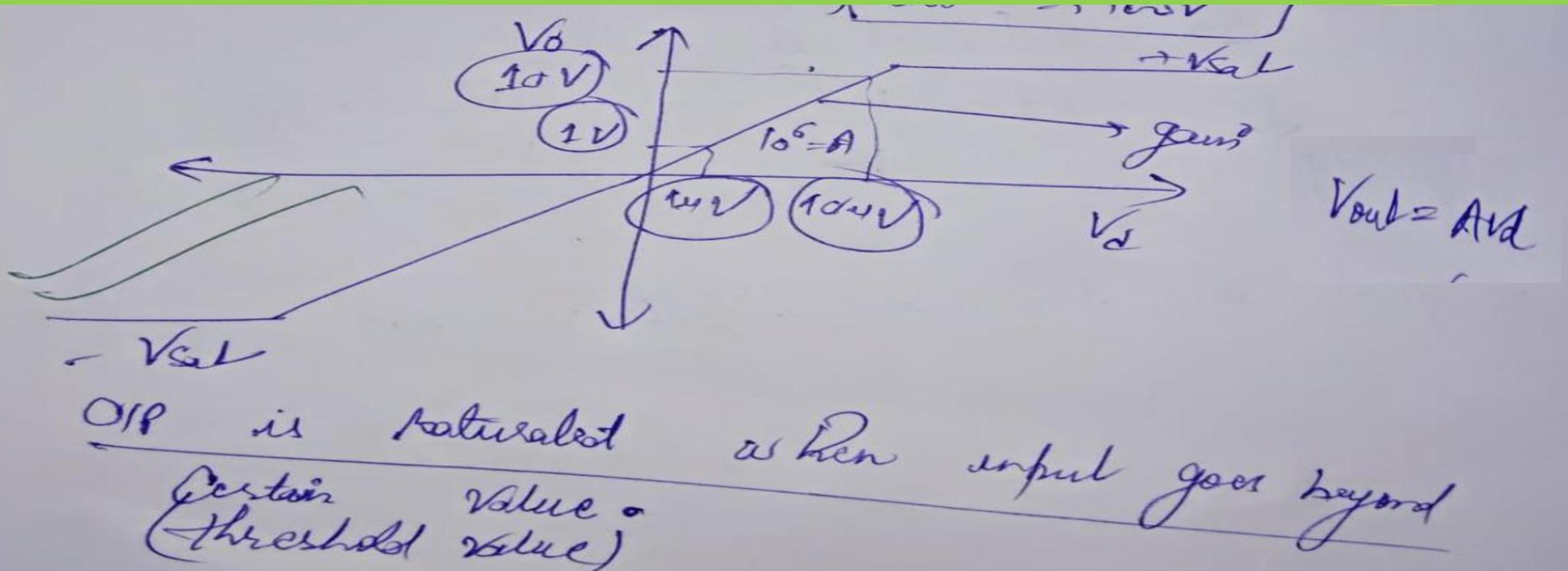


here phase is same as input voltage.

Operational Amplifier (OPAMP)

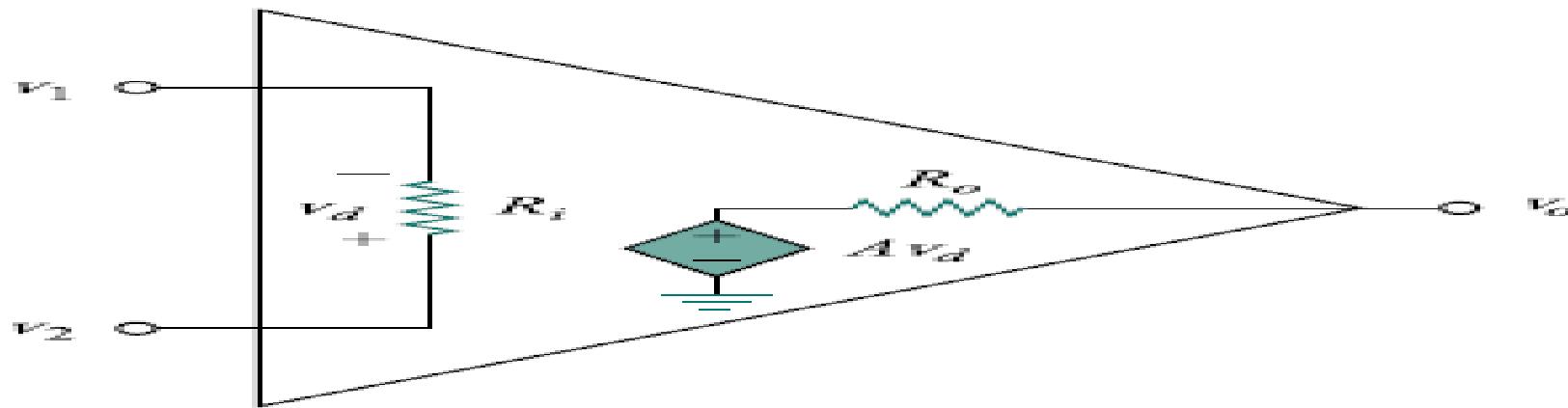


Operational Amplifier (OPAMP)



Saturation Curve/Ideal Voltage Transfer Characteristics

Operational Amplifier (OPAMP) Equivalent Circuit



The output v_o is given by= $v_o = A v_d = A(v_2 - v_1)$ (non-inverting voltage-
Inverting voltage)
The differential input voltage v_d is given by $v_d = v_2 - v_1$

A is called the *open-loop voltage gain* because it is the gain of the op amp without any external feedback from output to input.

where v_1 is the voltage between the inverting terminal and ground and v_2 is the voltage between the noninverting terminal and ground.

TABLE 5.1 Typical ranges for op amp parameters.

Parameter	Typical range	Ideal values
Open-loop gain, A	10^5 to 10^8	∞
Input resistance, R_i	10^6 to 10^{13} Ω	∞ Ω
Output resistance, R_o	10 to 100 Ω	0 Ω
Supply voltage, V_{cc}	5 to 24 V	

Discussions

❖ Explain Voltage Division Rule ?

Voltage Division Rules

1. Voltage Division Rule

The **voltage** is divided between two series resistors in direct proportion to their resistance.

VOLTAGE DIVISION RULE :-

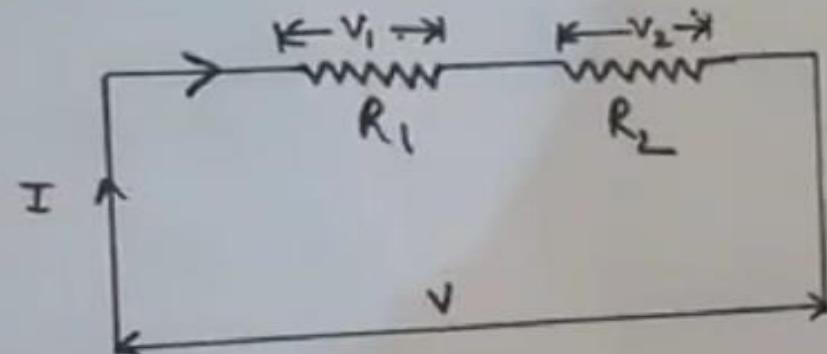
KVL

$$V = V_1 + V_2$$

$$V_1 = R_1 I$$

$$V_2 = R_2 I$$

$$I = V / (R_1 + R_2)$$



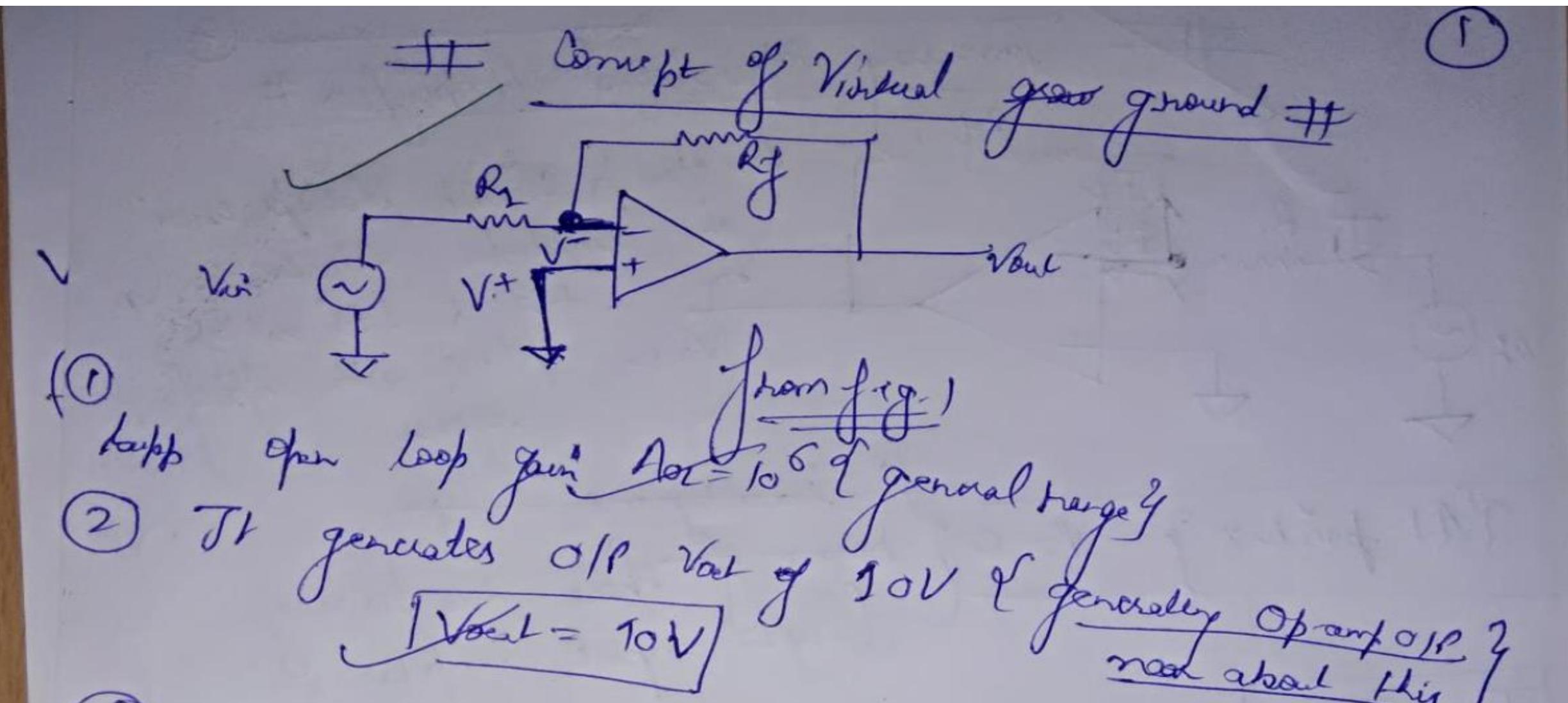
$$V = R_1 I + R_2 I$$

$$V = I (R_1 + R_2)$$

$$V_1 = V \times \frac{R_1}{R_1 + R_2}$$

$$V_2 = V \times \frac{R_2}{R_1 + R_2}$$

Operational Amplifier (OPAMP)



Operational Amplifier (OPAMP)

③ formula OP AMP

$$V_{out} = A \cdot V_d \quad [\text{gain terms differential voltage}]$$

$$[V_{out} = A \cdot V_d]$$

$$[I_o = 10^6 V_d]$$

$$[10^6 \times 10^{-6} = V_d]$$

$$[10^6 V = V_+ - V_-] \Rightarrow [10^6 V = V^+ - V^-]$$

$$[V^+ - V^- \approx 0V]$$

$$\frac{V^+ - V^- = 0}{[V^+ = V^-]}$$

$$\text{so } V^+ = 0 \quad \{ \text{ground from fig. 1} \}$$

$$[V = 0]$$

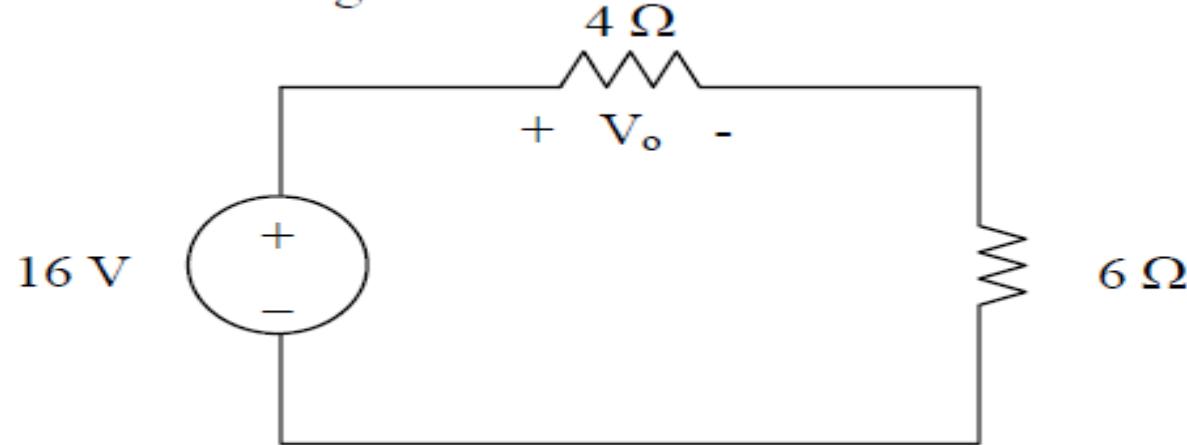
since V_L is zero

of bi-intercircuit voltage & 2nd intercircuit voltage are equal so are voltage wind ground.

which is very very small so

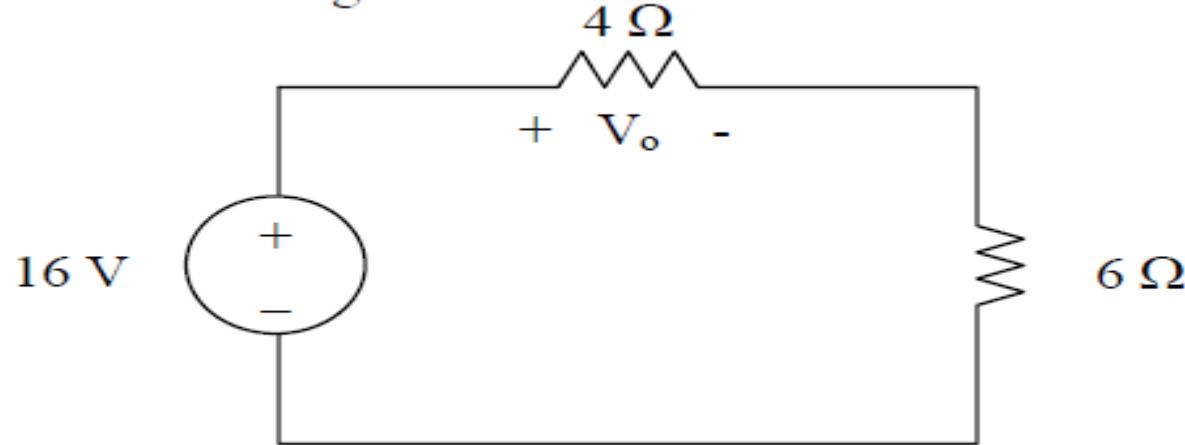
Discussions

Calculate V_o in the circuit of Fig. 2.91.



Discussions

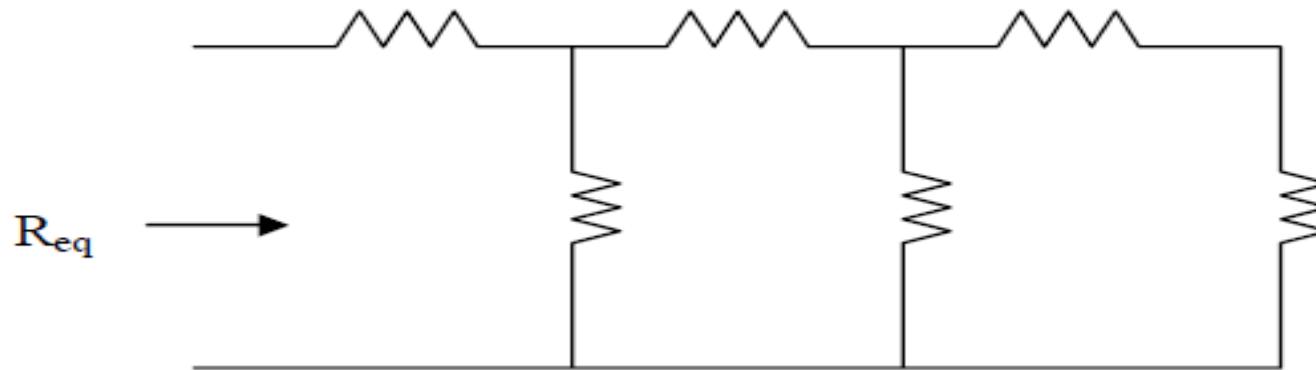
Calculate V_o in the circuit of Fig. 2.91.



$$V_o = \frac{4}{4+16}(16V) = \underline{6.4 \text{ V}}$$

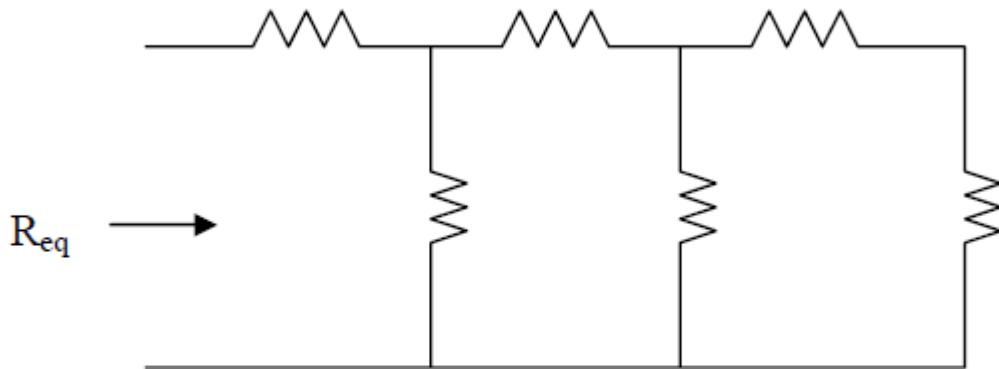
Discussions

All resistors in Fig. 2.93 are 1Ω each. Find R_{eq} .



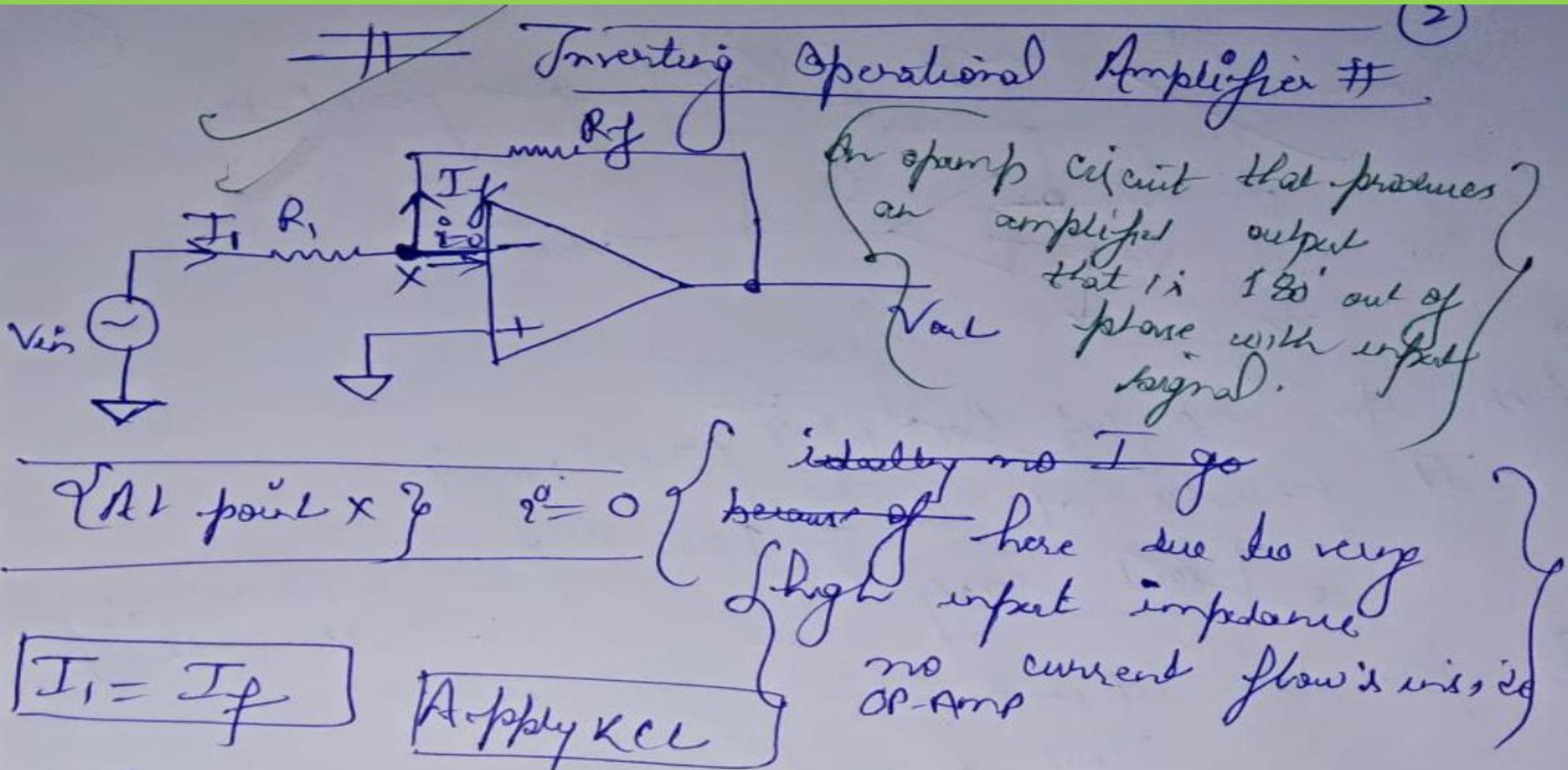
Discussions

All resistors in Fig. 2.93 are 1Ω each. Find R_{eq} .



$$R_{eq} = 1 + 1/(1 + 1//2) = 1 + 1//(1+ 2/3) = 1 + 1//5/3 = \underline{\underline{1.625 \Omega}}$$

Inverting Operational Amplifier



Inverting Operational Amplifier

$\{A_1 \text{ point}\} \quad i = 0 \quad \left\{ \begin{array}{l} \text{ideally no } I \text{ go} \\ \text{because here we have} \\ \text{high input impedance} \\ \text{no current flow is missed} \end{array} \right\}$

$I_i = I_f$ Apply KCL

$$\frac{V_{in} - x}{R_i} = \frac{x - V_{out}}{R_f}$$

Here due to virtual ground $x = 0V$

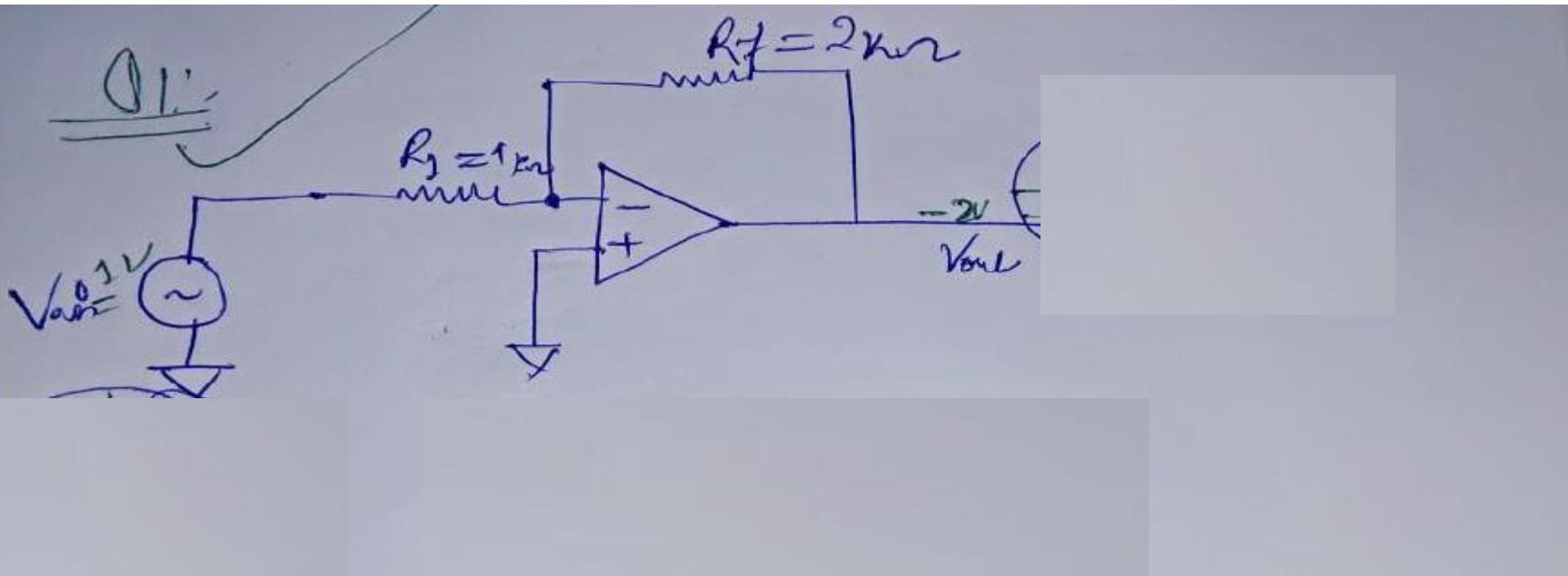
$$\frac{V_{in} - 0}{R_i} = \frac{-V_{out}}{R_f}$$

$$I = \frac{R_f}{R_i} \rightarrow \frac{-V_{out}}{V_{in}} \Rightarrow \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_i} = A_{ce}$$

+ closed loop gain

* [closed loop gain]

Inverting Operational Amplifier



$$\frac{V_{out}}{V_{in}} = -\frac{2 \times 10^3}{1 \times 10^3} \Rightarrow -2$$

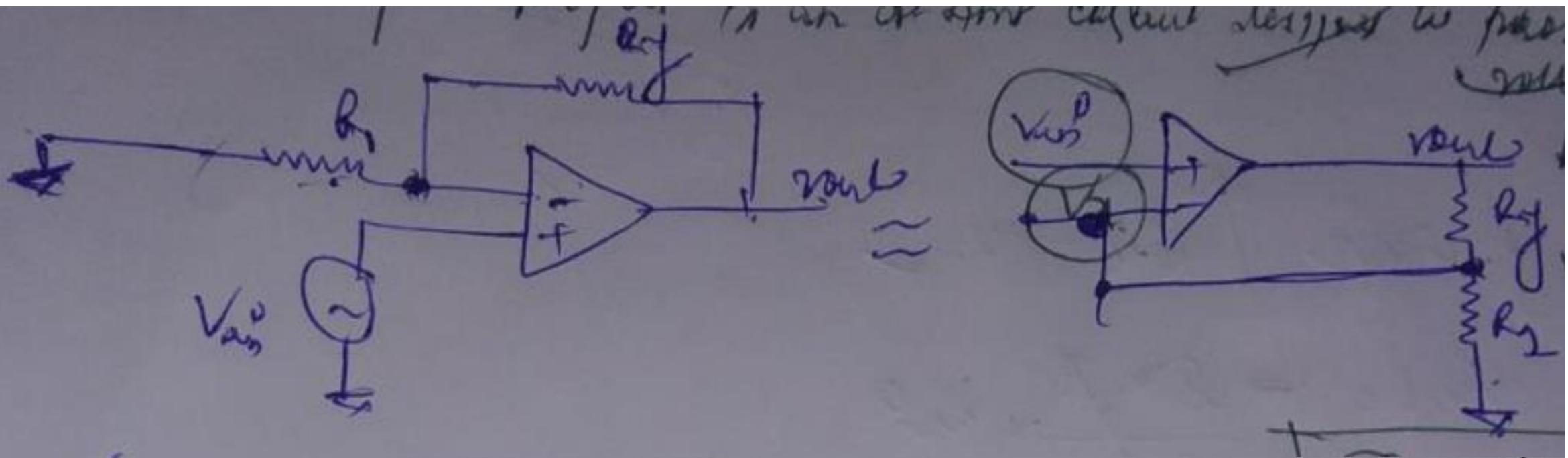
$V_{out} = -2 V_{in}$

$\boxed{V_{out} = -2 \times 1 \Rightarrow -2 V}$

Non- Inverting Operational Amplifier

- A non inverting Amplifier is an OPAMP which is designed to provide positive voltage gain.
- Here, input is applied to non-inverting terminals.

Non-Inverting Operational Amplifier



Voltage at V_x is

①
$$V_x = \frac{R_1}{R_1 + R_F} \times V_{out}$$

Non-Inverting Operational Amplifier

Voltage at V_x is

$$\textcircled{1} \quad V_x = \frac{R_1}{R_1 + R_F} \times V_{out}$$

\textcircled{2} Due to virtual shorting concept
 $(V^+ = V^-)$

\textcircled{3} So $V_{in}^o = V_x$

\textcircled{4} $V_{in}^o = V_x \left(\frac{R_1}{R_1 + R_F} \right) V_{out}$

Non-Inverting Operational Amplifier

④

$$V_{out}^0 = V_{in} \left(\frac{R_f}{R_f + R_i} \right) V_{out}$$

⑤

$$V_{out}^0 = \left(\frac{R_f}{R_f + R_i} \right) V_{out}$$

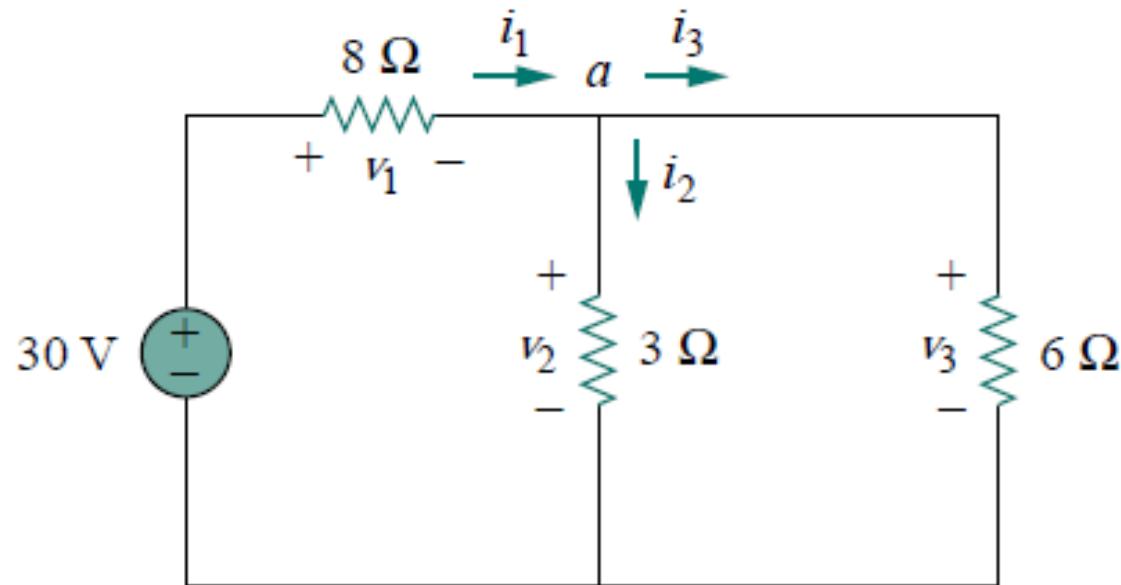
⑥

$$\frac{V_{out}}{V_{in}} = \frac{R_f}{R_f + R_i} \Rightarrow 1 + \frac{R_f}{R_i}$$

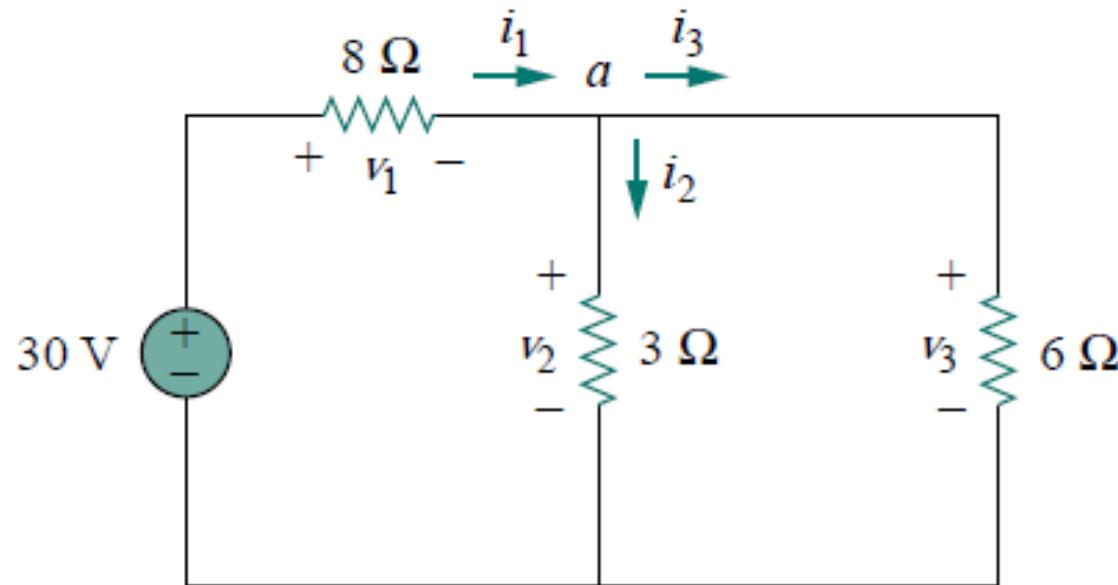
⑦

$$V_{out} = \left(1 + \frac{R_f}{R_i} \right) V_{in}$$

Discussions



Discussions



or $i_2 = 2$ A. From the value of i_2 , we now use Eqs. (2.8.1) to (2.8.5) to obtain

$$i_1 = 3 \text{ A}, \quad i_3 = 1 \text{ A}, \quad v_1 = 24 \text{ V}, \quad v_2 = 6 \text{ V}, \quad v_3 = 6 \text{ V}$$

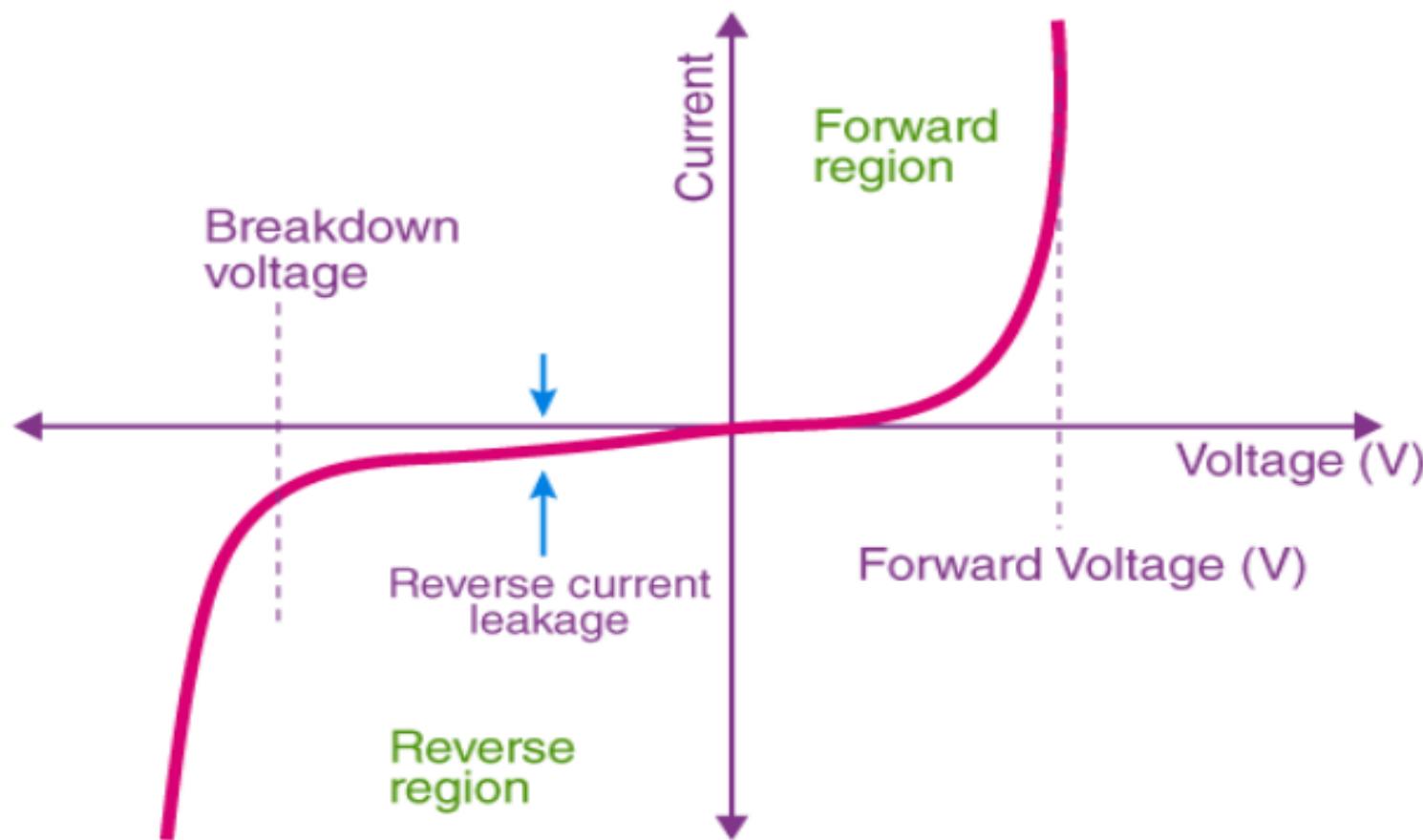
Discussions

3. Which of the following can measure an alternating current?

- a. Voltmeter
- b. Ammeter

VI Characteristics of Diode

V-I Characteristics of P-N Junction Diode



VI Characteristics of Diode

VI characteristics of P-N junction diodes is a curve between the voltage and current through the circuit.

Voltage is taken along the x-axis while the current is taken along the y-axis.

The above graph is the V-I characteristics curve of the P-N junction diode.

With the help of the curve, we can understand that there are three regions in which the diode works, and they are:

VI Characteristics of Diode

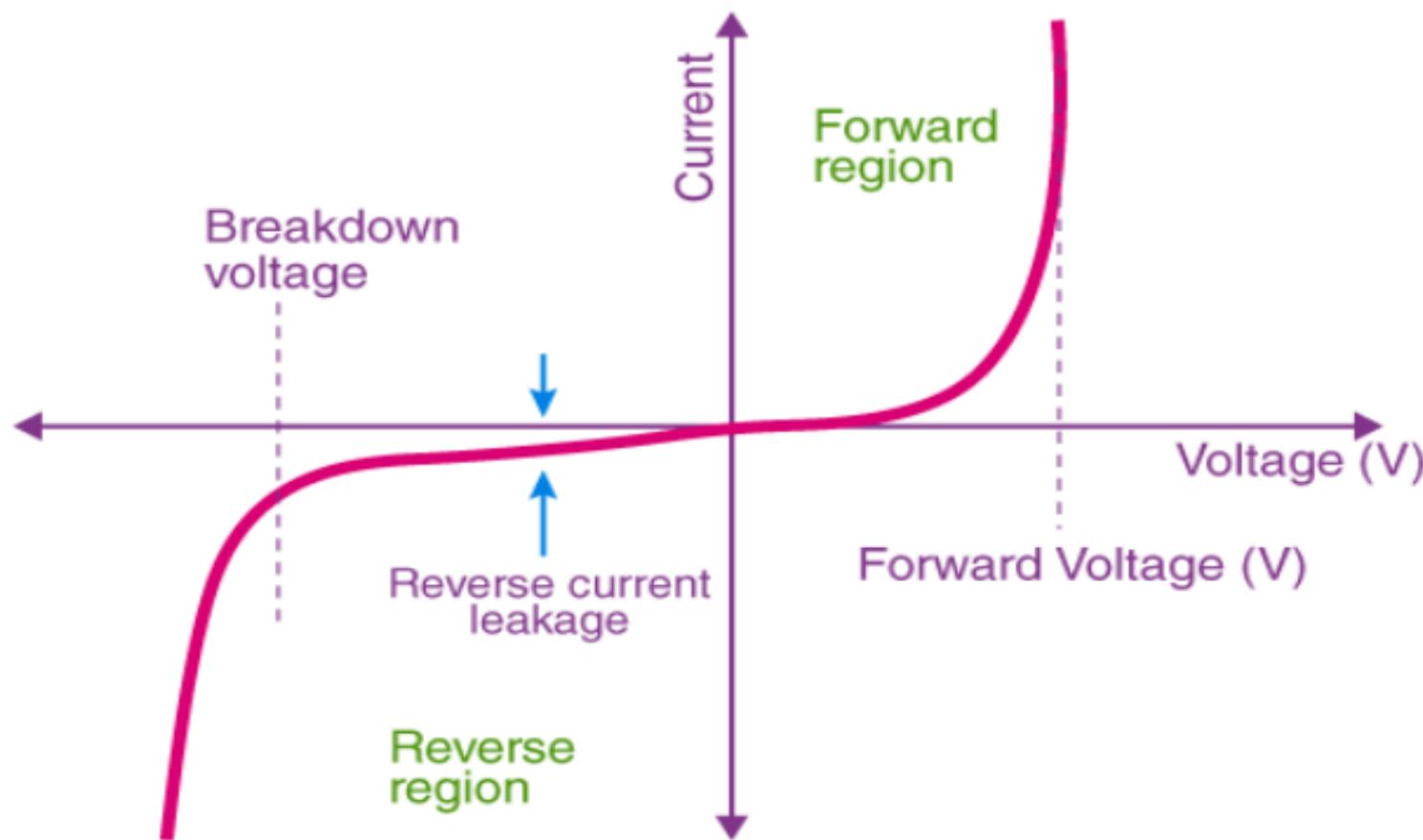
When the P-N junction diode is in **zero bias condition**, there is no external voltage applied and this means that the potential barrier at the junction does not allow the flow of current.

When the P-N junction diode is in **forward bias condition**, there is a reduction in the potential barrier.

The diode behaves normally, and the curve rises sharply as the external voltage increases.

VI Characteristics of Diode

V-I Characteristics of P-N Junction Diode



VI Characteristics of Diode

When the P-N junction diode is in **reverse bias condition**.

This results in an increase in the potential barrier.

So, very small amount of current will flow.

When the applied voltage is increased- This may also destroy the diode.

The maximum reverse bias voltage that can be applied to a p-n diode is limited by breakdown. **Breakdown is characterized by the rapid increase of the current under reverse bias. The corresponding applied voltage is referred to as the breakdown voltage.** The current increases tremendously which may result in the failure of the diode.

Applications of P-N Junction Diode

****When the diode is forward-biased, it can be used in LED lighting applications**

Discussions

Explain Independent Sources ?

Independent Source

Independent Source

The Source which does not depend on any other quantity (like voltage and current) in the circuit.



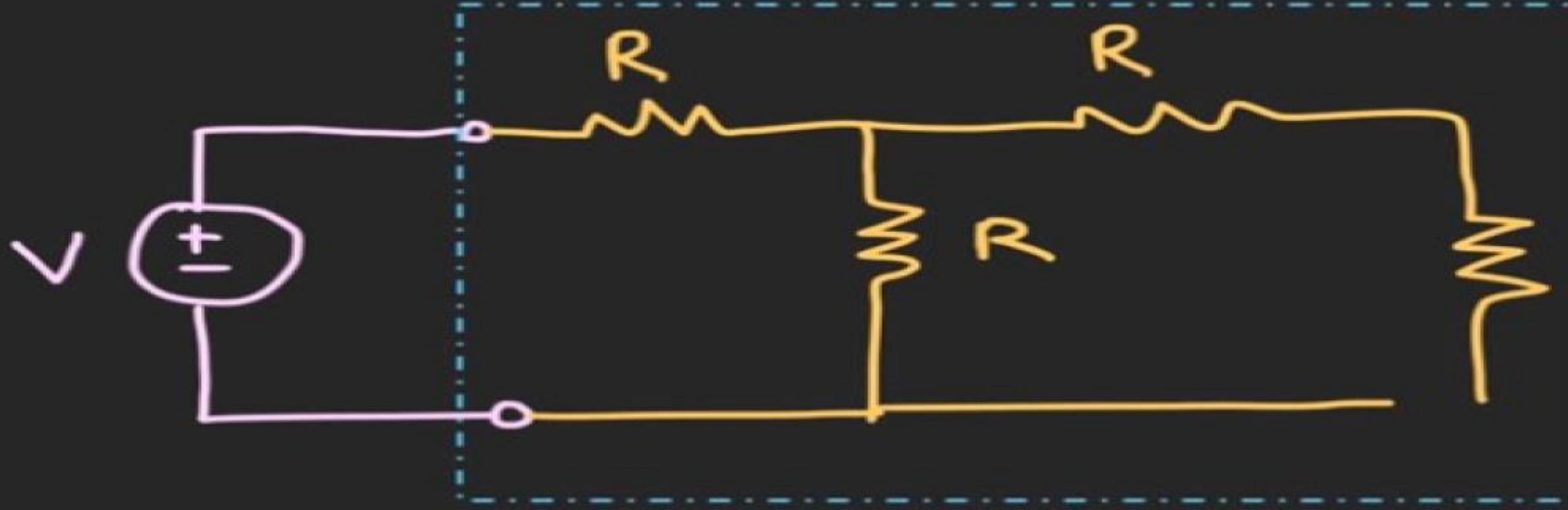
Voltage Source



Current Source

Independent Source

Independent Source



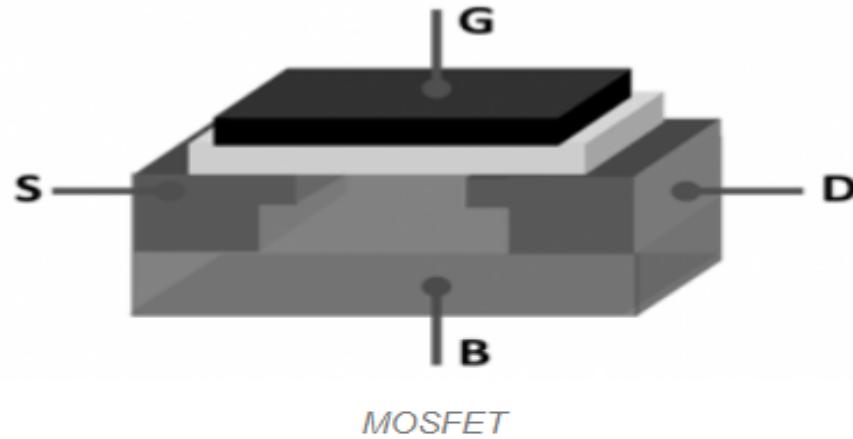
MOSFET

- The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) transistor is a semiconductor device that is widely used for switching purposes and for the amplification of electronic signals in electronic devices.

MOSFET

- A MOSFET is a four-terminal device having source(S), gate (G), drain (D) and body (B) terminals.
- In general, The body of the MOSFET is in connection with the source terminal thus forming a three-terminal device such as a field-effect transistor.
- MOSFET is generally considered as a transistor and employed in both the analog and digital circuits.
- This is the basic **introduction to MOSFET**. And the general structure of this device is as below :

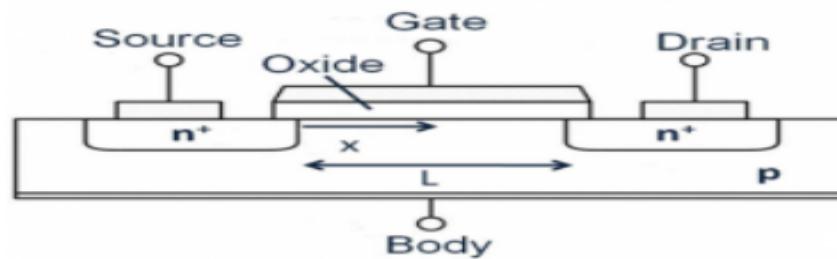
MOSFET



From the above **MOSFET structure**, the functionality of MOSFET depends on the electrical variations happening in the channel width along with the flow of carriers (either holes or electrons). The charge carriers enter into the channel through the source terminal and exit via the drain.

MOSFET

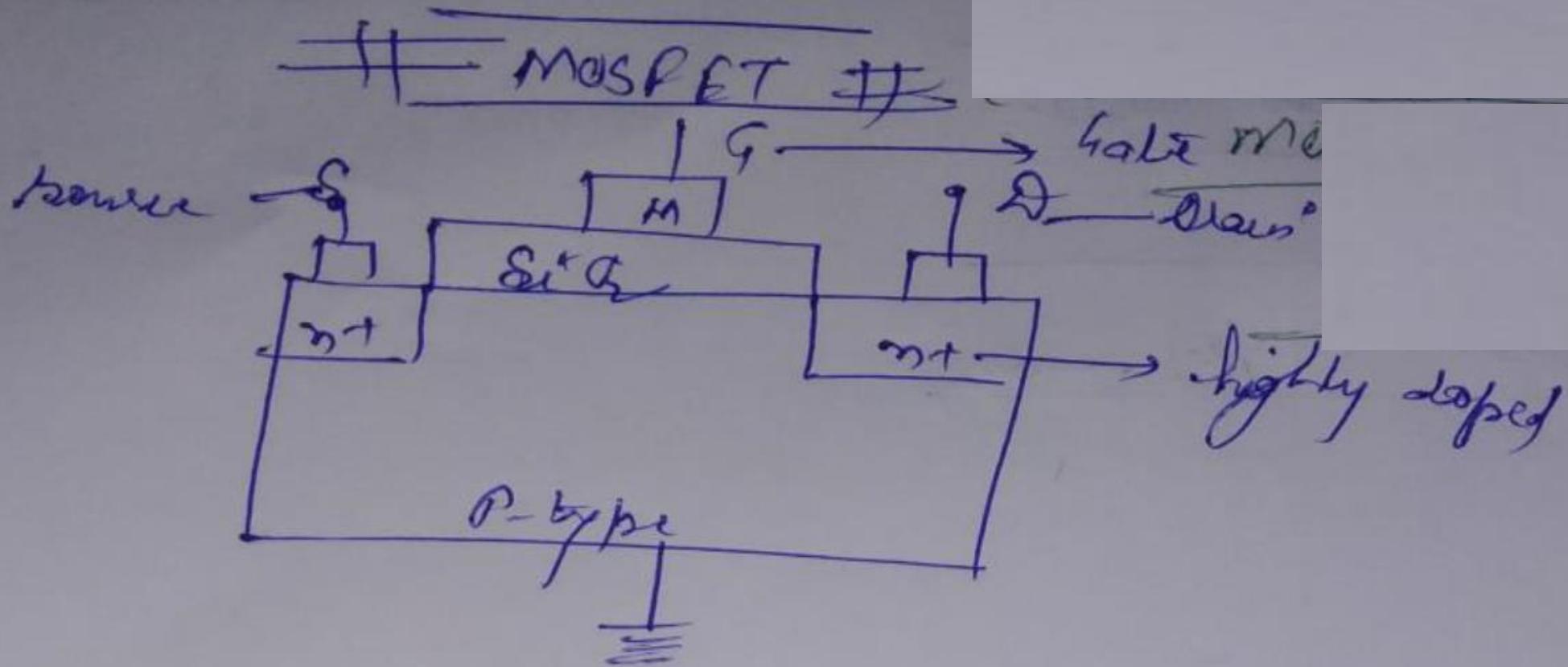
The width of the channel is controlled by the voltage on an electrode which is called the gate and it is located in between the source and the drain. It is insulated from the channel near an extremely thin layer of metal oxide. The MOS capacity that exists in the device is the crucial section where the entire operation is across this.



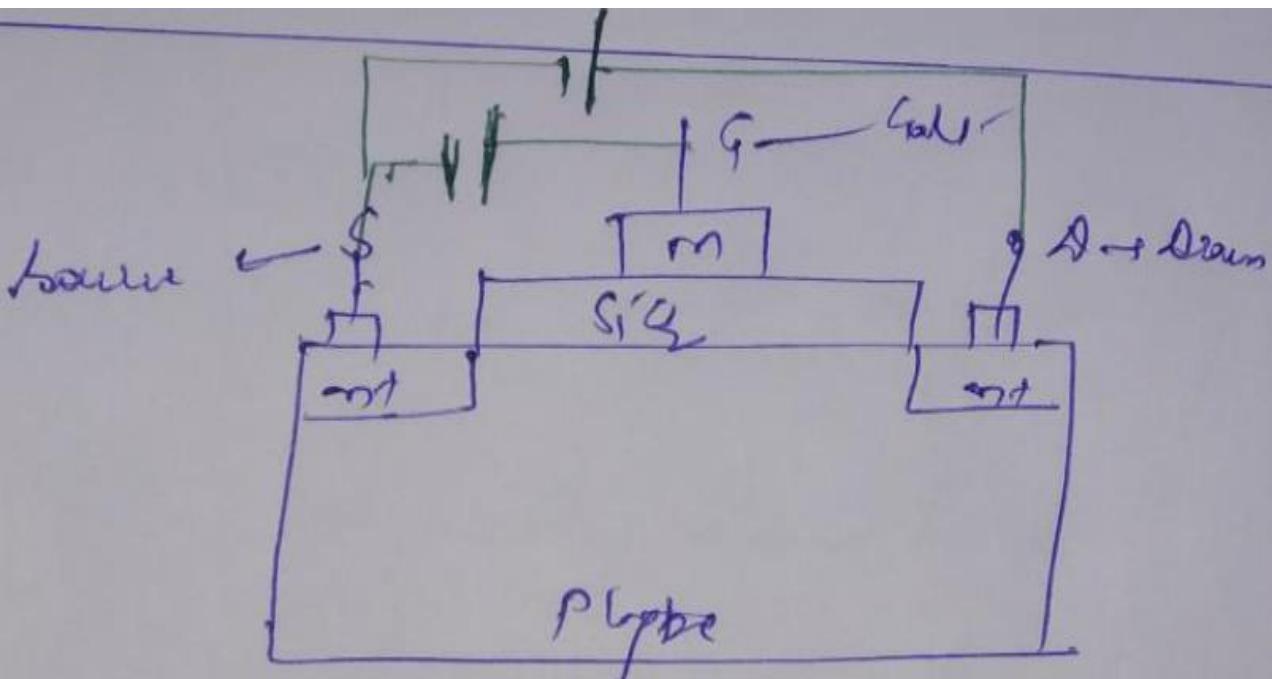
MOSFET With Terminals

Silicon di oxide is **used as an insulation layer between the gate and the conducting channel of the MOSFET.**

MOSFET



MOSFET



Working:-

- ✓ V_{DS}
- ✓ Negative Terminal connected with n+ so e- will move from n+
- ✓ Since, outer region is p-type.
- ✓ Electrons e- will diffuse into holes.
- ✓ Hence, conduction will never start here.

Discussions

Explain dependent Sources ?

Dependent Source

Dependent Source

The Source whose output value depends upon the voltage or current at some other part of the circuit.

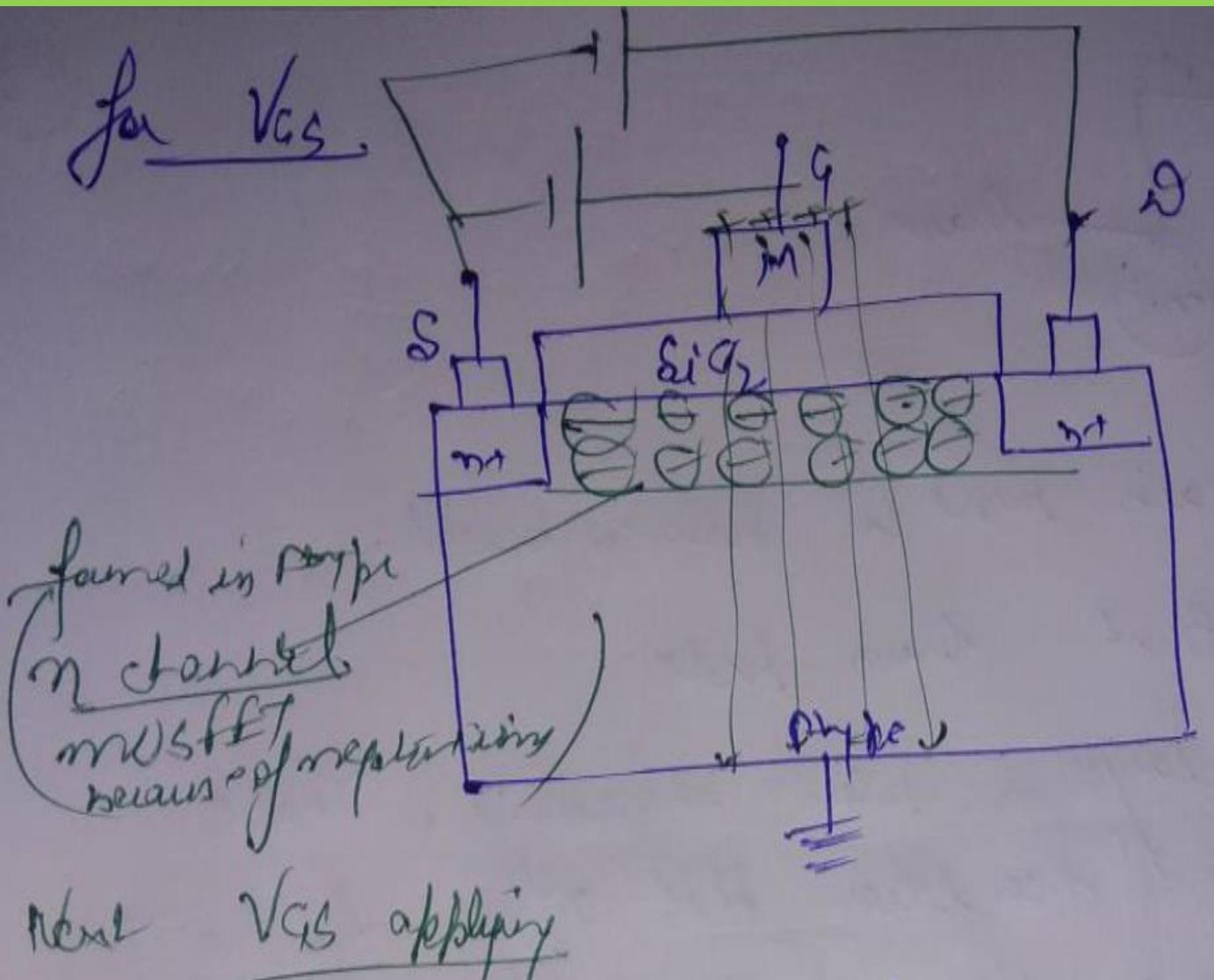


Dependent Voltage Source



Dependent Current Source

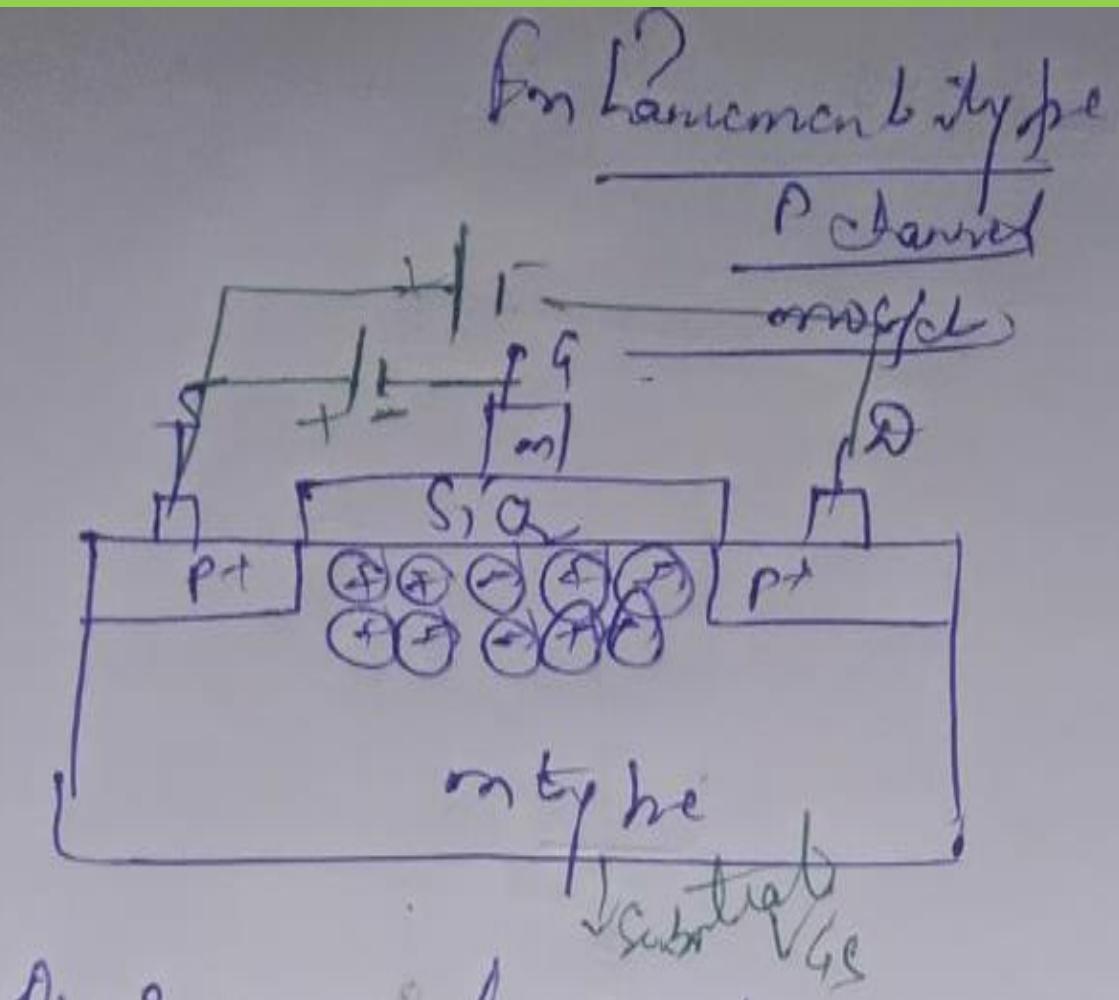
Enhancement Type- N-channel-MOSFET



Working:-

- ✓ V_{GS}
- ✓ Positive charge will appear on the metal surface.
- ✓ Hence, holes start moving.
- ✓ Leaving behind negative ions.
- Electric field exist.
- ✓ Now, if apply; V_{DS} - No holes are outside. Hence, conduction path is available for e-.
- ✓ $V_T \rightarrow V_{GS}$ { What is the value of V_{GS} when current start flowing}
- ✓ As soon as, V_{DS} increases the current I also increases. It will obtain one point when current is constant.

Enhancement Type- P-channel-MOSFET



Drain-> negative (-ve) & gate=0

- a) Holes push from source but deplete due to majority of electrons.

****Here Device is off.**

- b) Drain-> negative (-ve) & gate=negative (-ve) application of negative gate voltage.
It will attract more holes due to negative (-ve) voltage hence holes can move easily & conduct current.

****Here Device is switch ON.**

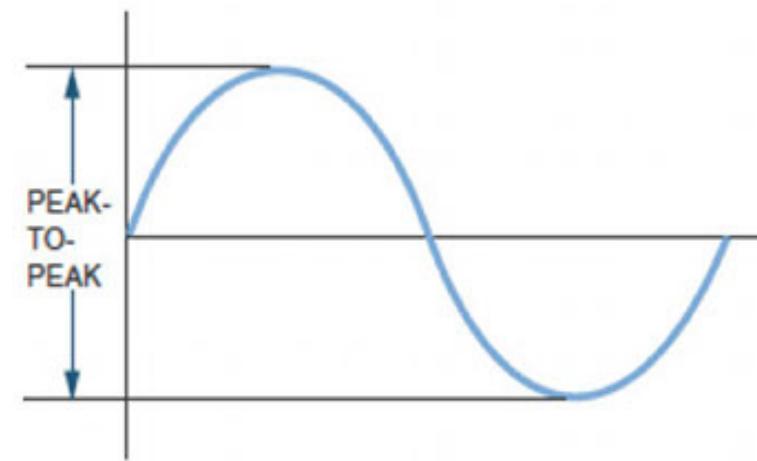
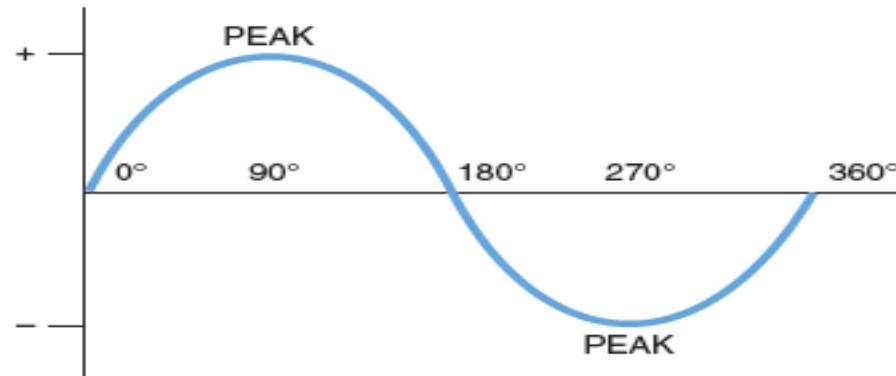
Discussions

What is Peak Value ?

What is Peak to Peak Value ?

AC Values

- **Peak value:** Absolute value of the point with the greatest amplitude.
- **Peak to Peak value:** Vertical distance b/w 2 peaks.
- The amplitude of an AC waveform is its height as depicted on a graph over time. An amplitude measurement can take the form of peak, peak-to-peak.



Discussions

What is semiconductor?

What is intrinsic semiconductor ?

What is extrinsic semiconductor ?

PN Junction Diode

- **Semiconductor:** A semiconductor material has an electrical conductivity value falling between that of a conductor, such as metallic copper, and an insulator, such as glass.
- The semiconductor in its pure form is known as **intrinsic semiconductor**.
- When a chemical impurity is added to an intrinsic semiconductor, then the resulting semiconductor is known as **extrinsic semiconductor**.

Discussions

What is p type semiconductor?

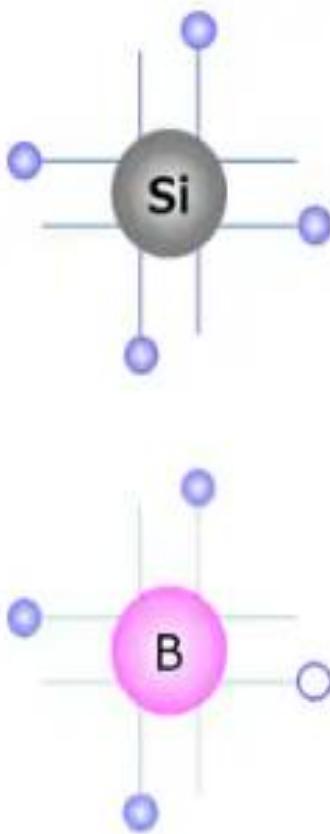
PN Junction Diode

- **P type SEMICONDUCTOR:**

- A p-type semiconductor is an intrinsic semiconductor doped with boron or indium.
- The majority of carriers in p-type semiconductors are holes.
- Electrons are minority carriers in a p-type semiconductor.
- In a p-type semiconductor, the hole density is much greater than the electron density.
- In an n-type semiconductor an intrinsic semiconductor doped with phosphorus or antimony as impurity.

PN Junction Diode

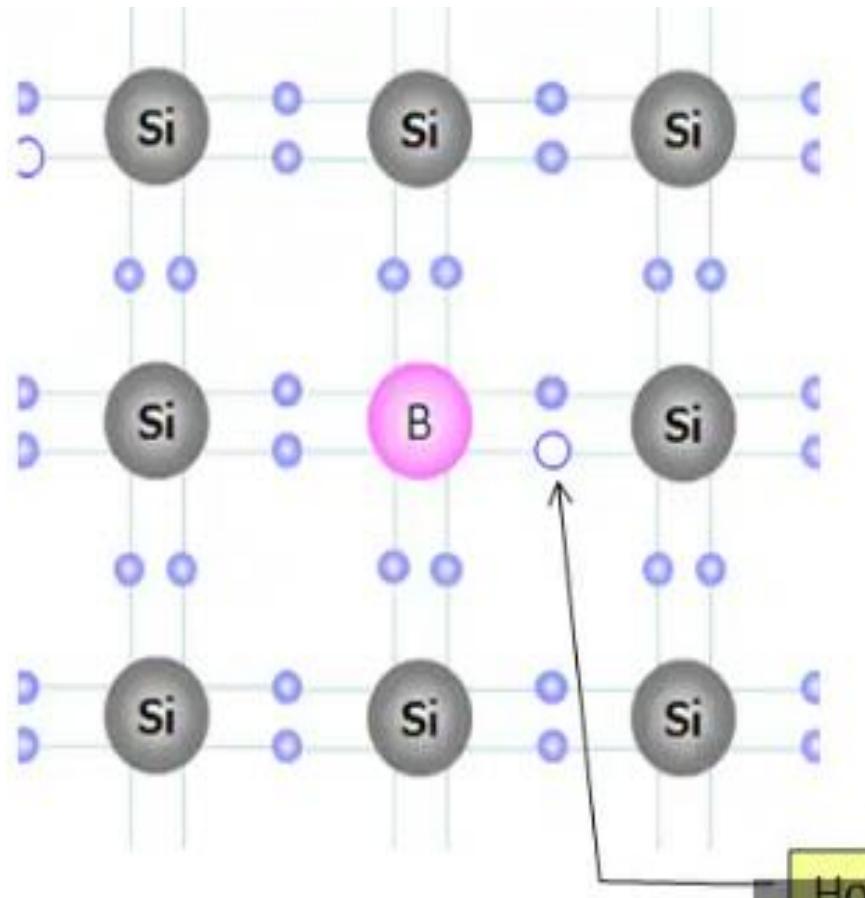
Silicon (Si):
Four valence
electrons



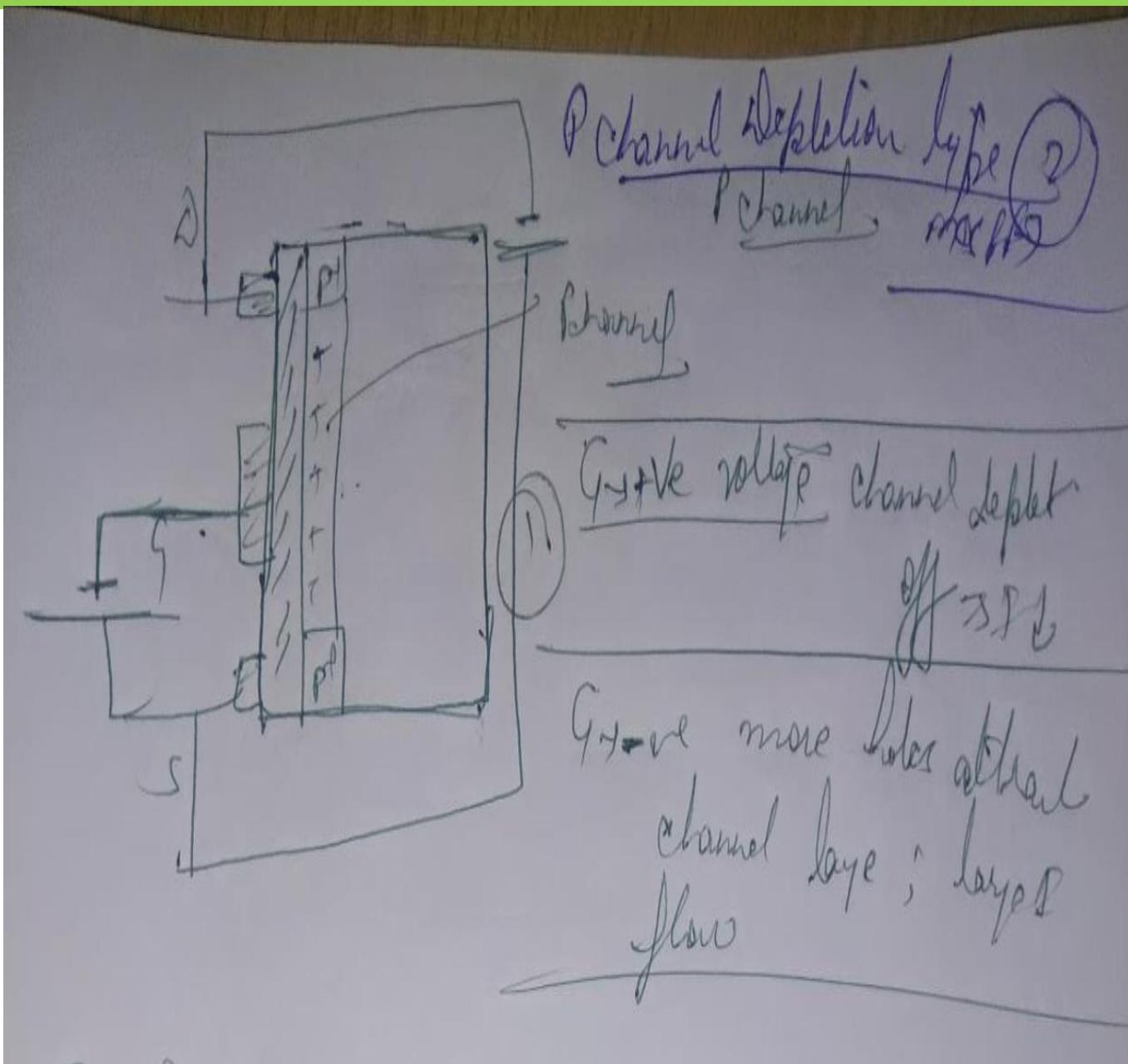
Boron (B):
Three valence
electrons



Adding boron to
pure silicon crystal
results in lack of an
electron. And it
becomes a hole.



P-channel Depletion Type MOSFET



Case-1:-

$V(\text{gate})=0$; $V(\text{DS})=\text{negative (-ve)}$

So positive (+ve) at source holes repeal & move due to this I flow.

Case-2:-

$V(\text{GS})=\text{negative (-ve)}$; $V(\text{DS})=\text{negative (-ve)}$

More holes will be attracted hence channel increase and I will also increase

Case-3:-

$V(\text{GS})=\text{positive (+ve)}$; $V(\text{DS})=\text{negative (-ve)}$

More holes will repeal & Channel decrease hence I decreases.

N-channel Depletion Type MOSFET

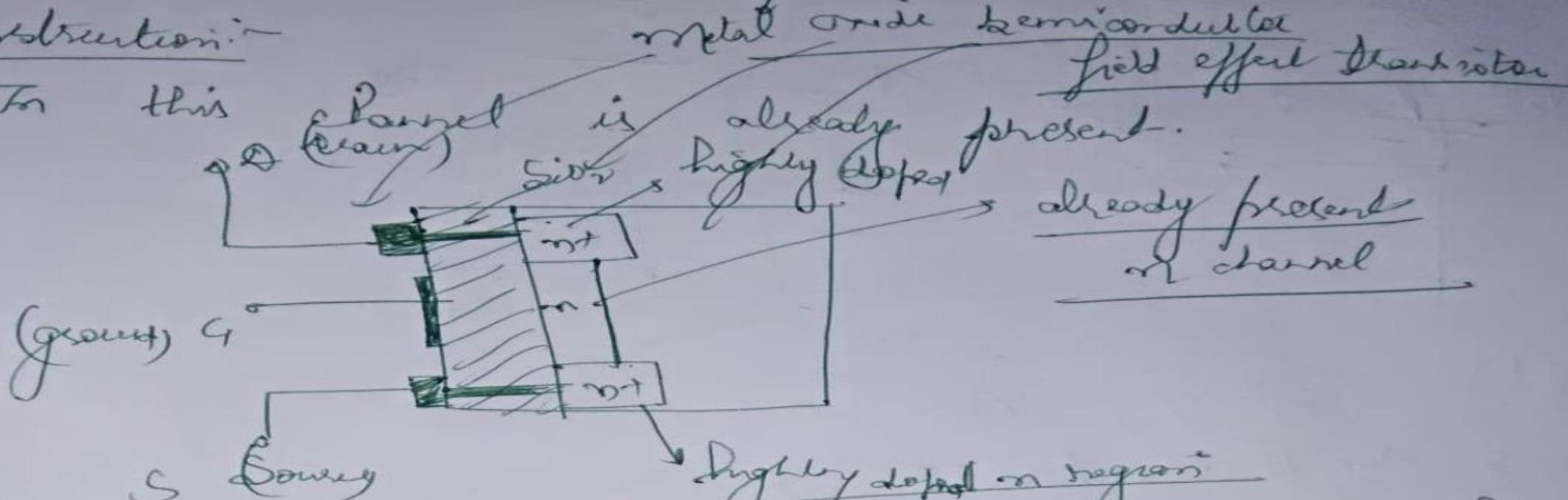
III Depletion type MOSFET

1

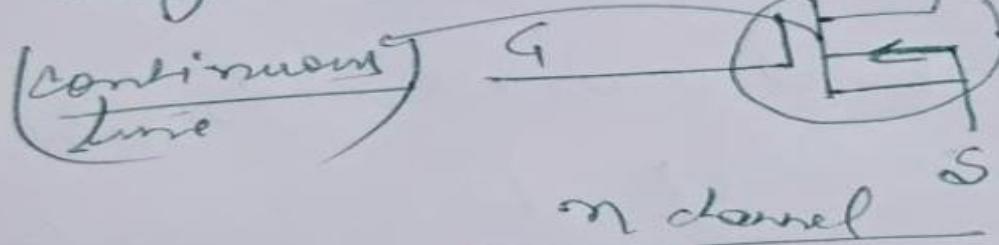
Construction:-

1

In this channel is already present.



Symbol:-



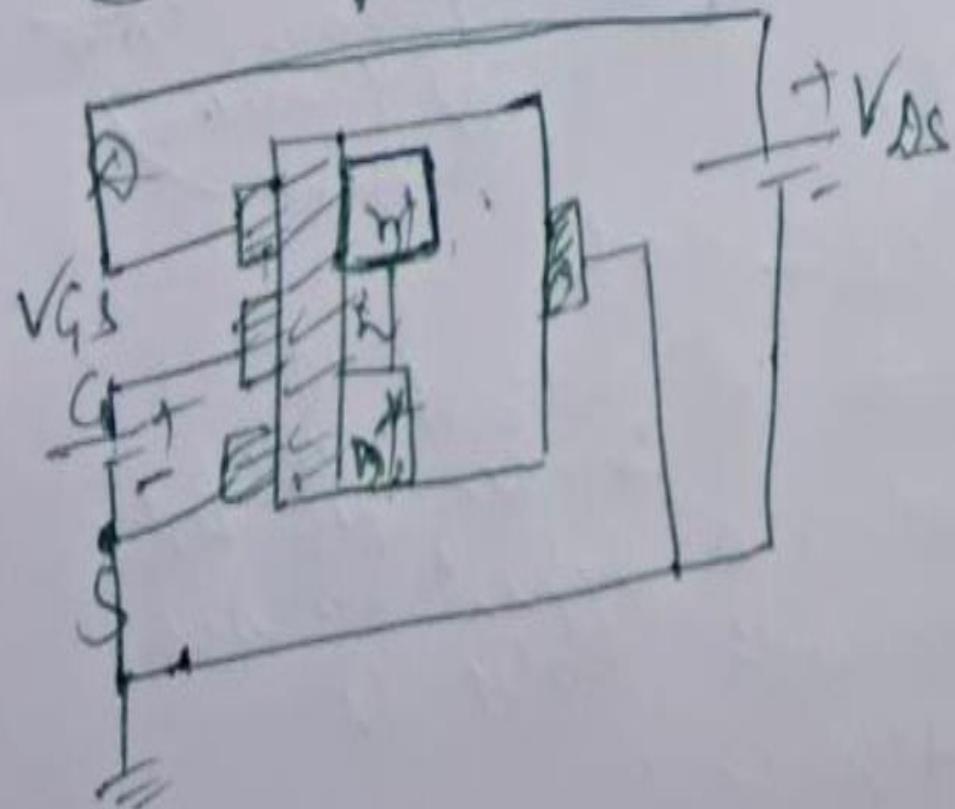
Slightly doped n region

{ For enhancement type dash is present }

N-channel Depletion Type MOSFET

①

Continuous channel in operation:-

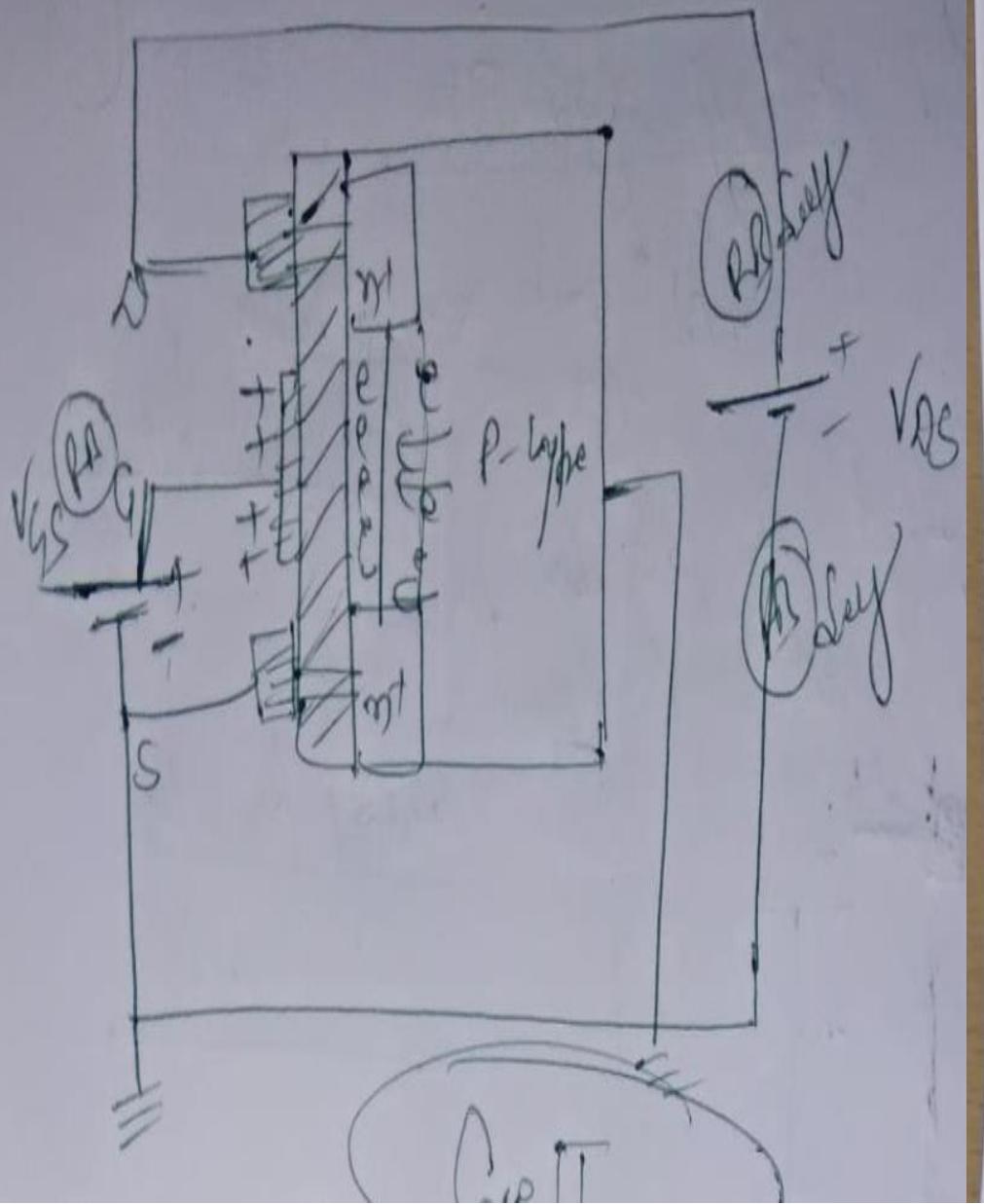


② Channel is present & ~~hence~~ make I_{DS} conduction possible

q) $V_{GS} \leq 0$

to e^- repeal from source &
more. So I_D stark flowing &
in opposite direction. After some
time pinch off will occur
from drain side
so it will be off.

N-channel Depletion Type MOSFET



Case II

① $V_{GS} = +ve$, $V_{DS} = +ve$

Q, Due to +ve biased gate e⁻ more attract toward channel
so holes will be repel

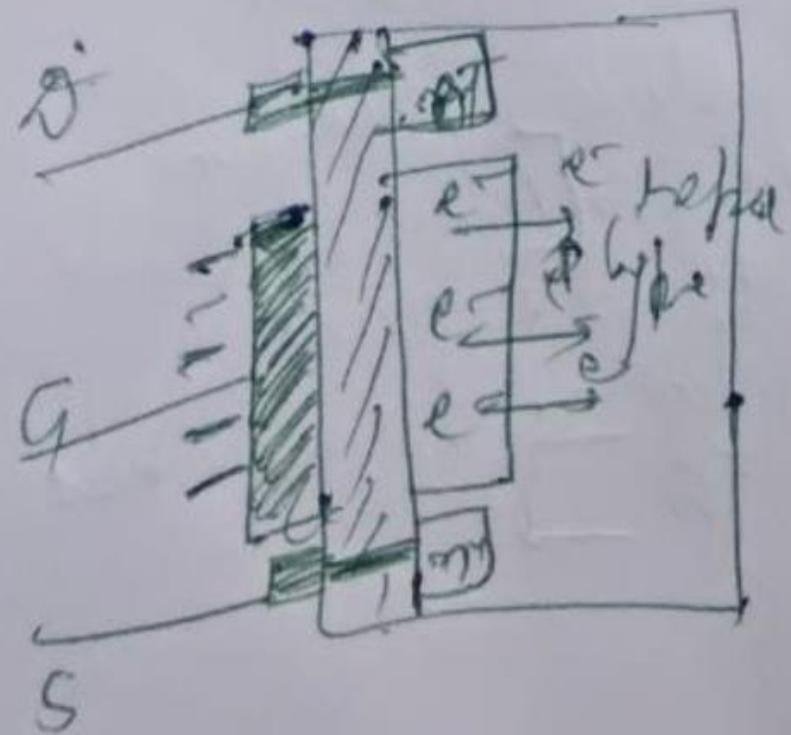
∴ hence due to more e⁻ channel width increase

C, If we keep on increasing (V_{DS}) then current
become saturate & pinch off with drain mean

current will be constant.

N-channel Depletion Type MOSFET

threshold voltage :- At which conduction start.



Qn III

say just connect
Drain and Gate
to ground.

- 1) $V_{GS} = -ve$; $V_{DS} = +ve$
2. Due to -ve V_{GS} $\rightarrow e^-$ repel & combine with holes
3. Again inverse $\rightarrow e^-$ attract more e^- combine with holes so channel depleted.

AND GATE

1. The AND gate is a logic circuit that has two or more inputs and a single output.
2. If any of the inputs are 0s, the output is 0.

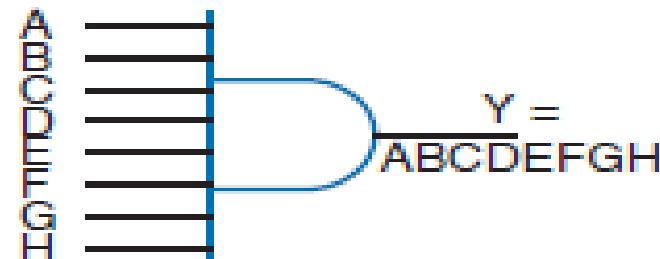
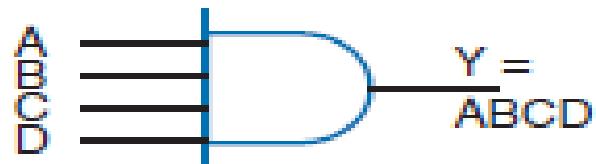
FIGURE 33–2

Truth table for a two-input AND gate.

INPUTS		OUTPUT
A	B	Y
0	0	0
1	0	0
0	1	0
1	1	1

FIGURE 33–1

Logic symbol for an AND gate.



$$Y = A \cdot B \text{ or } Y = AB.$$

OR GATE

1. An OR gate produces a 1 output if any of its inputs are 1s. The output is a 0 if all the inputs are 0s.

Refer Lab file of ECE-279

***IC Number**

***Pin diagram of IC**

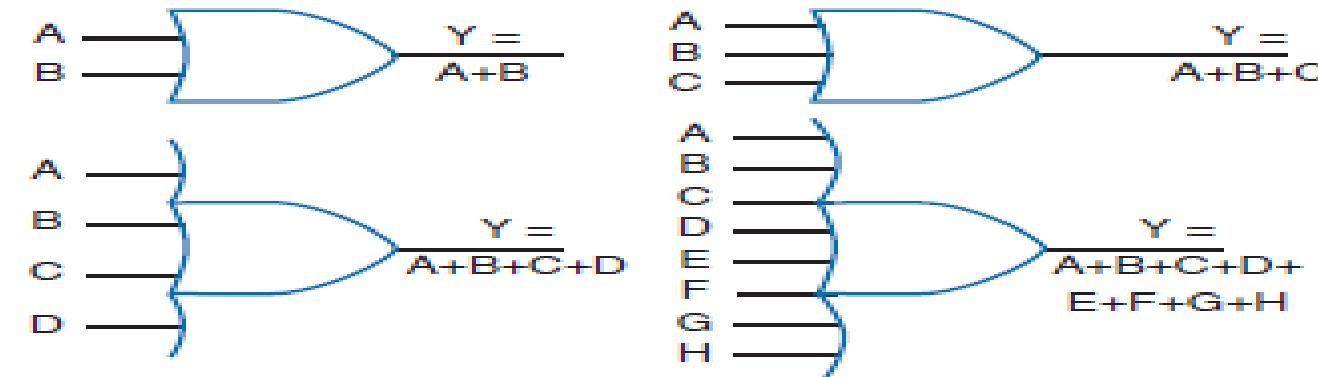
$$Y = A + B.$$

FIGURE 33-3

Truth table for a two-input OR gate.

INPUTS		OUTPUT
A	B	Y
0	0	0
1	0	1
0	1	1
1	1	1

FIGURE 33-4
Logic symbol for an OR gate.



NOT GATE

1. The simplest logic circuit is the NOT gate.
2. It performs the function called inversion, or complementation, and is commonly referred to as an Inverter.

FIGURE 33–6
Logic symbol for an inverter.

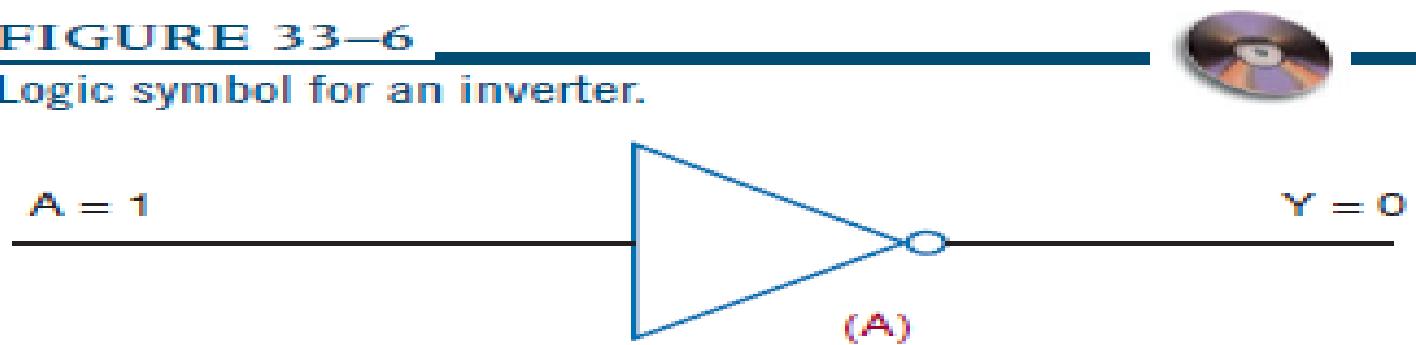


FIGURE 33–5
Truth table for an inverter.

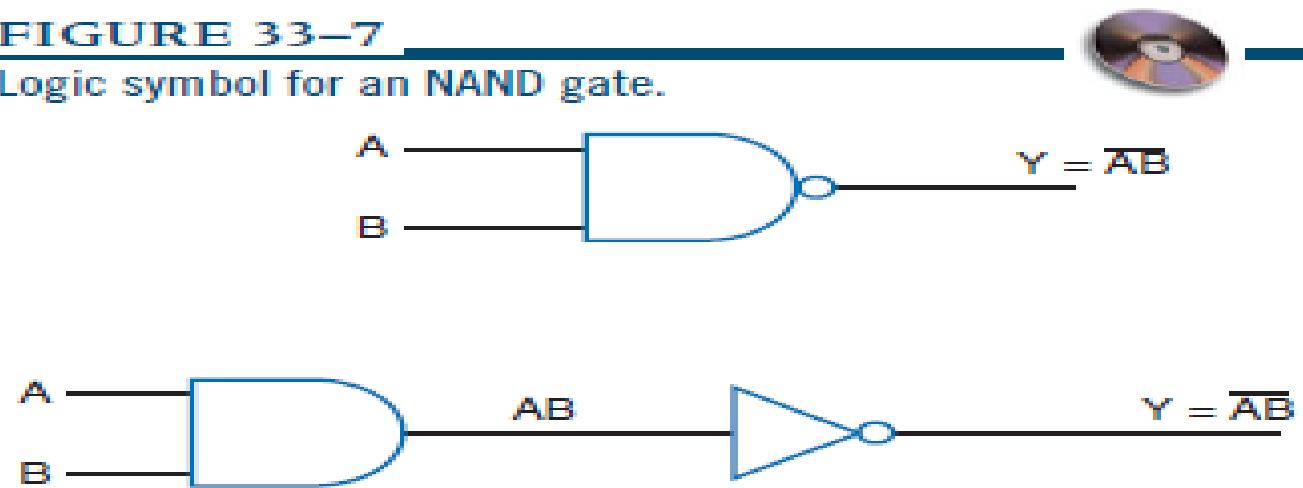
INPUTS	OUTPUT
A	Y
0	1
1	0

- The input to an inverter is labeled A and the output is labeled \overline{A} (read “A NOT” or “NOT A”).
- The bar over the letter A indicates the complement of A.

NAND GATE

1. A NAND gate is a combination of an inverter and an AND gate.

FIGURE 33–7
Logic symbol for an NAND gate.



- The algebraic formula for NAND-gate output $i_Y = \overline{AB}$,

FIGURE 33–8

Truth table for a two-input NAND gate.

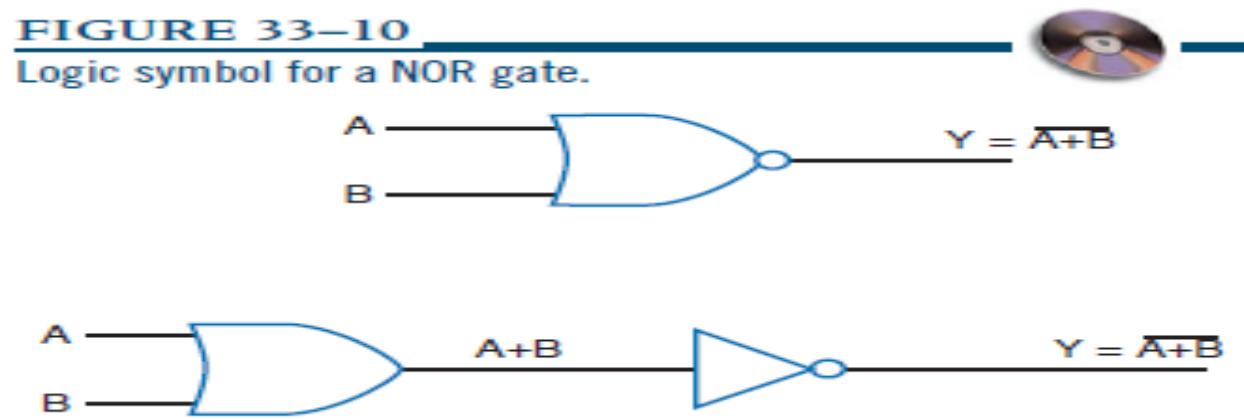
INPUTS		OUTPUT
A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

NOR GATE

1. A NOR gate is a combination of an inverter and an OR gate. Its name derives from its NOT-OR function.
2. Also shown is its equivalency to an OR gate and an inverter.

FIGURE 33–10

Logic symbol for a NOR gate.



- The algebraic expression for NOR-gate output is

$$Y = \overline{A + B},$$

A	B	out
0	0	1
0	1	0
1	0	0
1	1	0

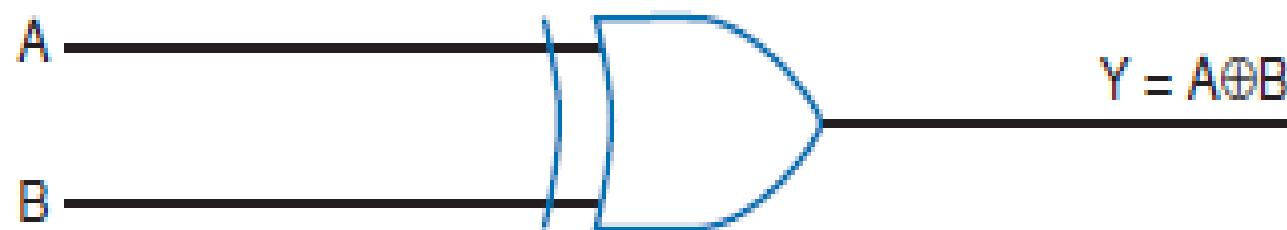
EXCLUSIVE -OR

- The XOR gate is a digital logic gate that implements an exclusive or; that is, a true output (1/HIGH) results if one, and only one, of the inputs to the gate is true.
- The algebraic output is written as

$$Y = A \oplus B.$$

FIGURE 33–12

Logic symbol for an exclusive OR gate.



A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

1. The complement of the XOR gate is the XNOR (**exclusive NOR**) gate.
2. Its symbol is shown in Figure 33–14.
3. The algebraic output is written as $\text{Y} = \overline{\text{A} \oplus \text{B}}$, read as “Y equals A exclusive nor B.”



Boolean Function, Diagram and Truth Table

- $Y = ABC$
- $Y = AB + C$



Binary, Octal and Hexadecimal number system

BINARY NUMBERS

1. The **binary system** is a base-two system because it contains two digits, 0 and 1.
2. The **decimal system** is called a base-10 system because it contains ten digits, 0 through 9.
3. The position of the 0 or 1 in a binary number indicates its value within the number. This is referred to as its place value or weight.

Power of 2:	Place Value					
	32	16	8	4	2	1
	2^5	2^4	2^3	2^2	2^1	2^0

1. To determine the largest value that can be represented by a given number of places in base 2, use the following formula:

where: n represents

Highest number = $2^n - 1$ (if place values used)

EXAMPLE: Two bits (two place values) can be used to count from 0 to 3 because:

$$2^n - 1 = 2^2 - 1 = 4 - 1 = 3$$

Example: Four bits (four place values) are needed to count from 0 to 15 because

$$2^4 - 1 = 2^4 - 1 = 16 - 1 = 15$$

BINARY AND DECIMAL CONVERSION

1. A binary number is a weighted number with a place value.
2. The value of a binary number can be determined by adding the product of each digit and its place value.

Convert the binary whole number 1101101 to decimal.

Weight: $2^6 \ 2^5 \ 2^4 \ 2^3 \ 2^2 \ 2^1 \ 2^0$

Binary number: 1 1 0 1 1 0 1

$$\begin{aligned}1101101 &= 2^6 + 2^5 + 2^3 + 2^2 + 2^0 \\&= 64 + 32 + 8 + 4 + 1 = 109\end{aligned}$$

10011011

1	1	0	1	1	0	0	1
---	---	---	---	---	---	---	---

Example:

1011001₂

1. Fractional numbers can also be represented in binary form by placing digits to the right of the binary zero point.
2. All digits to the right of the zero point have weights that are negative powers of two.

$$2^{-1} = \frac{1}{2^1} = \frac{1}{2} = 0.5$$

$$2^{-2} = \frac{1}{2^2} = \frac{1}{4} = 0.25$$

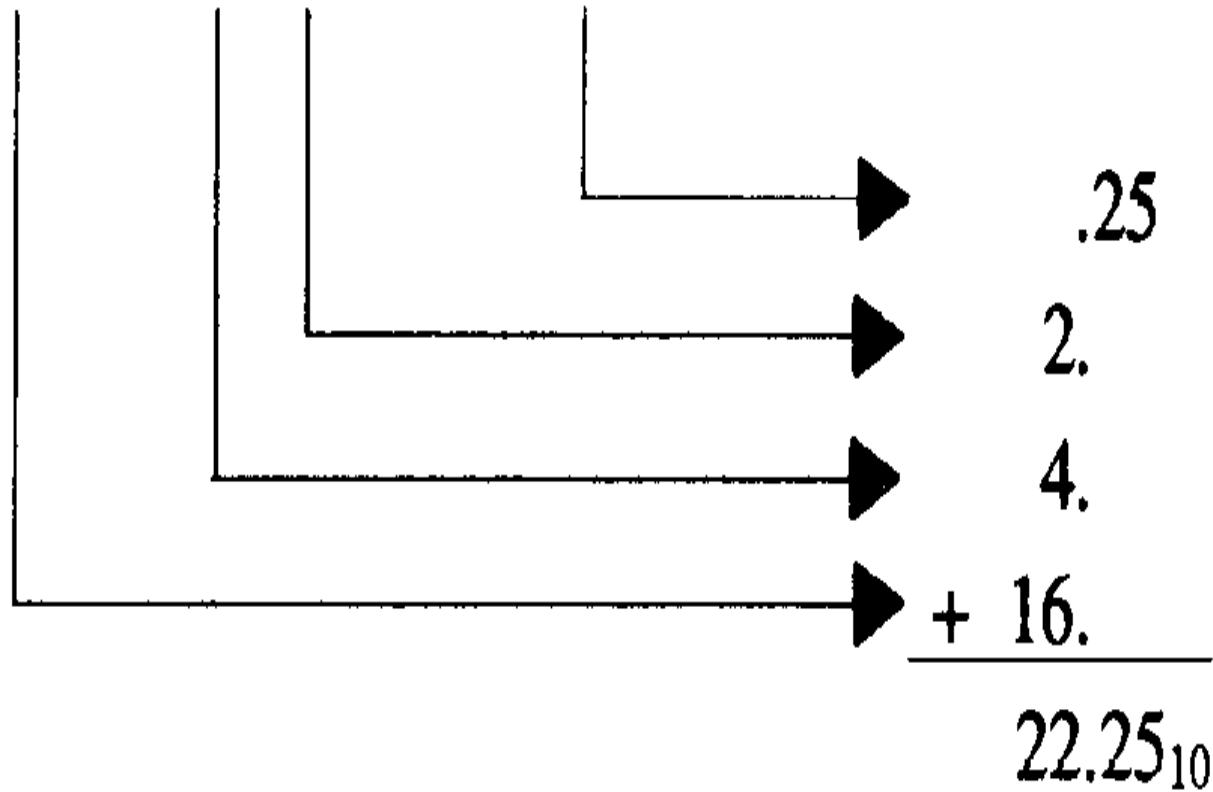
$$2^{-3} = \frac{1}{2^3} = \frac{1}{8} = 0.125$$

$$2^{-4} = \frac{1}{2^4} = \frac{1}{16} = 0.0625$$

Problem: 1 0 1 1 0. 0 1₂

Decimal 16 8 4 2 1. .5 .25

Value:



1. The most popular way to convert decimal numbers to binary numbers is to progressively divide the decimal number by 2.
2. Writing down the remainder after each division.
3. Start writing the binary number as mentioned below.
4. **EXAMPLE:** To convert 11_{10} to a binary number.

$11 \div 2 = 5$ with a remainder of 1

$5 \div 2 = 2$ with a remainder of 1

$2 \div 2 = 1$ with a remainder of 0

$1 \div 2 = 0$ with a remainder of 1

..... •

EXAMPLE 2-6

Convert the following decimal numbers to binary:

- (a) 19 (b) 45

Decimal Fraction

$$0.3125 \times 2 = 0.\underline{6}25$$

$$\downarrow$$

$$0.625 \times 2 = 1.\underline{2}5$$

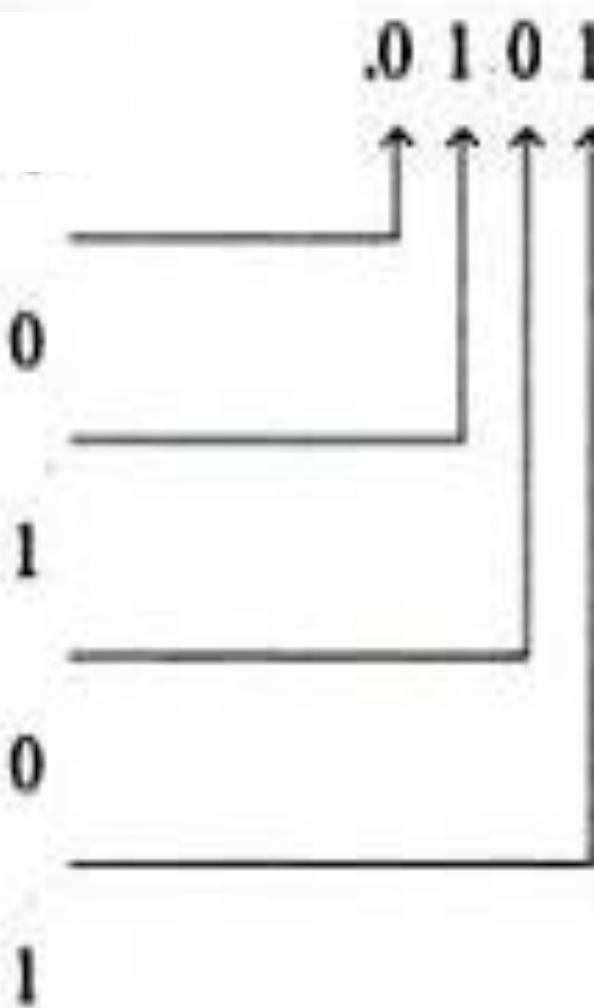
$$\downarrow$$

$$0.25 \times 2 = 0.\underline{5}0$$

$$\downarrow$$

$$0.50 \times 2 = 1.\underline{00}$$

$$\uparrow$$



Convert 13.6875_{10} to a binary fraction.

PART A:

Convert 13 to binary in the ordinary way.

$$\begin{array}{r} 2 \mid 13 & R=1 \\ \hline 2 \mid 6 & R=0 \\ \hline 2 \mid 3 & R=1 \\ \hline 2 \mid 1 & R=1 \uparrow \text{read} \uparrow \\ & 0 \end{array}$$

Therefore, $13_{10} = 1101_2$

Hence,

$13.6875_{10} = 1101.1011_2$

PART B:

Convert the decimal part in the following manner:

Read Down INTEGER PART

$$.6875 \times 2 = 1.375$$



1

$$.375 \times 2 = 0.75$$

0

$$.75 \times 2 = 1.50$$

1

$$.5 \times 2 = 1.00$$

1

Therefore, $.6875_{10} = .1011_2$

Octal Number

1. The octal number system is referred to as base-8.
2. There are 8 digits (0-7) .
3. To convert binary to an octal number requires dividing the binary number into groups of three starting from the right.

Binary Digit Value	001101010111001111
Group the bits into three's starting from the right hand side	001 101 010 111 001 111
Octal Number form	152717 ₈

CONVERTING OCTAL NUMBER TO BINARY

Converting from octal to binary is as easy as converting from binary to octal.

Simply look up each octal digit to obtain the equivalent group of three binary digits.

Octal:	0	1	2	3	4	5	6	7
Binary:	000	001	010	011	100	101	110	111

Octal = 3 4 5

Binary = 011 100 101 = 011100101 binary

OCTAL TO DECIMAL CONVERSION

- Like binary number each octal number is a weighted number with a place value.
- The value of an octal number can be determined by adding the product of each digit and its place value.

Power of 8	8^4	8^3	8^2	8^1	8^0
Place value	4096	512	64	8	1

$$\begin{aligned}2374_8 &= (2 \times 8^3) + (3 \times 8^2) + (7 \times 8^1) + (4 \times 8^0) \\&= (2 \times 512) + (3 \times 64) + (7 \times 8) + (4 \times 1) \\&= 1024 + 192 + 56 + 4 = 1276_{10}\end{aligned}$$

DECIMAL TO OCTAL NUMBER CONVERSION

- Repeated Division by 8
- Example
- $213_{10} = (?)_8$?

Divide-by -8	Quotient	Reminder
$213 / 8$	26	5
$26 / 8$	3	2
$3 / 8$	0	3

Answer = 325_8

Hexadecimal Numbers

- The hexadecimal number system is referred to as base 16.
- There are sixteen digits: 0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F.
- The advantage of hexadecimal is that they are converted directly from four bits of binary numbers.
- ❖ To convert binary to a hexadecimal number requires dividing the binary number into groups of four from right.

We take any binary number suppose 100010100101_2

Breaking it into groups of 4 we get

$1000|1010|0101$

Now converting all the groups into decimal numbers individually we get

$8 | 10 | 5$

So the desired hexadecimal equivalent of the binary number 100010100101_2 is $8A5_{16}$

EXAMPLE 2-32

Convert each of the following binary numbers to octal:

- (a) 110101 (b) 101111001 (c) 100110011010 (d) 11010000100

HEXADECIMAL TO BINARY

- Converting from hexadecimal to binary is as easy as converting from binary to hexadecimal.
- Simply look up each hexadecimal digit to obtain the equivalent group of four binary digits.

Hexadecimal:	0	1	2	3	4	5	6	7
Binary:	0000	0001	0010	0011	0100	0101	0110	0111
Hexadecimal:	8	9	A	B	C	D	E	F
Binary:	1000	1001	1010	1011	1100	1101	1110	1111

Hexadecimal = A 2 D E

Binary = 1010 0010 1101 1110 = 1010001011011110 binary

HEXADECIMAL TO DECIMAL

16^0	1
$16^1 = 16$	16
$16^2 = 16 \times 16$	256
$16^3 = 16 \times 16 \times 16$	4096
$16^4 = 16 \times 16 \times 16 \times 16$	65536

Convert the number **589** HEXADECIMAL to DECIMAL

MULTIPLICATION	RESULT
$9 \times (16^0)$	9
$8 \times (16^1)$	128
$5 \times (16^2)$	1280
ANSWER	1417

Decimal to hexadecimal

- Convert the number **256** DECIMAL to HEXADECIMAL

DIVISION	RESULT	REMAINDER (in HEX)
$256 / 16$	16	0
$16 / 16$	1	0
$1 / 16$	0	1
ANSWER		100

EXAMPLE 2-28

Convert the decimal number 650 to hexadecimal

BCD

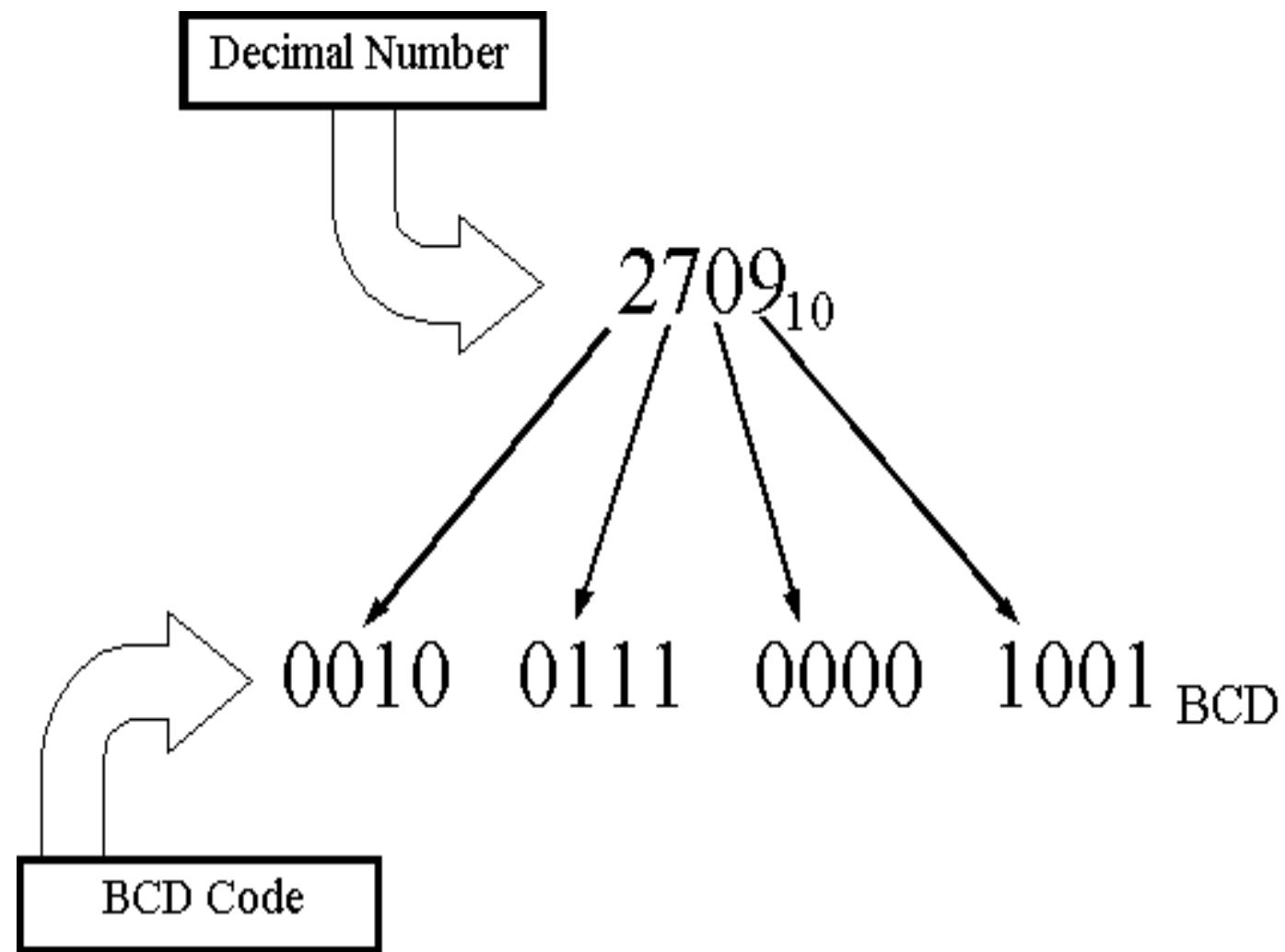
- **BCD** or **Binary Coded Decimal** is that number system or code which has the binary numbers or digits to represent a decimal number.
- A decimal number contains 10 digits (0-9). Now the equivalent binary numbers can be found out of these 10 decimal numbers.
- In case of **BCD** the binary number formed by four binary digits, will be the equivalent code for the given decimal digits.
- In **BCD** we can use the binary number from 0000-1001 only, which are the decimal equivalent from 0-9 respectively.

- An 8421 code is a binary-coded-decimal (BCD) code consisting of four binary digits.
- The 8421 designation refers to the binary weight of the 4 bits.

Power of 2: 2^3 2^2 2^1 2^0

Binary weight: 8 4 2 1

DECIMAL TO BCD CODE



BCD TO DECIMAL

Example:

Convert 0110100000111001 (BCD) to its decimal equivalent.

Solution:

Divide the BCD number into 4-bit groups and convert each to decimal.

0110	1000	0011	1001
6	8	3	9

BCD-to-Decimal Conversion

Convert BCD code 1001 0100 0111 0000 to decimal



Poll

Ans: 9460

Yes/No

Binary to Gray code

The most significant bit (left-most) in the Gray code is the same as the corresponding MSB in the binary number.

Going from left to right, add each adjacent pair of binary code bits to get the next Gray code bit. Discard carries.

For example, the conversion of the binary number 10110 to Gray code is as follows:

	-	+	→	0	-	+	→		-	+	→		-	+	→	0	Binary
↓		↓		↓		↓		↓		↓		↓		↓		↓	
1		1		1		0		1		1		0		1		1	Gray

The Gray code is 11101.

Gray to Binary Code

1. The most significant bit (left-most) in the binary code is the same as the corresponding bit in the Gray code.
2. Add each binary code bit generated to the Gray code bit in the next adjacent position. Discard carries.

For example, the conversion of the Gray code word 11011 to binary is as follows:

$$\begin{array}{ccccccccc} & 1 & & 1 & & 0 & & 1 & \\ & \downarrow & + & \downarrow & + & \downarrow & + & \downarrow & \downarrow \\ 1 & + & 0 & + & 0 & + & 1 & + & 0 \\ & \searrow & \swarrow & \searrow & \swarrow & \searrow & \swarrow & \searrow & \swarrow \\ & 0 & & 0 & & 1 & & 0 & \\ & & & & & \downarrow & & & \\ & & & & & 1 & & & \\ & & & & & \downarrow & & & \\ & & & & & \text{Binary} & & & \end{array} \quad \begin{array}{c} \text{Gray} \\ \text{Binary} \end{array}$$

The binary number is 10010.

Binary to gray

A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

It is an ordering of the binary system such that two successive values differ in only one bit.

BCD to Excess-3 Code

Decimal Number	BCD Code				Excess-3 Code			
	A	B	C	D	W	x	y	z
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

Law/Theorem	Law of Addition	Law of Multiplication
Identity Law	$x + 0 = x$	$x \cdot 1 = x$
Complement Law	$x + x' = 1$	$x \cdot x' = 0$
Idempotent Law	$x + x = x$	$x \cdot x = x$
Dominant Law	$x + 1 = 1$	$x \cdot 0 = 0$
Involution Law	$(x')' = x$	
Commutative Law	$x + y = y + x$	$x \cdot y = y \cdot x$
Associative Law	$x + (y + z) = (x + y) + z$	$x \cdot (y \cdot z) = (x \cdot y) \cdot z$
Distributive Law	$x \cdot (y + z) = x \cdot y + x \cdot z$	$x + y \cdot z = (x + y) \cdot (x + z)$
Demorgan's Law	$(x + y)' = x' \cdot y'$	$(x \cdot y)' = x' + y'$
Absorption Law	$x + (x \cdot y) = x$	$x \cdot (x + y) = x$

Discussions

$$\begin{aligned}& \overline{\overline{A} \cdot (A + C)} \\&= \overline{\overline{A}} + \overline{(A + C)} \\&= \overline{\overline{A}} + \overline{\overline{A}} \cdot \overline{\overline{C}} \\&= \overline{\overline{A}} (1 + \overline{\overline{C}}) \\&= \overline{\overline{A}} \cdot 1\end{aligned}$$

Questions

$$\cdot (A + B)(A + C) = A + BC$$

$$\begin{aligned}(A + B)(A + C) &= AA + AC + AB + BC \\&= A + AC + AB + BC \\&= A(1 + C) + AB + BC \\&= A \cdot 1 + AB + BC \\&= A(1 + B) + BC \\&= A \cdot 1 + BC \\&= A + BC\end{aligned}$$

Questions

Apply DeMorgan's theorems to the expressions \overline{XYZ} and $\overline{X + Y + Z}$.

Solve

Solutions

Apply DeMorgan's theorems to the expressions \overline{XYZ} and $\overline{X + Y + Z}$.

$$\overline{XYZ} = \overline{X} + \overline{Y} + \overline{Z}$$

$$\overline{X + Y + Z} = \overline{XYZ}$$

Sum of Product (SOP) form & Product of sum (POS) form

Any logic expression can be expressed in the following two standard form.

- 1) Sum of product (SOP)
- 2) Product of sum (POS)

Sum of Product (SOP) form

product

$$Y = \overbrace{AB + AC + BC}^{\substack{\uparrow \quad \uparrow \\ \text{sum of}}} \quad$$

It is in form of sum of three terms AB, AC, BC with each individual term is product of two variables

②
$$\boxed{Y = ABC + BCD + ABD}$$

5

Product of sum form (POS)

$$Y = (A+B) \cdot (B+C) \cdot (A+C)$$

sum terms

Product

It is in the form of product of three terms $(A+B)$, $(B+C)$ and $(A+C)$ with each term is in form of sum of two variables.

Standard or Canonical SOP form

Standard
SOP form

$$Y = A\bar{B}C + A\bar{B}\bar{C} + \bar{A}BC$$

Variates

Each product term consists of all the literals in the complemented or uncomplemented form

Standard
SOP form

$$Y = (A + B + \bar{C}) \cdot (A + \bar{B} + C) \cdot (\bar{A} + \bar{B} + \bar{C})$$

variables
literals
in the sum form

Each sum term consists of all the complemented & uncomplemented

$$Y = AB + A\bar{B}C + \bar{A}BC \quad \{ \text{Non Standard SOP} \}$$

$$Y = AB + A\bar{B} + \bar{A}\bar{B} \quad \{ \text{Standard SOP} \}$$

$$Y = (\bar{A}+B) (A+B) (A+\bar{B}) \quad \{ \text{Standard POS} \}$$

$$Y = (\bar{A}+B) (A+B+C) \quad \{ \text{Non-Standard POS} \}$$

Converting Product Terms to Standard SOP (example)

- Convert the following Boolean expression into standard SOP form:

$$A\bar{B}C + \bar{A}\bar{B} + A\bar{B}\bar{C}D$$

$$A\bar{B}C = A\bar{B}C(D + \bar{D}) = \boxed{A\bar{B}CD + A\bar{B}C\bar{D}}$$

$$\bar{A}\bar{B} = \bar{A}\bar{B}(C + \bar{C}) = \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}$$

$$\bar{A}\bar{B}C(D + \bar{D}) + \bar{A}\bar{B}\bar{C}(D + \bar{D}) = \boxed{\bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D}}$$

$$A\bar{B}C + \bar{A}\bar{B} + A\bar{B}\bar{C}D = \boxed{A\bar{B}CD + A\bar{B}C\bar{D}} + \boxed{\bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D}} + A\bar{B}\bar{C}D$$

Questions

Convert the expression $(A + \bar{B})(B + C)$ to standard POS form.

Solve

Solutions

Solution

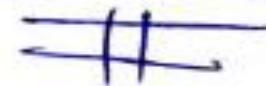
$$(A + \bar{B})(B + C)$$

$$\Rightarrow (A + \bar{B} + C\bar{C})(A + \bar{A} + B + C)$$

$$\Rightarrow (A + \bar{B} + C)(A + \bar{B} + \bar{C})(A + B + C)(\bar{A} + B + C)$$

$$\overbrace{x + y + z = (x + y) + (x + z)}^{\text{associative law}}$$

Concepts of Minterms(m) and Maxterms(M)



Concepts of Minterm & Maxterm

Y = (15th + A \bar{B})



Minterm :- Each individual term in standard pos form is called minterm.

$$Y = AB + A\bar{B}C + \bar{A}BC$$

Maxterm :-

$$Y = (A+B)(A+\bar{B})$$

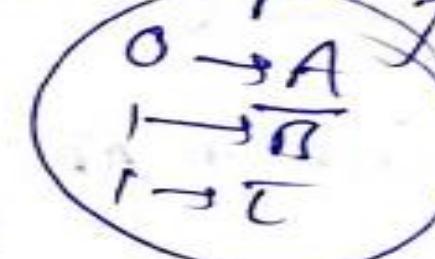
Each individual term in standard pos form is called Maxterm.

How are minterms and maxterms obtained

① How are the minterms obtained?
Ans: Let the minterm $A\bar{B}C = 011$
Minterm $\rightarrow \bar{A}B\bar{C}$
OR-complement of generally AND op. {
 $\begin{cases} 0 \rightarrow \bar{A} \\ 1 \rightarrow A \\ F \rightarrow C \end{cases}$ }
Minterm $\rightarrow \bar{A}B\bar{C}$ corresponding to $A\bar{B}C = 011$

Let $A\bar{B}C = 011$ of generally OR op. form
Maxterm $\rightarrow A + \bar{B} + \bar{C}$

corresp to $A\bar{B}C = 011$,



$A \quad \bar{B} \quad C$
0 1 1 → 1

for the truth table of two values white
mention 1 maxima.

Variables		Milena	Maxima
A	B	m_1	m_1
0	0	$m_0 \rightarrow \bar{A} \bar{B}$	$m_1 = A + B$
0	1	$m_1 \rightarrow \bar{A} B$	$m_1 = A + \bar{B}$
1	0	$m_2 \rightarrow A \bar{B}$	$m_1 = \bar{A} + B$
1	1	$m_3 \rightarrow AB$	$m_1 = \bar{A} + \bar{B}$

Representation of logical expression using Minterms & Maxterms

①

$$Y = ABC + \bar{A}BC + A\bar{B}\bar{C}$$

$\begin{matrix} 111 \\ m_7 \end{matrix} \quad \begin{matrix} 011 \\ m_3 \end{matrix} \quad \begin{matrix} 100 \\ m_4 \end{matrix}$

← complementation

$$Y = m_7 + m_3 + m_4$$

$$Y = \Sigma m(3, 4, 7)$$

Representation

~~Y = ABC + A'BC + AB'C~~, $\Sigma \rightarrow$ sum of product

$$(2) \quad Y = \frac{(A+B+C)(A+B+C)(A+\bar{B}+C)}{M_2 M_0 M_8}$$

Max/min

$A \rightarrow 0$

$\pi \rightarrow 1$

$\boxed{Y = \pi M(92,6)}$

product of sum

other way * Reffer

(from the truth table obtain logical exprns.)

A	B	y
0	0	0
0	1	1
1	0	1
1	1	0

a) Consider only those rows which can $\Rightarrow y = 1$

$$y_1 = \bar{A}B$$

$$y_2 = A\bar{B}$$

③

for SOP, $y = y_1 + y_2$ any of OR all the first term

$$y = \overline{A}B + A\bar{B}$$

Karnaugh - Map (K-Map) Simplification

(3)

Kmap is a general with graphical method of simplifying
a boolean equation.

Kmap Structure :-

- a) The structure of a 2 inputs (variables) Kmap is

		\bar{B}	B
\bar{A}	0	$\bar{A}\bar{B}$	$\bar{A}B$
A	1	$A\bar{B}$	AB

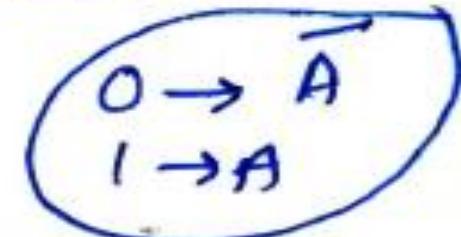
Here AB are IP

0 & 1 are values of A or B

Inside box, we can enter output
value of y .

(b) 3 Variable K-map :-

		BC	00	01	11	10	
		A	0	$\bar{A}\bar{B}\bar{C}$	$\bar{A}\bar{B}C$	$\bar{A}BC$	$\bar{A}B\bar{C}$
0	0		$\bar{A}\bar{B}\bar{C}$	$\bar{A}\bar{B}C$	$\bar{A}BC$	$\bar{A}B\bar{C}$	
	1		$A\bar{B}\bar{C}$	$A\bar{B}C$	ABC	$A\bar{B}\bar{C}$	



(c) 4 Variables Kmap :-

		CD	00	01	11	10
		AB	0000	0001	0010	0011
0000	00					
	01					
11						
10						

00
01
11
10
Gray code

(2)

A	B	0	1
0	00	01	
1	10	11	

decimal

00	→	0
01	→	1
10	→	2
11	→	3

A	B	C	00	01	11	10
0			000	001	011	010
1			100	101	111	110

decimal

000	→	0
001	→	1
011	→	3
010	→	2

A	B	C	00	01	11	10
0			m ₀	m ₁	m ₃	m ₂
1			m ₄	m ₅	m ₇	m ₆

(A)

AB	00	01	11	10
00	0000	0001	0011	0010
01	0100	0101	0111	0110
11	1100	1101	1111	1110
10	1000	1001	1011	1010

(B)

AB	00	01	11	10
00	m_0	m_1	m_3	m_2
01	m_4	m_5	m_7	m_6
11	m_{12}	m_{13}	m_{15}	m_{14}
10	m_8	m_9	m_{11}	m_{10}

$1010 \rightarrow 10$

Relation between truth table & Kmaps

(1)

	A	B	Y
m_0	0	0	0
m_1	0	1	1
m_2	1	0	0
m_3	1	1	1

A	B	Y
0	0	1
1	0	1

	A	B	C	Y
m_0	0	0	0	1
m_1	0	0	1	0
m_2	0	1	0	0
m_3	0	1	1	1
m_4	1	0	0	0
m_5	1	0	1	1
m_6	1	1	0	0
m_7	1	1	1	1

A	BC	00	01	11	10
0	0	1	0	1	0
1	0	0	1	1	0

Q. Represent the equation given below on K-map

Soln:-

$$Y = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C + ABC$$

		BC $\bar{B}\bar{C}$		BC		BC	
		00	01	11	10	10	
$\bar{A}\bar{B}\bar{C}$	A	0	1	1	0	0	
	\bar{A}	1	0	0	1	1	
$\bar{A}\bar{B}C$	A	1	1	0	1	1	
	B	0	1	1	0	1	
$A\bar{B}\bar{C}$	A	0	1	1	0	0	
	C	1	0	0	1	1	

SOP=FILL LOGIC 1

③

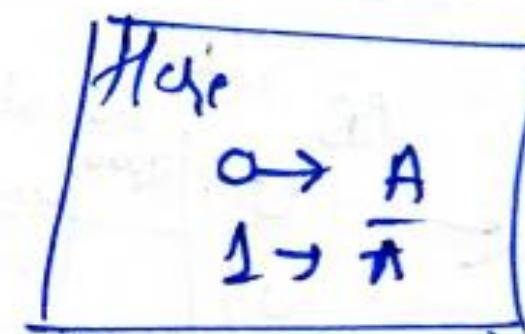
Q: Represent the following standard POS expression in K-Map

$$Y = (A+B+C) \cdot (A+\bar{B}+C) \cdot (\bar{A}+\bar{B}+C)$$

POS=FILL LOGIC 0

		BC	00	01	11	10	
		A	0	1	1	1	$\bar{A} + B + C$
A	BC	0	0	1	1	0	
		1	1	1	1	0	$\bar{A} + B + \bar{C}$

$$\begin{aligned} A+B+C &\Rightarrow 000 \rightarrow M_0 \\ A+\bar{B}+C &\Rightarrow 010 \rightarrow M_2 \\ \bar{A}+\bar{B}+C &\Rightarrow 110 \rightarrow M_6 \end{aligned}$$



Simplification of Boolean Expression Using K-Mat

- A) A group of two adjacent 1's or 0's is called pair.
- B) Quad :- A group of four adjacent 1's or 0's called quad.
- C) Octet :- A group of eight adjacent 1's or 0's called OCTET as Octet.

Grouping of two adjacent ones (II) Part

A)

	BC	$\bar{B}C$	$\bar{B}C$	BC	$\bar{B}\bar{C}$
\bar{A}	0	0	1	1	0
A	1	0	0	0	0

$$Y = \bar{A}B$$

otherwise :-

$$Y = \bar{A}BC + \bar{A}B\bar{C}$$

$$\Rightarrow \bar{A}B(C + \bar{C}) \Rightarrow \bar{A}B$$

B) A $\begin{array}{c} \bar{B} \\ \bar{A} \\ A \\ \bar{A} \end{array}$

$\bar{B}C$	$\bar{B}\bar{C}$	$\bar{B}C$	$\bar{B}\bar{C}$	$\bar{B}C$
$\bar{B}C$	0	1	0	0
$\bar{B}\bar{C}$	0	1	0	0
$\bar{B}C$	0	0	0	0

$$\begin{aligned}
 Y &= \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} \\
 &\Rightarrow \bar{B}C(\bar{A} + A) \\
 &\Rightarrow \bar{B}C
 \end{aligned}$$

③

		$\bar{B}C\bar{B}\bar{C}$	$\bar{B}C$	BC	BC
		00	01	11	10
\bar{A}	0	0	0	0	0
A	1	0	0	0	1

$$Y = A \cdot \bar{C}$$

$$Y = A\bar{B}\bar{C} + A\bar{B}C$$

$$\Rightarrow A\bar{C}(B + \bar{B})$$

$$\Rightarrow A\bar{C}$$

①

K Map for 4 Variables

		CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
		00	01	11	10	
$\bar{A}\bar{B}$	00	0	0	0	0	0
	01	1	1	0	0	0
$A\bar{B}$	11	1	1	0	0	0
	10	0	0	0	0	0

$$Y = BC\bar{D}$$

$$Y(A, B, C) = \Sigma m(4, 5, 12, 13)$$

Y(A, B, C, D)

**SUM minterm means
fill '1' logic**

②

$\bar{A}B$	AB	$C_0 C_1$	$\bar{C}_0 C_1$	$C_0 \bar{C}_1$	$\bar{C}_0 \bar{C}_1$
$\bar{A}B$	00	0	1	1	0
$\bar{A}B$	01	0	0	0	0
AB	11	0	0	0	0
$A\bar{B}$	10	0	1	1	0

$$Y = \bar{B}D$$

$$Y(A,B,C) = \sum m(1,3,9,11)$$

Y(A,B,C,D)

**SUM minterm means
fill '1' logic**

③

		C_0	\bar{C}_0	$\bar{C}_0 \bar{C}_1$	$C_0 \bar{C}_1$	$C_0 C_1$
		00	01	11	10	00
$\bar{A} \bar{B}$	00	0	0	0	0	0
	01	1	0	0	0	1
$\bar{A} B$	11	1	0	0	0	1
	10	0	0	1	0	0

$$Y = B \bar{A}$$

$$Y(A, B, C) = \Sigma m(4, 6, 12, 14)$$

Y(A,B,C,D)

**SUM minterm means
fill '1' logic**

(4)

Special

$\bar{A}B\bar{C}$	$\bar{A}B\bar{C}\bar{D}$	$\bar{A}B\bar{C}D$	$\bar{A}BC\bar{D}$	$\bar{A}BCD$	$\bar{A}B\bar{C}D$
$\bar{A}B$	00	01	11	10	
$A\bar{B}$	01	0	0	0	
AB	11	0	0	0	
$A\bar{B}$	10	1	0	0	110

$$Y = \bar{B}\bar{D}$$

$$Y(A, B, C) = \Sigma m(0, 2, 8, 10)$$

$$Y(A, B, C, D)$$

SUM minterm means
fill '1' logic

otherwise :-

Simplification of Boolean expression

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D$$

$$Y = \bar{B}\bar{C}\bar{D}(\bar{A}+A) + \bar{B}\bar{C}D(\bar{A}+A)$$

$$Y = \bar{B}\bar{C}\bar{D} + \bar{B}\bar{C}D \Rightarrow \bar{B}\bar{D}(C+\bar{C}) = \bar{B}\bar{D}$$

Advantage

Poll

3. The Boolean expression $Y = (AB)'$ is logically equivalent to what single gate?

- a) NAND
- b) NOR
- c) AND
- d) OR

Solutions

3. The Boolean expression $Y = (AB)'$ is logically equivalent to what single gate?

- a) NAND
- b) NOR
- c) AND
- d) OR

 [View Answer](#)

Answer: a

Explanation: If A and B are the input for AND gate the output is obtained as AB and after inversion we get $(AB)'$, which is the expression of NAND gate. NAND gate produces high output when any of the input is 0 and produces low output when all inputs are 1.

Map the following standard SOP expression on a Karnaugh map:

$$\overline{A}\overline{B}CD + \overline{A}\overline{B}\overline{C}\overline{D} + A\overline{B}\overline{C}D + ABCD + A\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}D + A\overline{B}CD$$

Solu

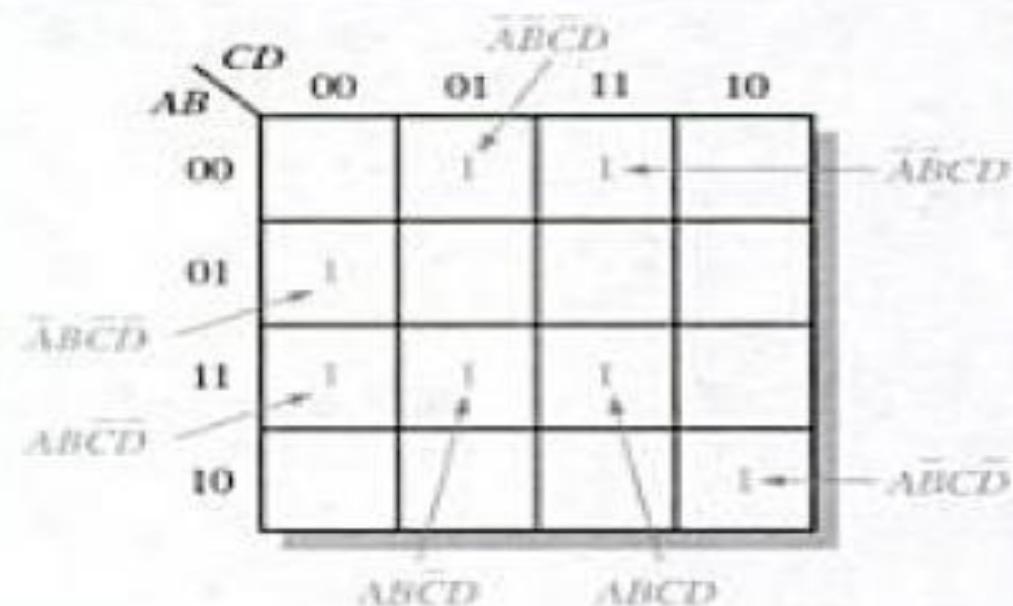
Map the following standard SOP expression on a Karnaugh map:

$$\overline{ABCD} + \overline{ABC\bar{D}} + A\overline{BCD} + ABCD + A\overline{B\bar{C}D} + \overline{A\overline{B}CD} + A\overline{B\bar{C}\bar{D}}$$

Solution The expression is evaluated as shown below. A 1 is placed on the 4-variable Karnaugh map in Figure 4-25 for each standard product term in the expression.

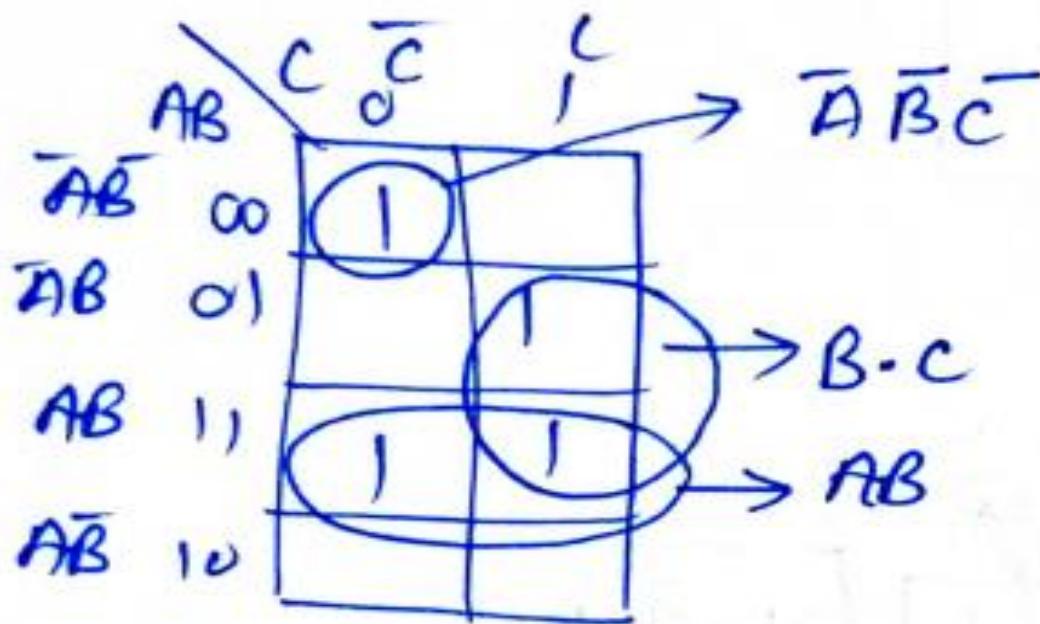
$$\overline{ABCD} + \overline{ABC}\overline{D} + A\overline{BCD} + ABCD + A\overline{BC}\overline{D} + \overline{ABC}\overline{D} + A\overline{BCD}$$

► FIGURE 4-25



Q:- determine the product terms of Kmap by writing the resulting minimum SOP expressions.

Solution :-

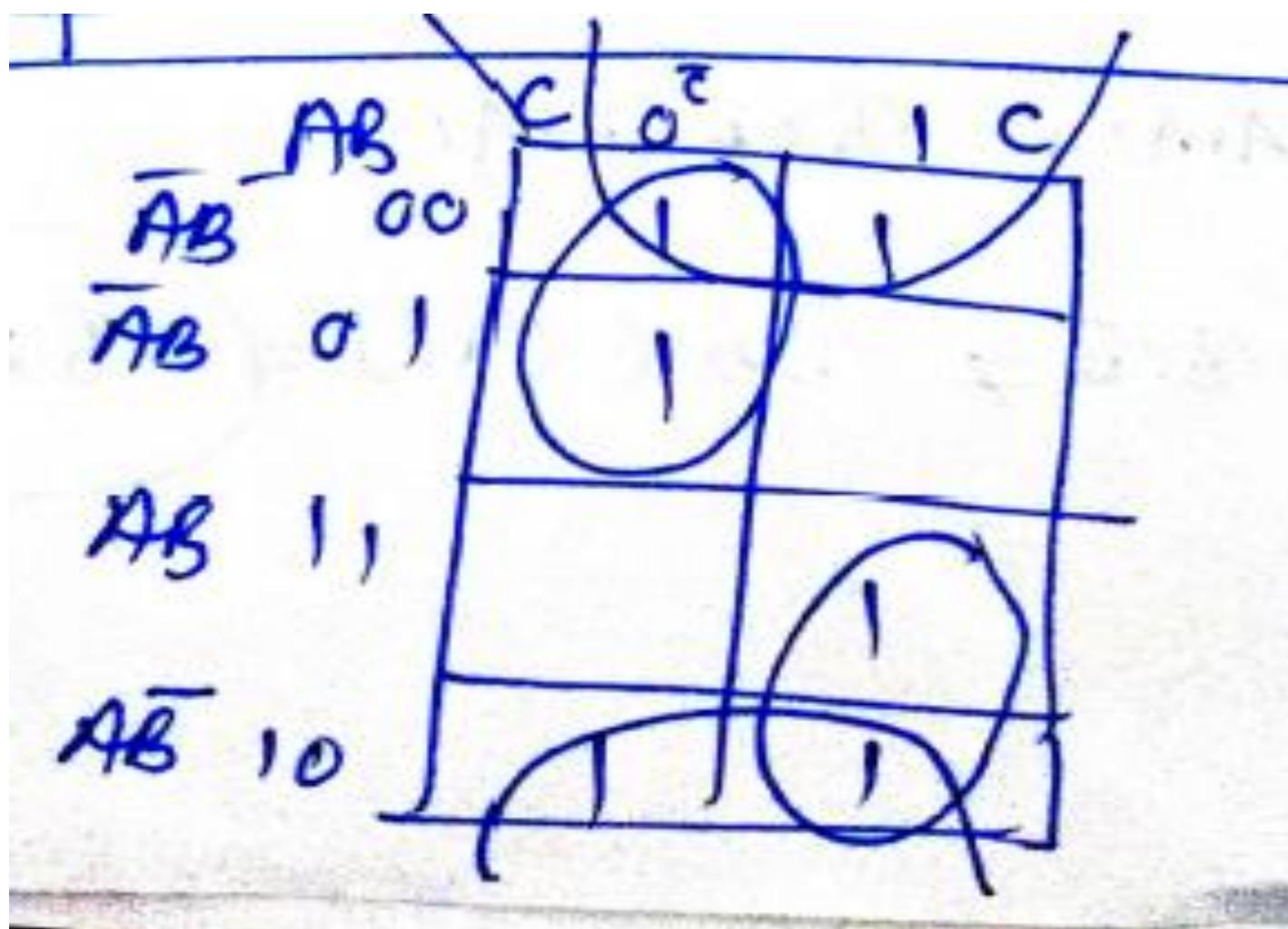


1. Overlapping pairs are allowed like this
2. No logic 1 should be left
3. Go from higher (octet) to lower (single)

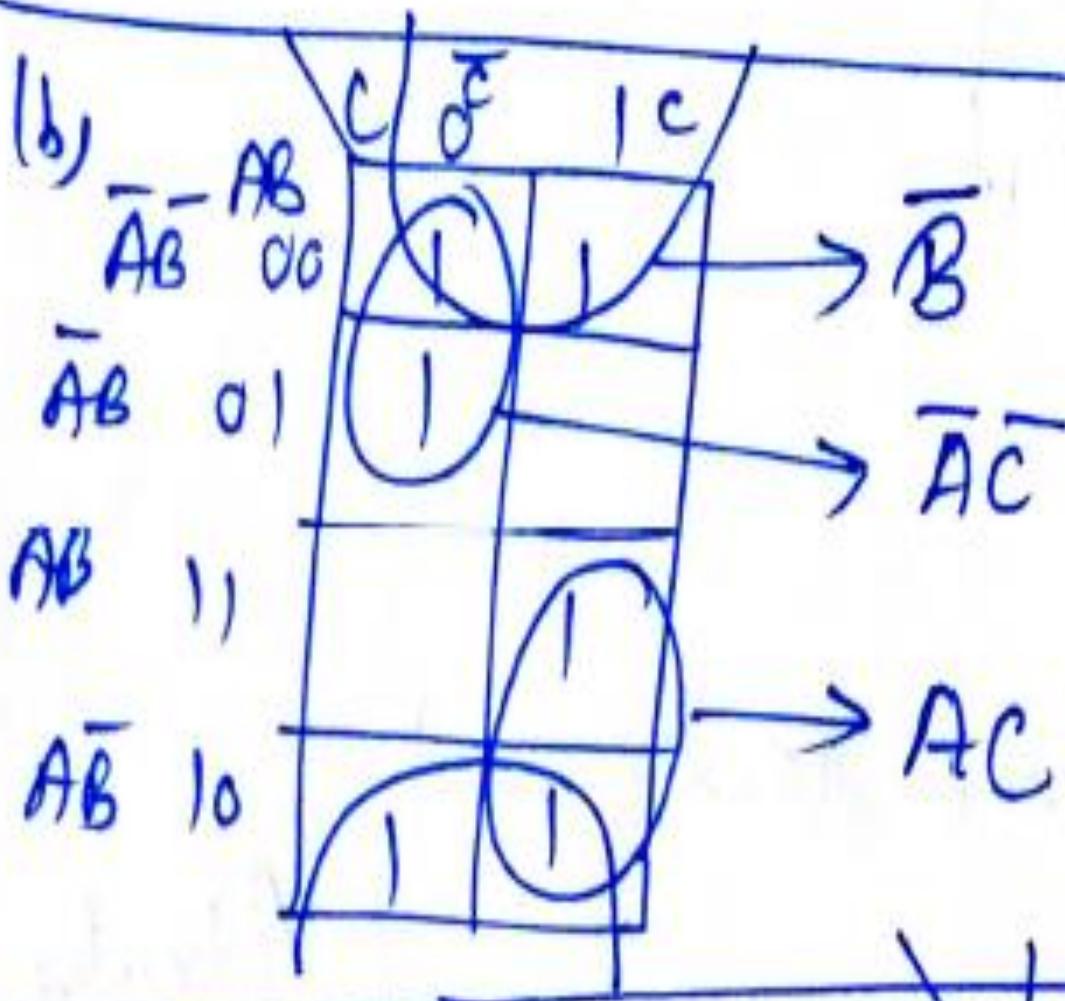
Ans:-

$$AB + BC + \bar{A}\bar{B}\bar{C}$$

Question



Solution



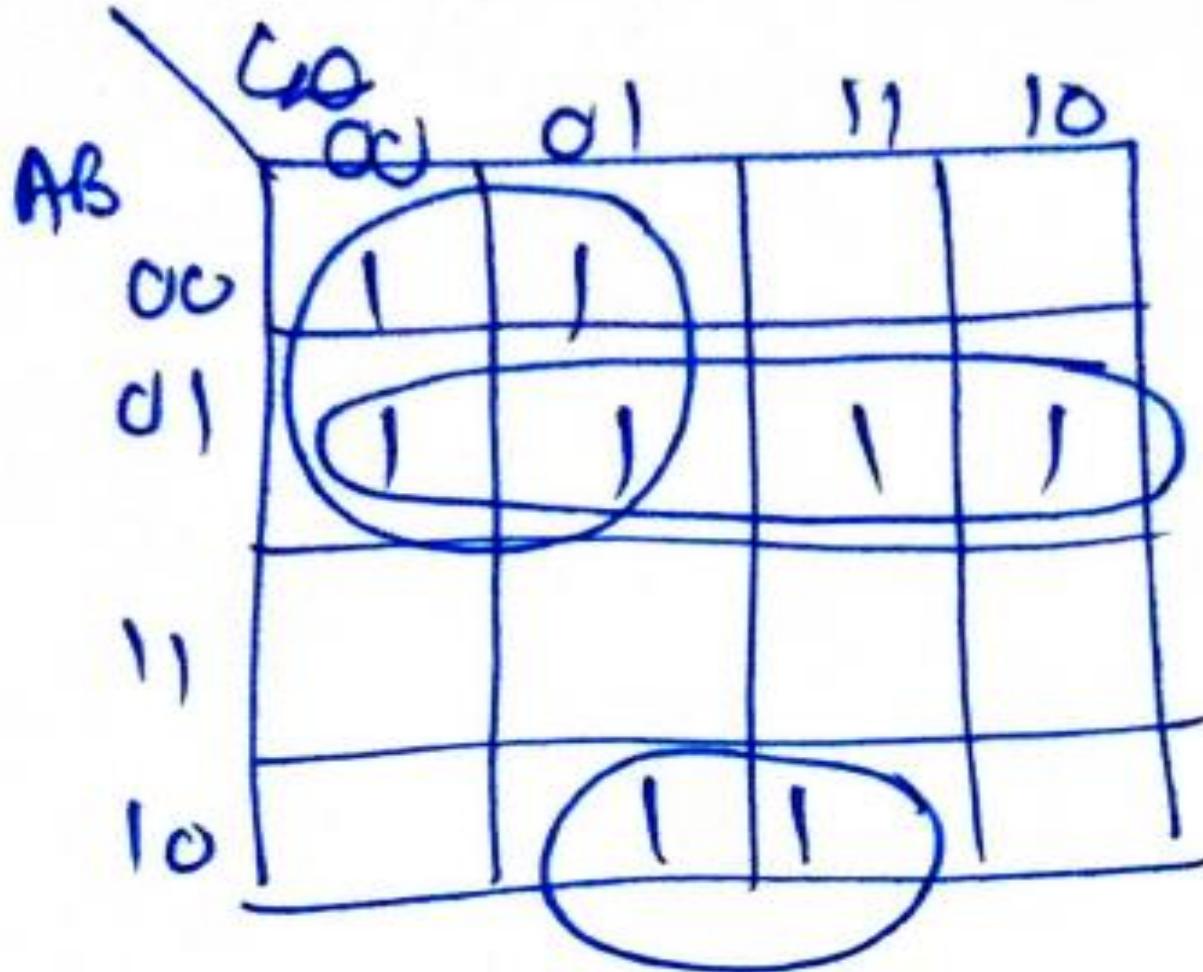
Ans: $\bar{B} + \bar{A}\bar{C} + AC$

Follow this logic

1. Check left-for common variable
2. Check top for common variable
3. Done

Questions

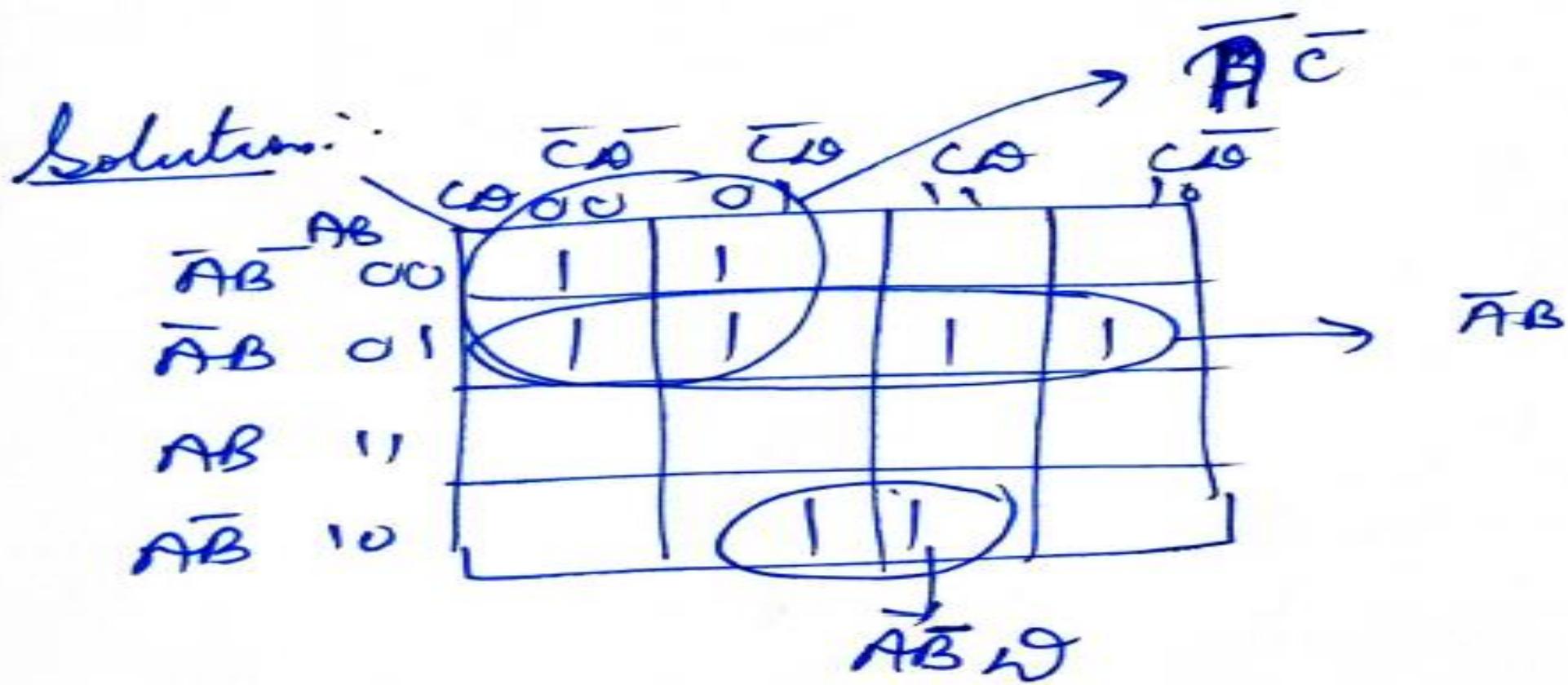
③



Follow this logic

1. Check left-for common variable
2. Check top for common variable
3. Done

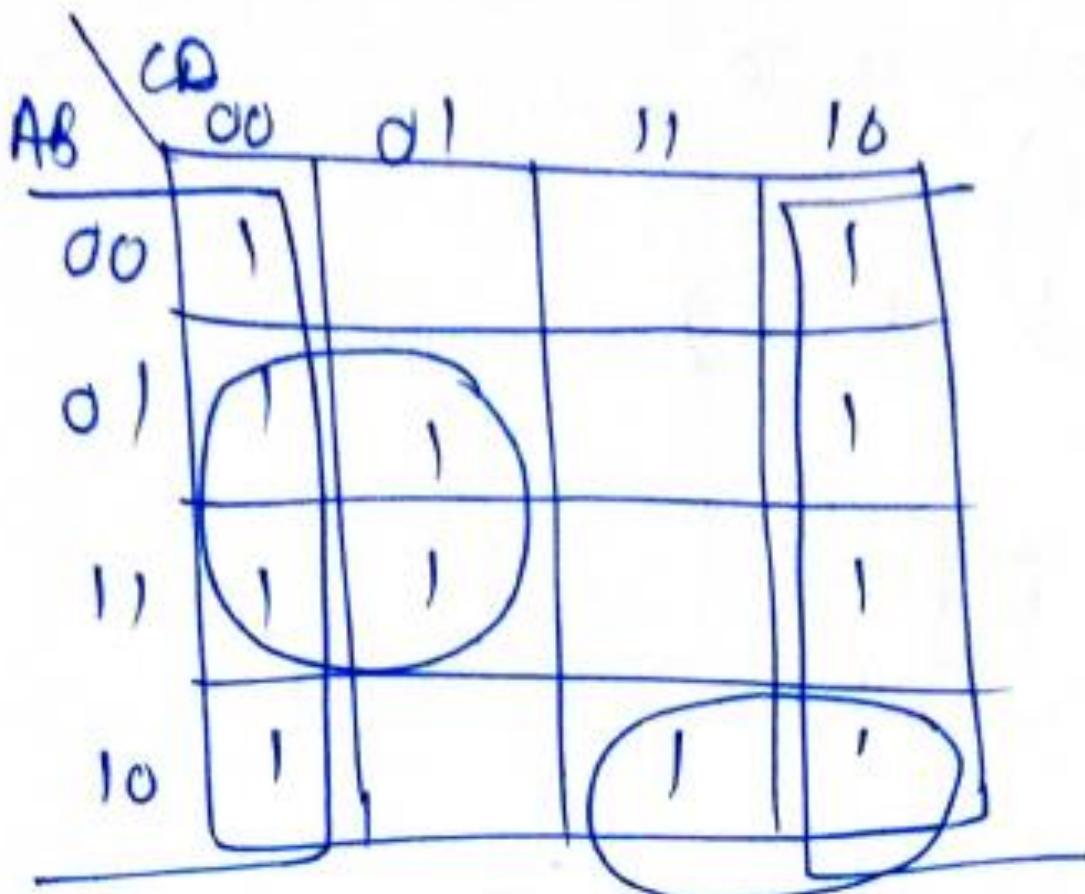
Solution



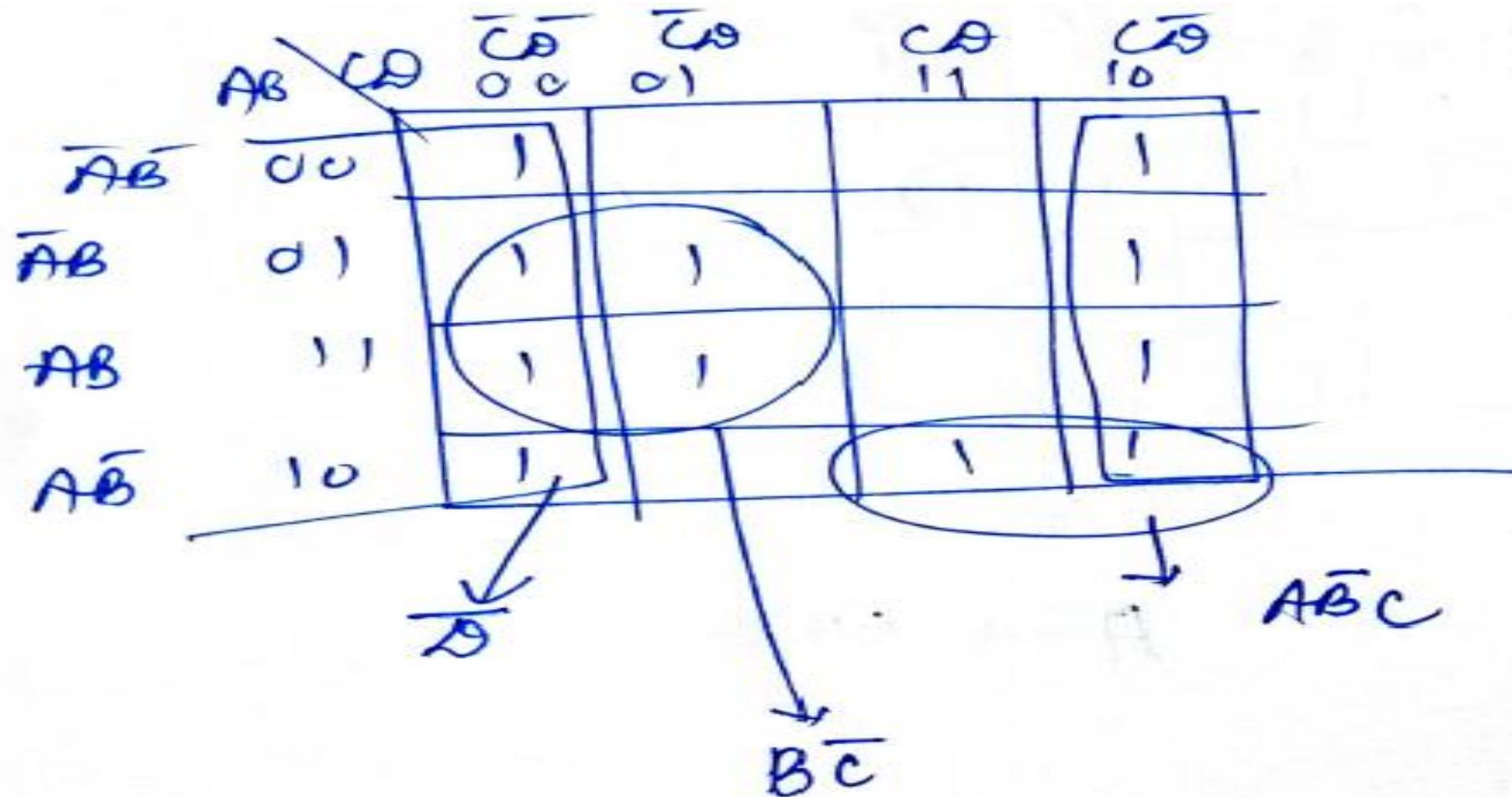
Ans: $\bar{A}\bar{B} + \bar{A}C + \bar{B}C'$

Questions

Q.



Solution



Ans:-

$$\bar{D} + B\bar{C} + \bar{A}\bar{B}C$$

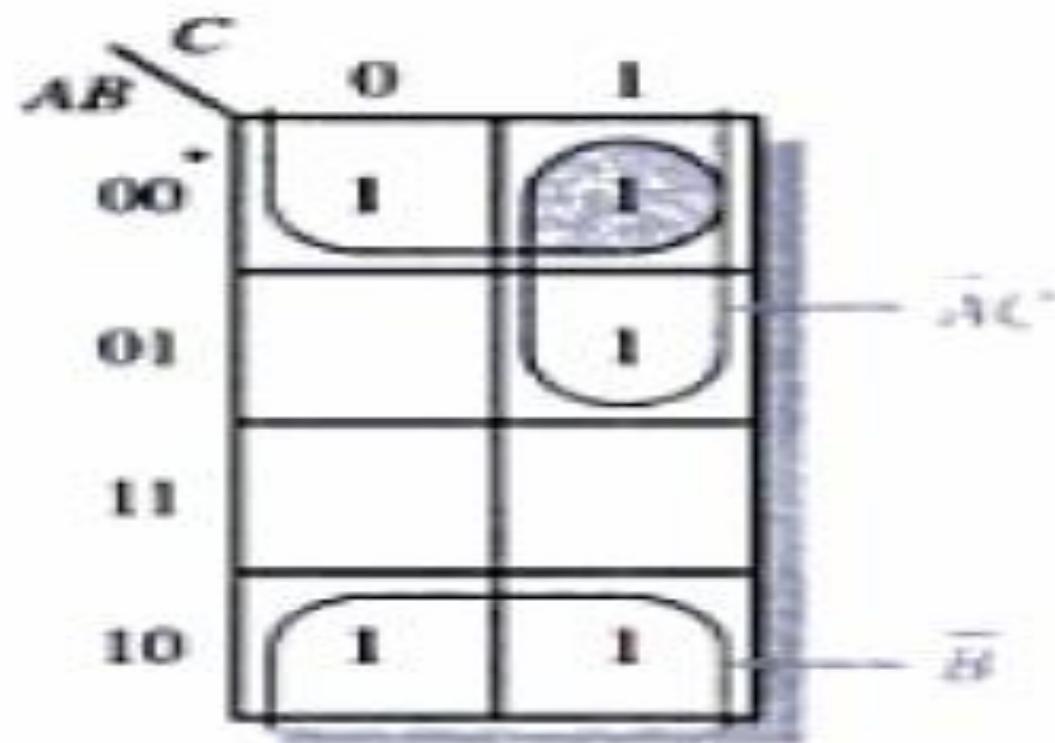
Use a Karnaugh map to minimize the following standard SOP expression:

$$A\bar{B}C + \bar{A}BC + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$$

Solu

The binary values of the expression are

$$101 + 011 + \overset{001}{011} + 000 + 100$$



Octet Conditions

①

$\bar{A}\bar{B}$	AB	$\bar{C}D$	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	$C\bar{D}$
$\bar{A}\bar{B}$	00	0	0	0	0	0
$\bar{A}B$	01	1	1	1	1	1
$A\bar{B}$	11	1	1	1	1	1
$A\bar{B}$	10	0	0	0	0	0

Ans - B

$\bar{A}\bar{B}$	AB	$\bar{C}D$	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	$C\bar{D}$
$\bar{A}\bar{B}$	00	1	1	0	0	0
$\bar{A}B$	01	1	1	0	0	0
AB	11	1	1	0	0	0
$A\bar{B}$	10	1	1	0	0	0

Ans - C

Questions

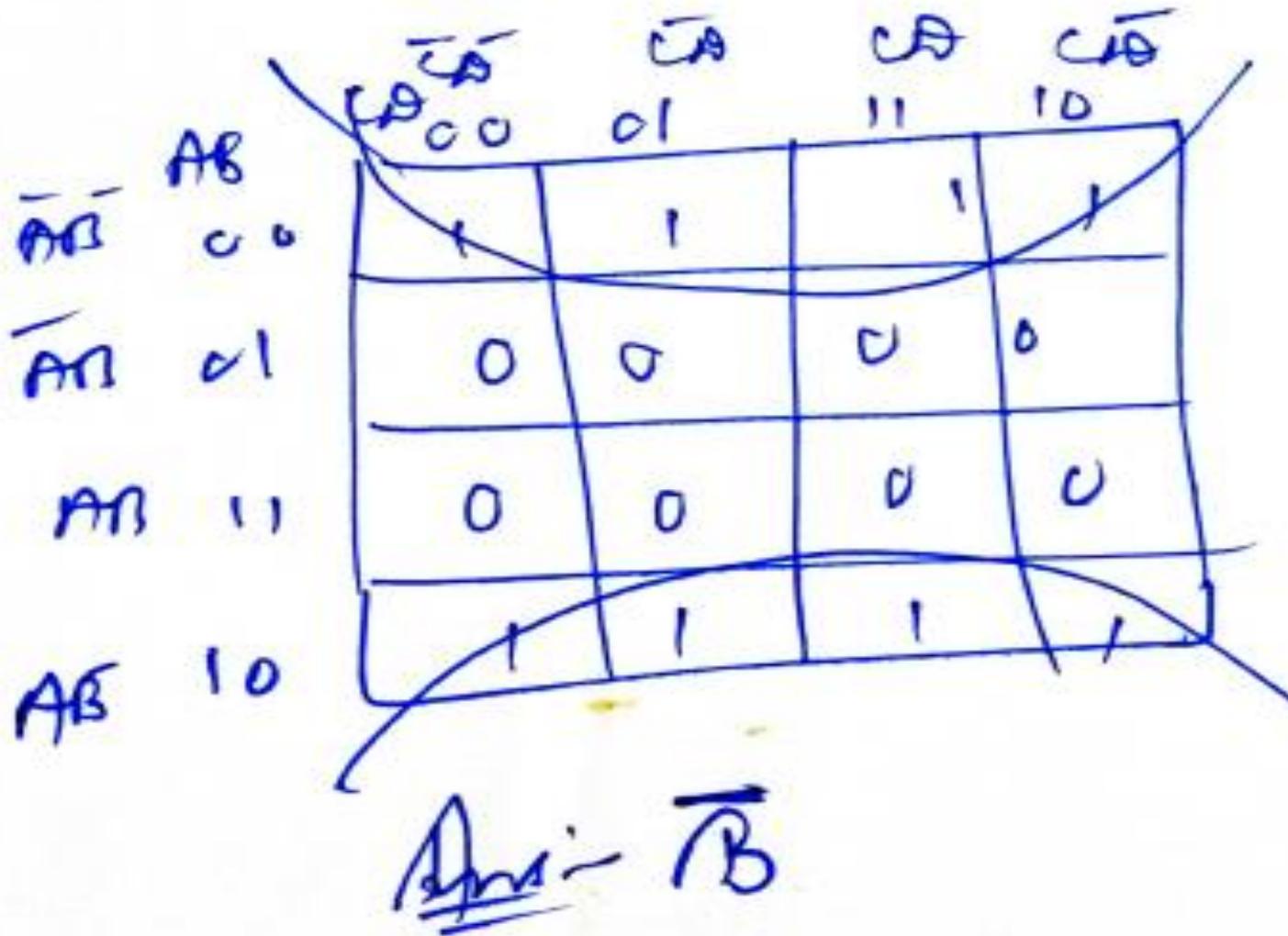
①

AB	CD	00	01	11	10
00	1	1	1	1	
01	0	0	0	0	
11		0	0	0	0
10		1	1	1	1

check yourself also

- ① $C \bar{A}$
② $B \bar{C}$
③ C
None

Solu



Ques

Use a Karnaugh map to minimize the following SOP expression:

$$\overline{BCD} + \overline{ABC}\overline{D} + A\overline{B}\overline{C}\overline{D} + \overline{ABC}\overline{D} + A\overline{B}CD + \overline{ABC}\overline{D} + \overline{ABC}\overline{D} + ABC\overline{D} + A\overline{B}CD$$

\downarrow $\overline{BCD} \rightarrow \text{Not } f_0$
MISSING A

$$(A + \bar{A}) \overline{BCD} \rightarrow A\overline{B}\overline{C}\overline{D} + \overline{ABC}\overline{D}$$

f_0

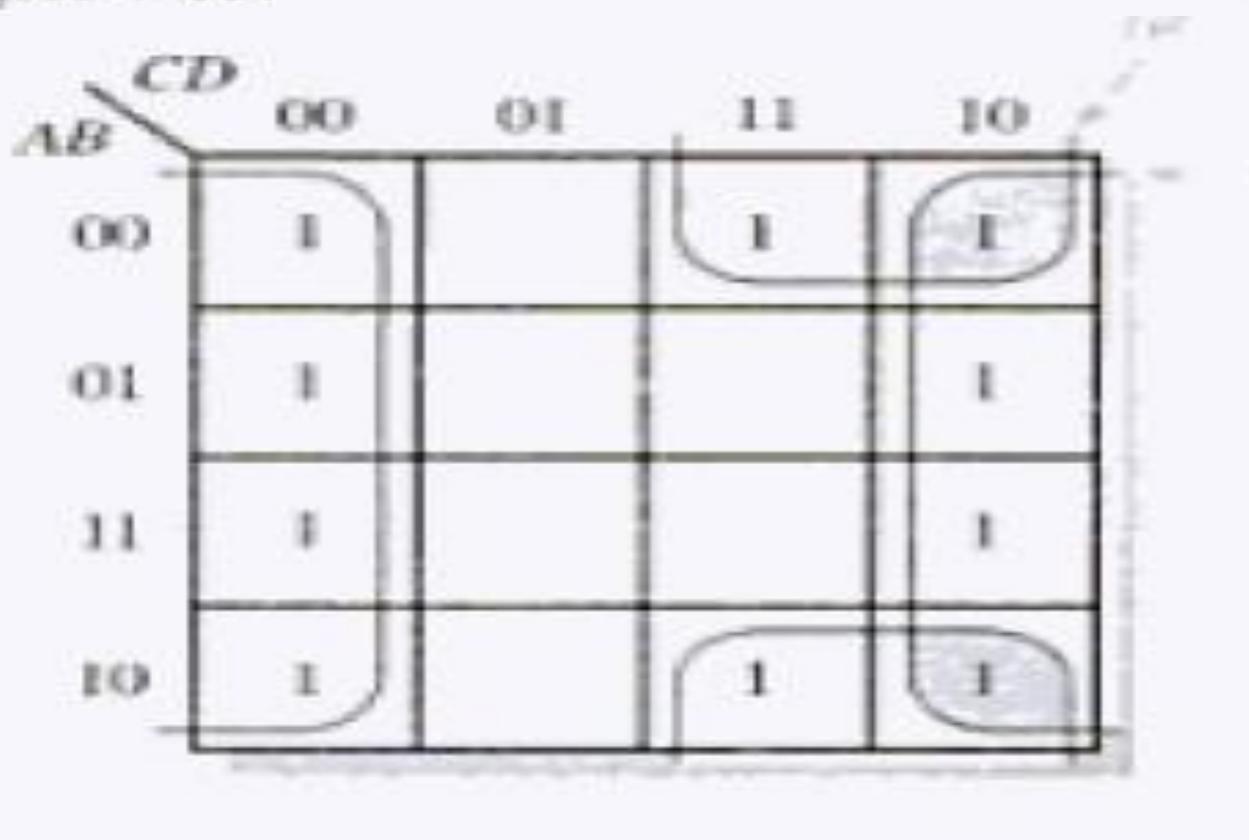
	CD	11	10	01	00
AB	00	01	11	10	00
C	1	1	0	0	1
D	0	1	1	0	0

fill
???

use \rightarrow High. 'Kmap'
Part \rightarrow Answer in
HPU Logic

Solutions

The first term $\bar{B}\bar{C}\bar{D}$ must be expanded into $A\bar{B}CD$ and $\bar{A}\bar{B}CD$ to get the standard SOP expression, which is then mapped; and the cells are grouped as shown in Figure 4–33.

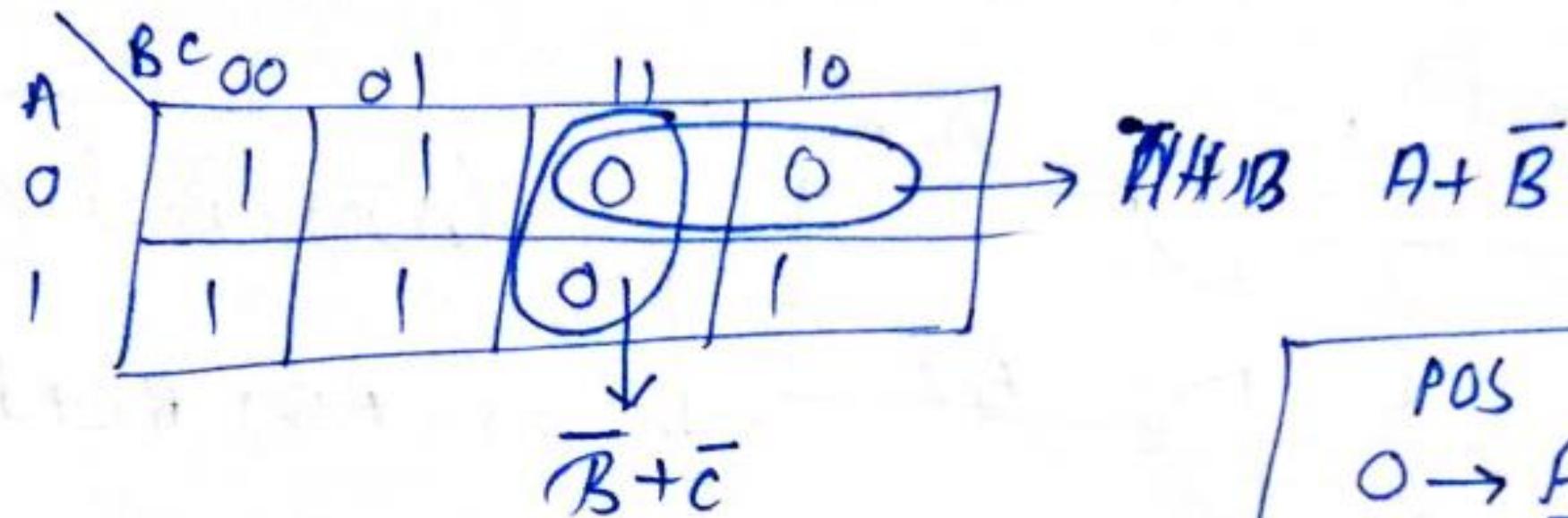


$$\bar{D} + \bar{B}C$$

①

Simplification of Standard POS form using Kmap

- ① Find the expression in POS form for Kmap given

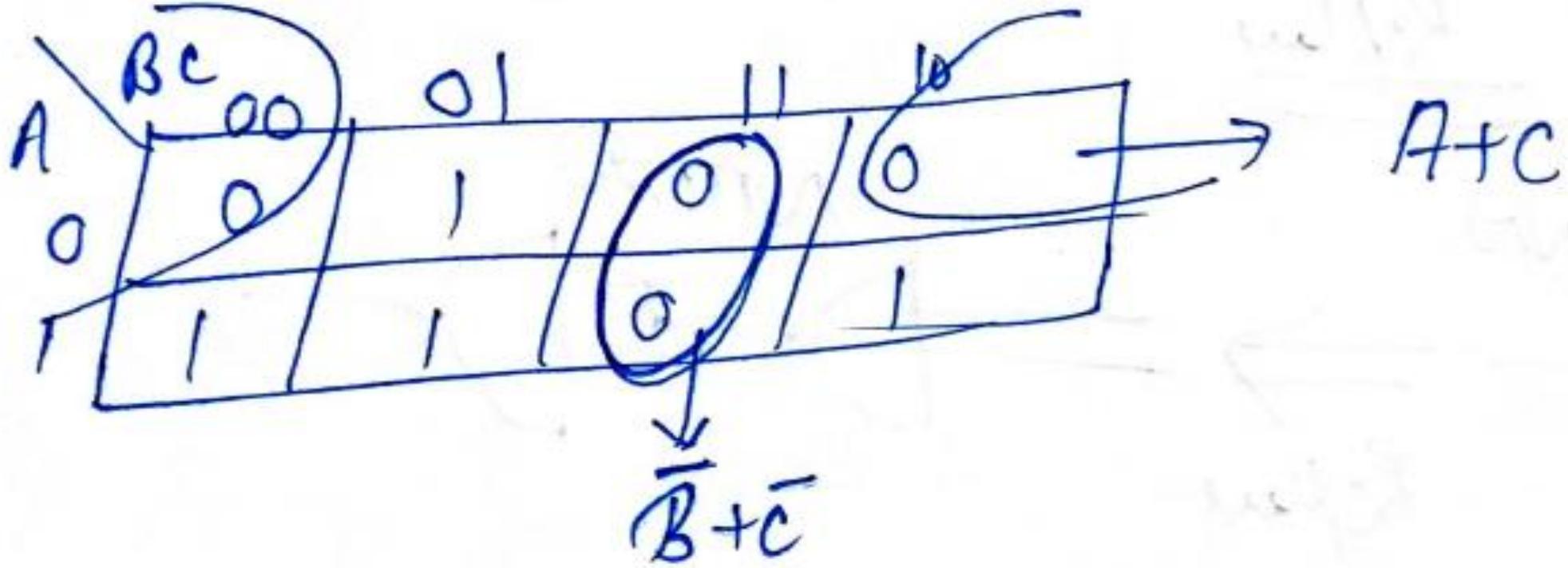


POS	
0 →	A
1 →	\overline{A}

Ans $Y = (A + \overline{B})(\overline{B} + \overline{C})$

②

$$Y = T \bar{J} M (0, 2, 37)$$



$$Y = (A+C)(\bar{B}+\bar{C})$$

Using Kmap realize the following expression using
gates.

$$Y(A, B, C, D) = \Sigma m(1, 3, 4, 5, 7, 9, 11, 13, 15)$$

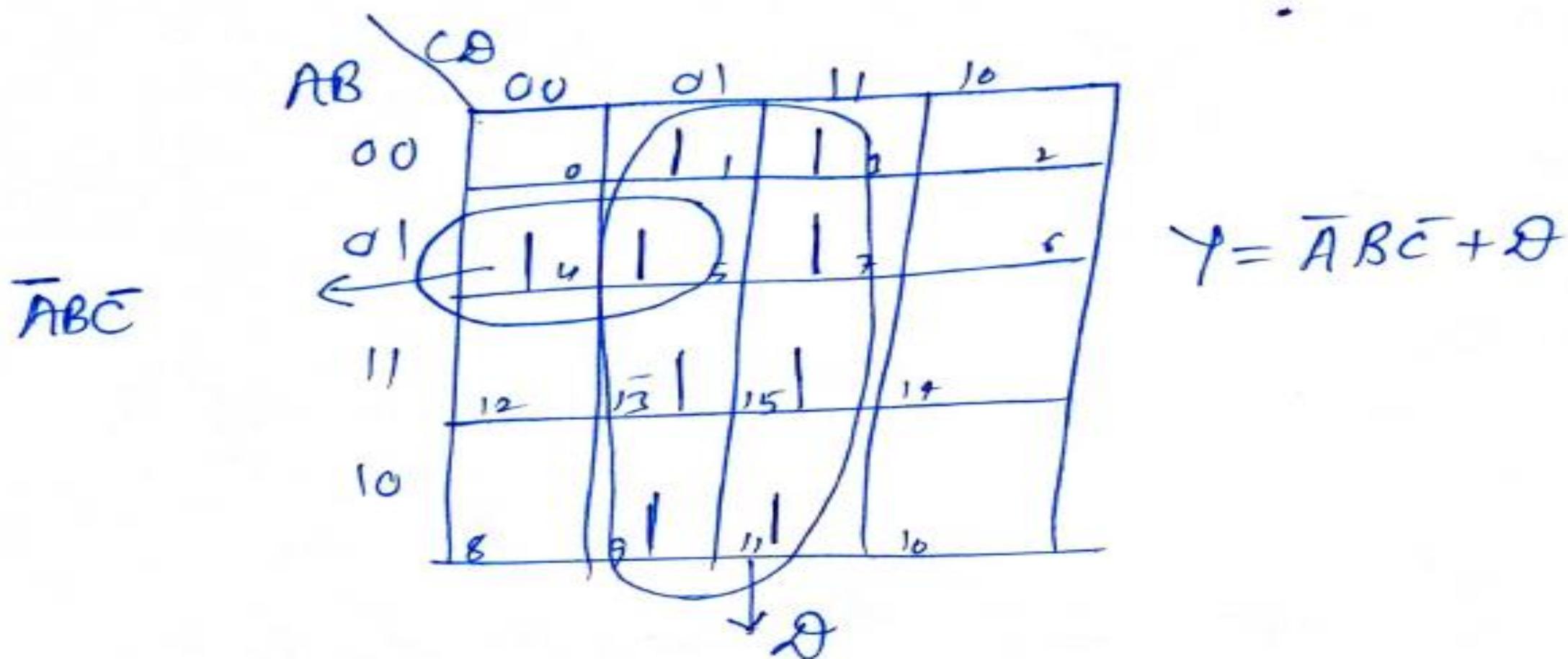
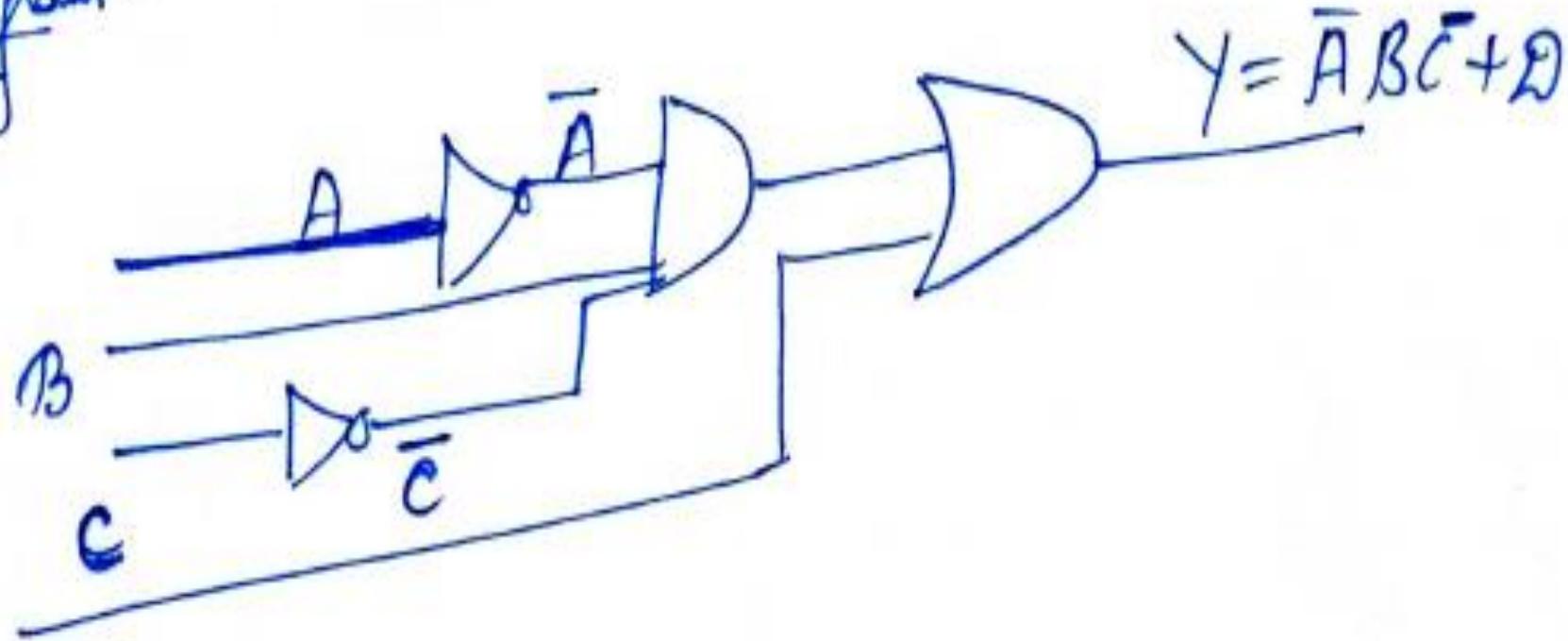


Diagram:



Poll

10. Which of the following expressions is in the sum-of-products form?

- a) $(A + B)(C + D)$
- b) $(A * B)(C * D)$
- c) $A * B * (CD)$
- d) $A * B + C * D$

Solutions

10. Which of the following expressions is in the sum-of-products form?

- a) $(A + B)(C + D)$
- b) $(A * B)(C * D)$
- c) $A * B * (CD)$
- d) $A * B + C * D$

 [View Answer](#)

Answer: d

Explanation: Sum of product means that it is the sum of all product terms. Thus, the number is multiplied first and then it is added: $A * B + C * D$.

~~#~~ Do not care conditions ~~#~~

①

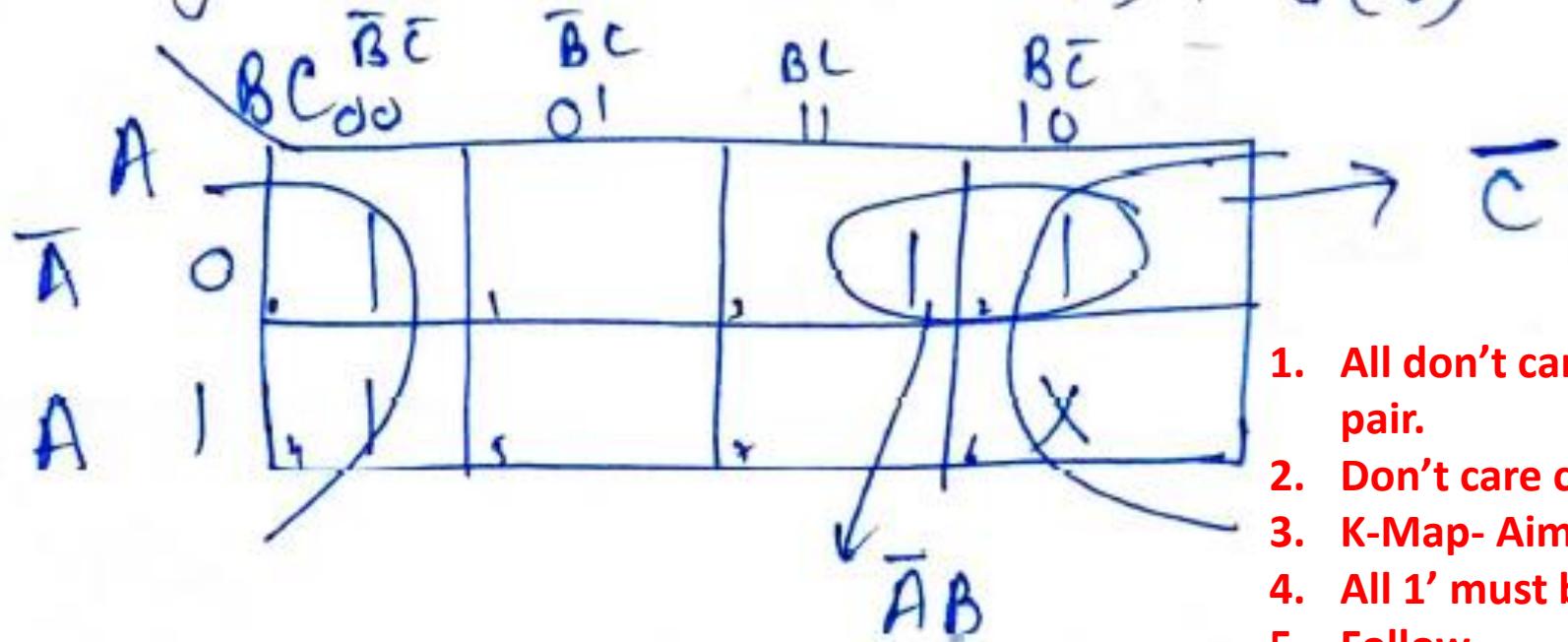
① These are reported as don't care condition because in some cases the output for certain IP combinations has no effect on overall output.

② 'x' are to be adjusted in such a way that the function output will be minimized expressions.

Q:-

Minimize the following function on Kmap

$$y(A, B, C) = \sum_m(0, 2, 3, 4) + d(6)$$



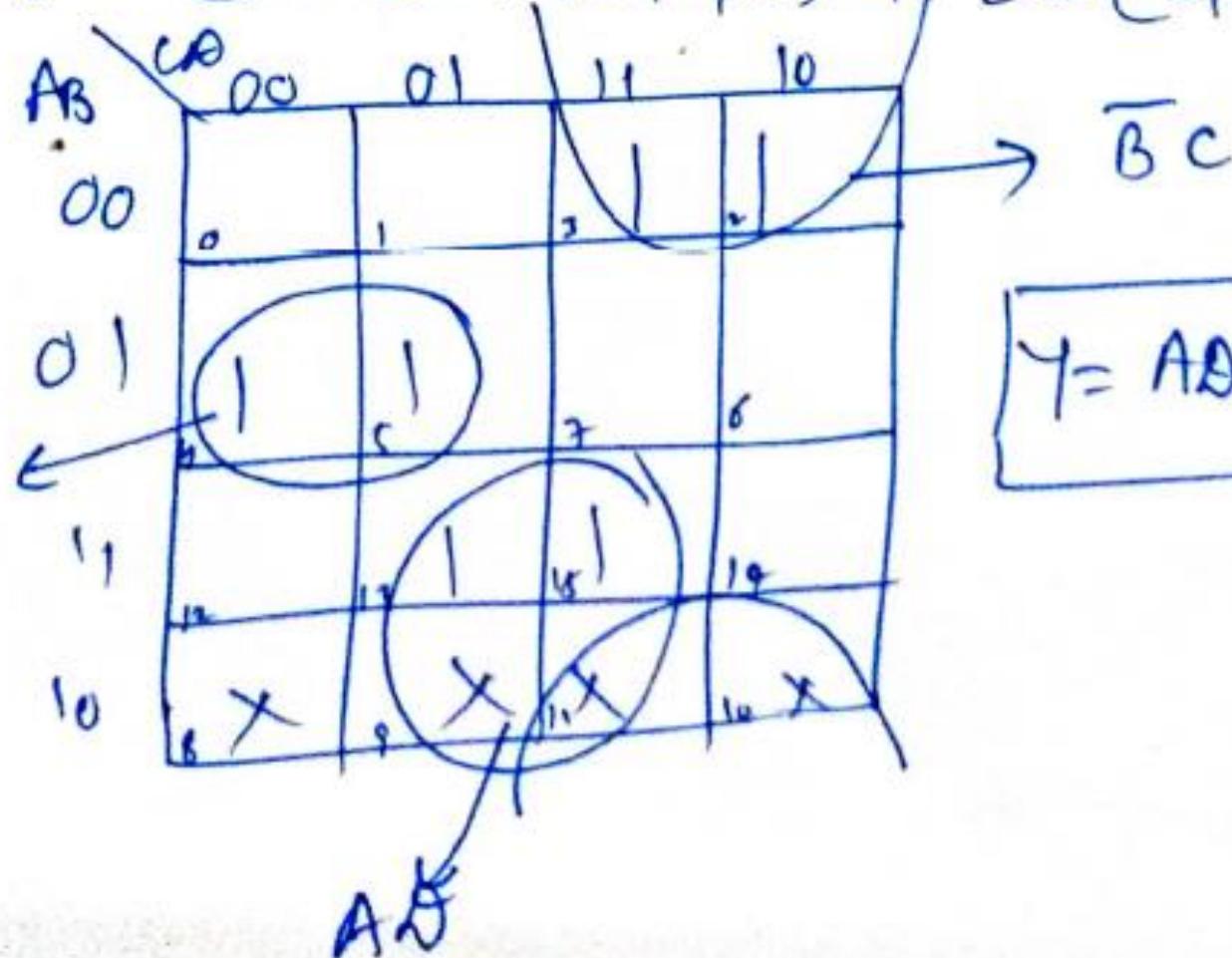
1. All don't care- can not make pair.
2. Don't care can help in pairing
3. K-Map- Aim
4. All 1' must be covered.
5. Follow-
6. 16 then 8 then 4 then 2 then 1

$$Y = \bar{A}B + \bar{C}$$

Q. Minimize the following expression on Kmap?

$$Y(A, B, C, D) = \sum_m (2, 3, 4, 5, 13, 15) + \sum_d (8, 9, 10, 11)$$

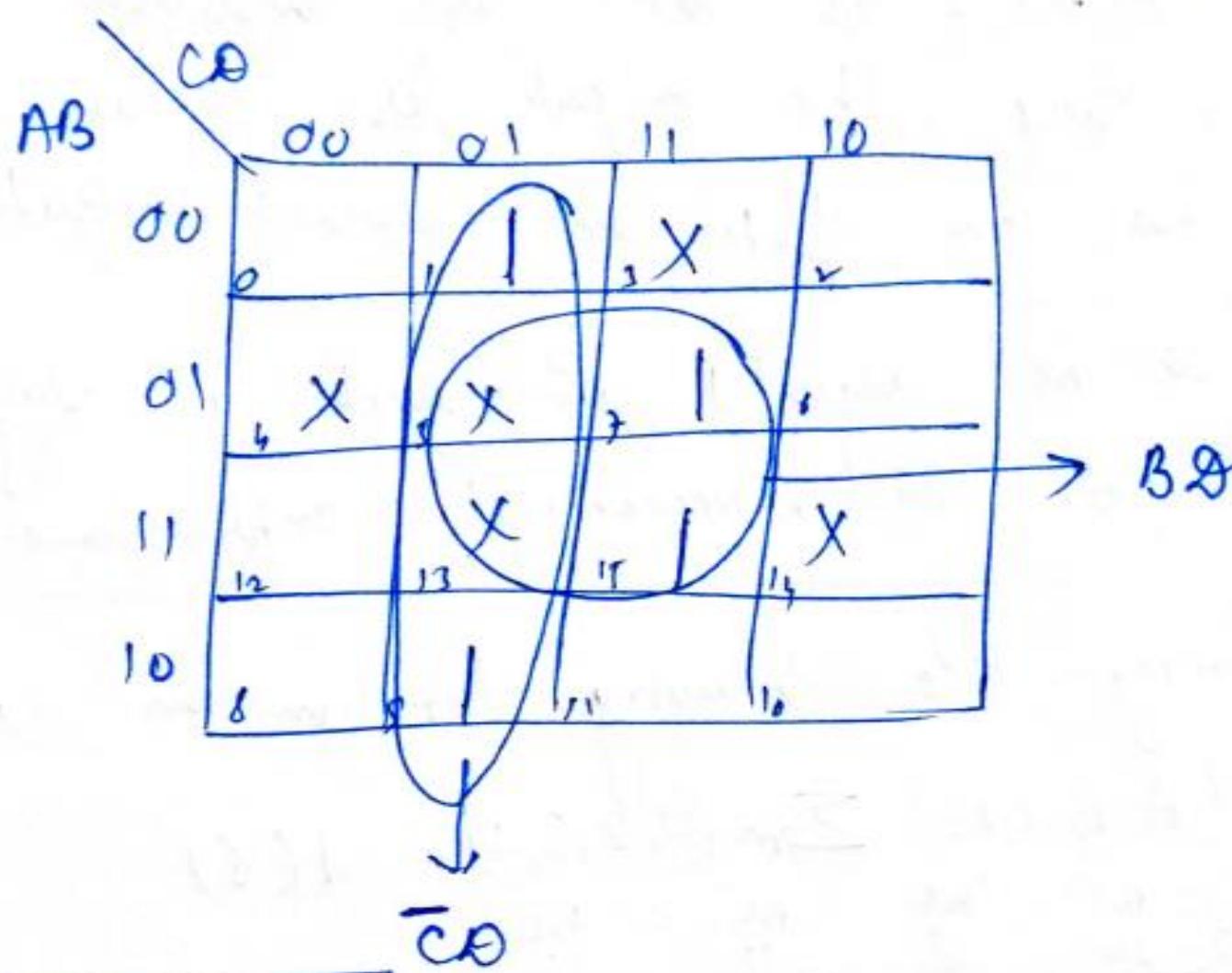
$$\bar{ABC}$$



(2)

$$Y(A, B, C, D) = \sum_m(1, 7, 9, 15) + \sum_d(3, 4, 5, 13, 14)$$

(3)



$$Y = \overline{CD} + BD$$

Poll

12. Which of the following expressions is in the product-of-sums form?

- a) $(A + B)(C + D)$
- b) $(AB)(CD)$
- c) $AB(CD)$
- d) $AB + CD$

Solutions

12. Which of the following expressions is in the product-of-sums form?

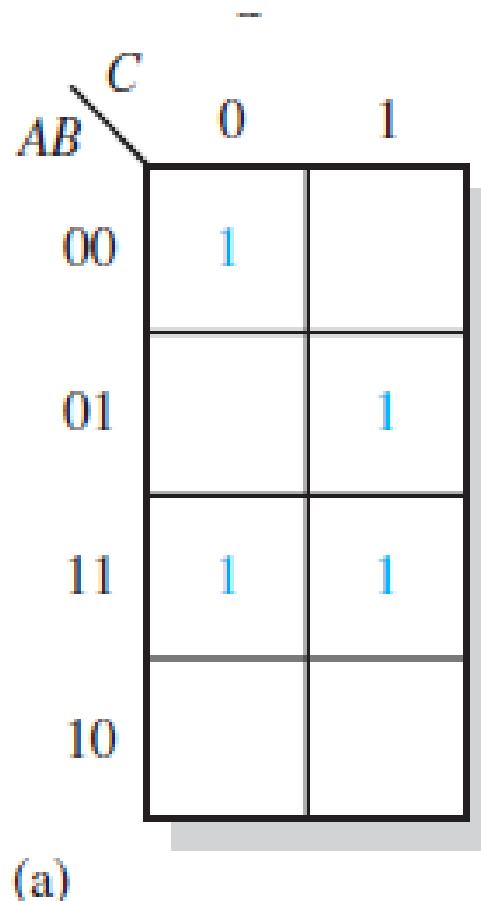
- a) $(A + B)(C + D)$
- b) $(AB)(CD)$
- c) $AB(CD)$
- d) $AB + CD$

 [View Answer](#)

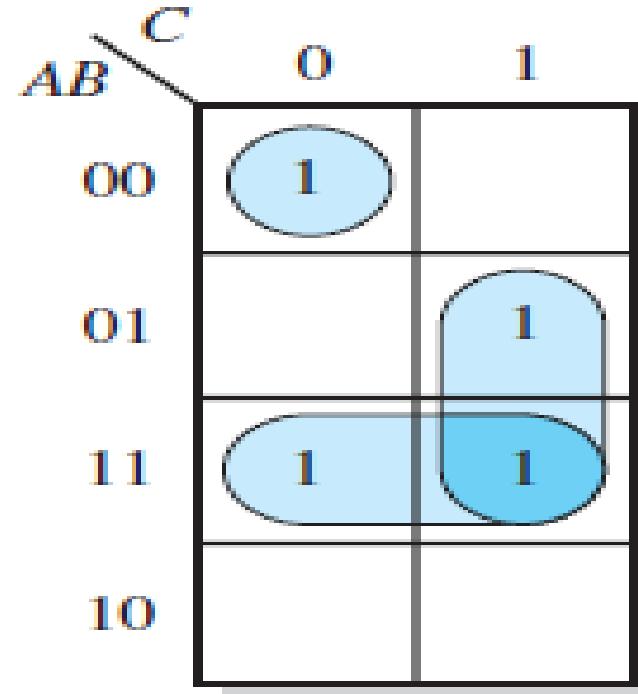
Answer: a

Explanation: $(A + B)(C + D)$ represents the product-of-sums form.

Group the 1s in each of the Karnaugh maps in Figure 4–33.



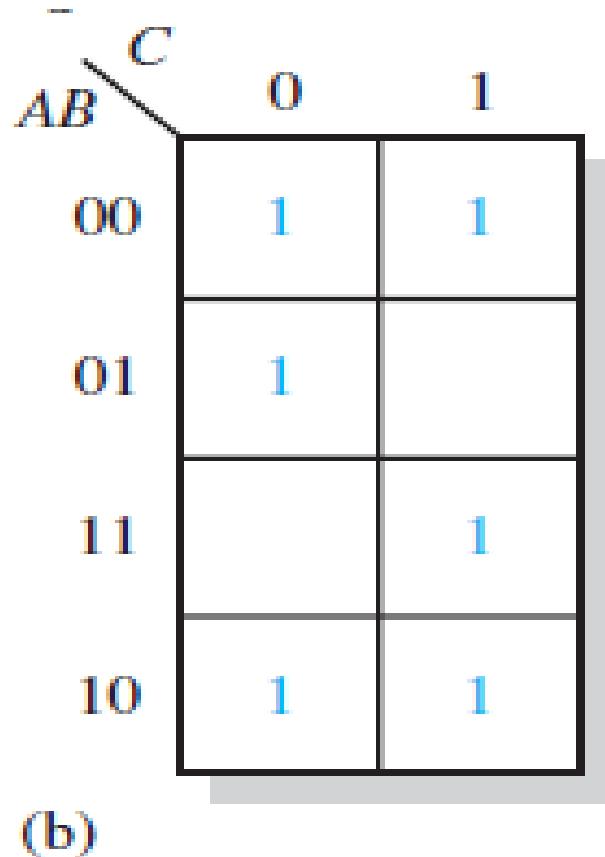
(a)



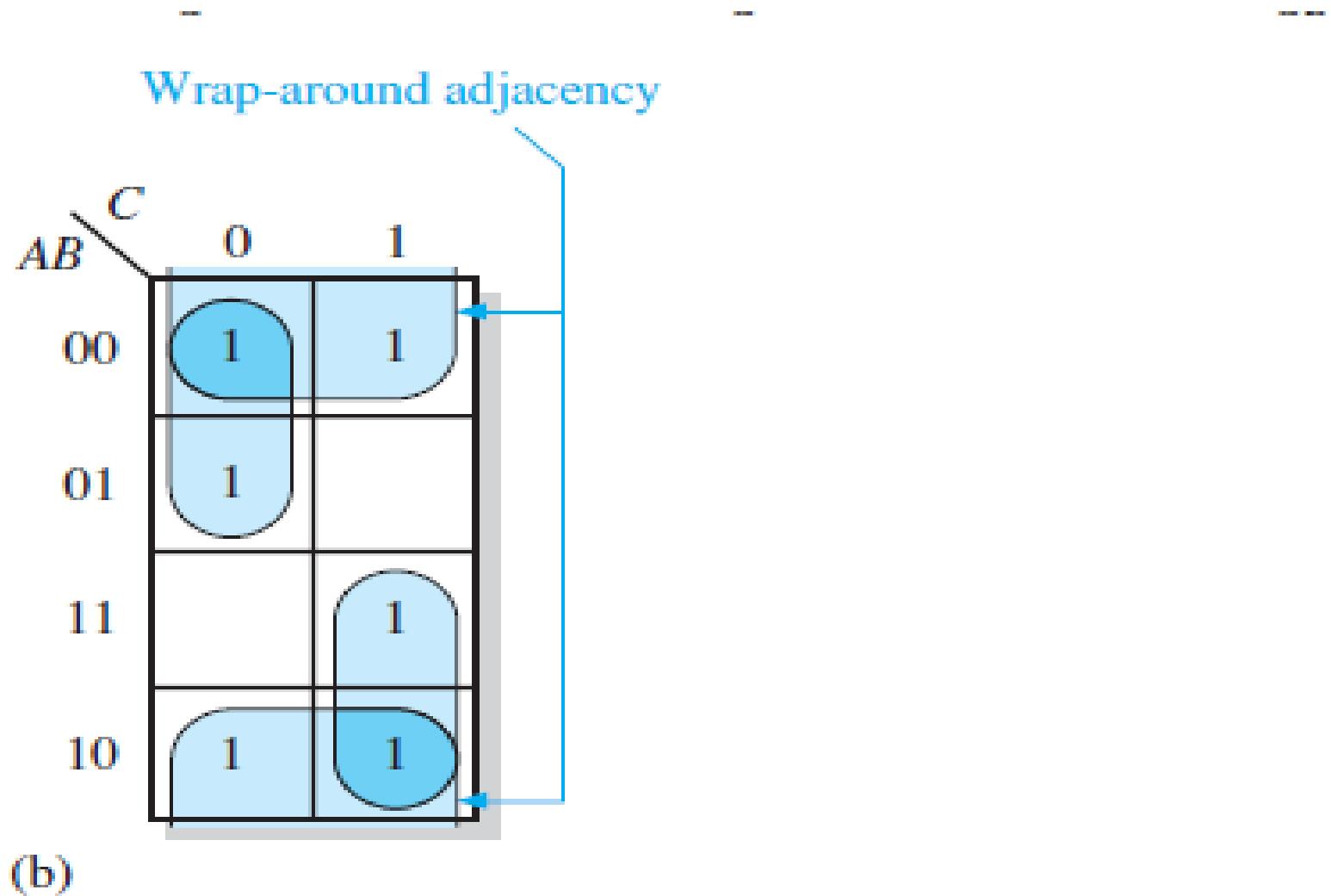
(a)

FIGURE 4–34

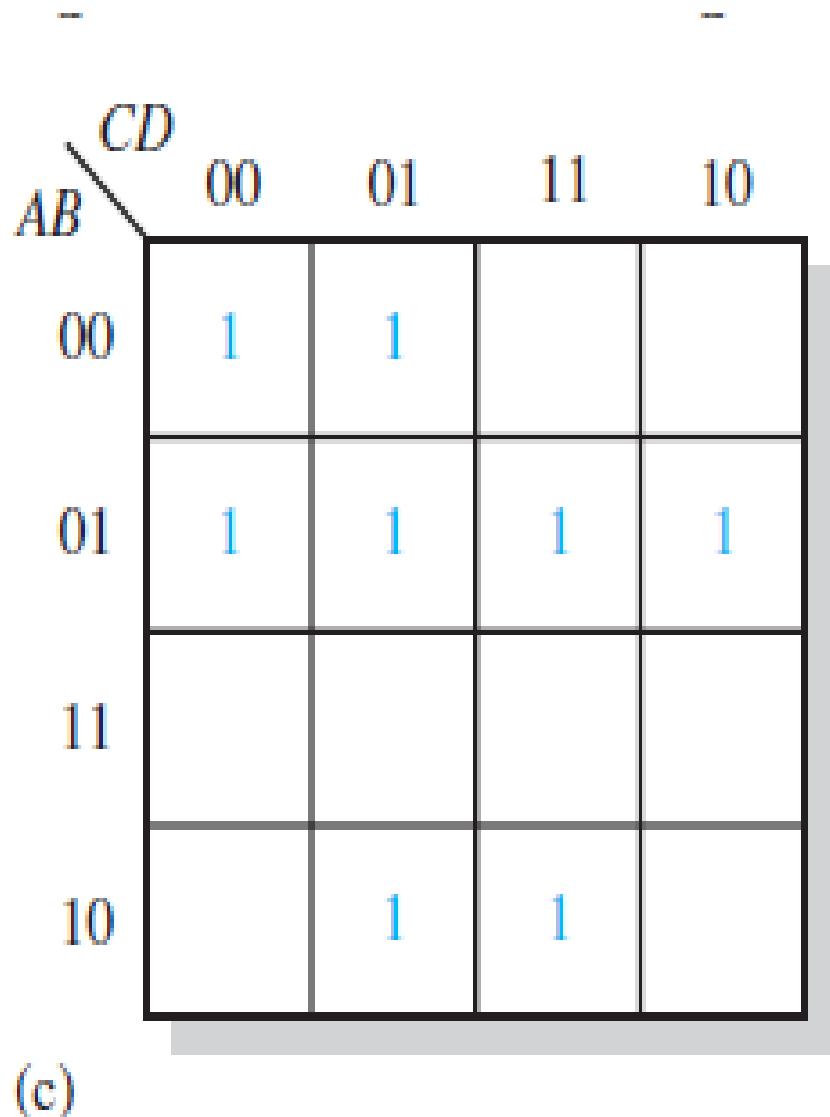
Group the 1s in each of the Karnaugh maps in Figure 4–33.



Group the 1s in each of the Karnaugh maps in Figure 4–33.



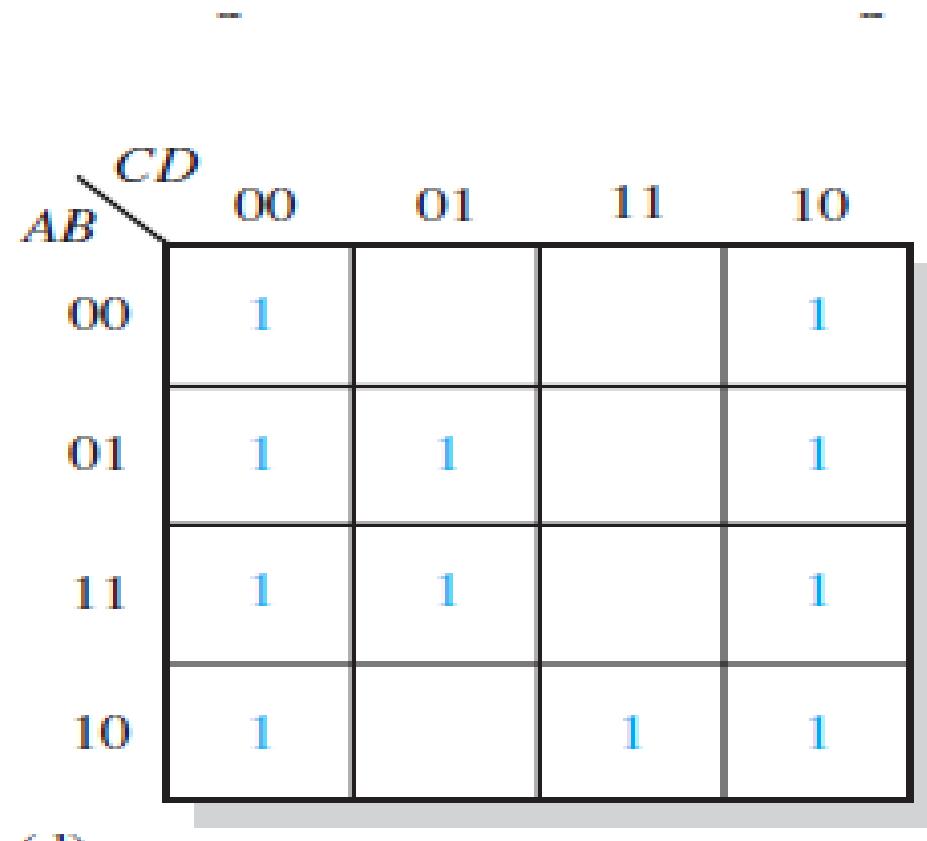
Group the 1s in each of the Karnaugh maps in Figure 4–33.



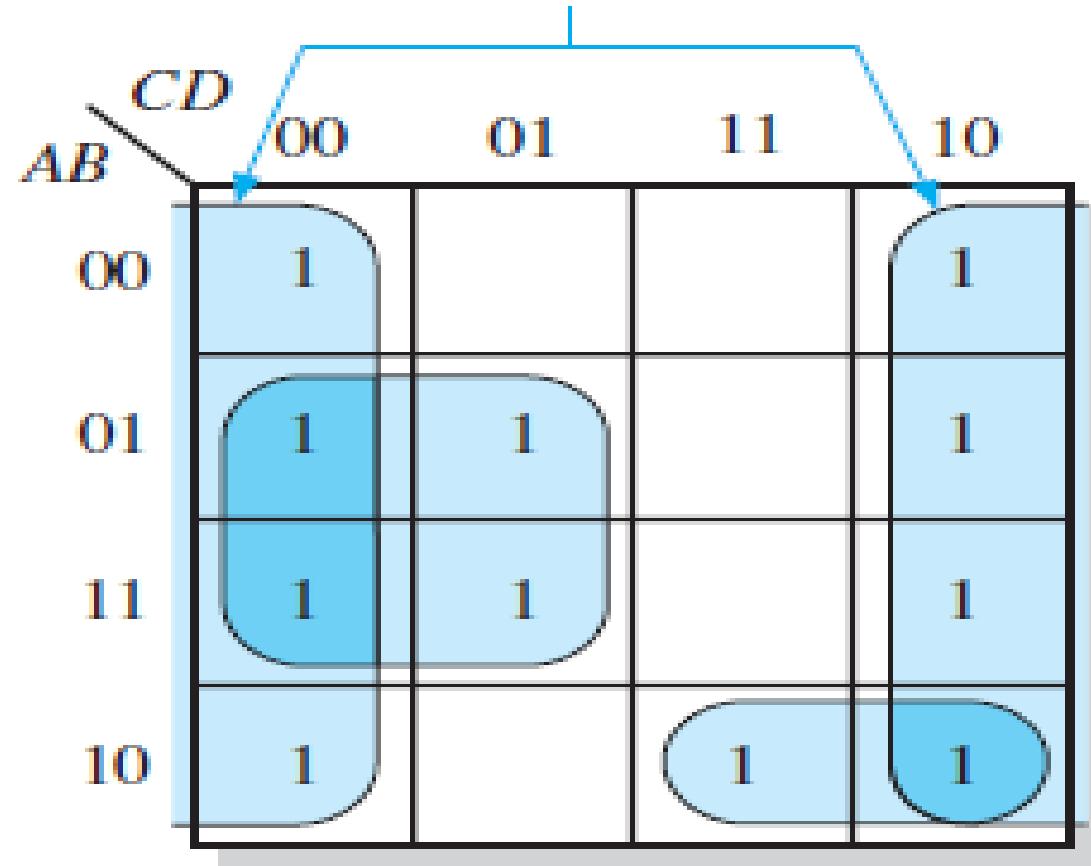
AB	CD	00	01	11	10
00		1	1		
01		1	1	1	1
11					
10			1	1	

(c)

Group the 1s in each of the Karnaugh maps in Figure 4–33.

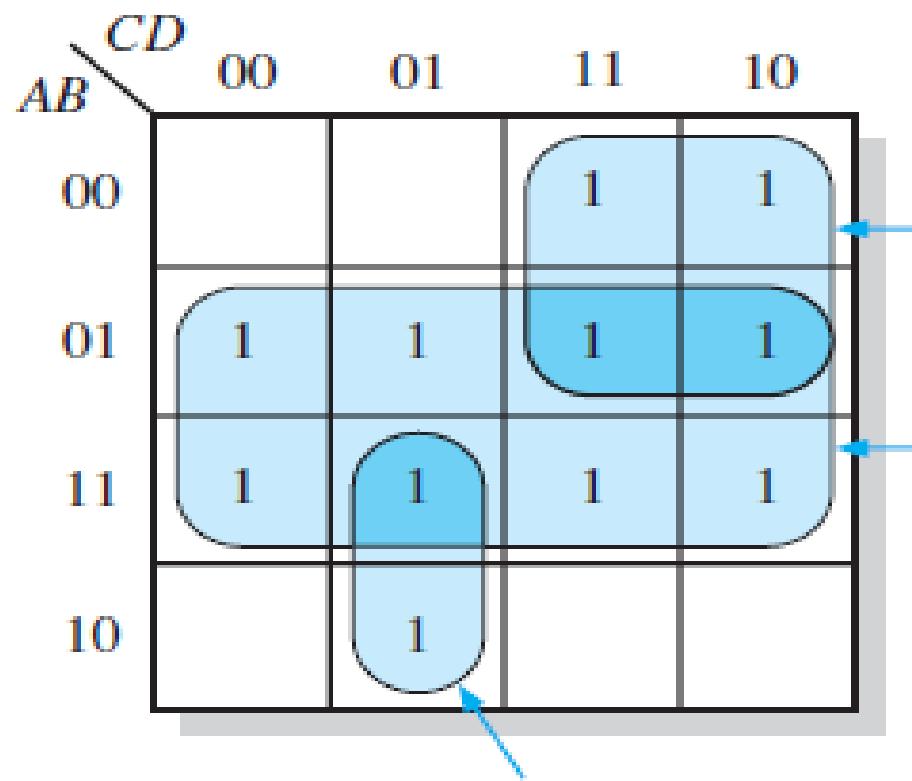


Wrap-around adjacency

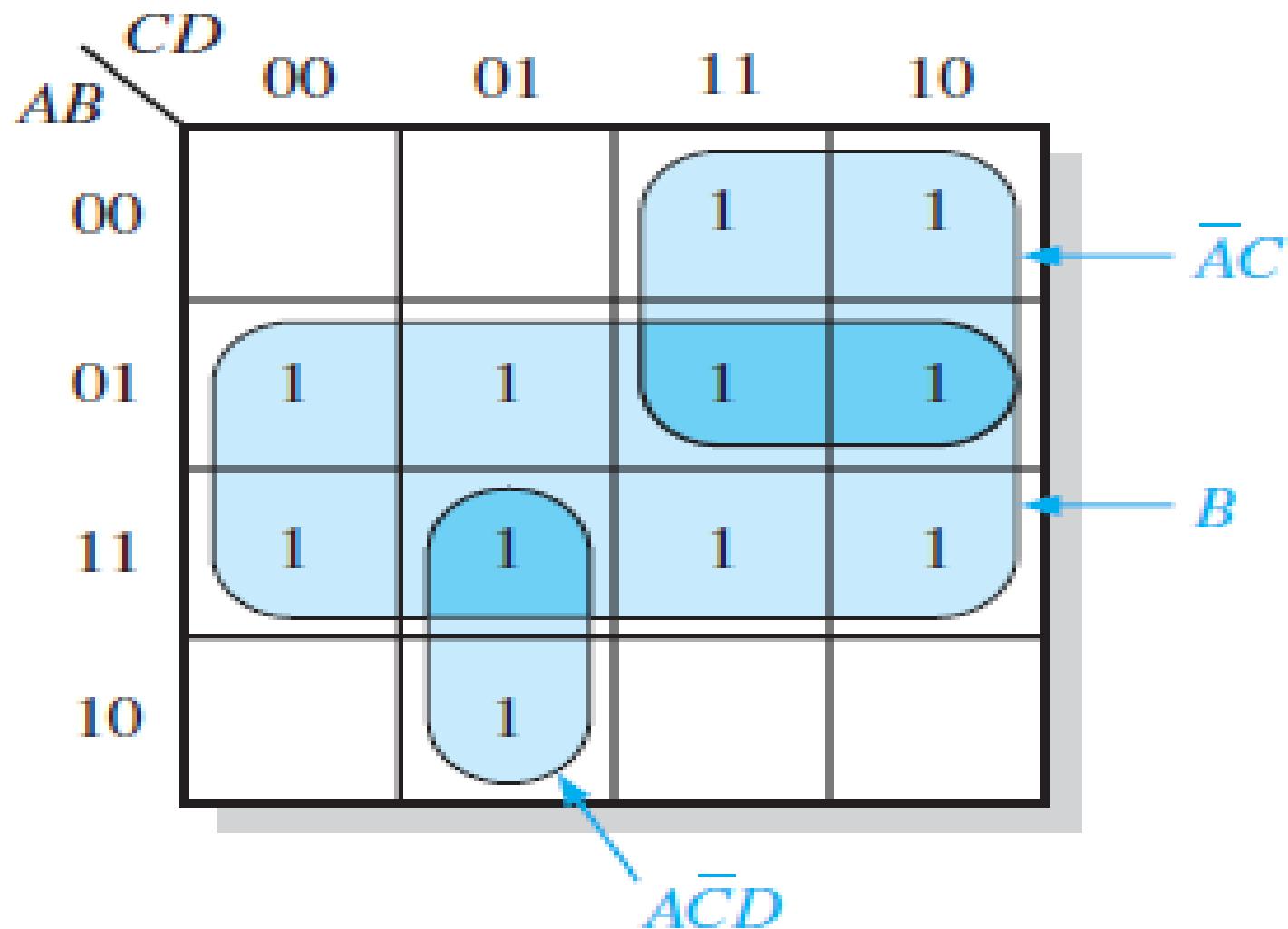


(d)

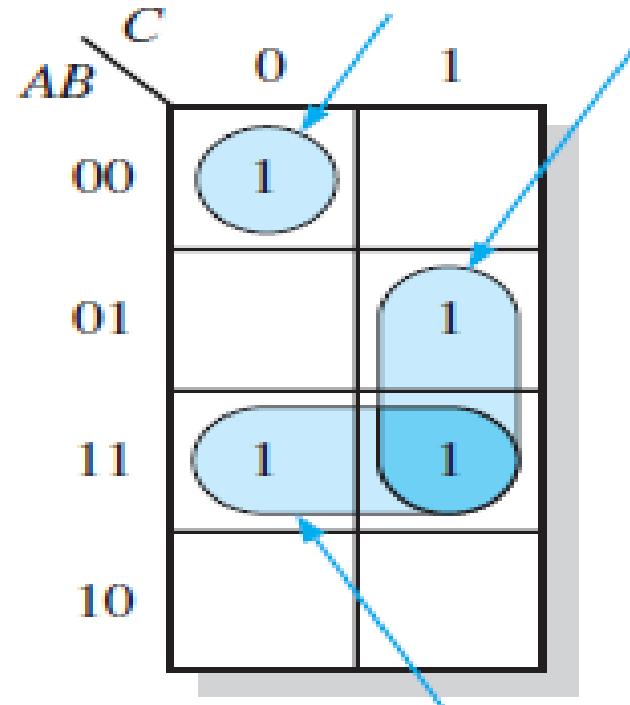
Determine the product terms for the Karnaugh map in Figure 4–35 and write the resulting minimum SOP expression.



Solutions



Determine the product terms for each of the Karnaugh maps in Figure 4–36 and write the resulting minimum SOP expression.



(a)

FIGURE 4–36

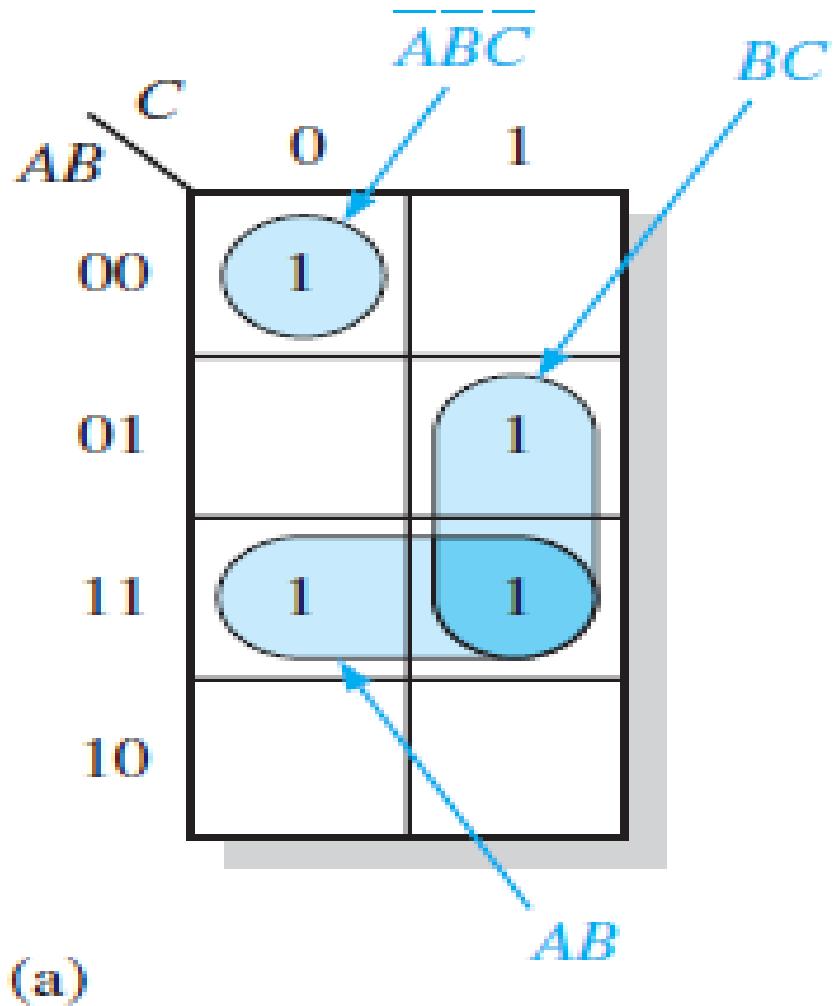
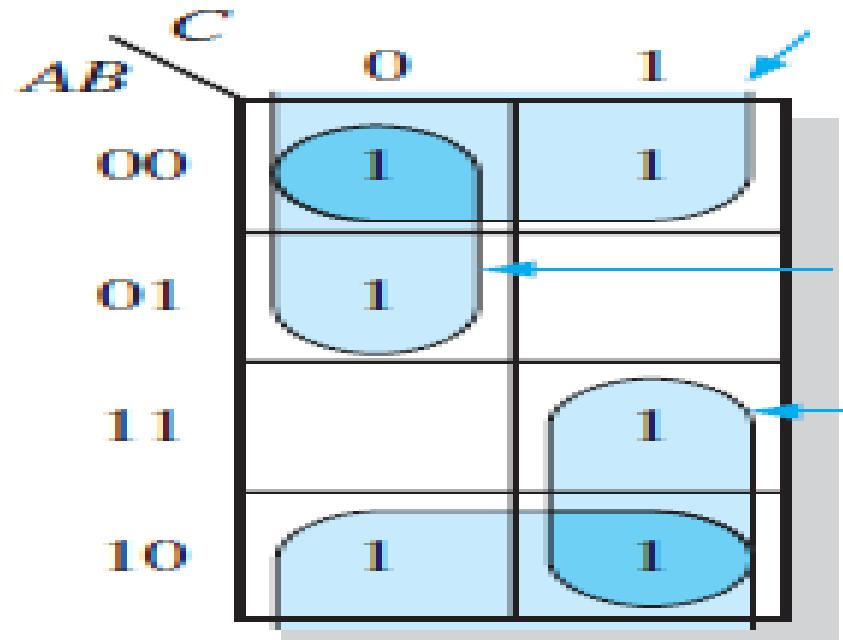


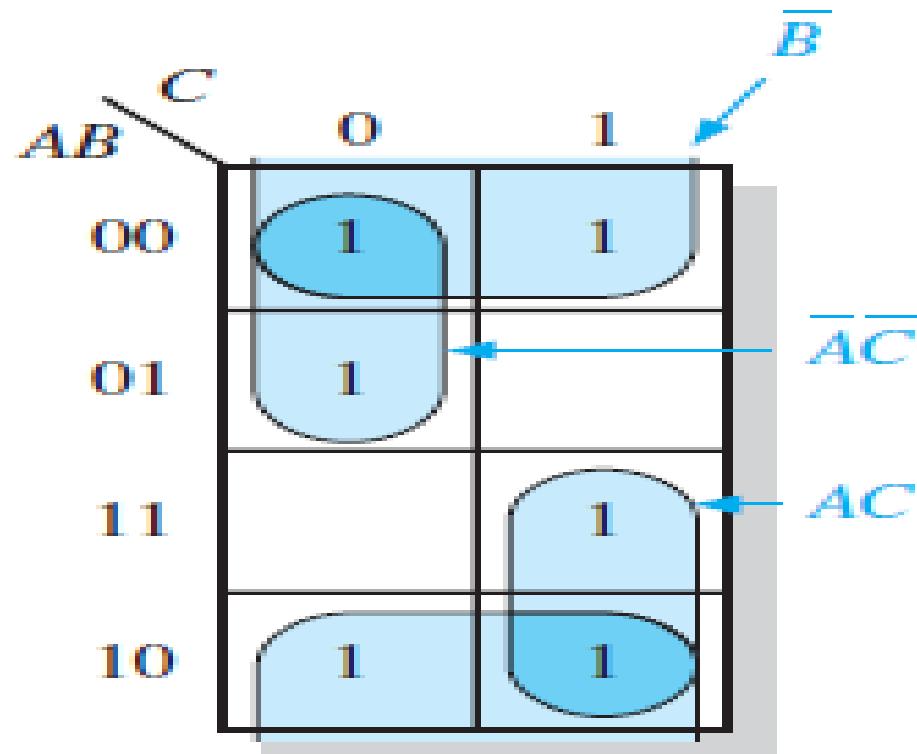
FIGURE 4–36

Questions



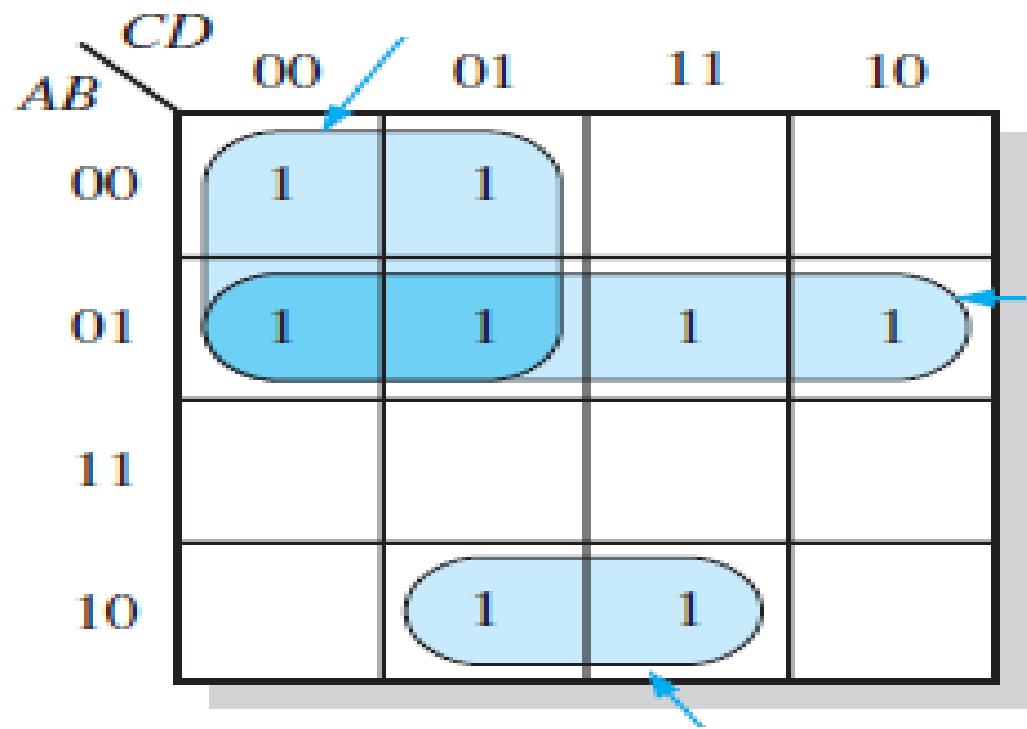
(b)

Solutions

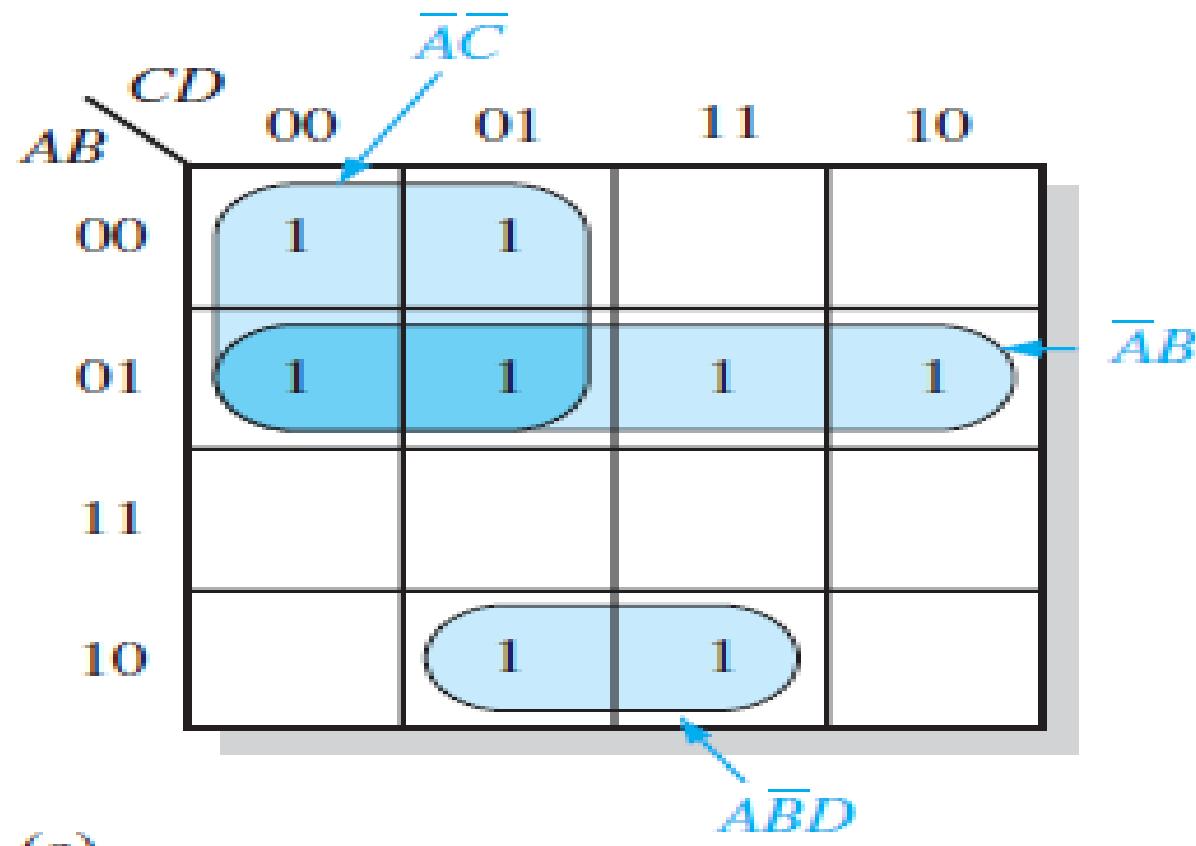


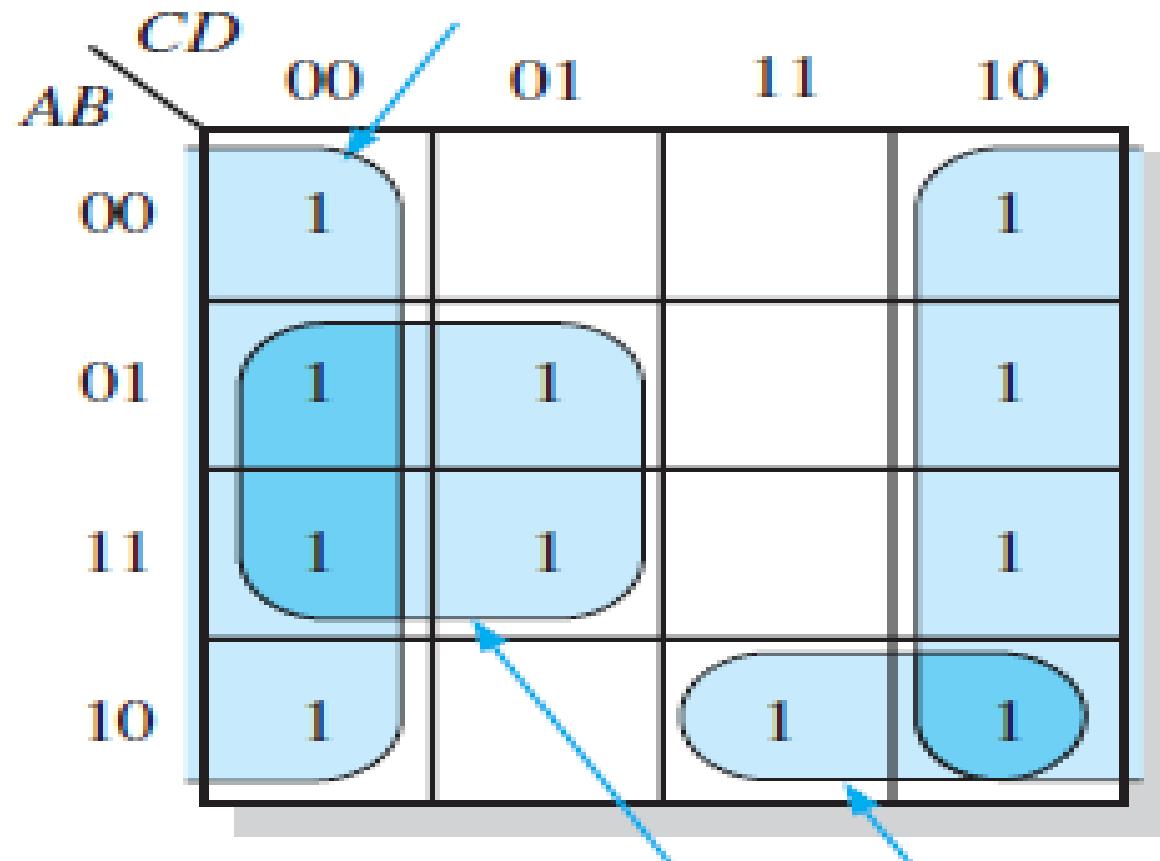
(б)

Questions



(c)





(d)

