

Counter



Date _____

Counters

- ① The digital circuit used for counting pulses is known as Counter. It is a Sequential circuit.
- ② Counters are the important application of flip-flops.
- ③ It is a group of flip-flop with a clock signal applied.

Counter

#

Type of Counter #

②

Aynchronous or ripple counter:
Synchronous counter

①

Aynchronous or ripple counters:-

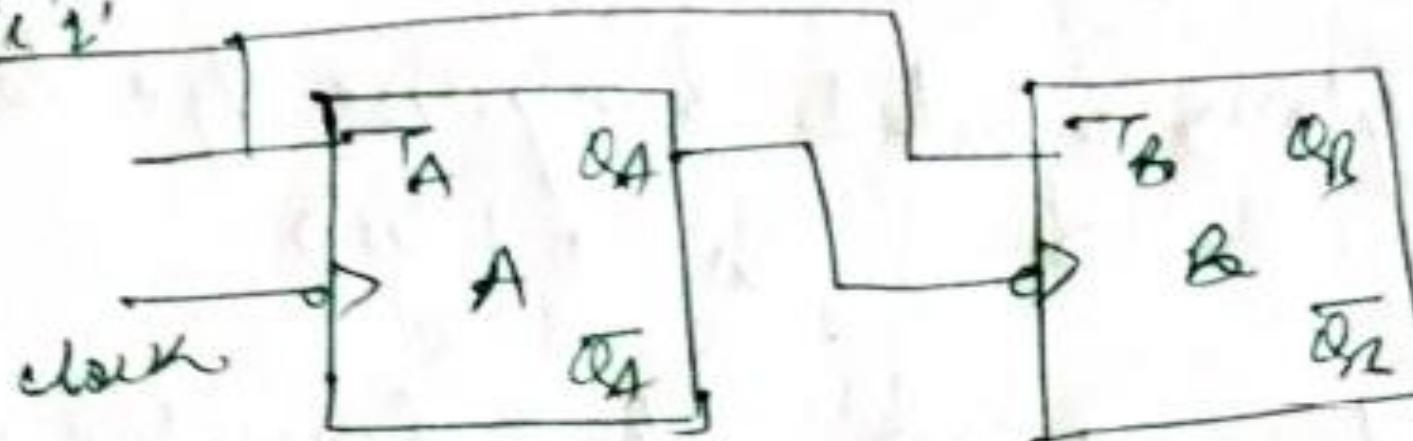
In these counters external clock signal is applied to one flip-flop & then the output of preceding preceding flip flop is connected to clock of next flip flop.

②

Synchronous Counters:- In Synchronous counters all the flip-flops receive external clock pulse simultaneously.

~~#~~ 2 Bit Asynchronous Counter (Ripple Counter) ~~#~~ ①

logic is:



A two bit Synchronous binary counter

- ① In the given fig, the no. of flip-flops are 2.
- ② Thus, the no. of bits will always be equal to no. of flip flop.

- ① In the given fig, the no. of flip-flops are 2
- ② Thus, the no. of bits will always be equal to no. of flip-flop.
- ③ External clock is applied to the clock input of first flip flop & S_A (output) is applied to clock input of next flip-flop.

operations:- ① Initially both flip-flops are in
reset condition

① on first negative edge

① FF-A \rightarrow input 1 \rightarrow Toggle $\rightarrow Q_A$ from 0 to 1

② Q_A is connected as clock input to
FF-B & on is changing from 0 to 1 at
positive edge. So no change in output of $Q_B = 0$

$$\boxed{F_B \text{ } Q_A = 01}$$

②

On 2nd falling edge of clock

i) Q_A , ff-A again toggle \rightarrow input 1 & negative edge clock
 $\longrightarrow Q_A \rightarrow 1 \text{ to } 0$

b) Q_A changes from 1 to 0 \checkmark {negative edge}

c) Hence Q_B changes (toggle) $\Rightarrow Q_B \rightarrow 0 \text{ to } 1$

$$\cancel{Q_B Q_A = 10}$$

On 3rd falling edge of clock

① a, On 3rd neg edge of clock \rightarrow FF-A toggle from 0 to 1
 $Q_A = 1$

b) $Q_A \xrightarrow{0 \rightarrow 1}$ positive edge

c) No change in $Q_B = 1$,

$$\boxed{T Q_B Q_A = 11}$$

On 4th negative clock edge

① ff-A toggle (input 1) & Q_A changes from 1 to 0

② $Q_A \xrightarrow{1 \rightarrow 0}$ negative edge clock $Q_A = 0$

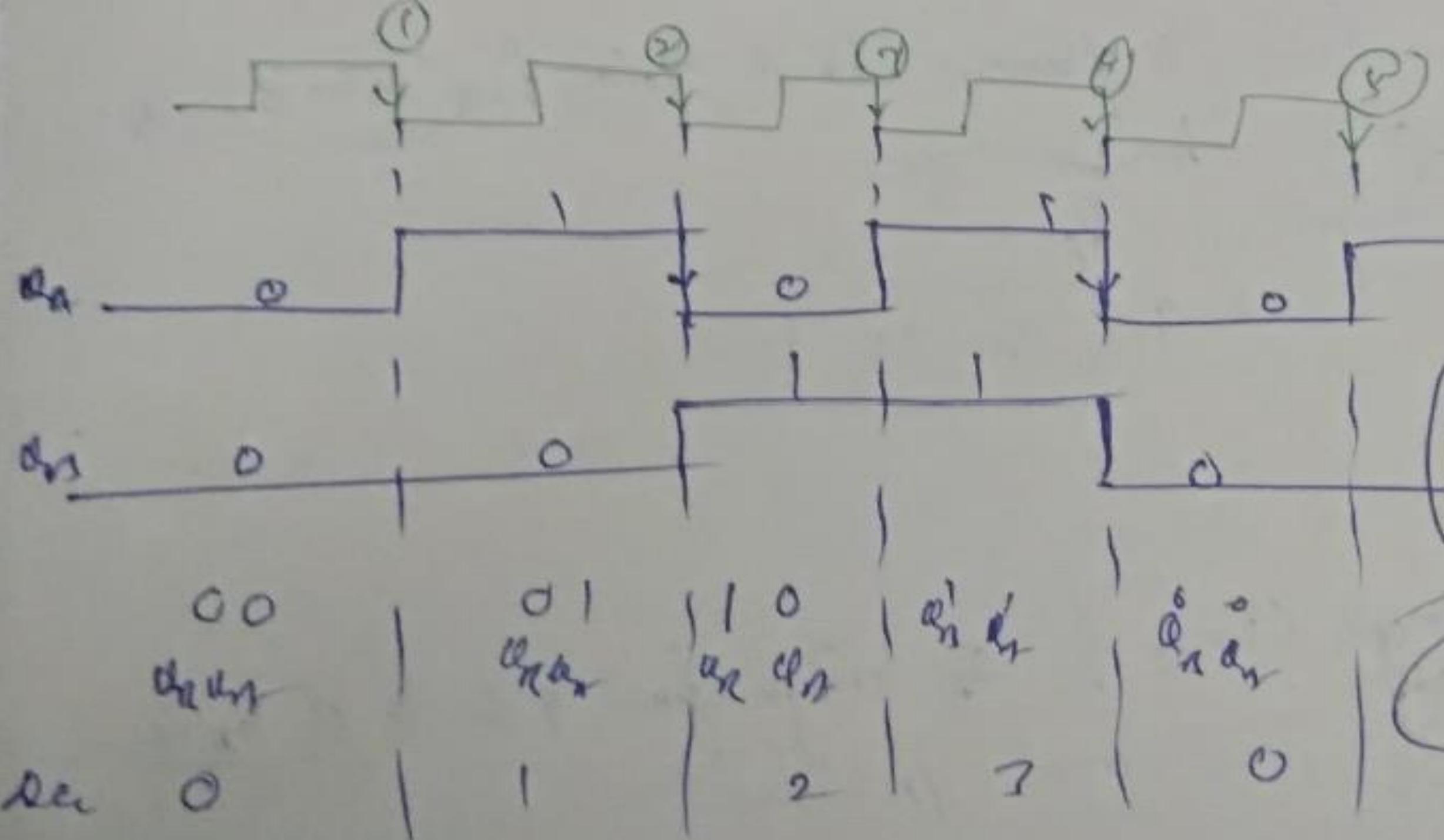
③ Q_B toggle from 1 to 0
 $\boxed{(Q_B Q_A = 00)}$ $Q_B = 0$

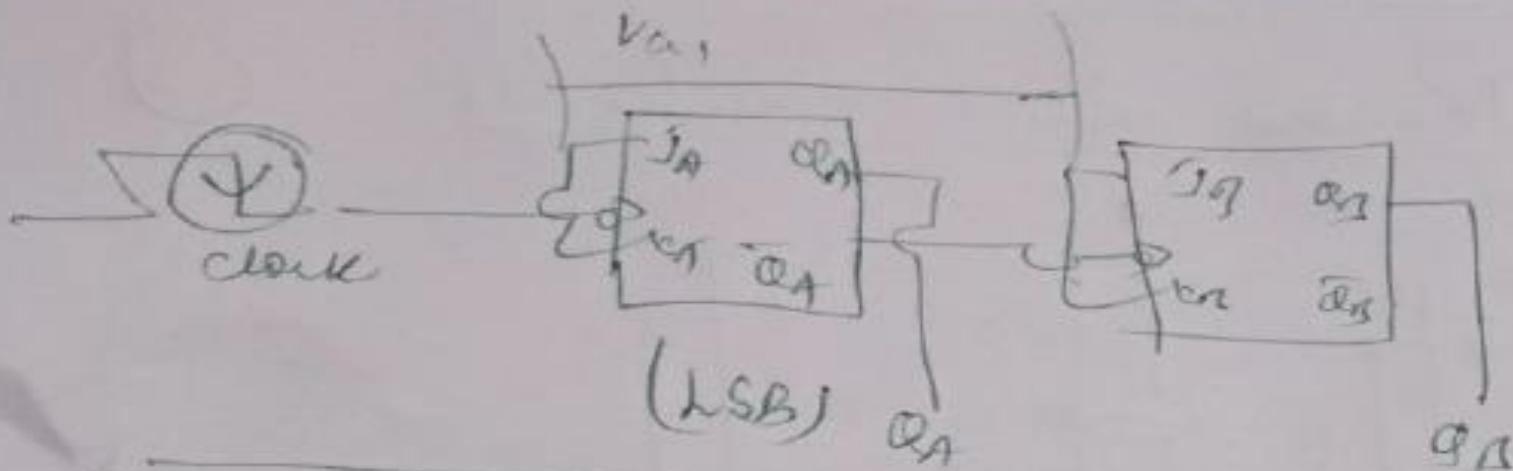
No. of states = 2^n (n no. of flipflop)

Minimum count =

2^{n-1} ($2^2 \approx 8$)

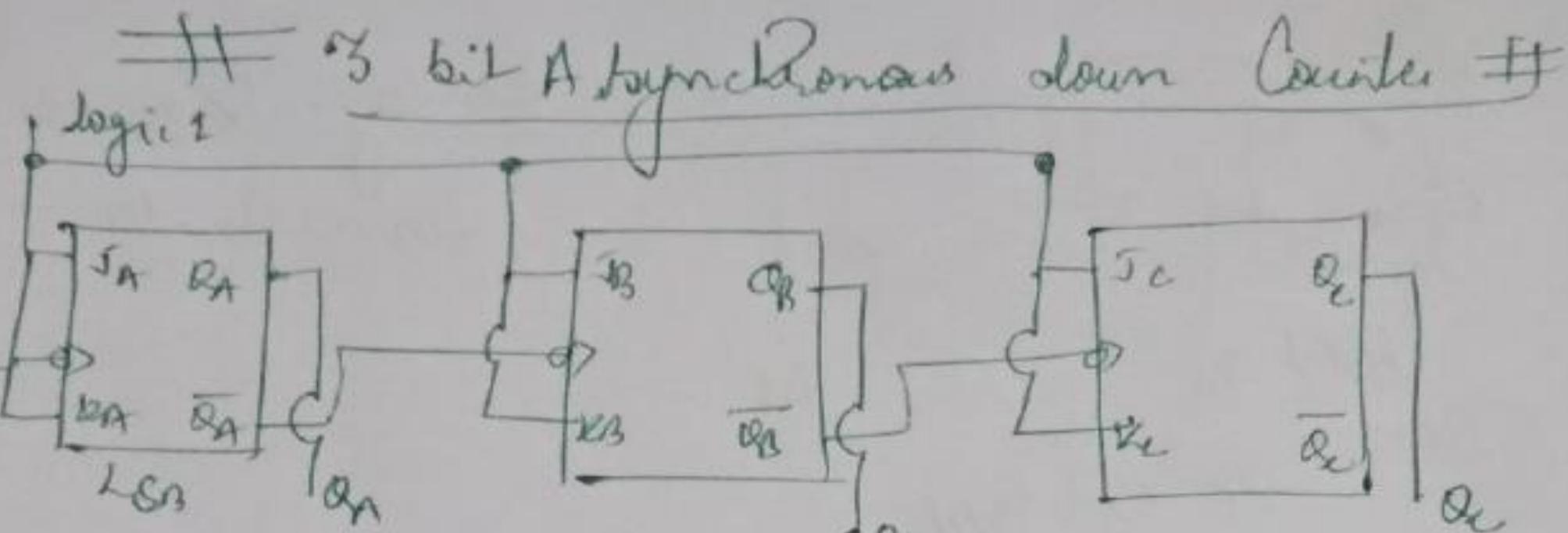
class	α_n	$\alpha_n \cup \beta_1$	β_n
normally	0	0	0
good	0	1	1
bad	1	0	2
new	1	1	3
old	0	0	0





2 Bit asynchronous
down Counter

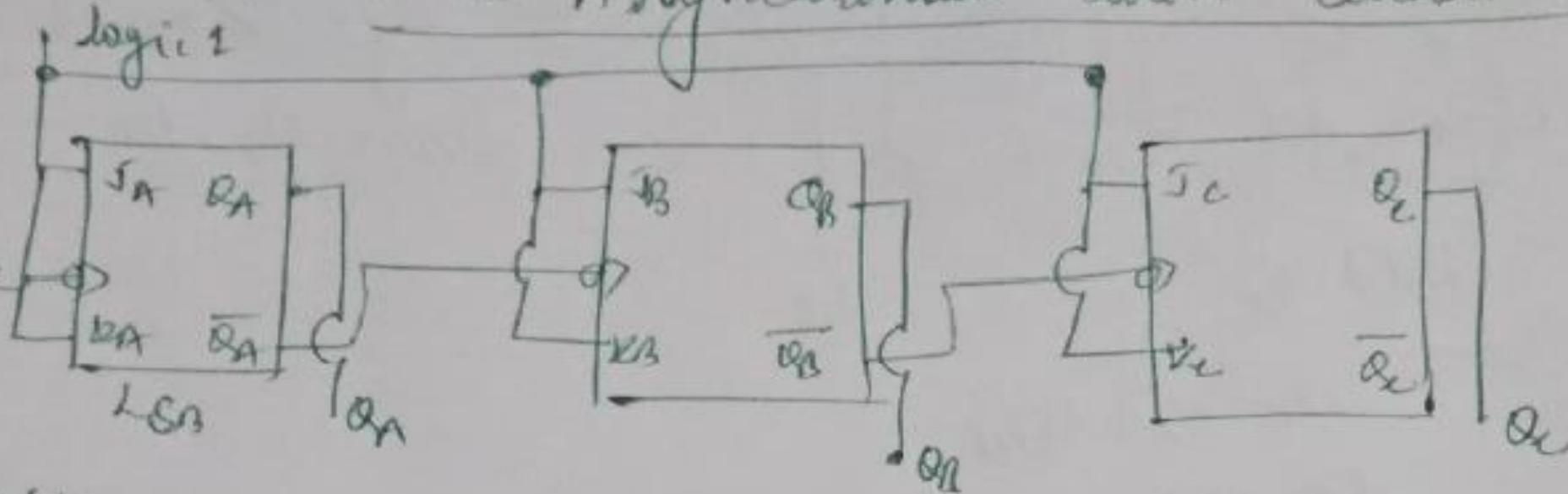
	Q _A	Q _B (LSB)	
Initial	0	0	
clock 1 →	1	1	3 { $\begin{array}{l} Q_A \rightarrow 0 \text{ to } 1 \\ \bar{Q}_A \rightarrow 1 \text{ to } 0 \end{array}$ } <u>neg</u>
clock 2 →	1	0	2 { $\begin{array}{l} Q_A \rightarrow 1 \text{ to } 0 \\ \bar{Q}_A \rightarrow 0 \text{ to } 1 \end{array}$ }
clock 3 →	0	1	1 { $\begin{array}{l} Q_A \rightarrow 0 \text{ to } 1 \\ \bar{Q}_A \rightarrow 1 \text{ to } 0 \end{array}$ }
clock 4 →	0	0	0 { $\begin{array}{l} Q_A \rightarrow 1 \text{ to } 0 \\ \bar{Q}_A \rightarrow 0 \text{ to } 1 \end{array}$ }



Initially

Q_1, Q_2, Q_3
0 0 0

~~3~~ 3 bit Asynchronous down Counter # 29



Initially

$Q_1 \quad Q_2 \quad Q_3$
0 0 0

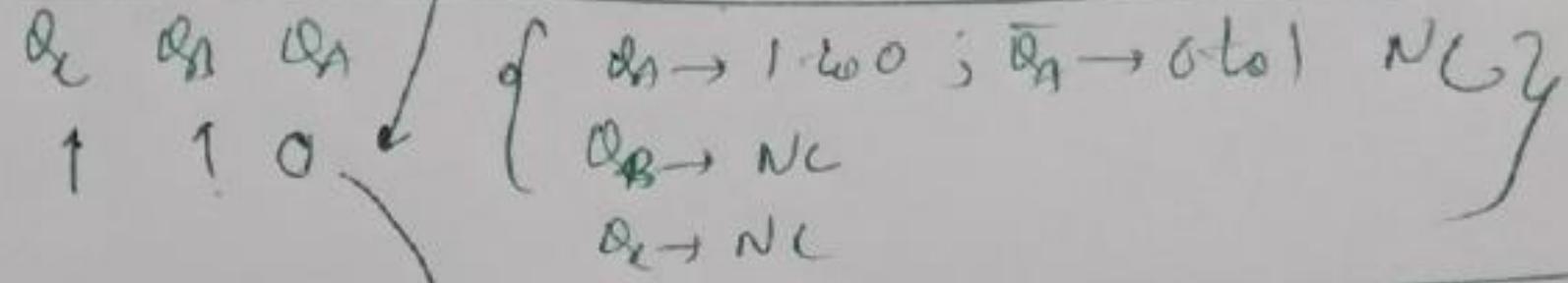
$Q_1 \quad Q_2 \quad Q_3$
1 1 1

clock → (7)

- { $Q_1 \rightarrow 0 \text{ to } 1$ ↗
 $\bar{Q}_1 \rightarrow 1 \text{ to } 0$ ↘
- { $Q_2 \rightarrow 0 \text{ to } 1$ ↗
 $\bar{Q}_2 \rightarrow 1 \text{ to } 0$ ↘
- { $Q_3 \rightarrow 0 \text{ to } 1$ ↗
 $\bar{Q}_3 \rightarrow 1 \text{ to } 0$ ↘

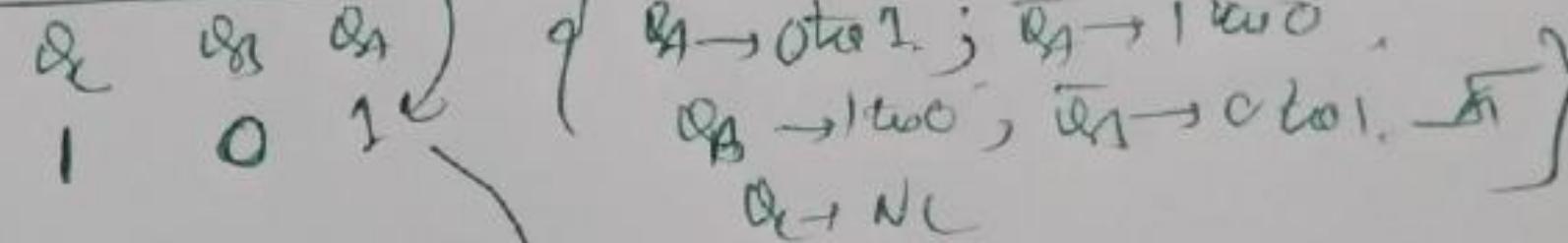
clock 2

(6)



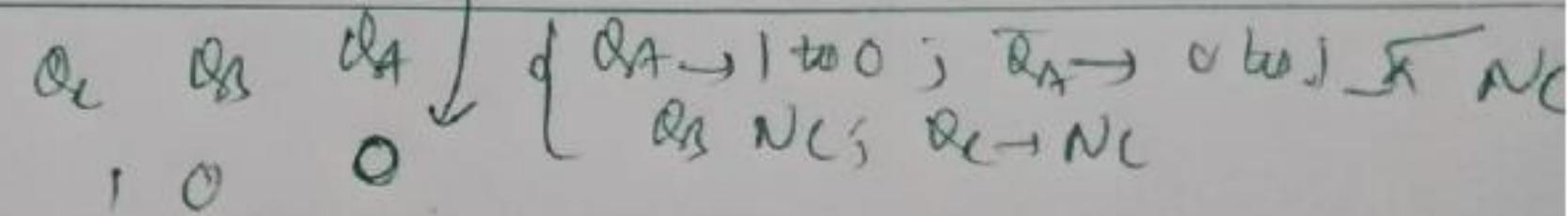
clock 3

(5)



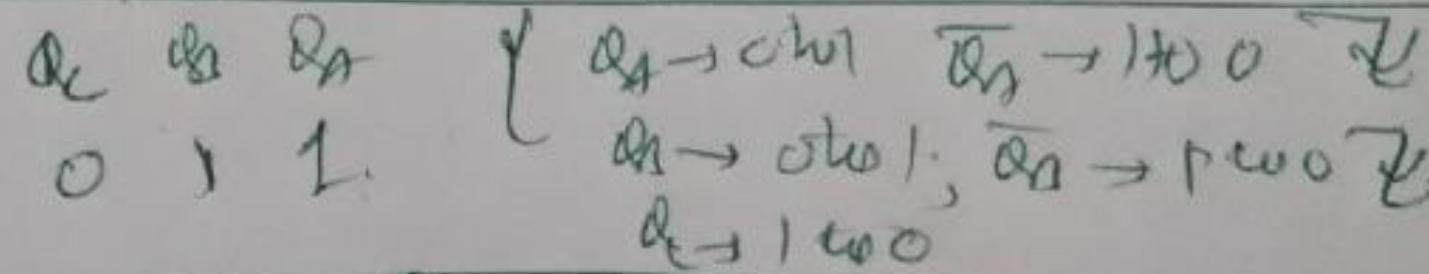
clock 4

(4)



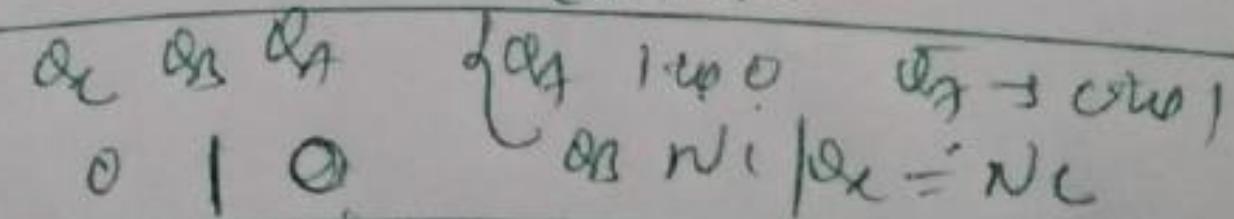
clock 5

(3)



clock 6

(2)



clock 5

(1)

Q_x	Q_1	Q_2	$\left\{ \begin{array}{l} Q_1 \rightarrow \text{ctrl}, \overline{Q_2} \rightarrow \text{HOO} \\ Q_1 \rightarrow \text{ctrl}, \overline{Q_2} \rightarrow \text{PWO} \\ Q_x \rightarrow \text{HOO} \end{array} \right.$
0	1		

clock 6

(2)

Q_x	Q_1	Q_2	$\left\{ \begin{array}{l} Q_1 \rightarrow \text{HOO}, \overline{Q_2} \rightarrow \text{ctrl} \\ Q_1 \rightarrow \text{ctrl}, \overline{Q_2} \rightarrow \text{ctrl} \\ Q_x \rightarrow \text{ctrl} \end{array} \right.$
0	1	0	

clock 7

(1)

Q_x

Q_1

Q_2

clock 8

(0)

Q_x

Q_1

Q_2

Modules of the Counter

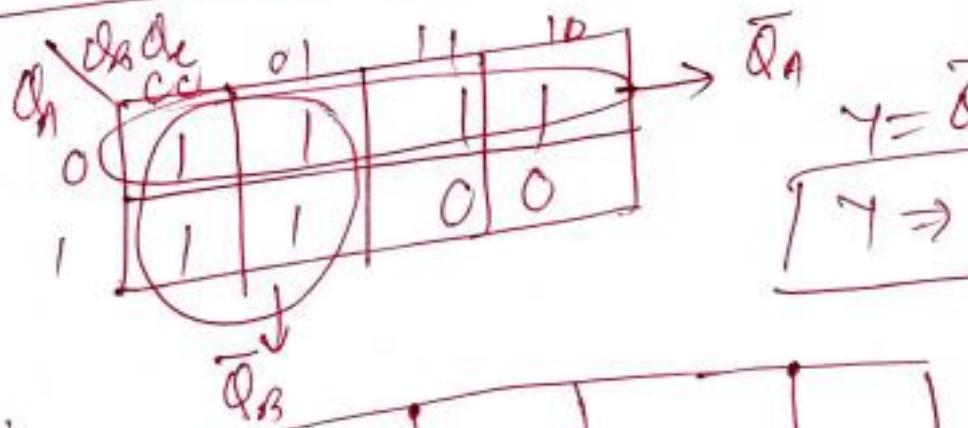
The 2 bit ripple counter is called mod-4. 3 bit
ripple counter is called mod-8.

So n bit ripple counter is called modulo n
counter.

$$\boxed{\text{mod no} = 2^n}$$

~~#~~ Mat 6 Asynchronous Counter

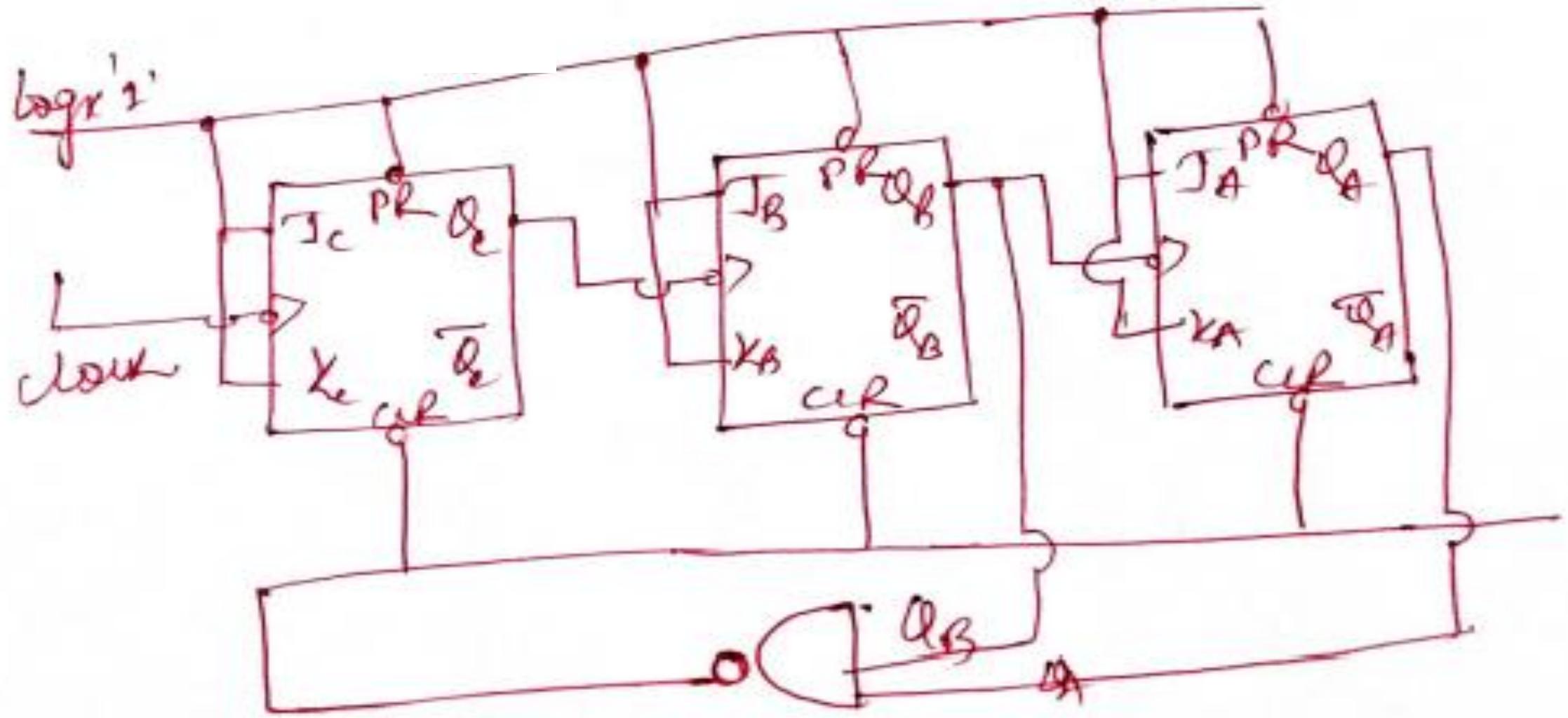
clock	Q_A	Q_B	Q_C	Count	Y
↓	0	0	0	0	1
↓	0	0	1	1	1
↓	0	1	0	2	1
↓	0	1	1	3	1
↓	1	0	0	4	1
↓	1	0	1	5	1
↓	1	1	0	6	0
↓	1	1	1	7	0



$$Y = \overline{Q_A} + \overline{Q_B}$$

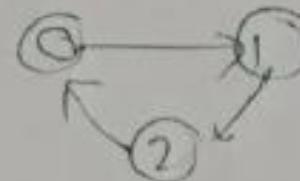
$$\boxed{Y \Rightarrow \overline{Q_A} \cdot \overline{Q_B}}$$

NAND gate



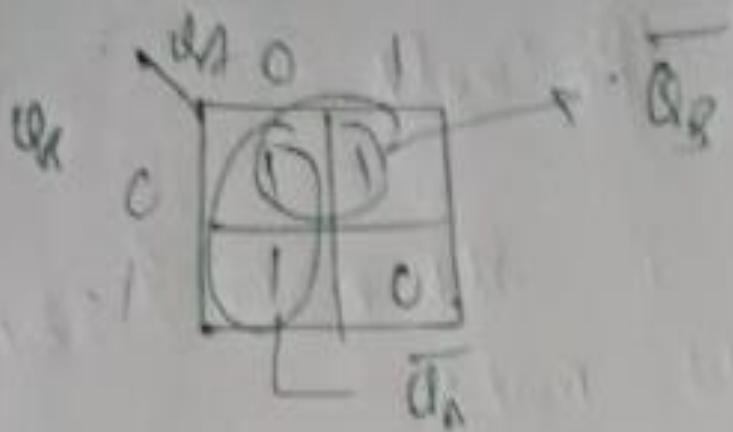
Q1 Design a mod-3 asynchronous counter using a 2 bit ripple counter?

Soluⁿ - mod-3 counter is a counter having three states 00, 01, 10. After 10 it will be taken back to 00.



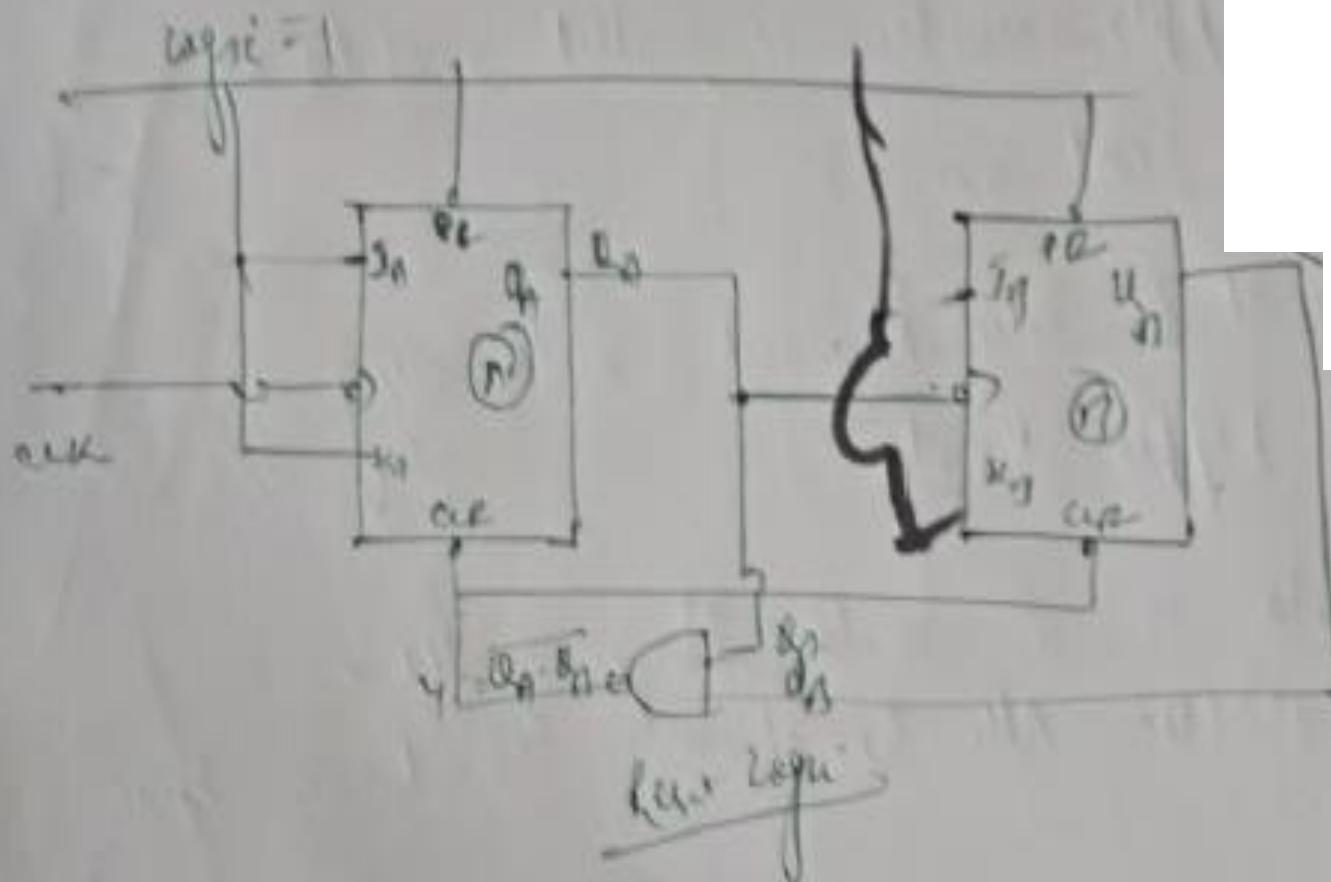
* As soon as flip flop number state 2, its clear logic should become 0 at 0101 clear all the ff logic so jump back to 0 state.

Q_1	Q_0	Y_{010}	
0	0	1	
0	1	1	
1	0	1	
1	1	0	clear all ff

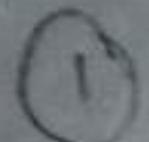


$$y = \bar{Q}_k + \bar{Q}_h$$

$y \Rightarrow \bar{Q}_k \cdot \bar{Q}_h \text{ sind } \theta$



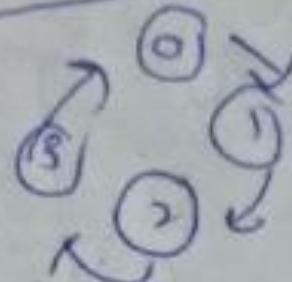
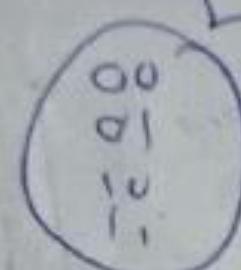
Synchronous Counter



2 bit Synchronous Counter

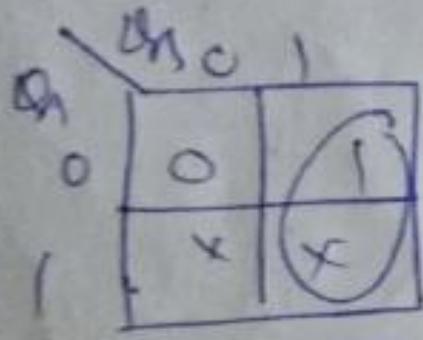
J-K ff for both (T)

Q_1	Q_0	J_K
0	0	0x
0	1	1x
1	0	x1
1	1	x0

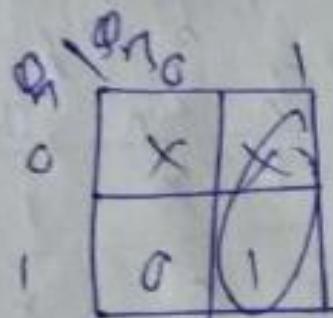


Present State	Next State		Flip flop			
	Q_A	Q_B	J_A	K_A	J_B	K_B
00	0	0	0	0	0	x
01	0	1	0	1	1	x
10	1	0	1	0	0	1
11	1	1	x	1	x	x

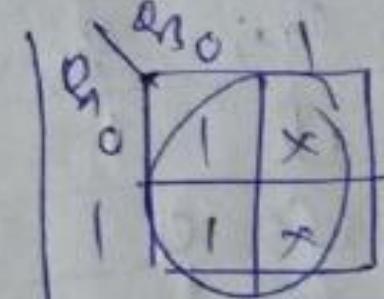
base remain same as in down counter



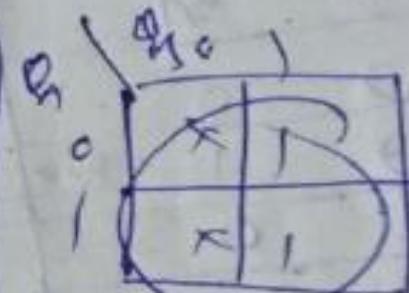
$$J_A = Q_3$$



$$k_A = Q_3$$

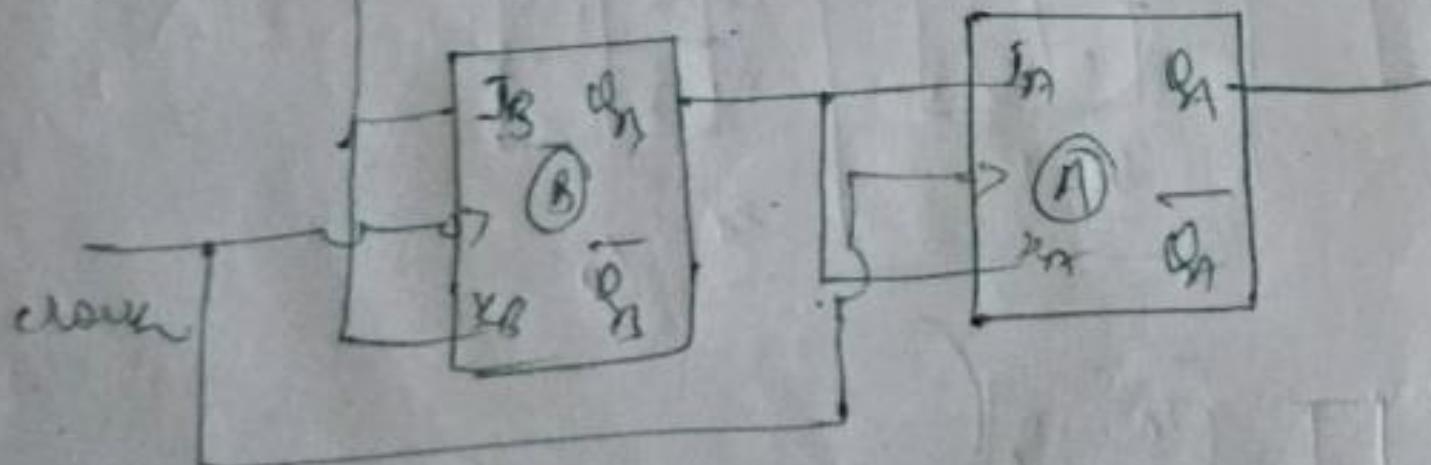


$$J_B = 1$$



$$k_B = 1$$

Logic



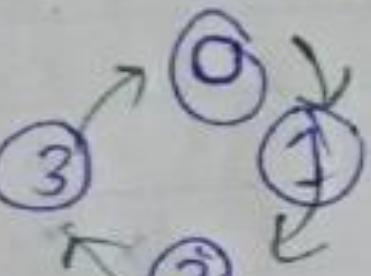
* 2 bit Synchronous down Counter

J-K flip flop

Qn	Qn+1	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0



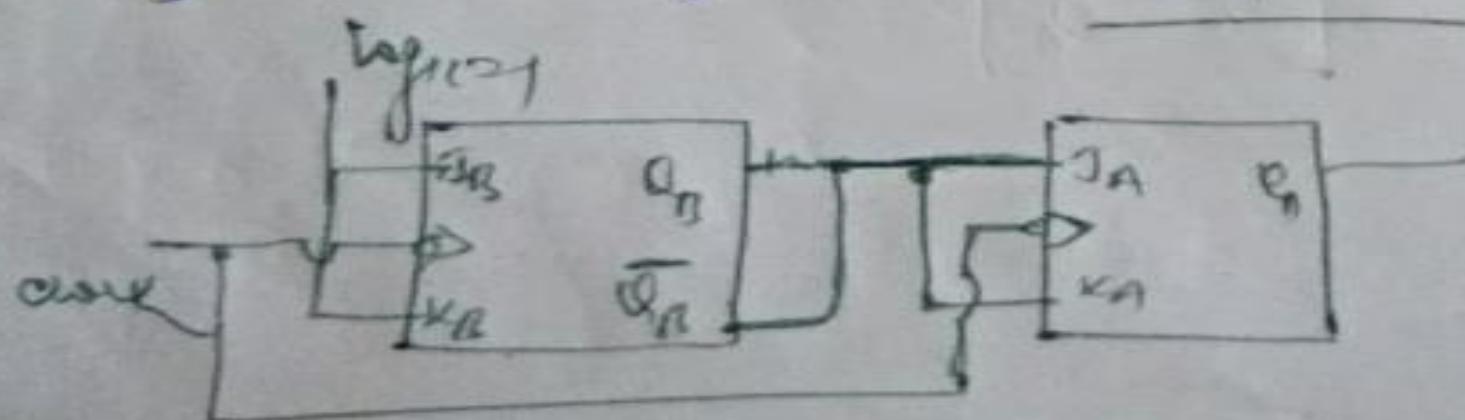
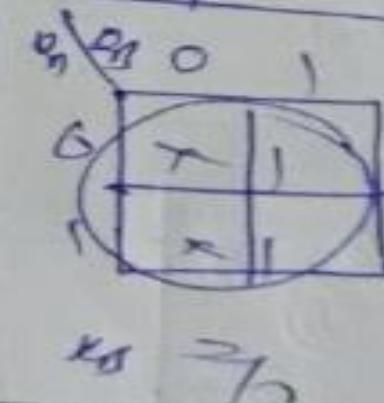
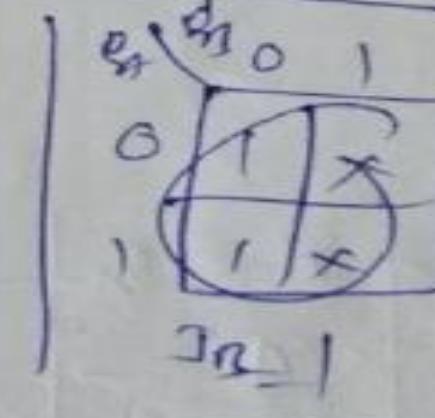
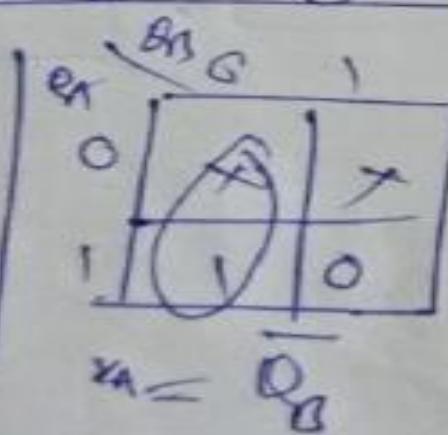
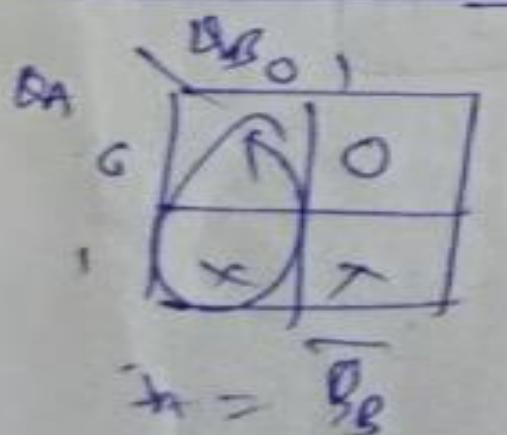
up counter



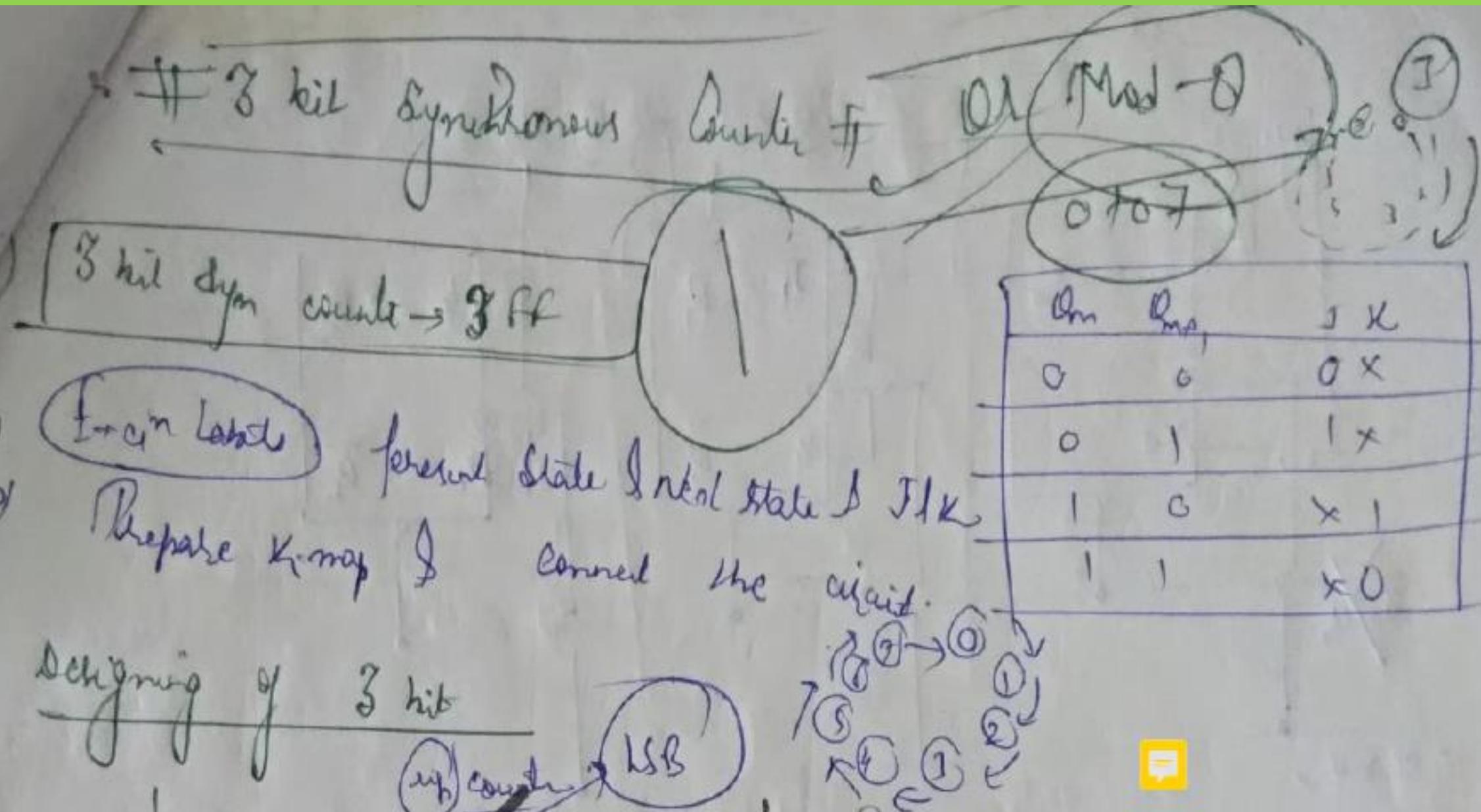
down counter

Present State | Next State / by

Current State		Next State		Flag	Prop	Exp	
Q_0	Q_1	Q_{0+1}	Q_{1+1}	J_B	K_B	J_R	K_R
0	0	0	1	↓	1	1	x
0	1	1	0	↓		x	
1	0	0	0			x	
1	1	0	1				x

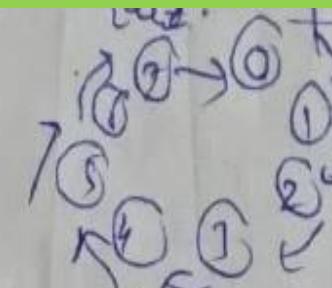
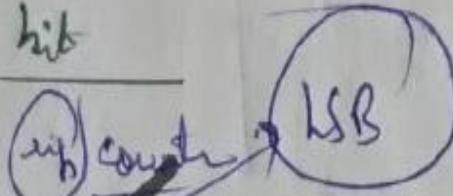


3 bit Synchronous-Up-Counter



3 bit Synchronous-Up-Counter

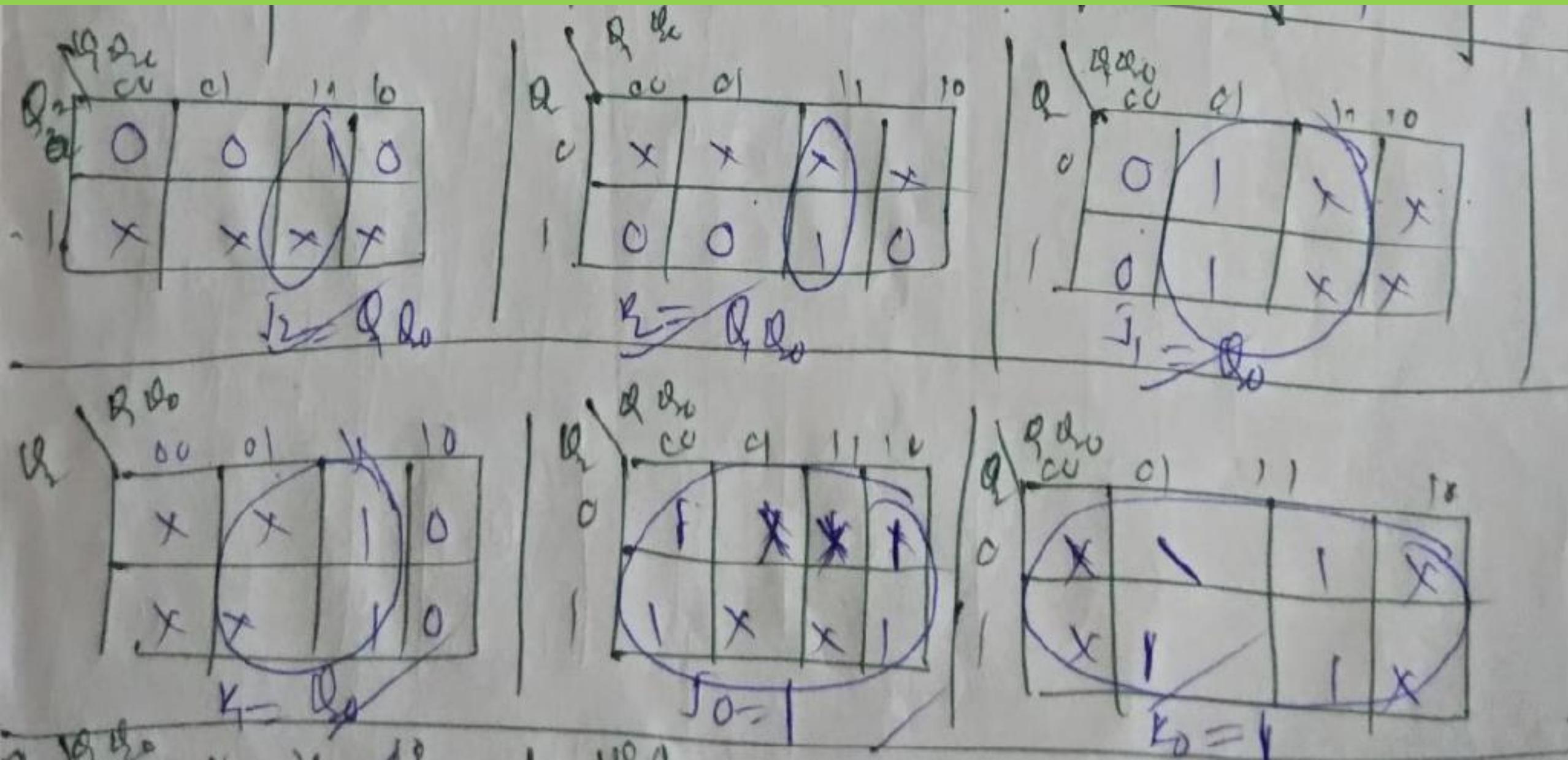
Design of 3 bit



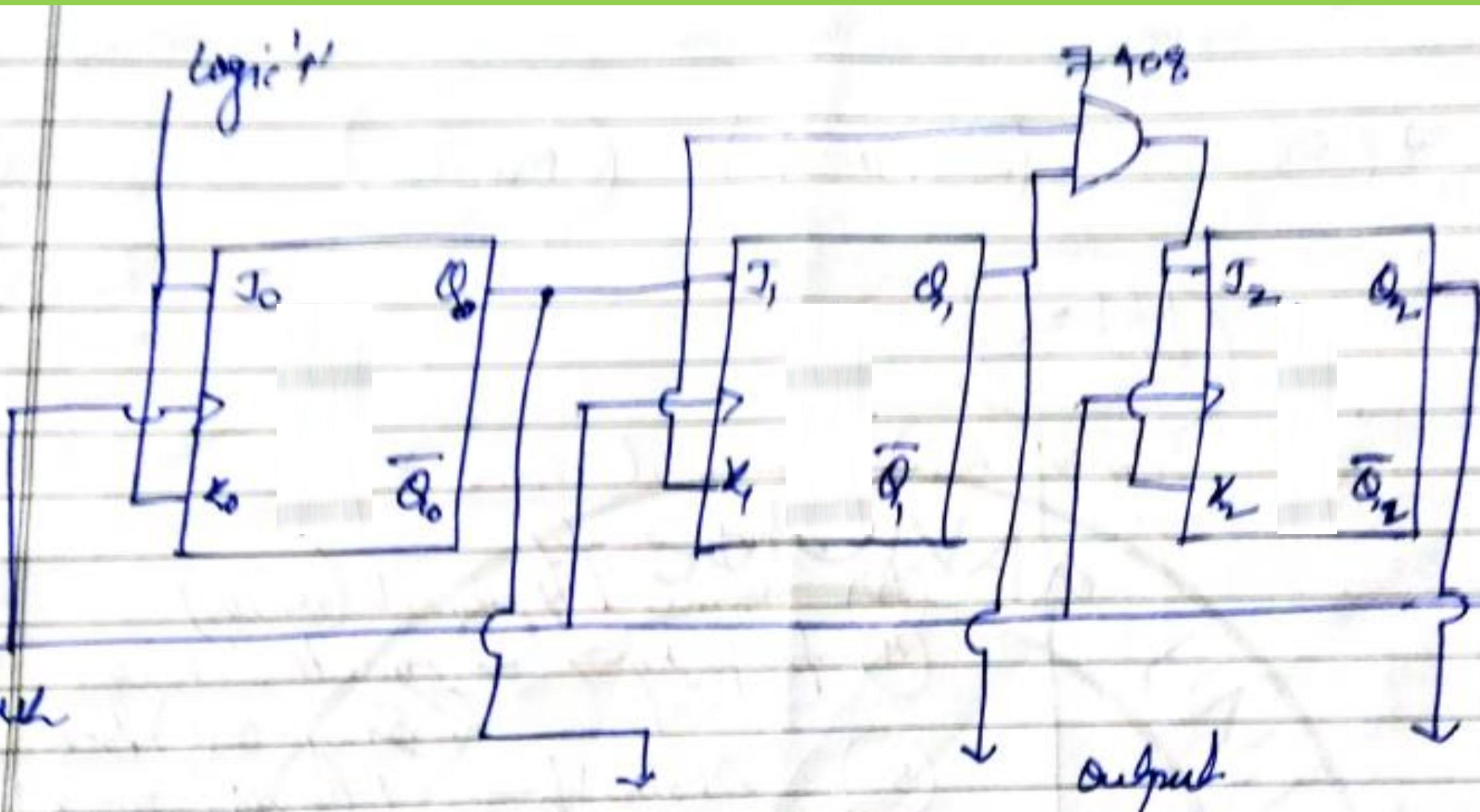
Sequenz	Bereit State	Neue State	Flip flop
0	0 0 0	0 0 1	0 X
1	0 0 1	0 1 0	0 X
2	0 1 0	0 1 1	1 X
3	0 1 1	1 0 0	X 0
4	1 0 0	1 0 1	X 1
5	1 0 1	1 1 0	0 X
6	1 1 0	1 1 1	1 X
7	1 1 1	0 0 0	X 0

R _m	R _{m1}	J K
0	0	0 X
0	1	1 X
1	0	X 1
1	1	X 0

3 bit Synchronous-Up-Counter



3 bit Synchronous-Up-Counter



3 bit Synchronous-Down-Counter

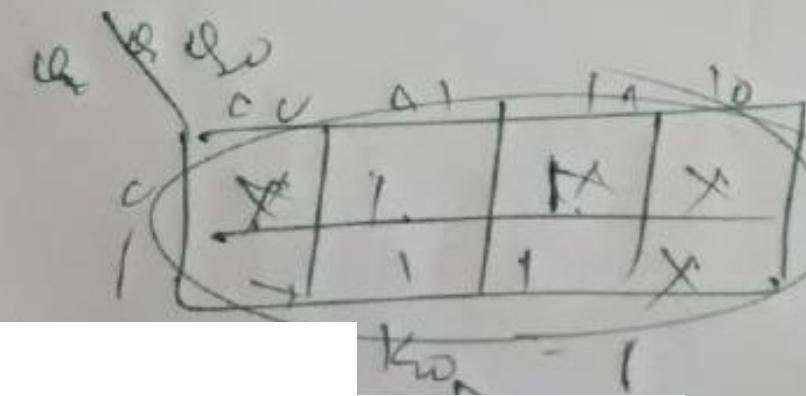
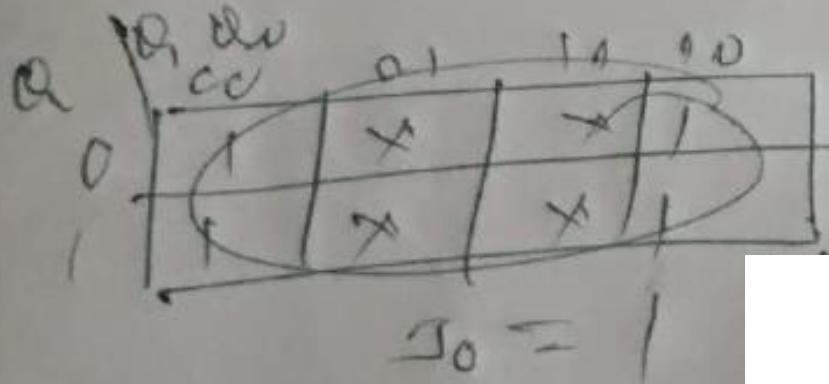
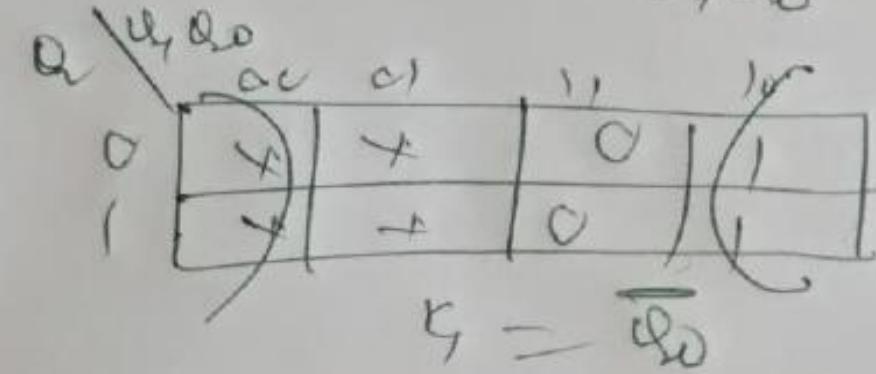
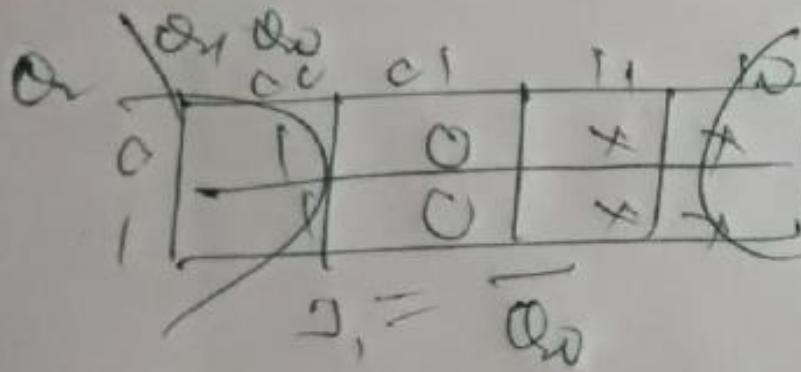
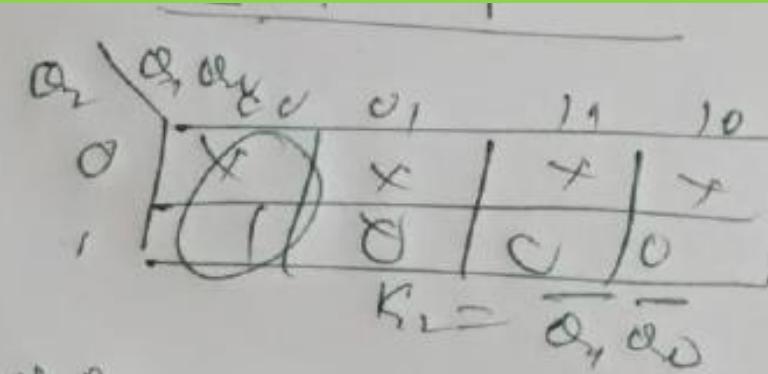
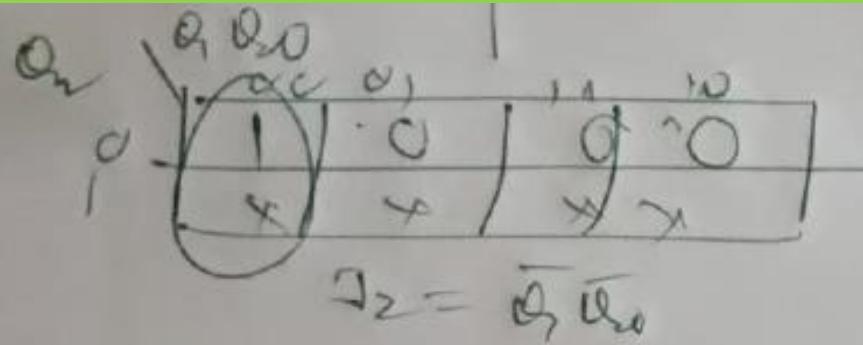
000	0x
010	1x
100	x1
110	x0

3 bit Synchronous down Counter

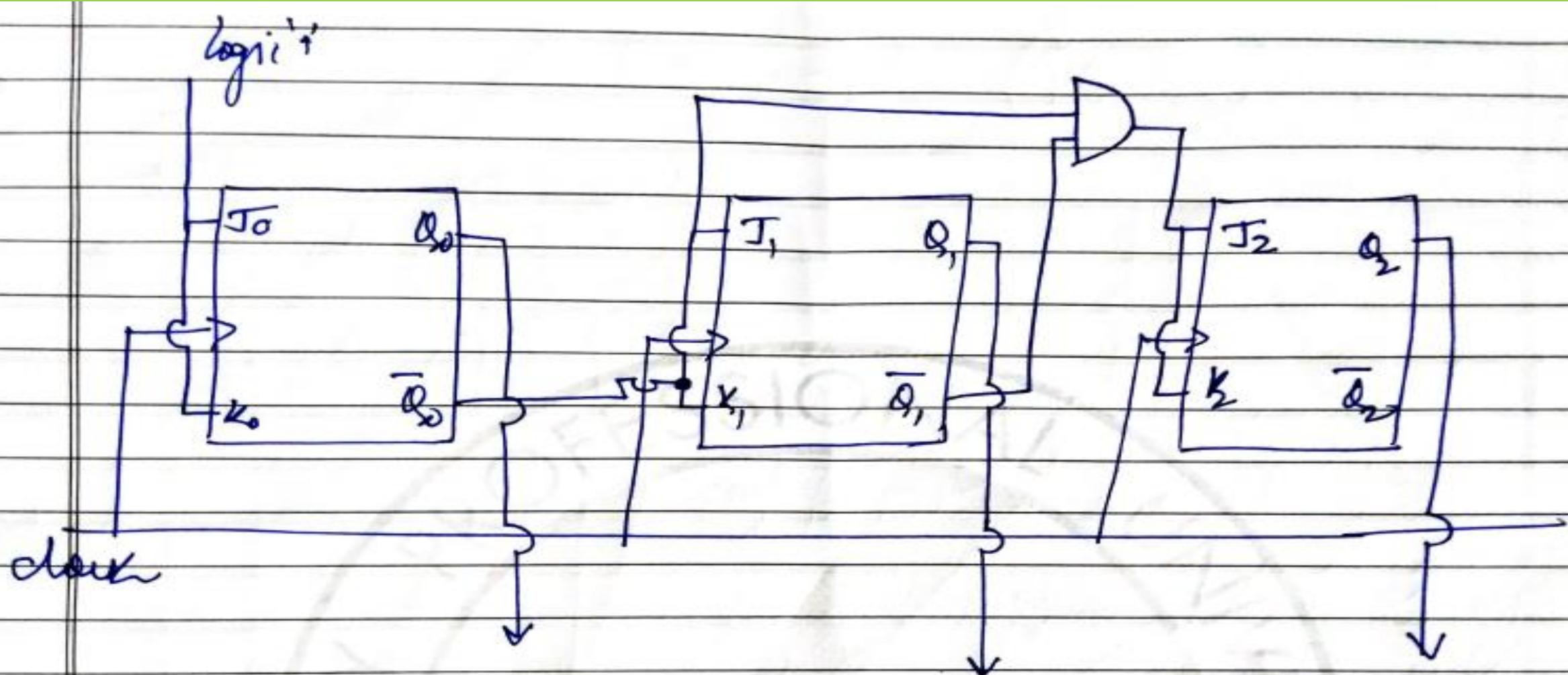
Serial No	Q_2	Q_1	Q_0	i_2	i_1	i_0	Q_2	Q_1	Q_0	i_2	i_1	i_0
0	0	0	0	1x	1x	1x	1	0	0	0	0	0
1	0	0	1	0x	0x	x1	0	0	1	0	1	1
2	0	1	0	0x	x1	1x	0	1	0	0	1	0
3	0	1	1	0x	x0	x1	0	1	1	0	0	1
4	1	0	0	0x	x1	1x	1	0	0	0	0	0
5	1	0	1	x1	1x	1x	0	0	1	0	1	1
6	1	1	0	x0	0x	x1	0	0	0	0	0	0
7	1	1	1	x0	x1	1x	x0	x0	x1	0	1	0

Q_2	Q_1	Q_0	i_2
0	0	0	0x
0	1	1x	
1	0	x1	
1	1	x0	

3 bit Synchronous-Down-Counter



3 bit Synchronous-Down-Counter



Circuit diagram of 3 bit synchronous-down Counter

Module-N or Mod-N synchronous counter

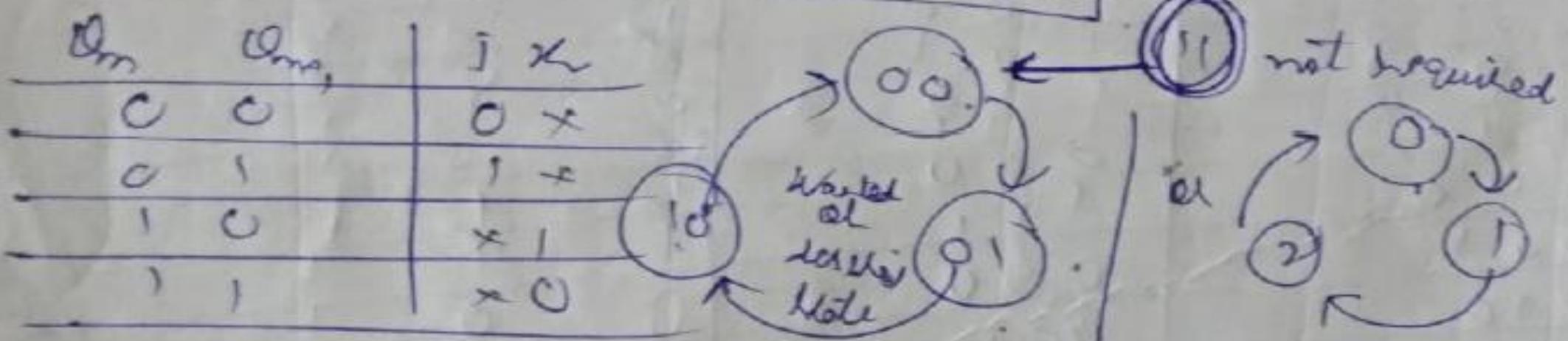
Mod-N counter has N different states. It is called as divide by N counter. It will count upto $N-1$.

e.g. Mod-5 counter. The counter has 5 different states. It will count upto 31. i.e., 0, 1, 2, 3, 4.

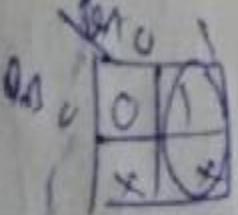
Ques
Ans.

Design the mod-7 synchronous counter

mod-3 \rightarrow 0, 1 & 2



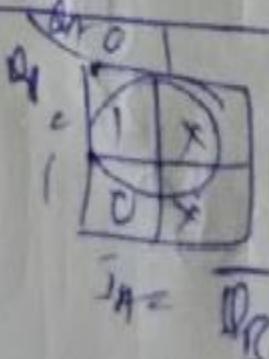
Present State	Next State	Flip Flop f_3
$q_B\ q_A$	$q_B\ q_A$	x_3
0 0	0 1	0x
1 0	1 0	1x
0 1	0 0	1x
1 1	0 0	x1
0 0	1 1	x1
1 1	1 1	0x
0 0	0 0	x1



$$f_3 = q_A$$



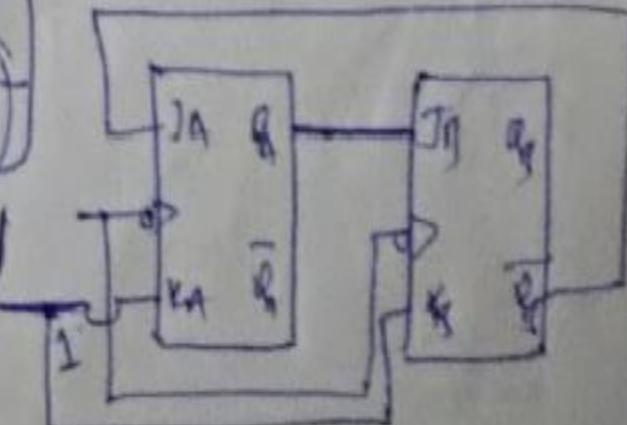
$$x_3 = 1$$



$$x_3 = \overline{q_B}$$

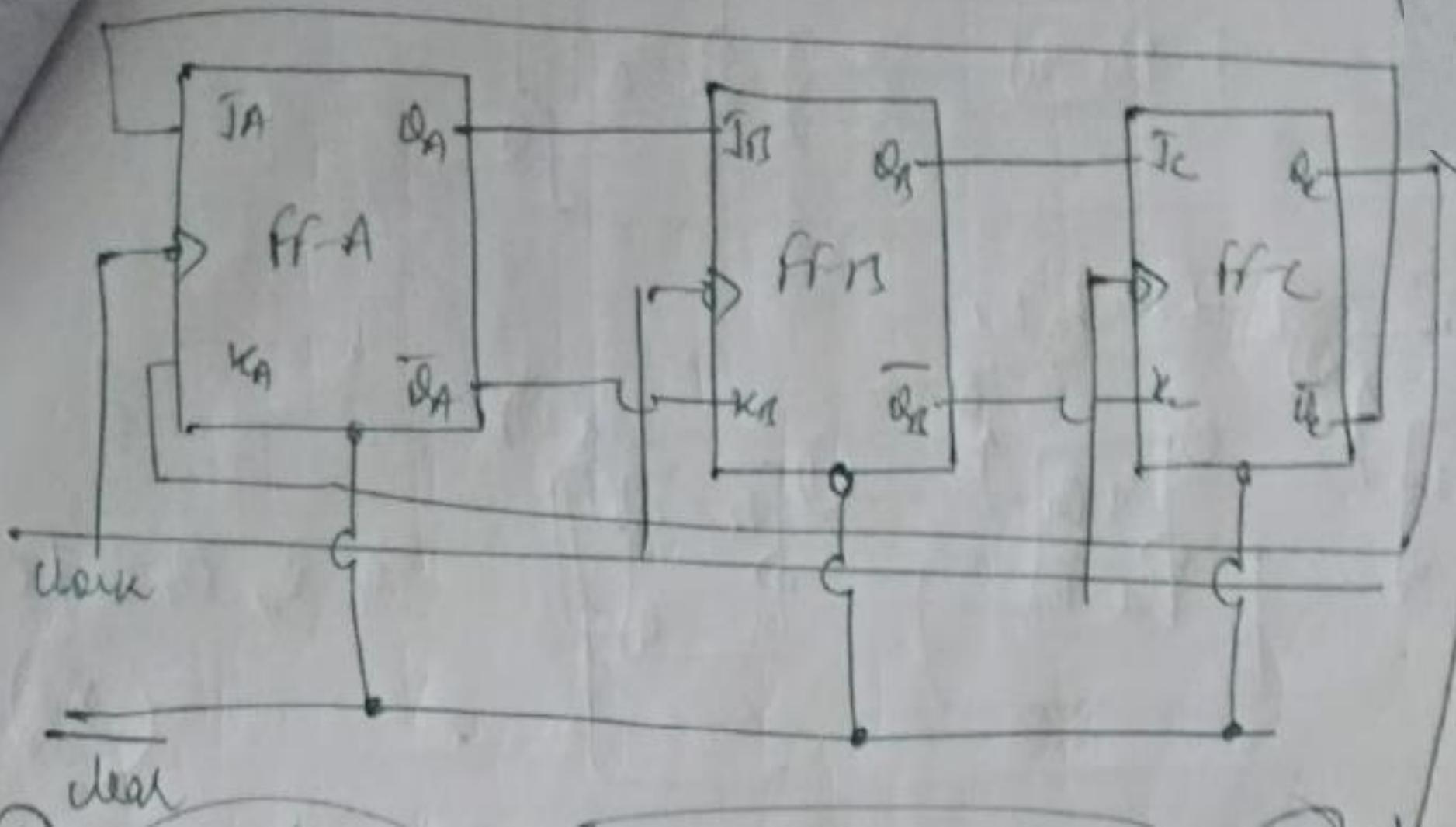


$$x_3 = 1$$



Q_m	Q_{m_1}	$J\ X$
0	0	0x
0	1	1x
1	0	x1
1	1	x0

Johnson or Twisted Ring Counter



clear

①

clear law = 0

$$I_1, Q_1, Q_2, Q_3 = 000 \quad \text{---} \quad 0$$

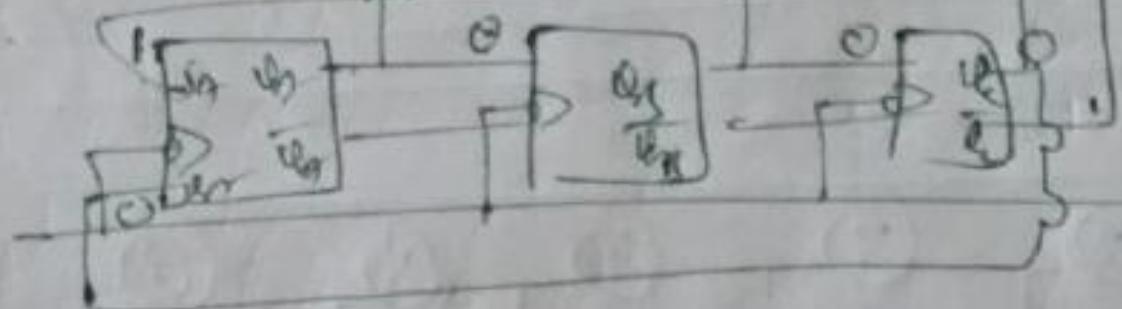
②

$$\text{Ex } [Q_2 = 0] ; Q_2 = 1$$

$$I_A = Q_2 = 1 ; Q_1 = 000$$

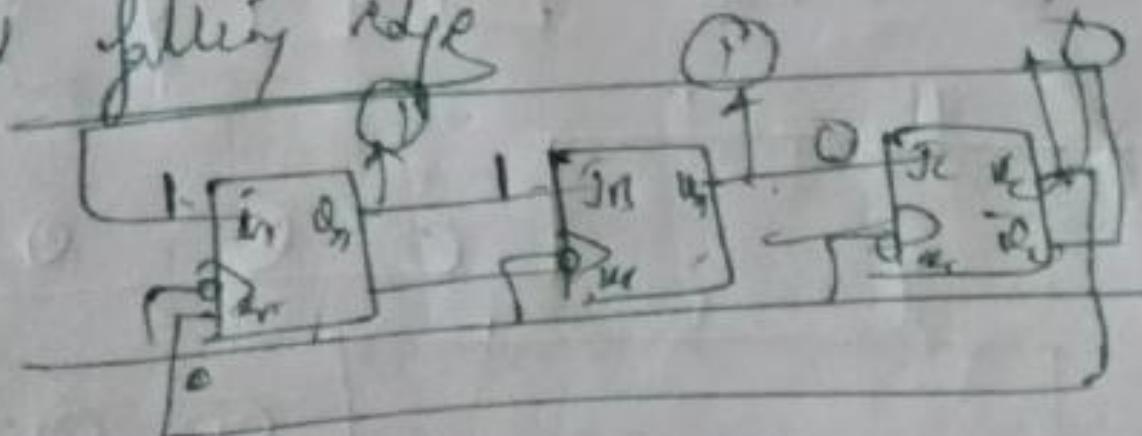
③

just falling up my clear law

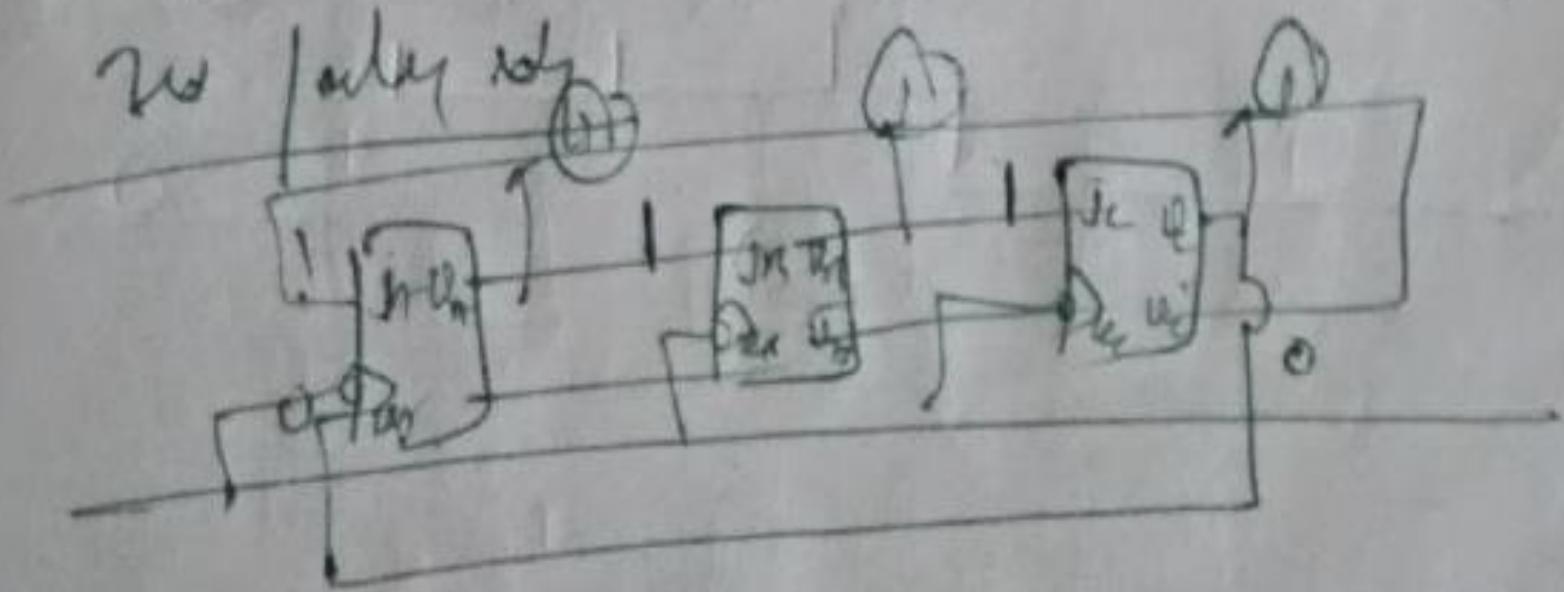


$$Q_1, Q_2, Q_3 = 000 \rightarrow 1$$

2nd falling edge

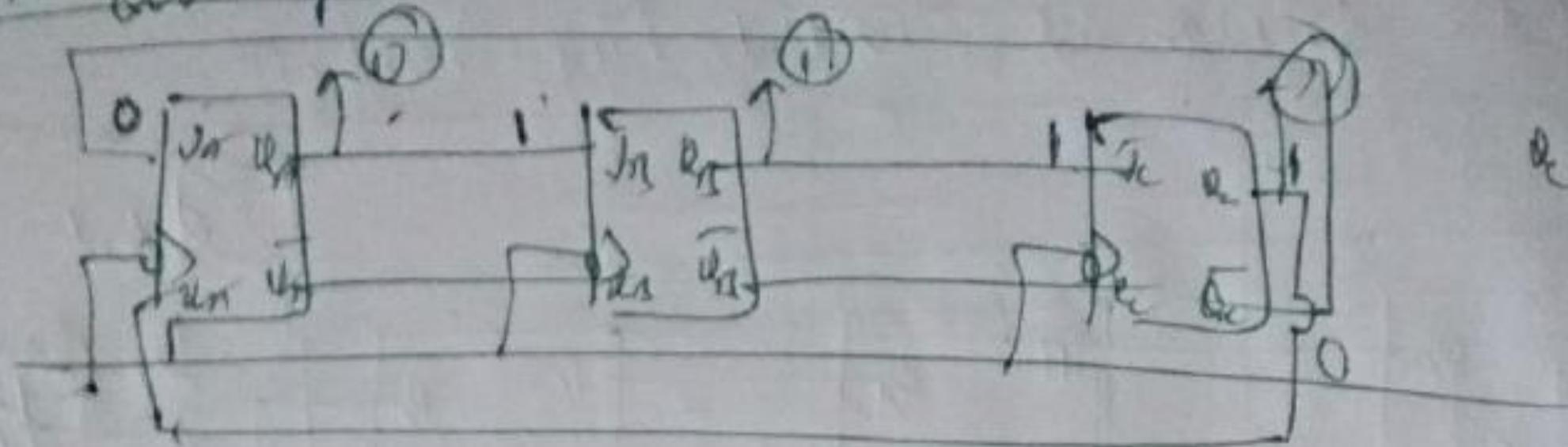


$$Q_1, Q_2, Q_3 = 011 \rightarrow 0$$



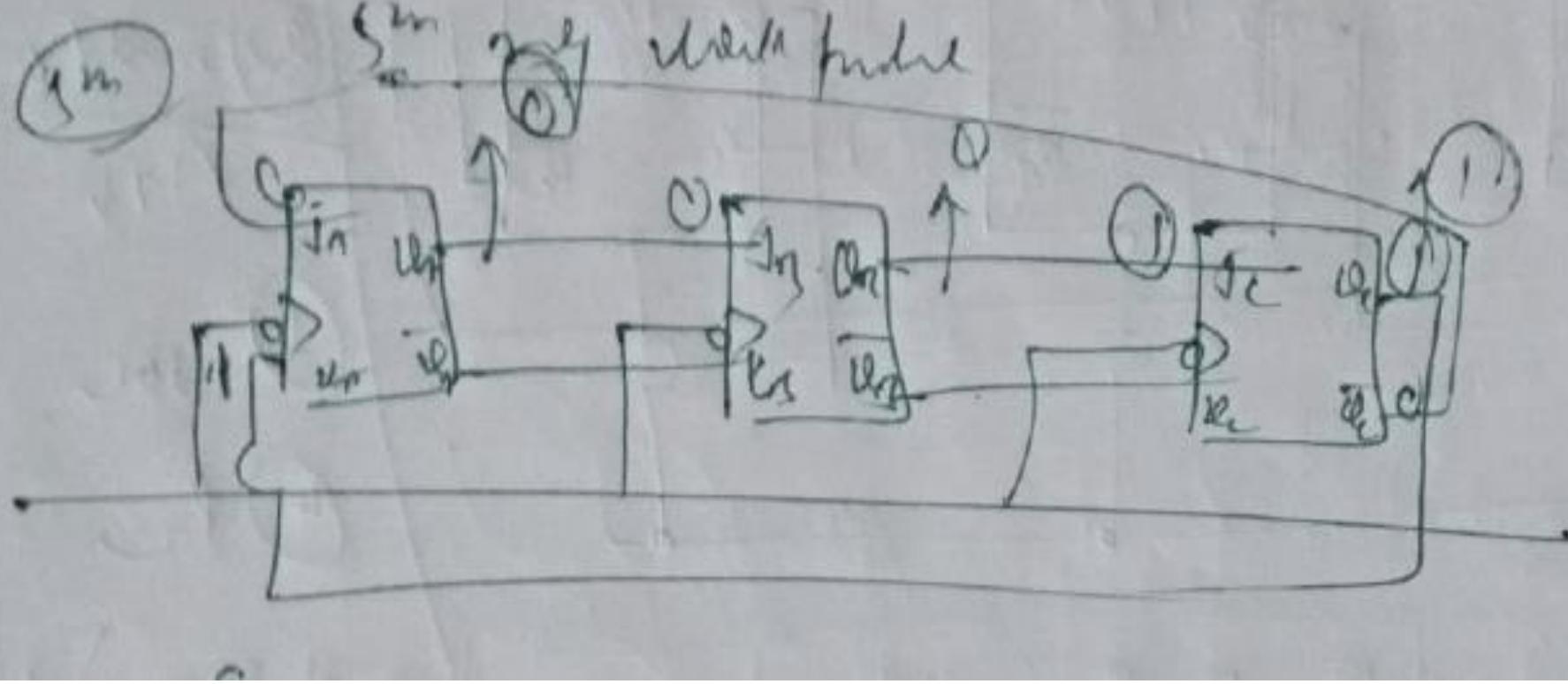
Q 4, Q₁₂ (111 →)

4th sheet of

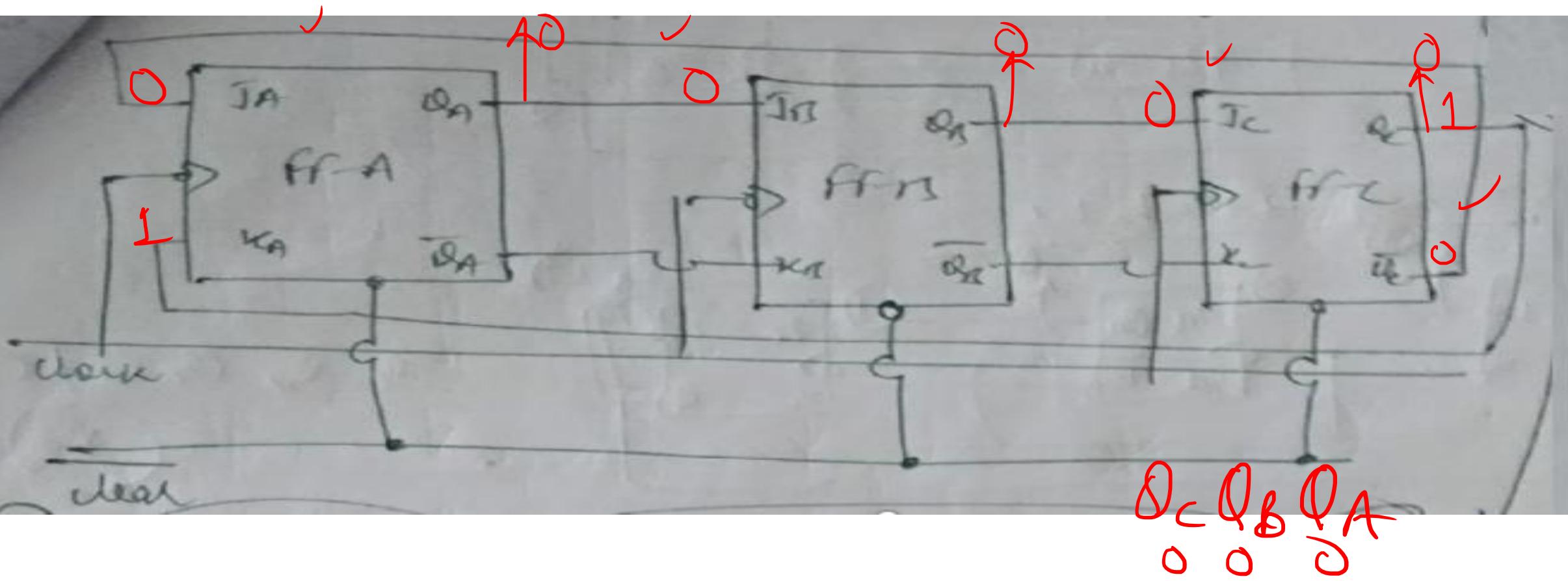


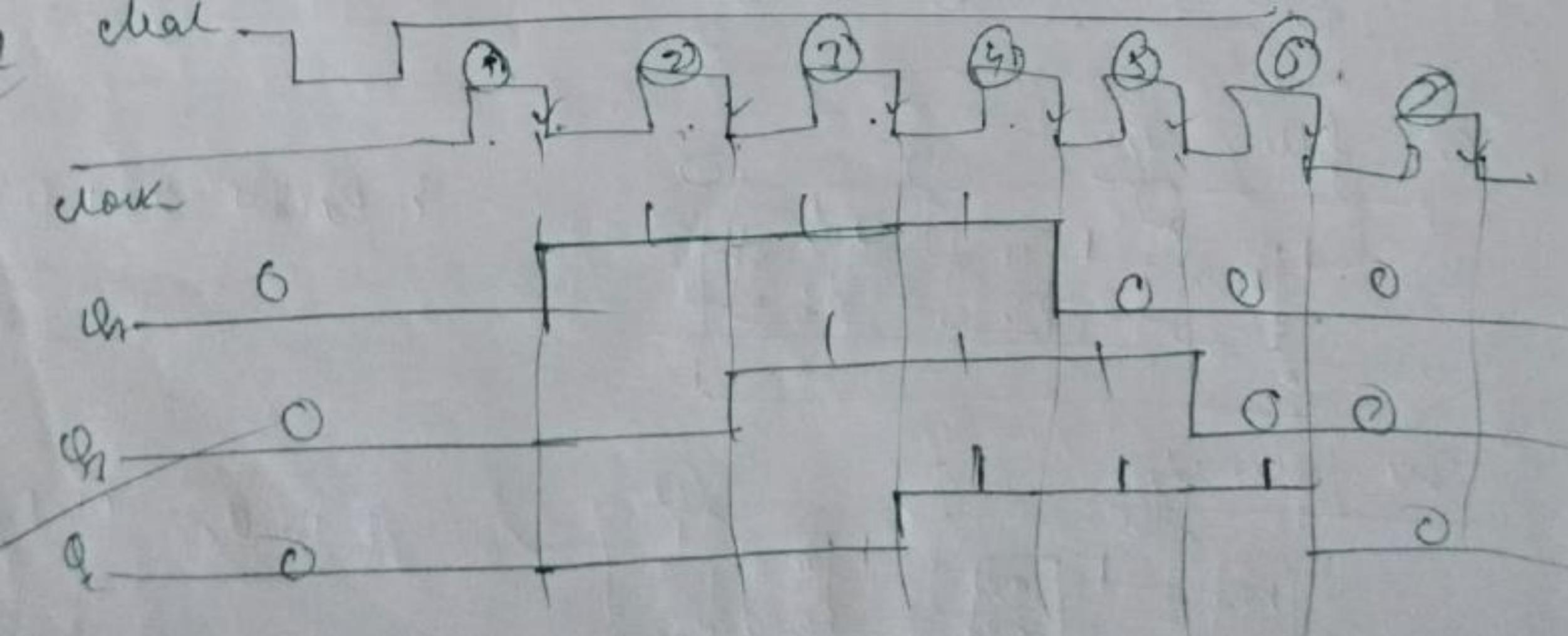
Q. No. 2

110



4 4 2 / 0 0

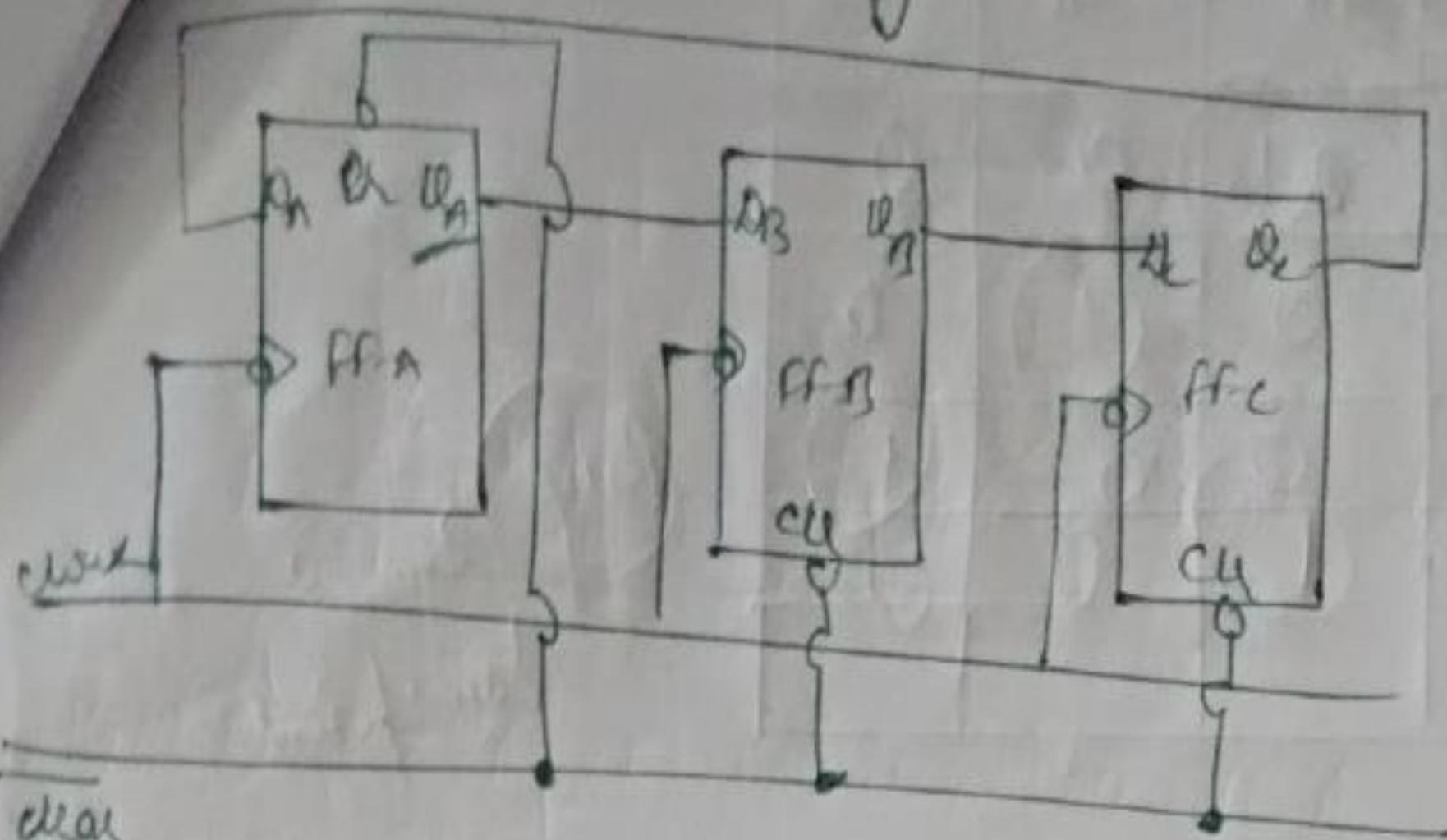




۲۷

~~#1, King County~~

6



① When few clear bit is given to all flipflops

Due to $A=0$ then $Q_1=1$

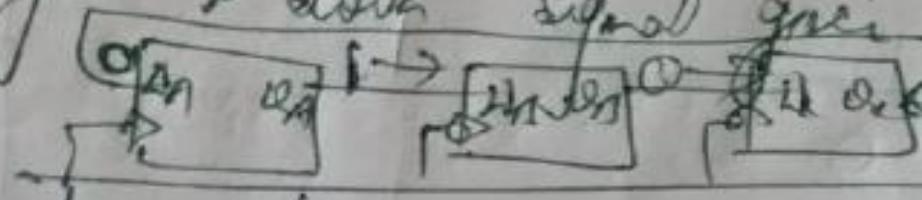
Due to $C_1=0$ then $Q_2=0$

Due to $C_2=0$ then $Q_3=0$

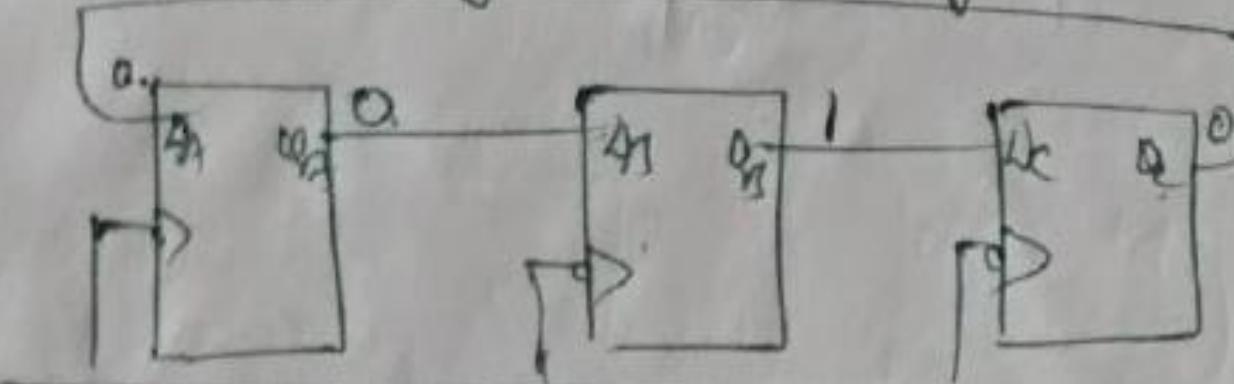
$Q_1 Q_2 Q_3 = 001$

CK	D	Q
0	0	0
1	1	1

Then clear bit become high & down signal give now 2 pulse
shift register.

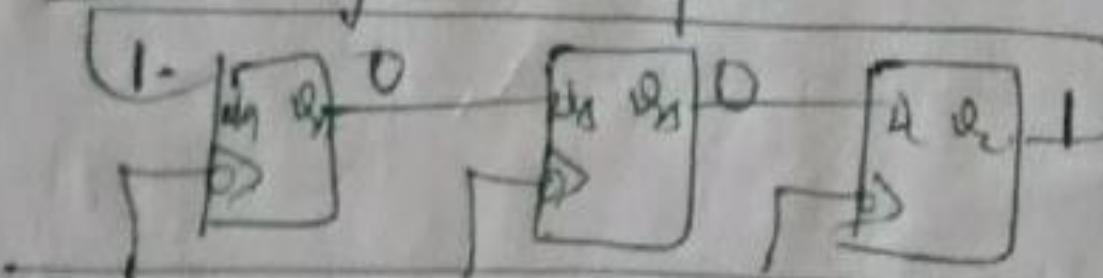


① for first negative clock edge



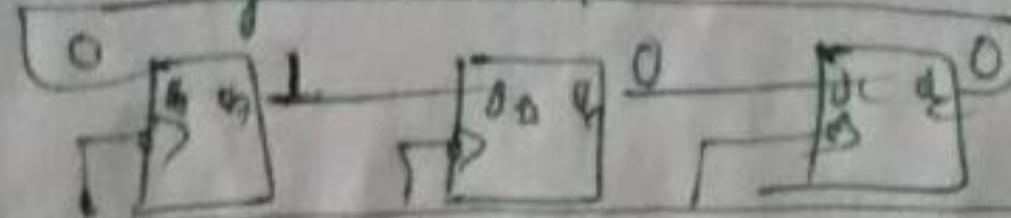
$$Q_1 Q_3 Q_4 = 010$$

② 2nd neg clock edge



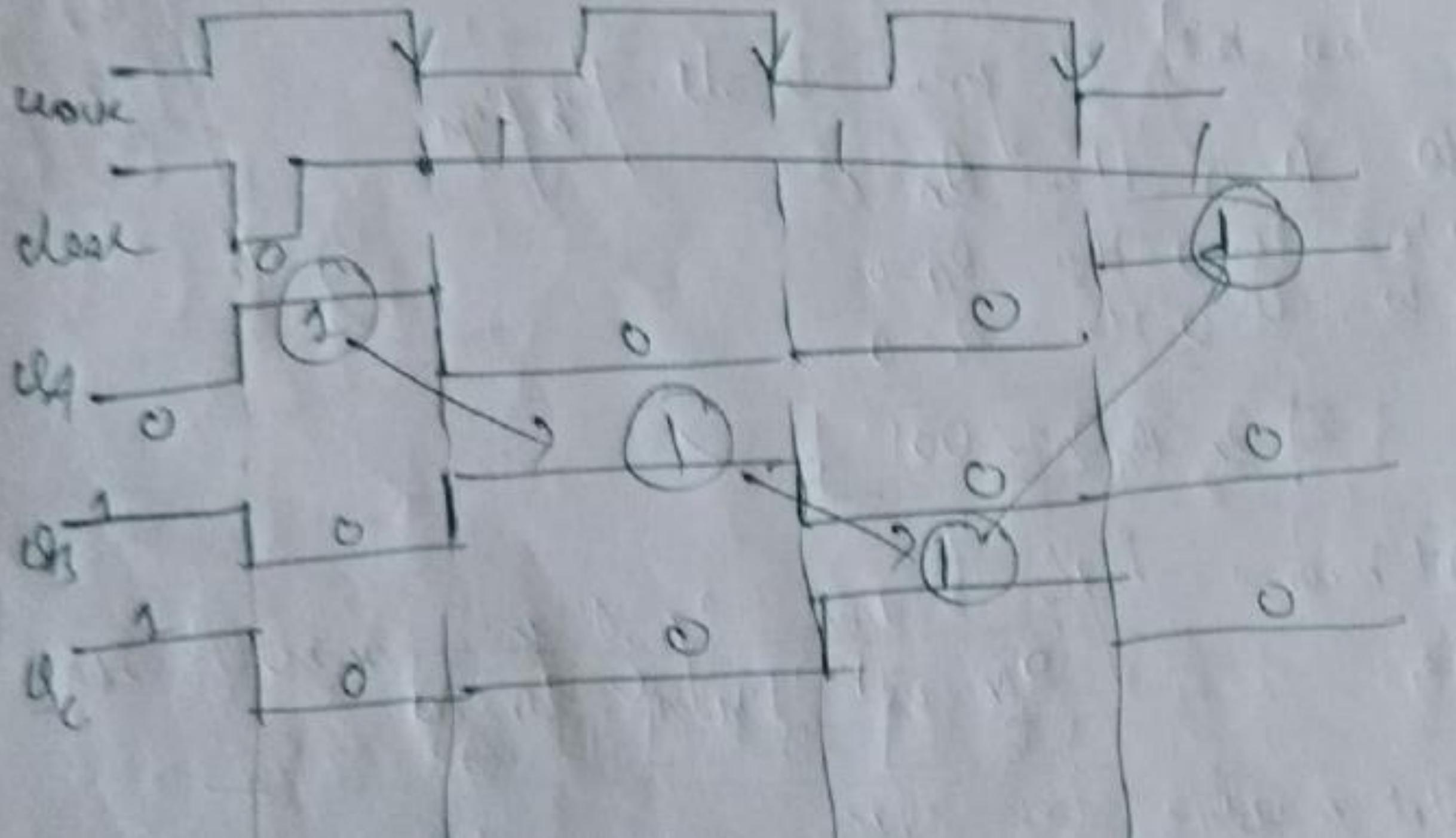
$$Q_1 Q_3 Q_2 = 100$$

③ 3rd neg clock edge



$$Q_1 Q_3 Q_2 = 001$$

curv	curv	Q_n	∂_n	δ
✓	✗	1	0	0
1	1	0	1	0
1	1	0	0	1



SHIFT REGISTERS

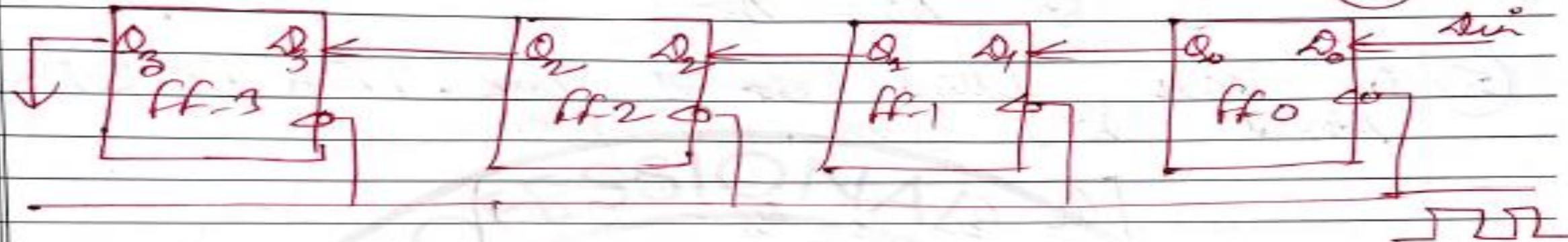
1. The binary data in a register can be moved from one flip flop to other with the application of clock pulses.
2. The registers that allow such data transfer are called as shift registers.
3. Shift registers are used for data storage, data transfer.

MODE OF OPERATIONS OF SHIFT REGISTERS

1. Serial input serial output
2. Serial input parallel output
3. Parallel input serial output
4. Parallel input parallel output

~~# Serial in Serial out (Shift Register) #~~ Serial ~~to I/P~~

(1) 1 1



① Let all the flip flops be in the initial condition

$$Q_3 = Q_2 = Q_1 = Q_0 = 0$$

② We are going to capture the entry of a 4 bit binary no. 1111 into register.

③ MSB applied first

④ Q_0 is connected to serial data input SIN. Output of FF-0 that is Q_0 is connected to the input of next flip-flop that is Q_1 . So

① Before application of clock signal let $Q_3 Q_2 Q_1 Q_0 = 0000$
apply MSB of bit to q_{in}
 $\therefore q_{in} = q_0 = 1$

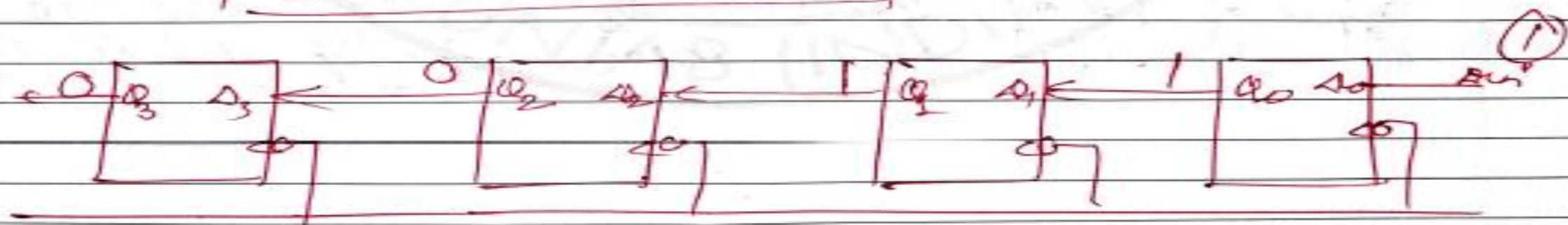
② On first falling edge of clock ff_0 is set &
stored bit in register.

$$[Q_3 Q_2 Q_1 Q_0 = 0001]$$

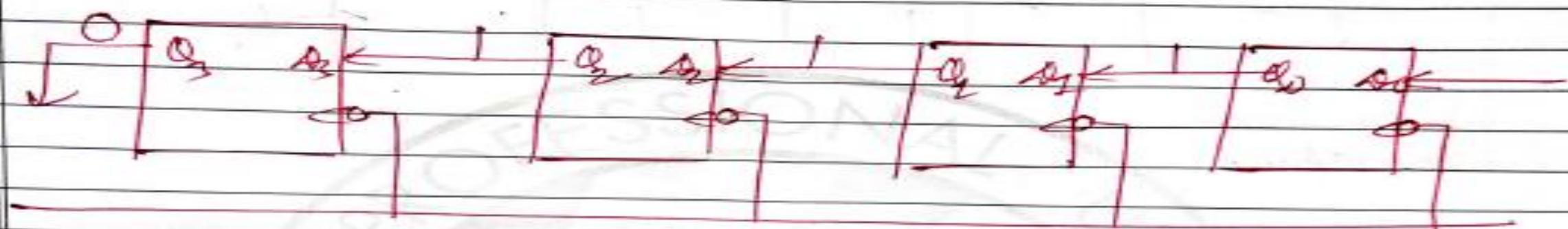


③ As soon as next negative edge of clock hits ff_1
then it let's 1 stored bit changes to

$$[Q_3 Q_2 Q_1 Q_0 = 0011]$$

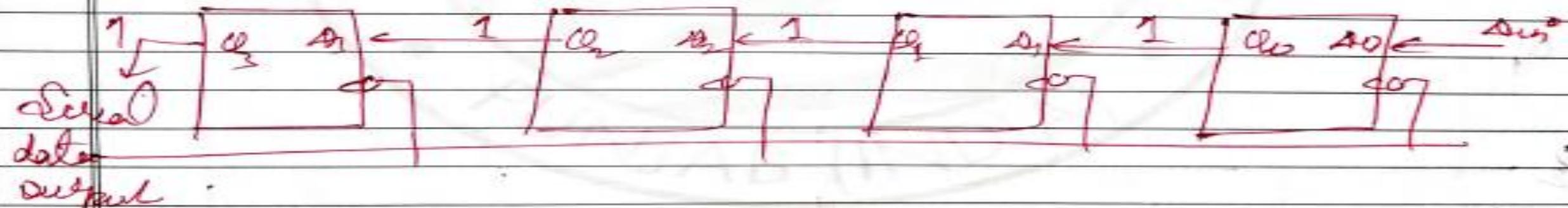


(4) As soon as third negative clock edge bits flip,
 FF-2 just get modified to
 $Q_3 Q_2 Q_1 Q_0 = 0111$



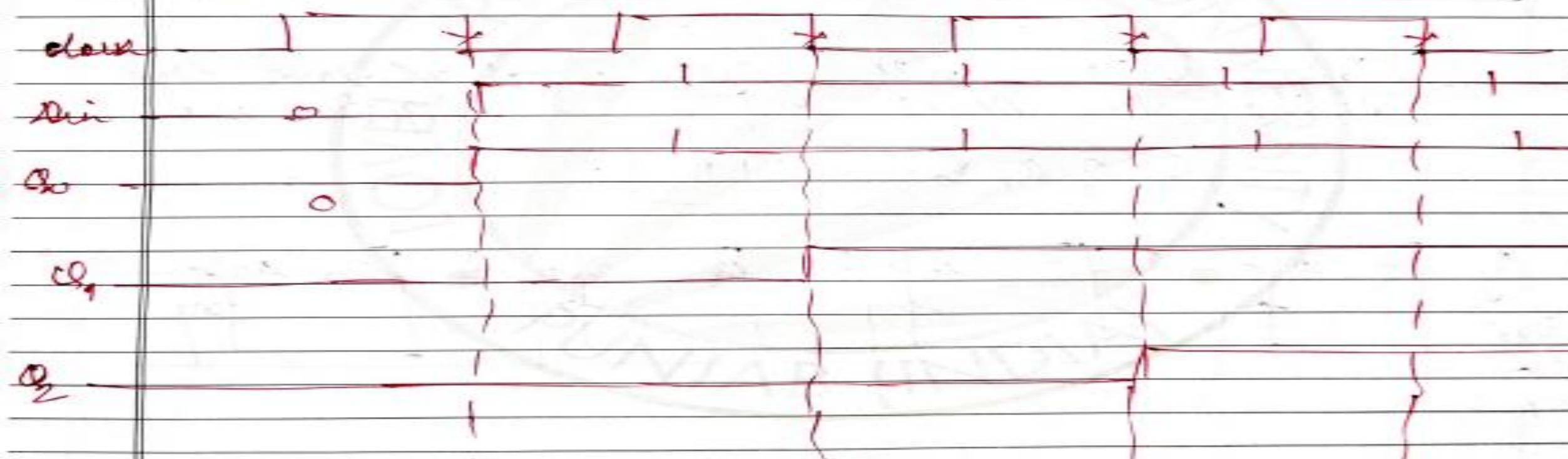
(5) Similarly $n=1$ with fourth negative clock edge
 arriving, the stored bits in register are

$$\boxed{Q_3 Q_2 Q_1 Q_0 = 1111}$$





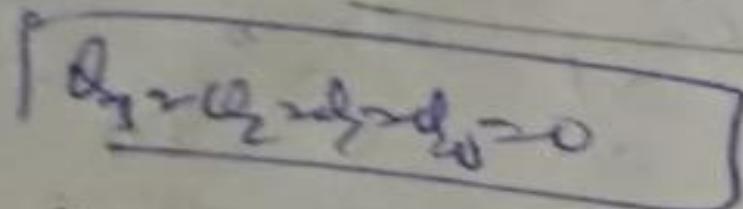
Intergame



Serial in serial out (Shift Right Mode)

Serial in

Serial out Shift Right mode



①

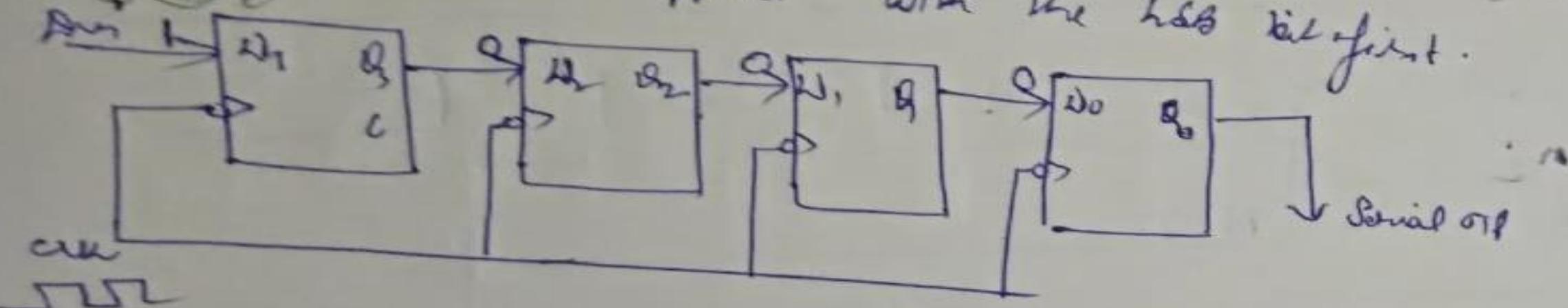
Explain entry of one bit binary no 111 into register.

②

One should be

affixed

with the less bit first.



Open ① before close $D_1 Q_2 Q_{10} = 2000$] & apply LBB of
the no. to be added to dis. $[dis = D_3 21]$

② Apply falling edge of close. ff. 3 is set & clear
this is negative in $D_1 Q_2 Q_{10} = 1000$

③ Disj.; All doors at most negative edge of close bits.
ff. 2 will set $\frac{1}{11.00}$ slow bits stays to
 $D_2 Q_2 Q_{10}$

④ Disj.; 3s neg. of close
 1110

③ shirt ; All deer at most negative sign of dark lines.
ff-2 will be slow tails stays to
beginning $\boxed{1100}$

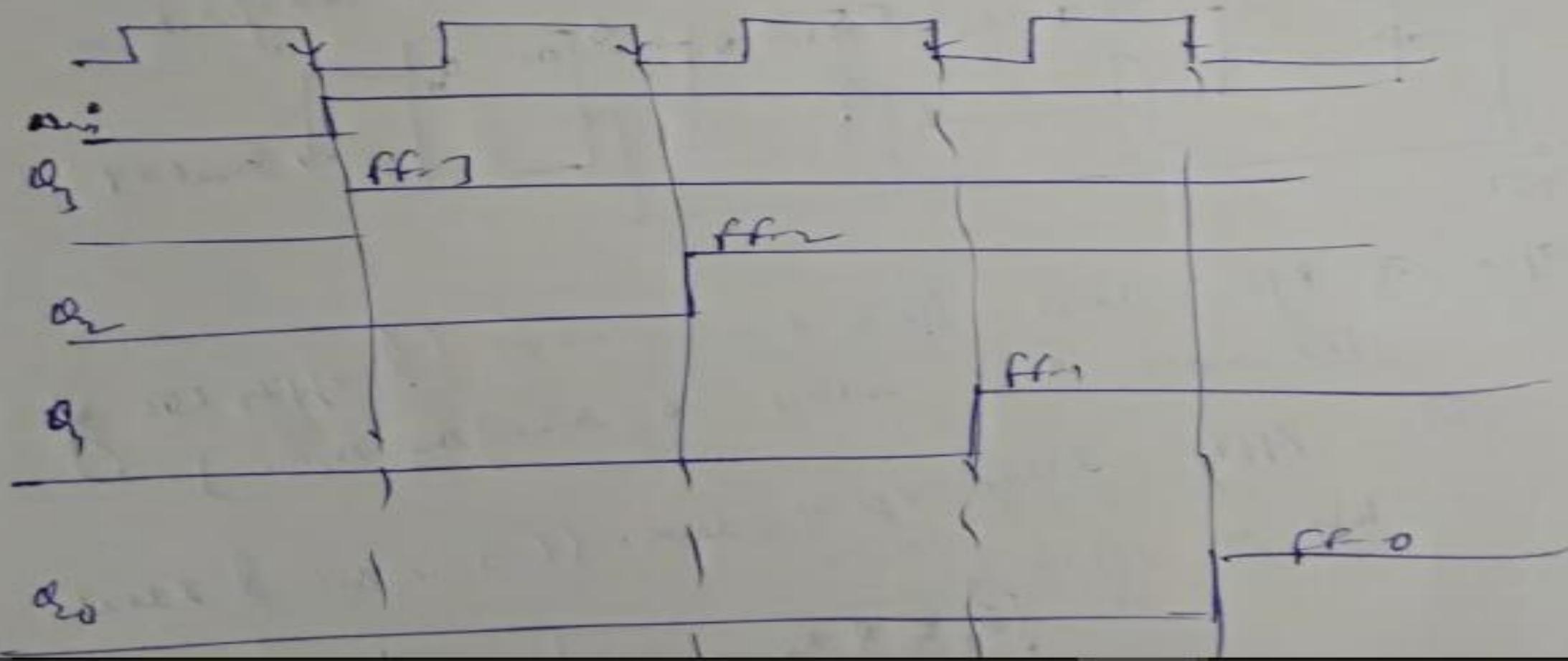
④ shirt ; In neg. of deer

$\boxed{1110}$

⑤ shirt in neg. open

$\boxed{1111}$

Time	1st	2nd	3rd	4th	5th	6th	7th
1	0	1	0	0	0	0	0
2	1	0	1	0	0	0	0
3	0	1	0	1	0	0	0
4	1	0	1	0	1	0	0
5	0	1	0	1	1	0	0
6	1	0	1	0	1	0	0
7	0	1	0	1	1	0	0

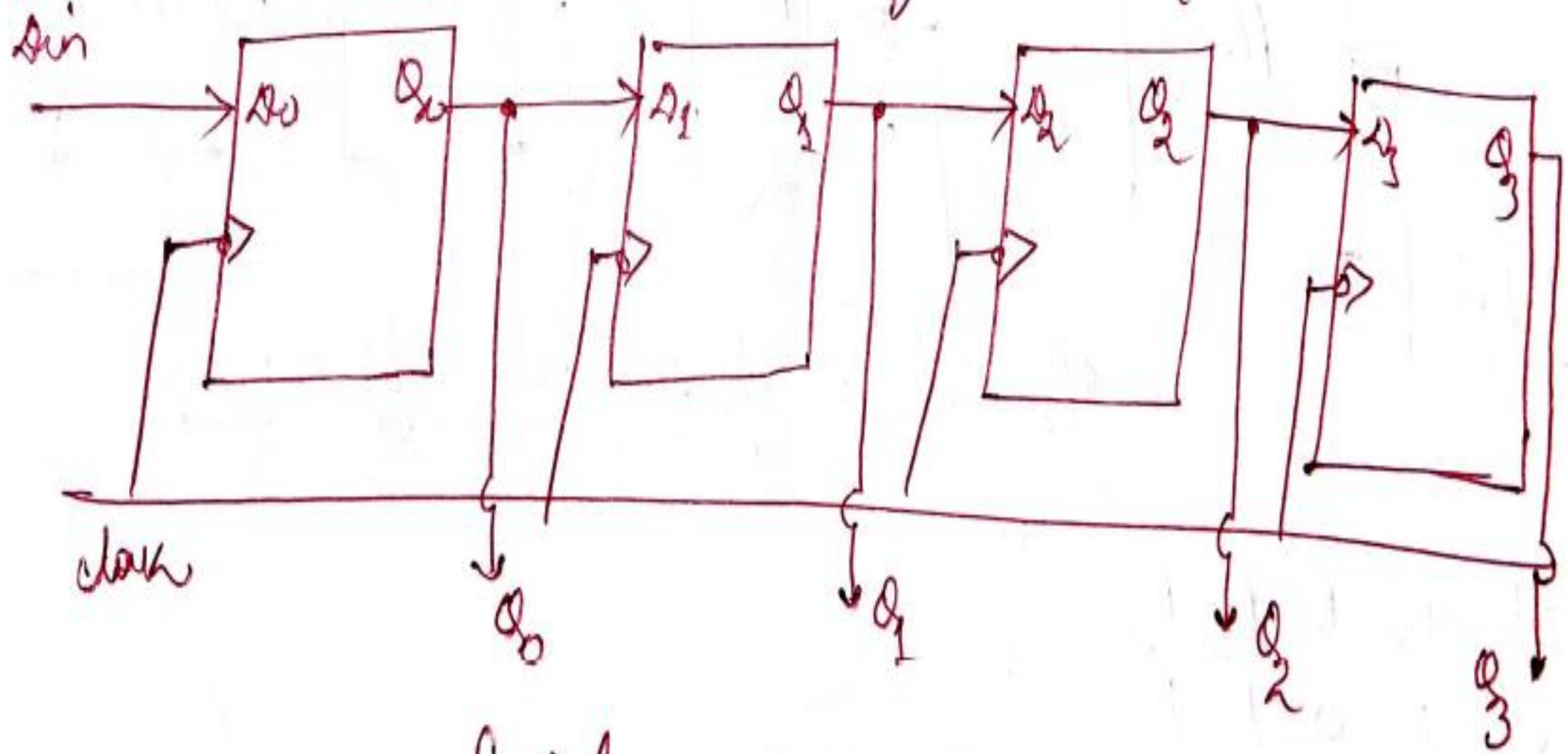


Serial in parallel out (SPO)

(1)

- ① In this operation the data is entered serially to taken out in parallel.
- ② It means first data is loaded bit by bit. Then the outputs are disabled as long as loading is taking place.

⑤ As soon as, loading is completed. All the flip-flops contain required data. Finally, the O/P's are enabled so that loaded data is made available over all outputs lines simultaneously [J1 means we load 1111, so at 4 clock pulses, all the flip-flop will have 1111 at that moment take output simultaneously from Q1 Q2 Q3 Q4.



Serial input parallel output mode

1. In digital logic, a counter is a device which _____

- a) Counts the number of outputs
- b) Stores the number of times a particular event or process has occurred
- c) Stores the number of times a clock pulse rises and falls
- d) Counts the number of inputs

1. In digital logic, a counter is a device which _____

- a) Counts the number of outputs
- b) Stores the number of times a particular event or process has occurred
- c) Stores the number of times a clock pulse rises and falls
- d) Counts the number of inputs

 View Answer

Answer: b

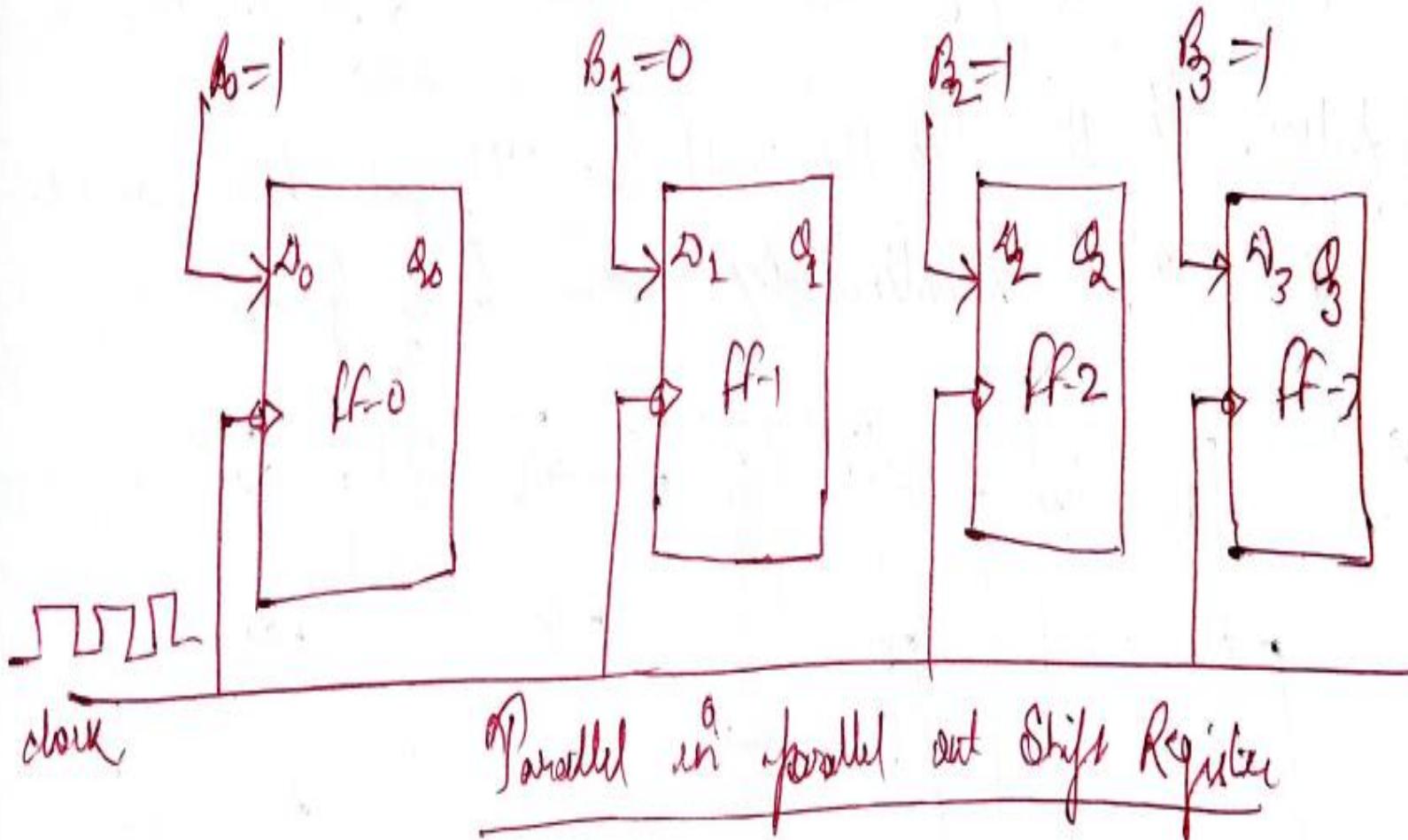
Explanation: In digital logic and computing, a counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal.

(2)

Parallel in Parallel out (PIP)

- ① The 4 bits binary inputs B_0, B_1, B_2, B_3 are applied to the data inputs D_0, D_1, D_2 & D_3 respectively to four flip flops.
- ② As soon as a negative clock edge is applied the input binary bits will be loaded into flip flops simultaneously.

③ The loaded bits will appear simultaneously to the output lines. Only one clock pulse is essential to load all the bits.



- ① if $B_0 \ B_1 \ B_2 \ B_3$
1 0 1 1
- ② At my edge of clock
- ③ output will appear as
 $Q_0 \ Q_1 \ Q_2 \ Q_3$
1 0 1 1

3. What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?

- a) 0 to 2^n
- b) 0 to $2^n + 1$
- c) 0 to $2^n - 1$
- d) 0 to $2^{n+1/2}$

3. What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?

- a) 0 to 2^n
- b) 0 to $2^n + 1$
- c) 0 to $2^n - 1$
- d) 0 to $2^{n+1/2}$

 View Answer

Answer: c

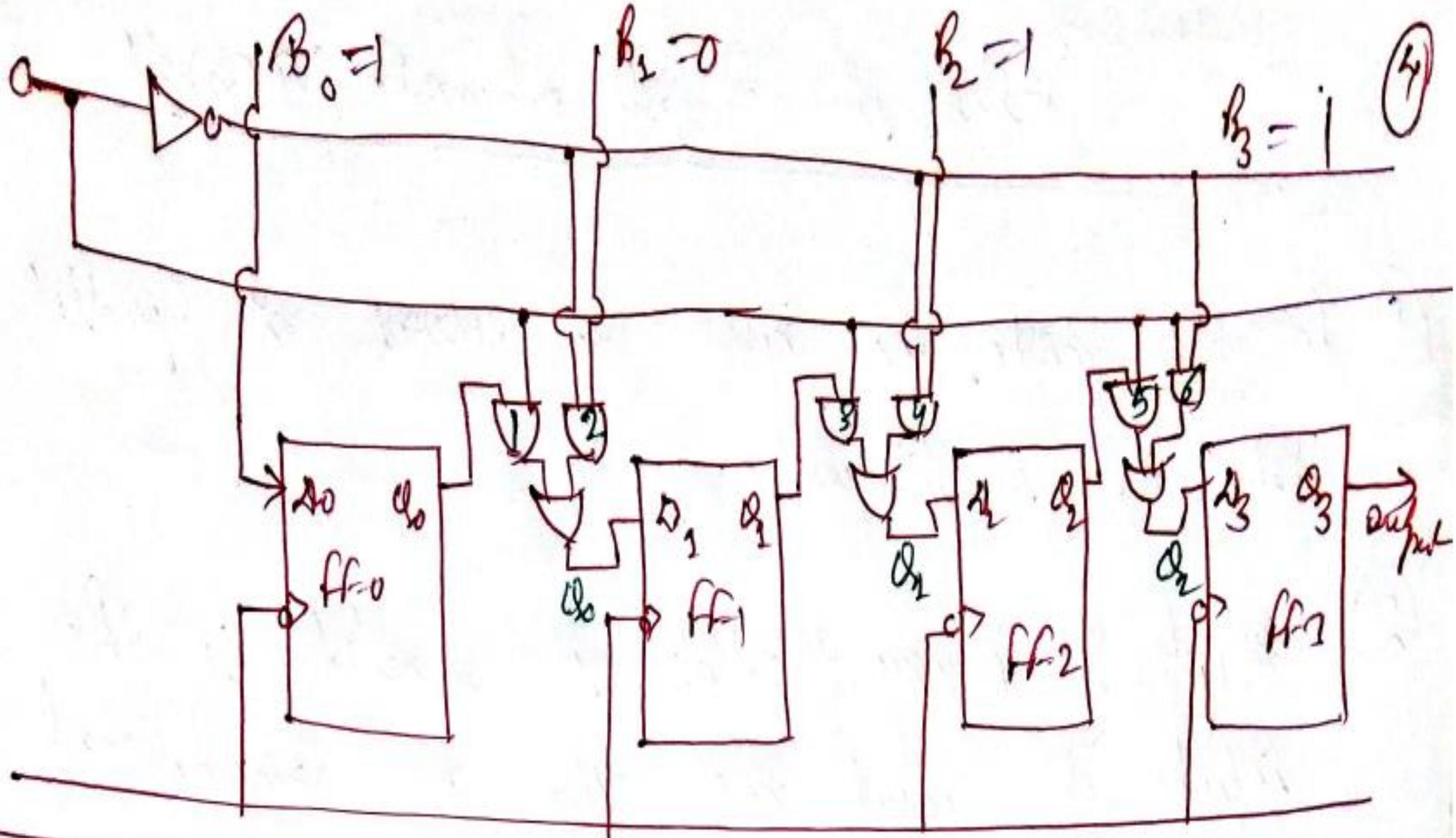
Explanation: The maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops is 0 to $2^n - 1$. For say, there is a 2-bit counter, then it will count till $2^2 - 1 = 3$. Thus, it will count from 0 to 3.

Parallel in Serial out mode (PISO) # . ③

- ① In this mode, the bits are entered in parallel that is simultaneously.
- ② Output of previous flip flop is connected to the input of next one via a combinational circuit.

③ The binary input B_0, B_1, B_2, B_3 is applied through some combinational circuit.

④ There are two modes in which the circuit can work namely Load / Shift mode.



load mode

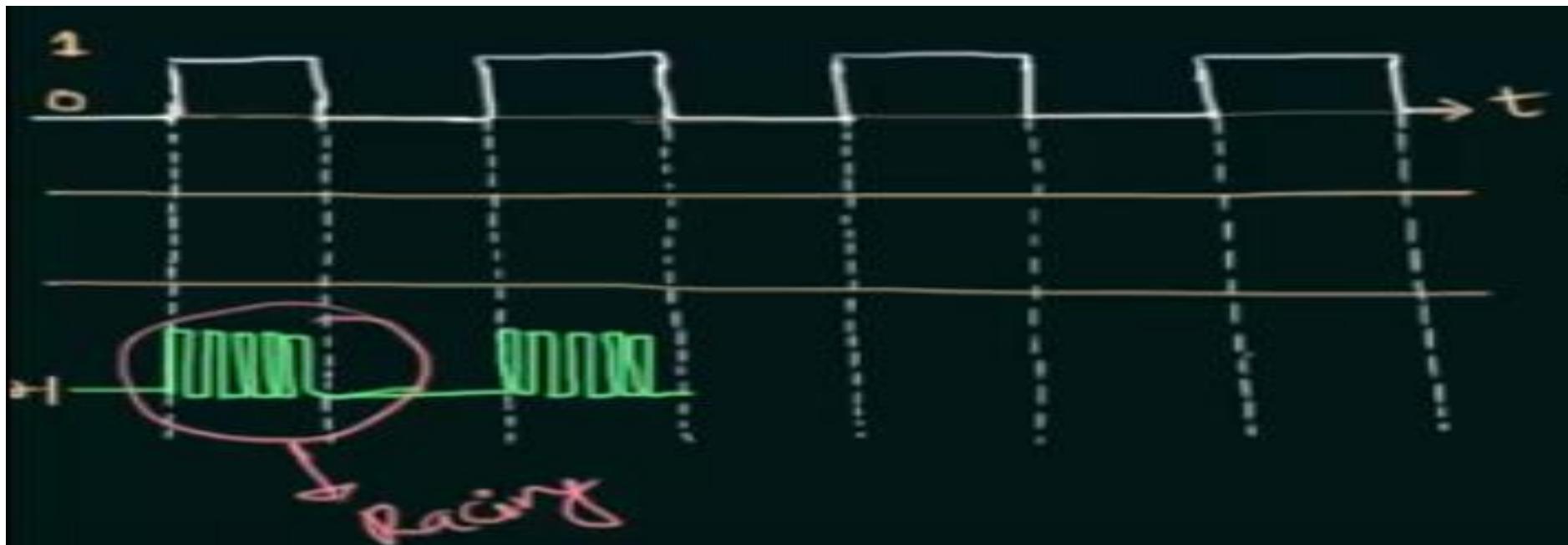
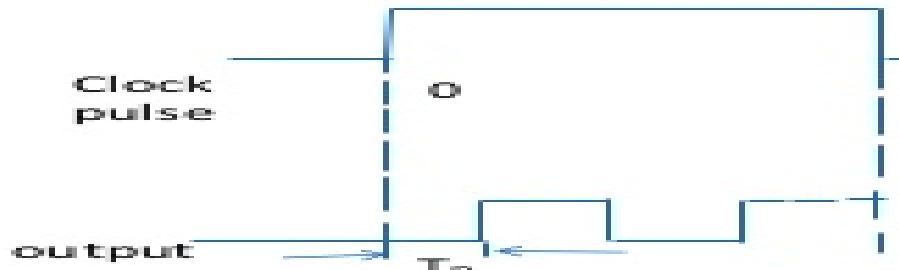
- A) When shift/load line is low (0). AND gates 2, 4, 6 are active. This will pass B_1, B_2, B_3 bits to the corresponding flip flop.
- B) On low going edge of clock, The B, B_1, B_2, B_3 will be loaded into flip flop.
- C) Thus parallel loading takes place
- | | | | |
|-------|-------|-------|-------|
| Q_0 | Q_1 | Q_2 | Q_3 |
| 1 | 1 | 1 | , |

Shift mode

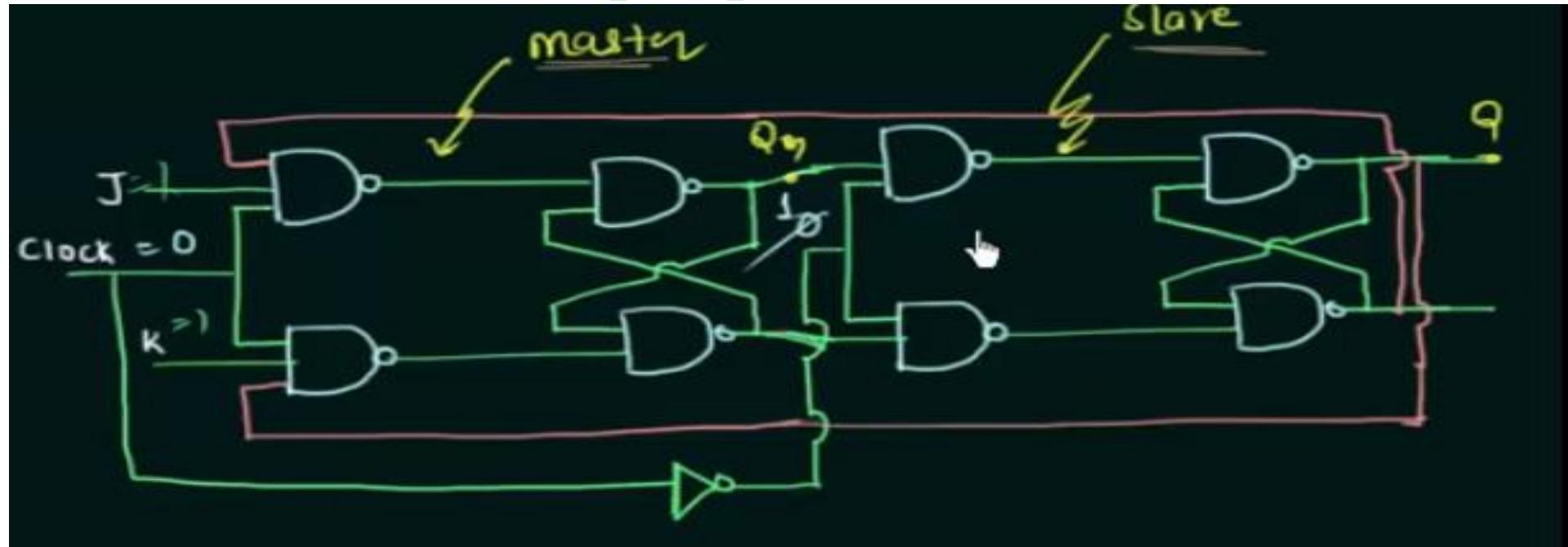
- ① When shift load is high (1). The and gate 2, 4, 6 become inactive. Hence parallel loading of data become impossible.
- ② Now AND gates 1, 3, 5 become active. Therefore
- shifting of data from left to right bit by bit on the application of clock pulses.
- ③ Shift from 1010 $\xrightarrow{\text{out}}$
to 1010 $\xrightarrow{\text{neg edge}}$
 $--10$ $\xrightarrow{\text{neg}}$
 $--0$ $\xrightarrow{\text{neg}}$

Race around condition

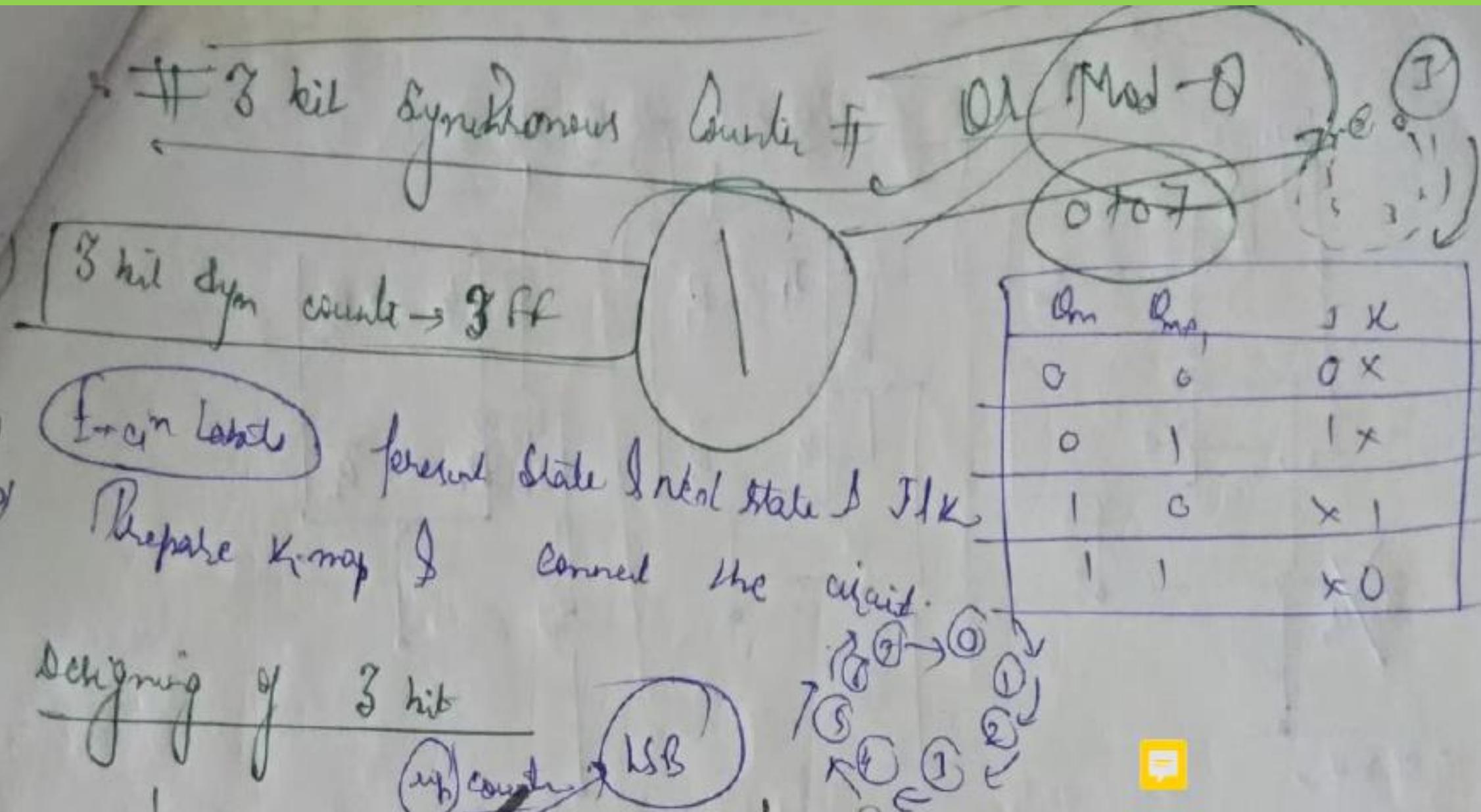
- It occurs when both inputs JK are 1 and when the state of the flip flop keeps on changing from 0 to 1, 1 to 0 and 0 to 1 so on.
- This phenomenon is called as race around condition.



Master-Slave JK flip flop

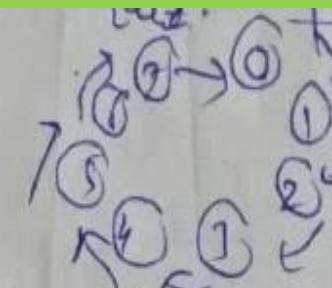
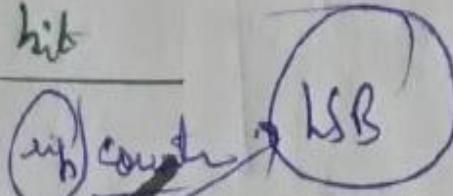


3 bit Synchronous-Up-Counter



3 bit Synchronous-Up-Counter

Design of 3 bit



R_m	R_{m_1}	$J K$
0	0	0 X
0	1	1 X
1	0	X 1
1	1	X 0

Sequence

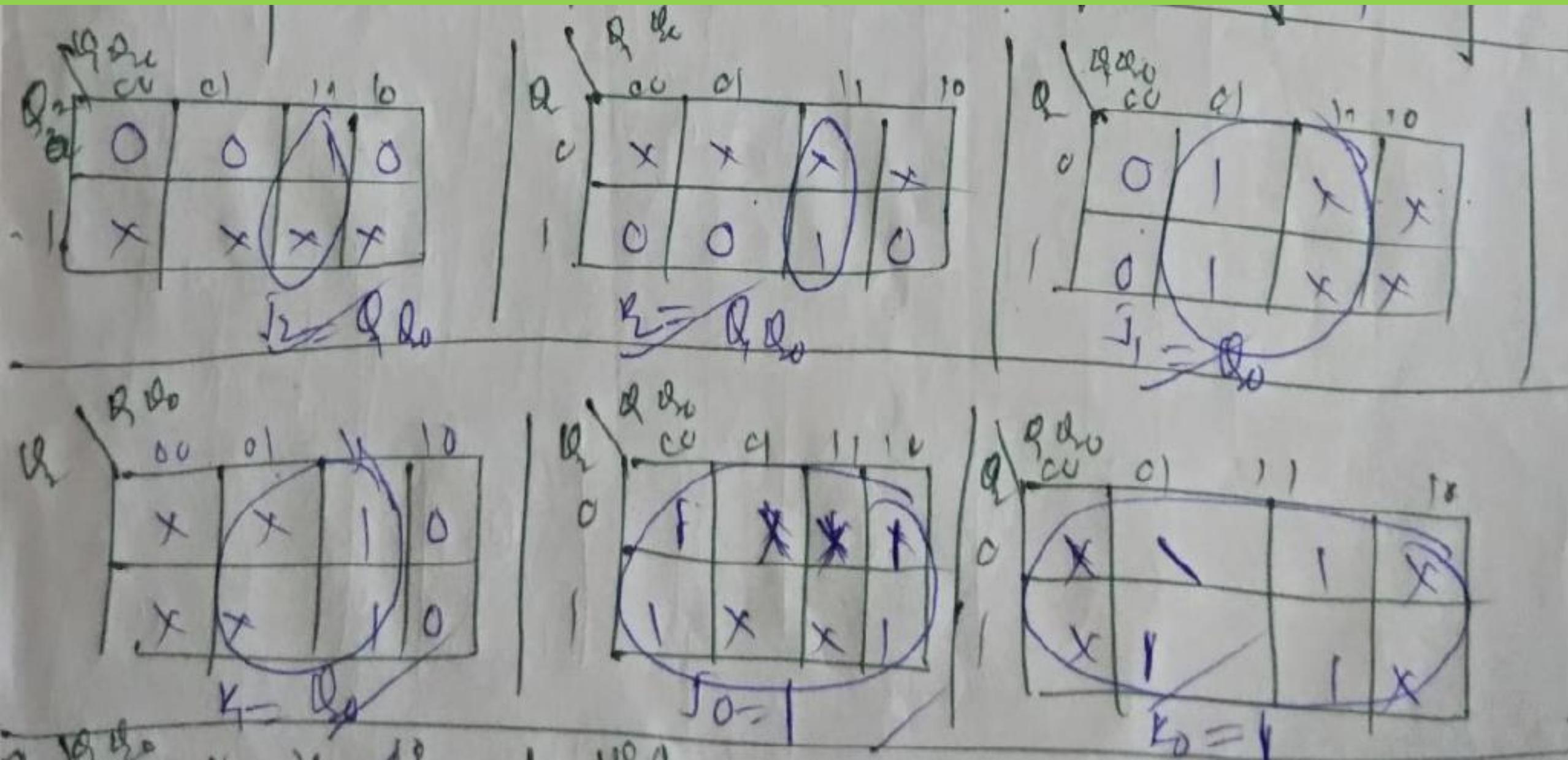
Burst State

New State

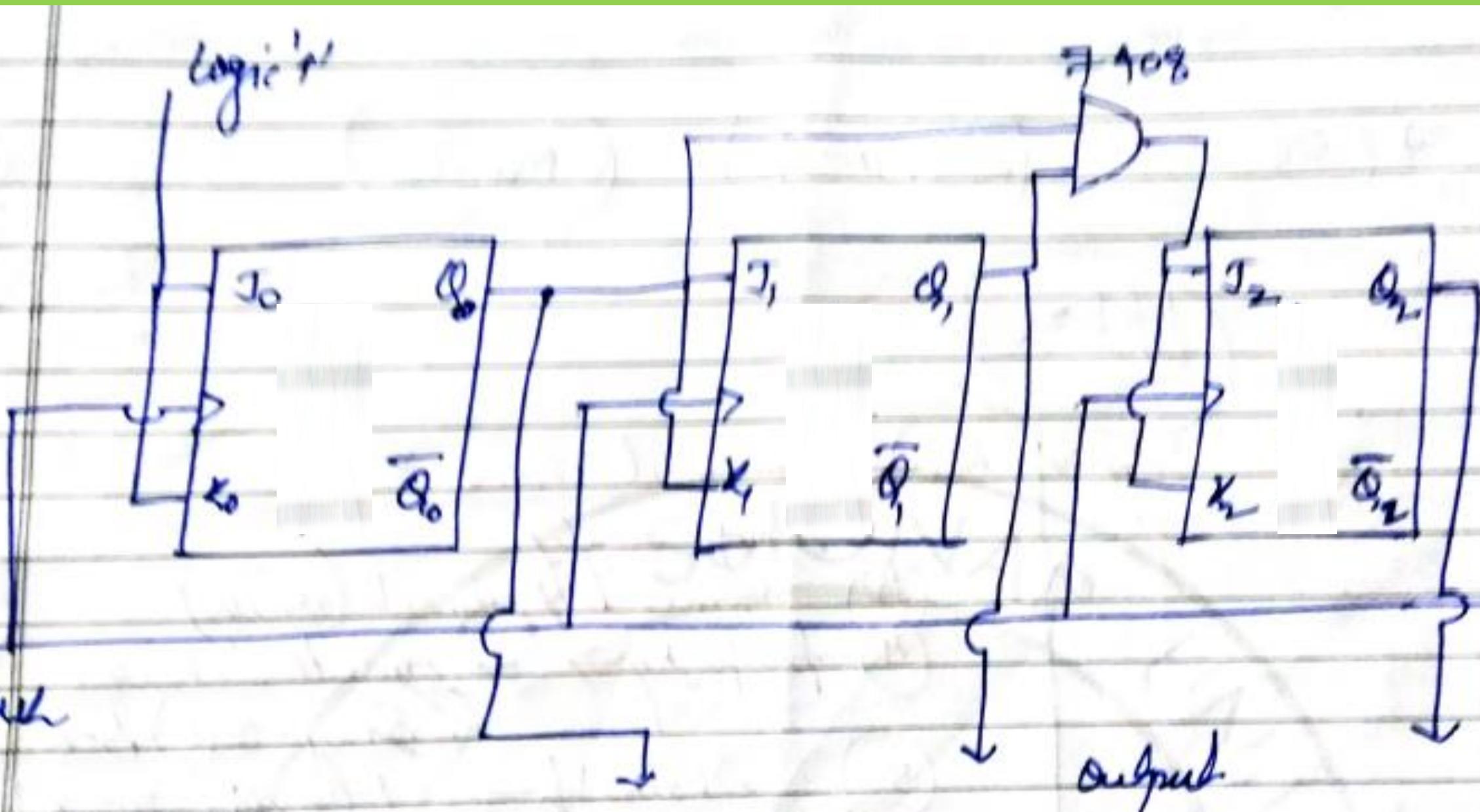
flip flop

	Q_0	Q_1	Q_2	Q_{m_1}	Q_{m_2}	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	X	0	X	1	X
1	0	0	1	0	0	0	X	0	X	1	X
2	0	1	0	0	1	0	X	1	X	X	1
3	0	1	1	0	0	1	X	X	0	1	X
4	1	0	0	0	0	1	X	X	1	X	1
5	1	0	1	0	1	X	0	X	1	X	1
6	1	0	1	1	0	X	0	0	X	1	X
7	1	1	0	1	1	X	0	1	X	X	1
	1	1	1	0	0	X	1	X	0	1	X

3 bit Synchronous-Up-Counter



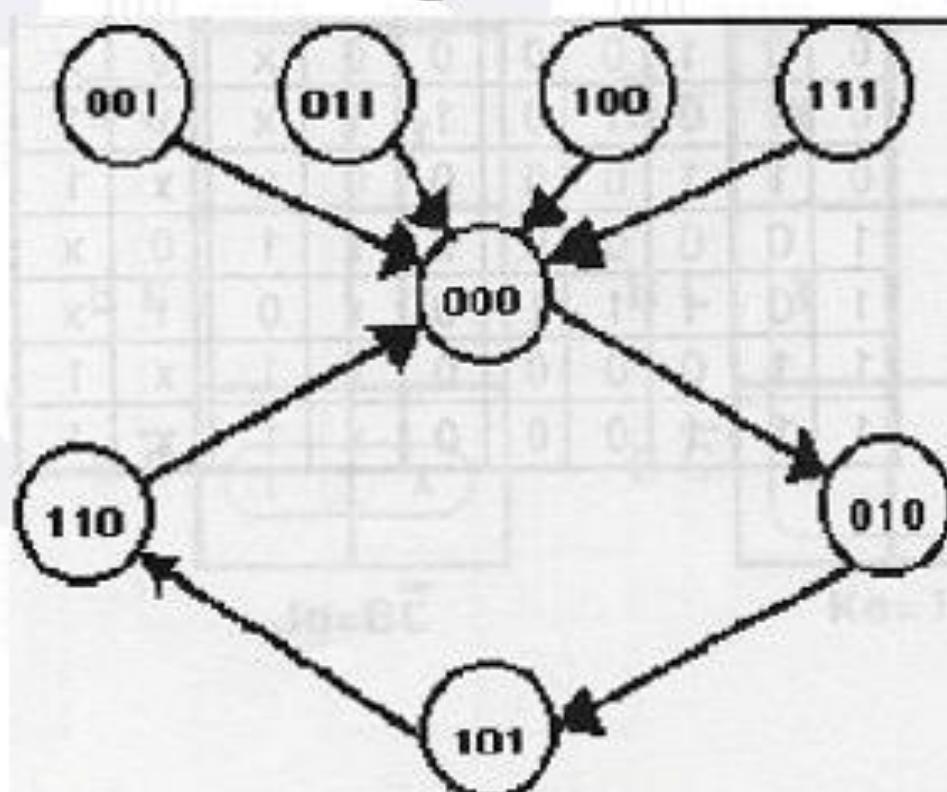
3 bit Synchronous-Up-Counter





? Design a JK synchronous counter that has the following sequence: 000, 010, 101, 110 and repeat. The undesired states 001, 011, 100 and 111 must always go to 000 on the next clock pulse.

STEP -1 :State Transition Diagram



Synchronous Counter Design / Example (2)cont.

STEP- 2 : Table to list PRESENT and NEXT status

PRESENT State			NEXT State		
C	B	A	C	B	A
0	0	0	0	1	0
0	0	1	0	0	0
0	1	0	1	0	1
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	0	0	0

Synchronous Counter Design / Example (2)cont.

STEP- 3 : Table indicate the Level required at each J and K inputs in order to produce the transition to the NEXT

Present State			Next State								
C	B	A	C	B	A	Jc	Kc	Jb	Kb	Ja	Ka
0	0	0	0	1	0	0	x	1	x	0	x
0	0	1	0	0	0	0	x	0	x	x	1
0	1	0	1	0	1	1	x	x	1	1	x
0	1	1	0	0	0	0	x	x	1	x	1
1	0	0	0	0	0	x	1	0	x	0	x
1	0	1	1	1	0	x	0	1	x	x	1
1	1	0	0	0	0	x	1	x	1	0	x
1	1	1	0	0	0	x	1	x	1	x	1

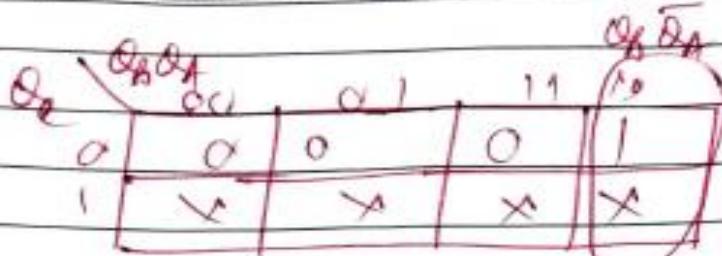
Q _n	Q _{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Synchronous Counter Design / Example (2)cont.

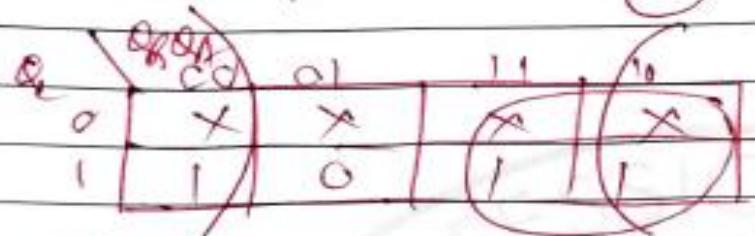
STEP- 4 :Design the logic circuits to generate the levels required at each J and K inputs

*Present
State*

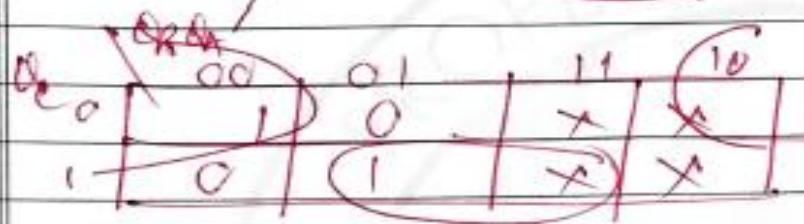
C	B	A	Jc	Kc	Jb	Kb	Ja	Ka
0	0	0	0	x	1	x	0	x
0	0	1	0	x	0	x	x	1
0	1	0	1	x	x	1	1	x
0	1	1	0	x	x	1	x	1
1	0	0	x	1	0	x	0	x
1	0	1	x	0	1	x	x	1
1	1	0	x	1	x	1	0	x
1	1	1	x	1	x	1	x	1



$$F_C = \overline{Q_A} Q_B$$

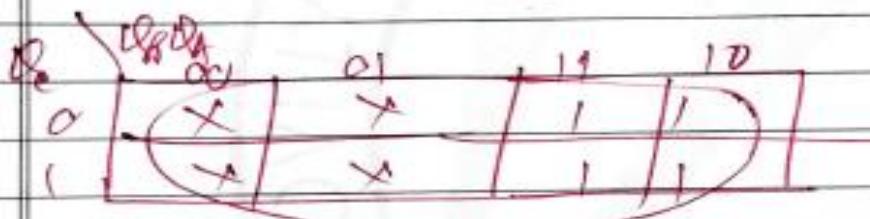


$$K_C = Q_B + \overline{Q}_A$$

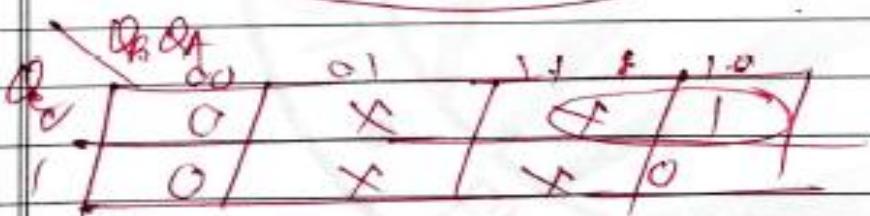


$$J_B = Q_C (Q_A + \overline{Q}_B \overline{Q}_A)$$

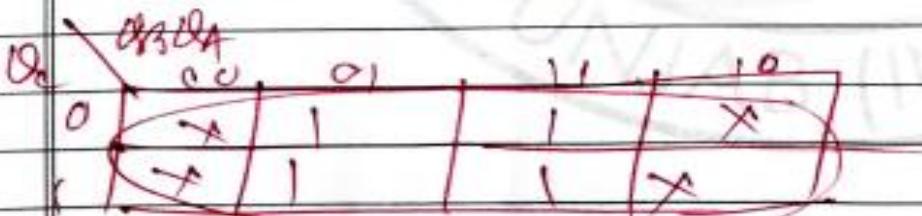
$$J_D = Q_1 Q_2$$



$$K_B = 1$$



$$T_B = \overline{Q}_2 \bullet Q_B$$



$$K_A = 1$$

EXAMINER'S SHEET

Date of Test _____

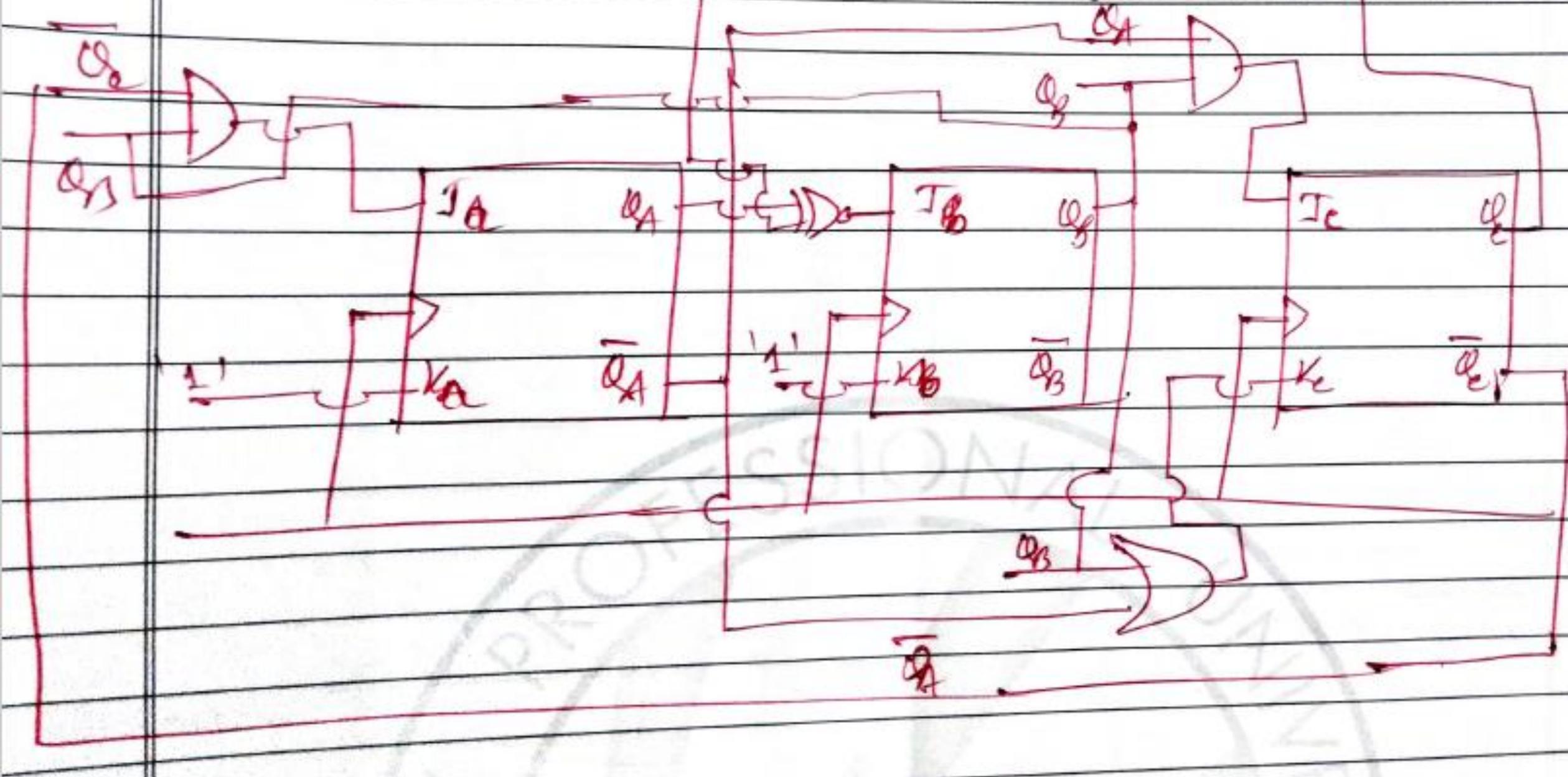
Roll No. _____

Reg. No. _____

Course Code _____

Section _____

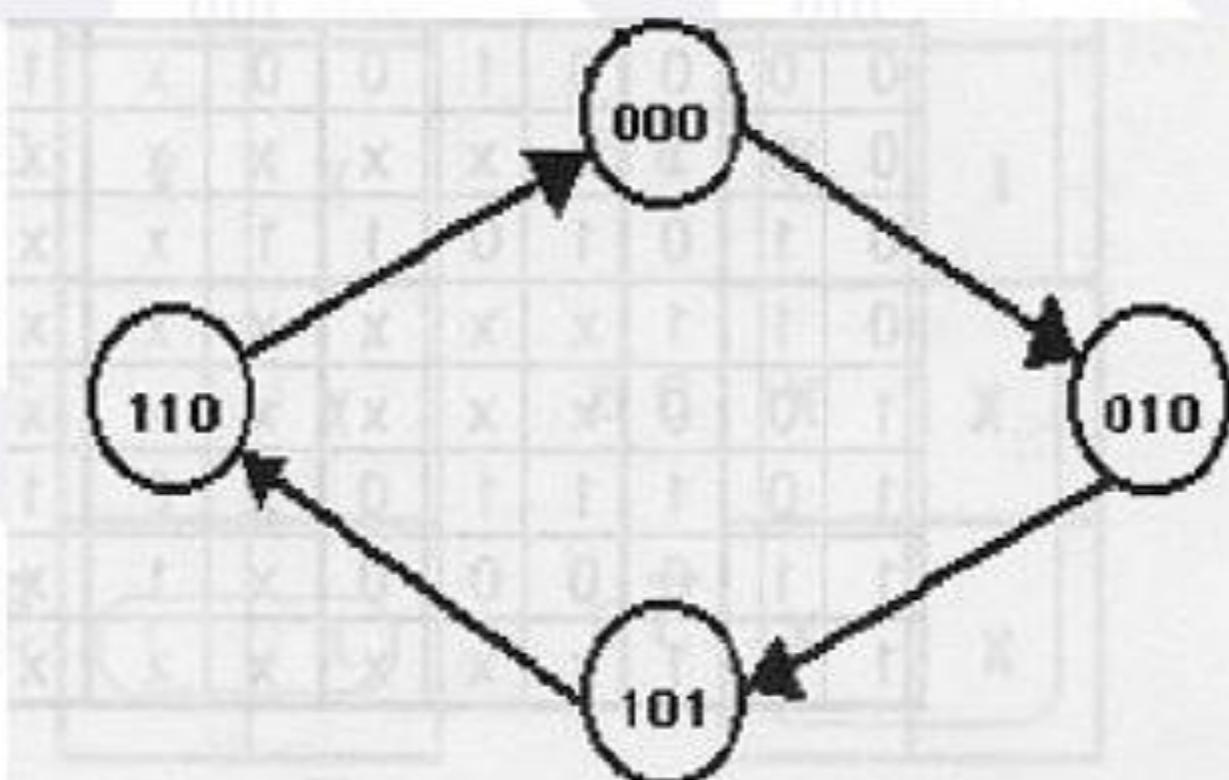
Test No. _____





Design a JK synchronous counter that has the following sequence: 000, 010, 101, 110 and repeat. For undesired states their NEXT states can be DON'T CARES.

STEP -1 : State Transition Diagram



Synchronous Counter Design / Example (3)cont.

STEP- 2 : Table to list PRESENT and NEXT status

PRESENT State			NEXT State		
C	B	A	C	B	A
0	0	0	0	1	0
0	0	1	x	x	x
0	1	0	1	0	1
0	1	1	x	x	x
1	0	0	x	x	x
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	x	x	x

Synchronous Counter Design / Example (3)cont.

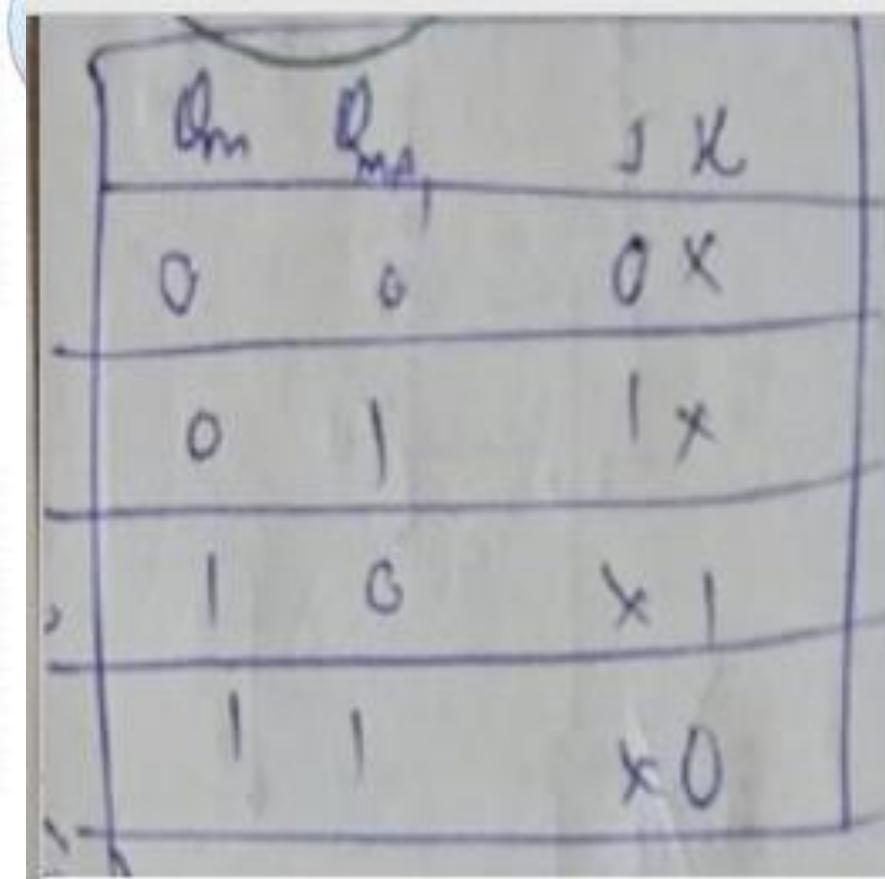
STEP- 3 : Table indicate the Level required at each J and K inputs in order to produce the transition to the NEXT

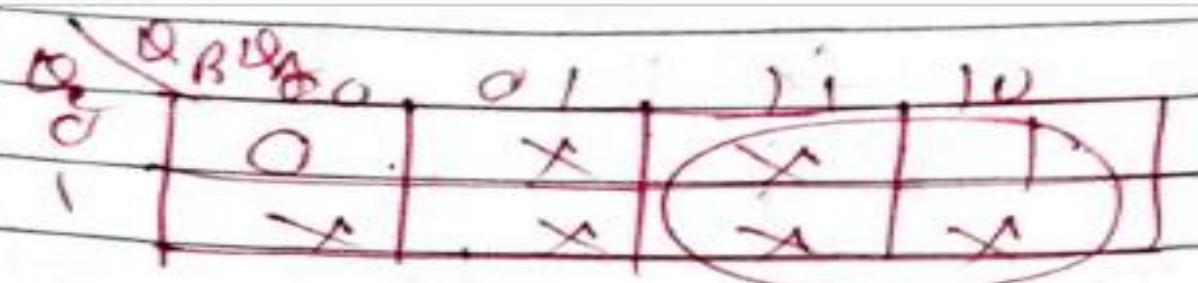
Present State			Next State														
C	B	A	C	B	A	Jc	Kc	Jb	Kb	Ja	Ka						
0	0	0	0	1	0	0	x	1	x	0	x						
0	0	1	x	x	x	x	x	x	x	x	x						
0	1	0	1	0	1	1	x	x	1	1	x						
0	1	1	x	x	x	x	x	x	x	x	x						
1	0	0	x	x	x	x	x	x	x	x	x						
1	0	1	1	1	0	x	0	1	x	x	1						
1	1	0	0	0	0	x	1	x	1	0	x						
1	1	1	x	x	x	x	x	x	x	x	x						

Synchronous Counter Design / Example (3)cont.

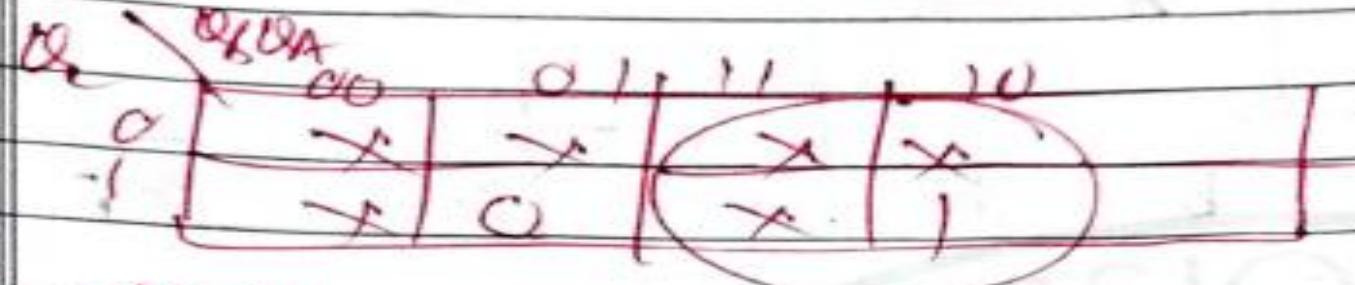
STEP- 4 :Design the logic circuits to generate the levels required at each J and K inputs

Present State									
C	B	A	Jc	Kc	Jb	Kb	Ja	Ka	
0	0	0	0	x	1	x	0	x	
0	0	1	x	x*	x	x	x	x	
0	1	0	1	x	x	1	1	x	
0	1	1	x	x	x	x	x	x	
1	0	0	x	x	x	x	x	x	
1	0	1	x	0	1	x	x	1	
1	1	0	x	1	x	1	0	x	
1	1	1	x	x	x	x	x	x	

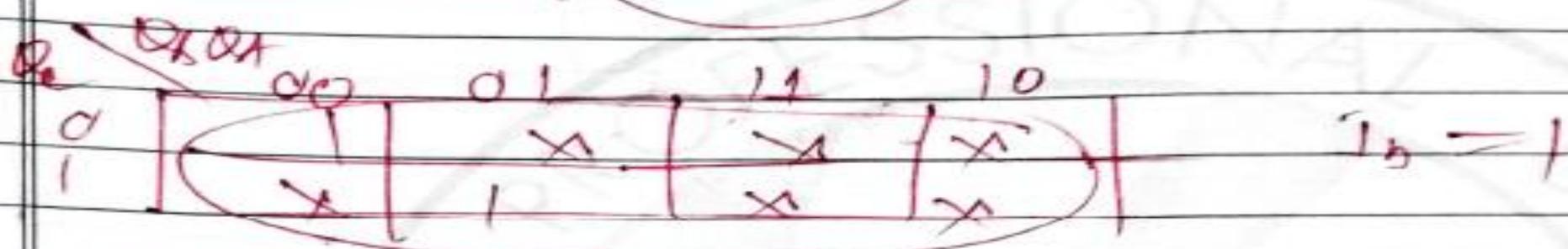




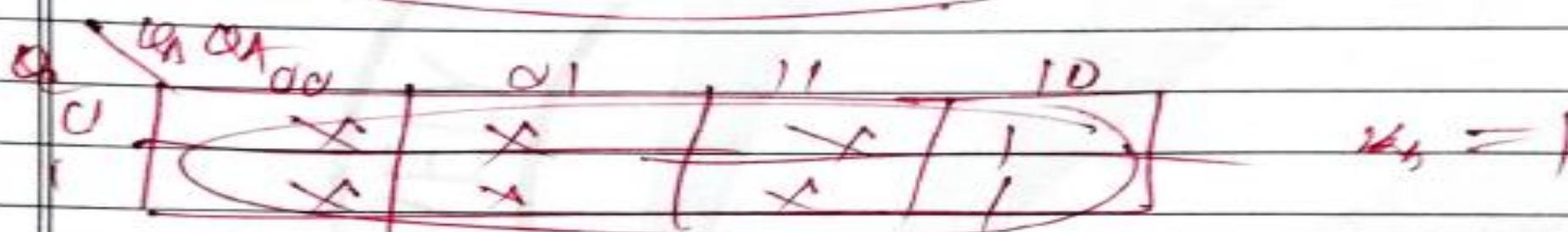
$$T_c = \frac{Q_2}{g_2}$$



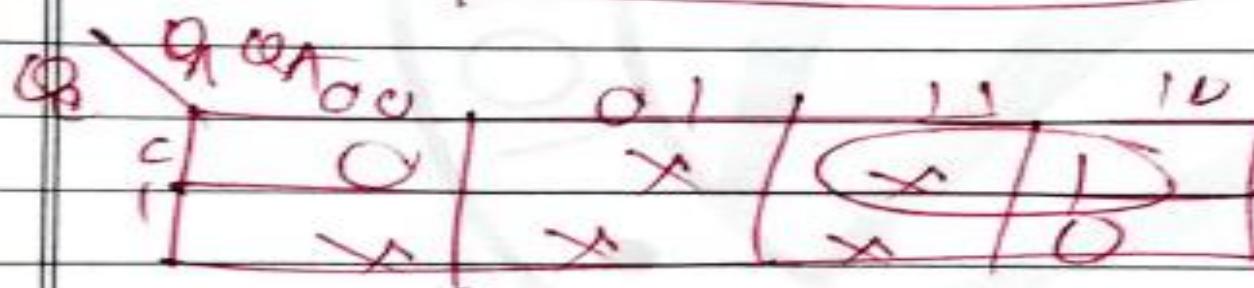
$$K_c = \frac{Q_2}{g_2}$$



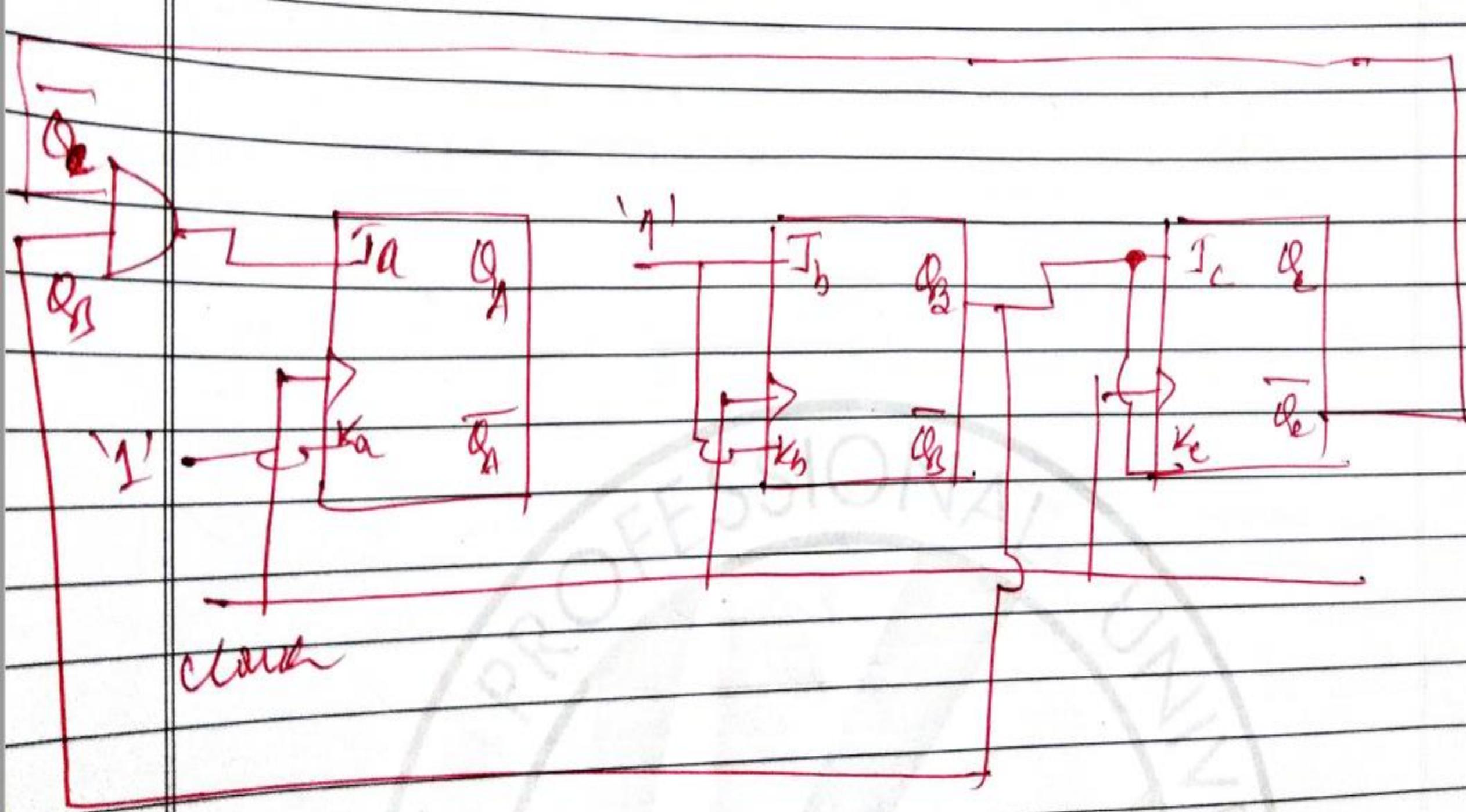
$$T_b = 1$$



$$K_b = 1$$



$$K_T = \overline{\alpha_c} \cdot \overline{\alpha_b}$$



~~11~~ 3 bit Synchronous Up/Down Counter 11

Present State	Next State	Sig. Fig. S ₁₂
Q ₂ Q ₁ Q ₀	Q _{2n+1} Q _{n+1} Q ₀	1
0 0	0 0	0
0 1	1 0	1
1 1	0 0	0

Mod M
Up Down

Prev State
 Q_2 Q_B Q_A

Next State
 Q_{2+1} Q_B+ Q_{A+1}

T_2 T_B T_A
 P_{2B} P_B P_A

0	0 0	0
0	0 0	1
0	0 1	0
0	0 1	1
0	1 0	0
0	1 0	1
0	1 1	0
1	0 0 0	
1	0 0 1	
1	0 1 0	
1	0 1 1	
1	1 0 0	
1	1 0 1	
1	1 1 0	
1	1 1 1	

0 0 1	0 0 0
0 1 0	0 0 1
0 1 1	0 1 0
1 0 0	0 1 1
1 0 1	1 0 0
1 1 0	1 0 1
1 1 1	1 1 0

0 0 1	0 0 1	1
0 1 0	0 1 1	1
0 1 1	1 0 0	1
1 0 0	1 0 1	1
1 0 1	1 1 0	1
1 1 0	1 1 1	1
1 1 1	0 0 0	1

for Down Counter

	θ_1	θ_2	θ_3	θ_4
θ_1	0	0	1	0
θ_2	0	0	1	0
θ_3	1	0	0	0
θ_4	0	0	0	0

$$T_C = \bar{m} \theta_3 \theta_4 + M \bar{\theta}_3 \bar{\theta}_4$$

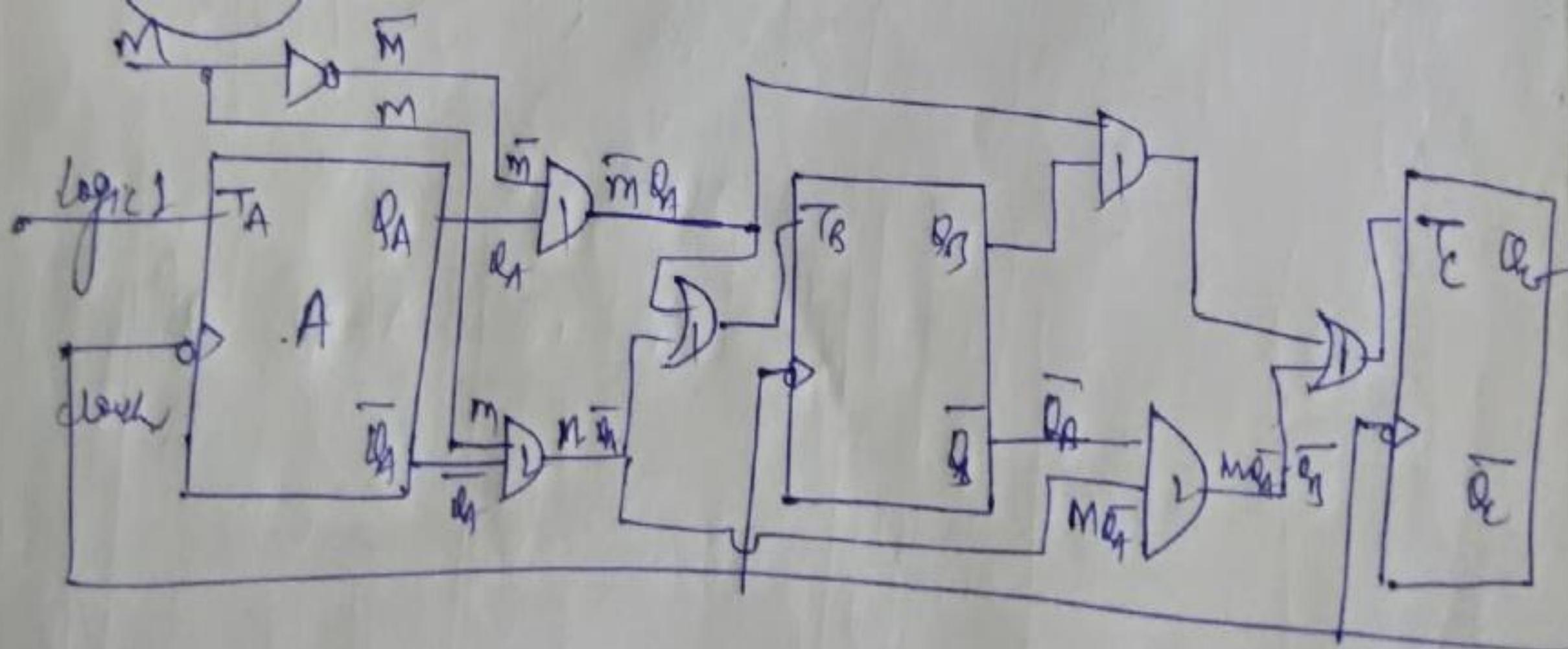
	θ_1	θ_2	θ_3	θ_4
θ_1	1	1	1	1
θ_2	1	1	1	1
θ_3	1	1	1	1
θ_4	1	1	1	1

$$T_A = 1$$

	θ_1	θ_2	θ_3	θ_4
θ_1	0	1	1	0
θ_2	0	1	1	0
θ_3	1	0	0	1
θ_4	0	0	0	1

$$T_B = \bar{m} \theta_1 + M \bar{\theta}_4 \Rightarrow m \theta_1$$

$$\theta_1 \theta_2 \theta_4 \rightarrow 4n$$



Conversion of Flip-Flops(SR Flip Flop to D Flip Flop)

SR FLIP FLOP==EXCITATION TABLE ; D FLIP FLOP==CHARACTERISTIC TABLE

Characteristic table of D

①

Q_{in}	D	Next Q_{out}	S	R
0 ✓	0	0	0	0
0 ✓	1	1	0	X
1 ✓	0	0	1	0
✓	1	1	0	1

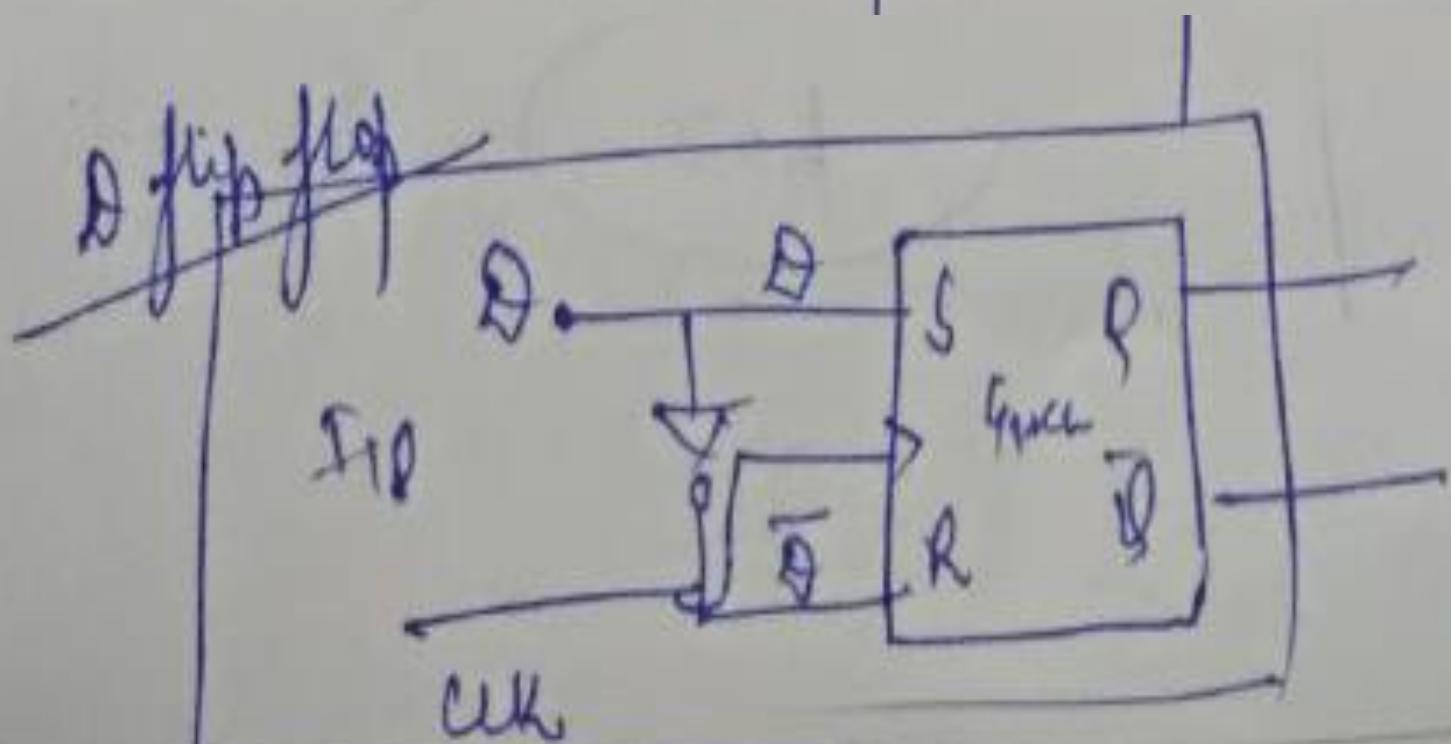
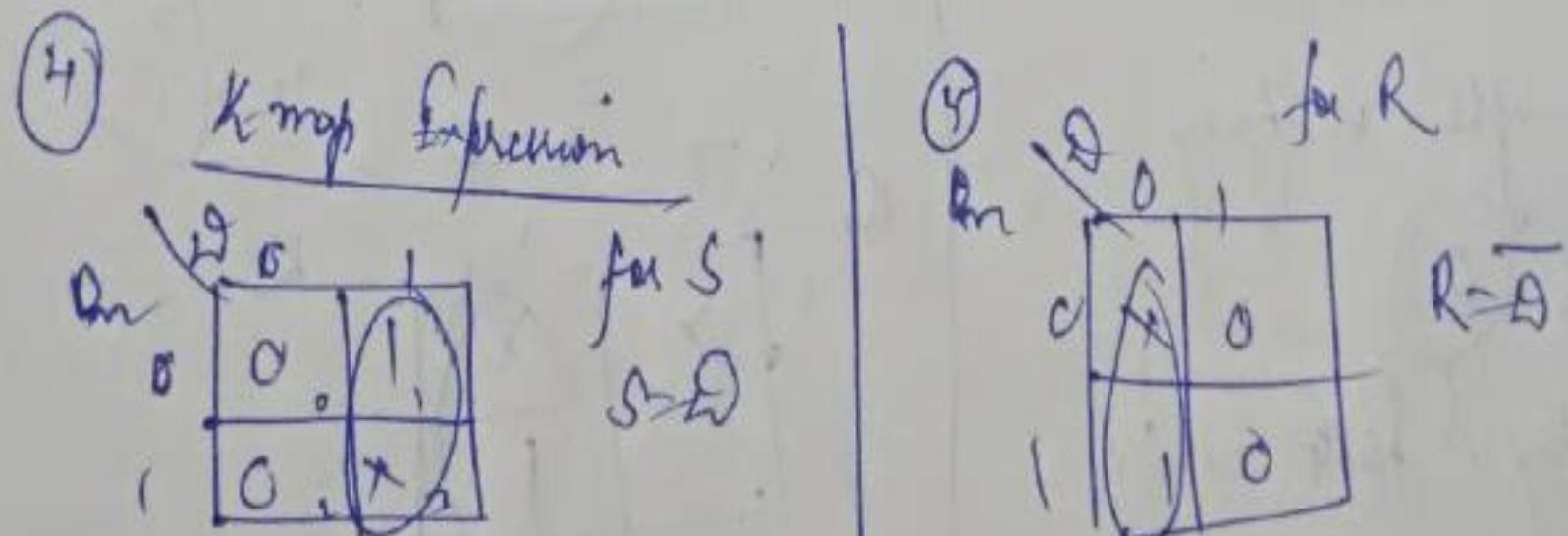
Excitation table of SR

②

Q_{in}	Q_{in+}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Characteristics table of D

D	Q_m	N	S	R
0	0	0	0	1
0	1	1	1	x
1	0	0	0	0
1	1	1	1	0



Conversion of Flip-Flops(D Flip Flop to T Flip Flop)

D FLIP FLOP==EXCITATION TABLE ; T FLIP FLOP==CHARACTERISTIC TABLE

Characteristic of T FF

Q_{in}	T	Q_{out}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

Excitation table of D FF

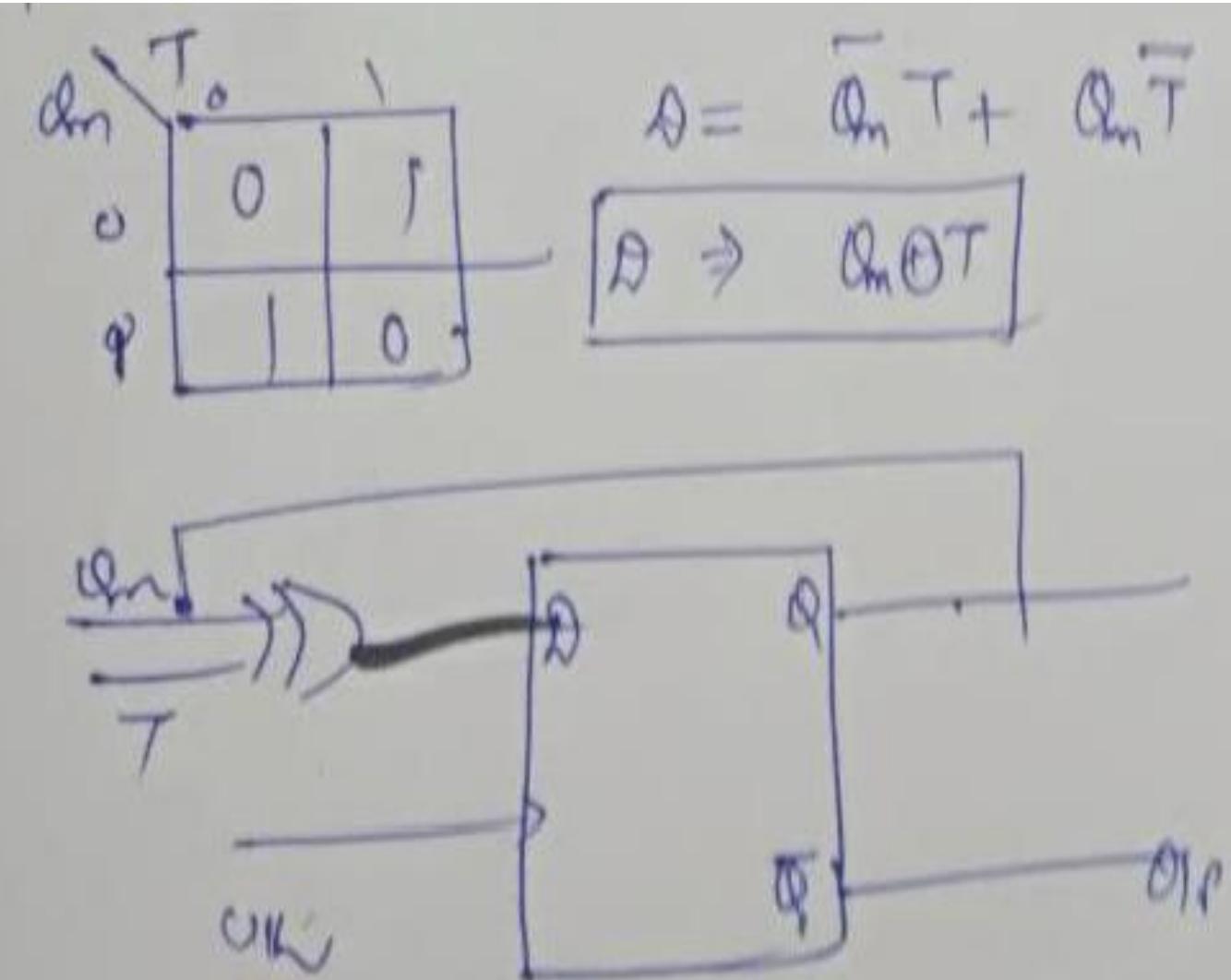
Q_{in}	Q_{in1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Conversion of Flip-Flops(D Flip Flop to T Flip Flop)

D FLIP FLOP==EXCITATION TABLE ; T FLIP FLOP==CHARACTERISTIC TABLE

Characteristic of TAF

D_m	T	Q_{m+1}	D
0	0	0	0
1	1	1	1
0	1	1	0



Conversion of Flip-Flops(SR Flip Flop to JK Flip Flop)

SR FLIP FLOP==EXCITATION TABLE ; J-K FLIP FLOP==CHARACTERISTIC TABLE

② Character for JK

Q_{n+1}	J	K	Q_n	S	R
0	0	0	0	0	X
0	0	1	0	0	X
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	1	X	0
1	0	1	0	0	1
1	1	0	1	X	0
1	1	1	0	0	1

③ Excitation table for Analysis of SR

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Conversion of Flip-Flops(SR Flip Flop to JK Flip Flop)

SR FLIP FLOP==EXCITATION TABLE ; J-K FLIP FLOP==CHARACTERISTIC TABLE

② Character for JK

Q_{n+1}	J	K	Q_n	S	R
0	0	0	0	0	X
0	0	1	0	0	X
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	1	X	0
1	0	1	0	0	1
1	1	0	1	X	0
1	1	1	0	0	1

③ Excitation table for Analysis of SR

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Conversion of Flip-Flops(SR Flip Flop to JK Flip Flop)

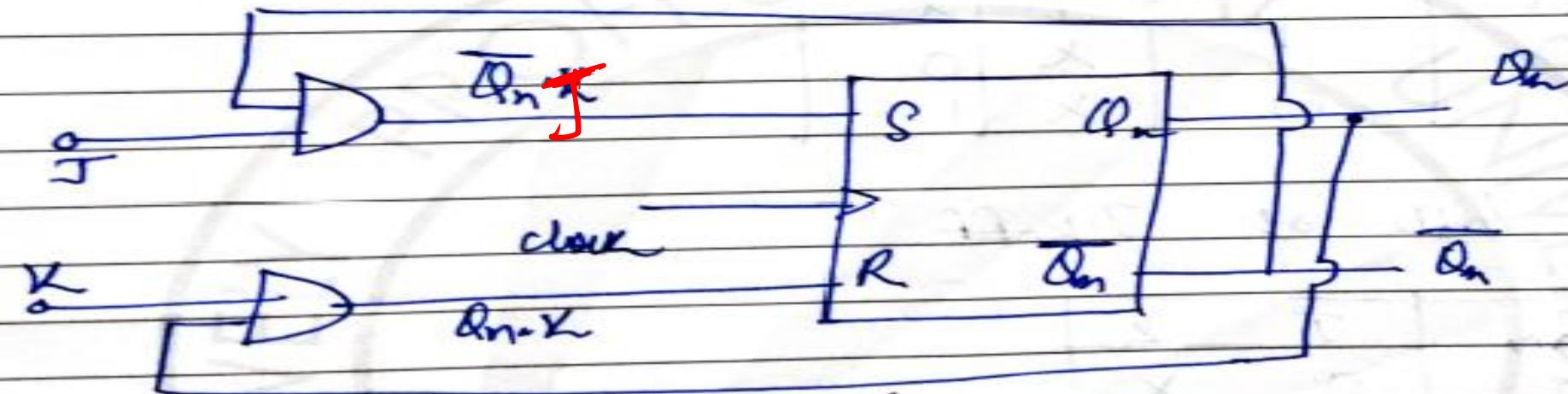
K-map

\bar{Q}_n	\bar{Q}_n	00	01	11	10
\bar{Q}_n	0	0	0	1	1
Q_n	1	x	0	0	x

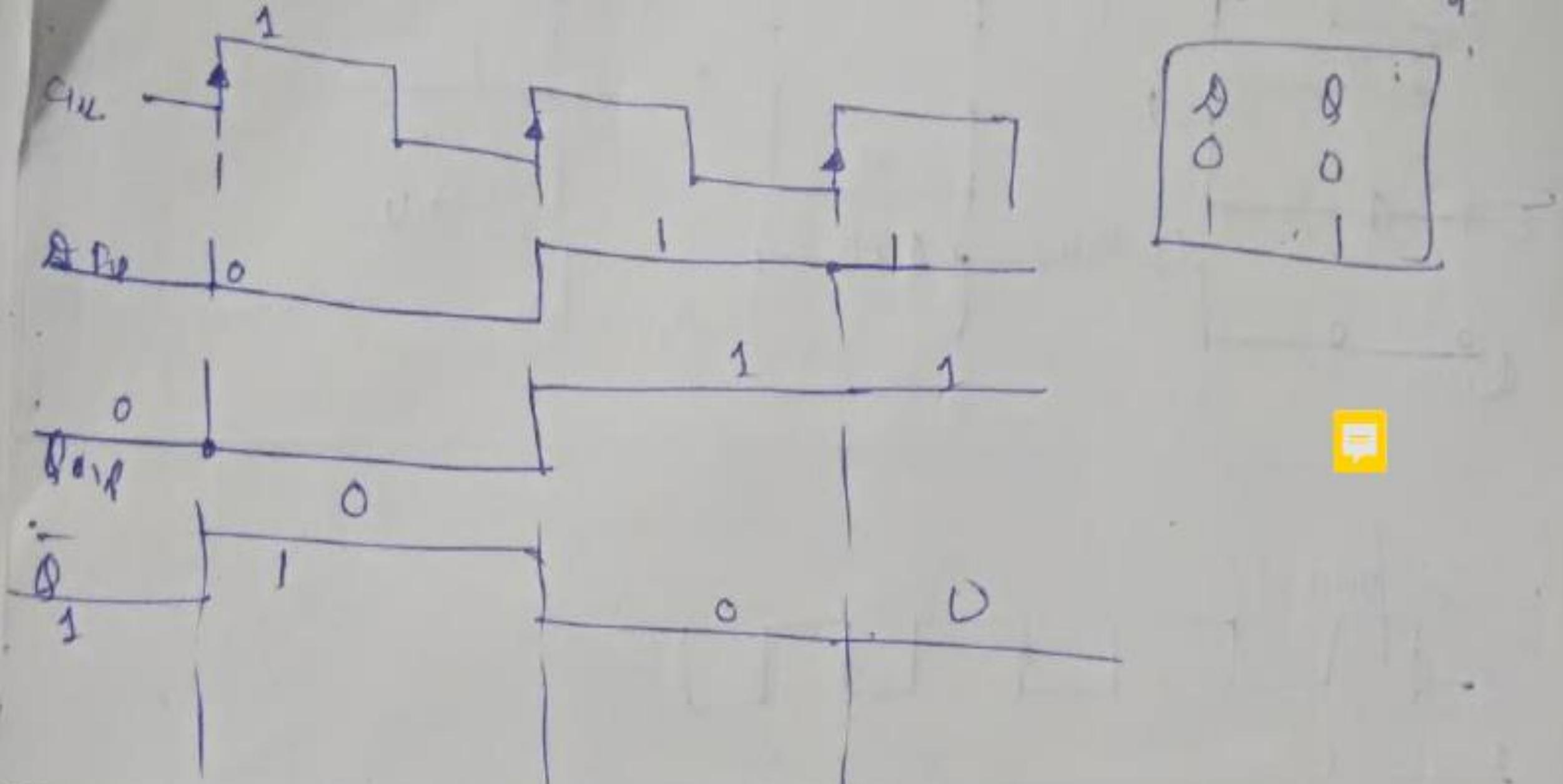
$$S = \bar{Q}_n J$$

\bar{Q}_n	00	01	11	10
\bar{Q}_n	0	x	x	0
Q_n	1	0	1	1

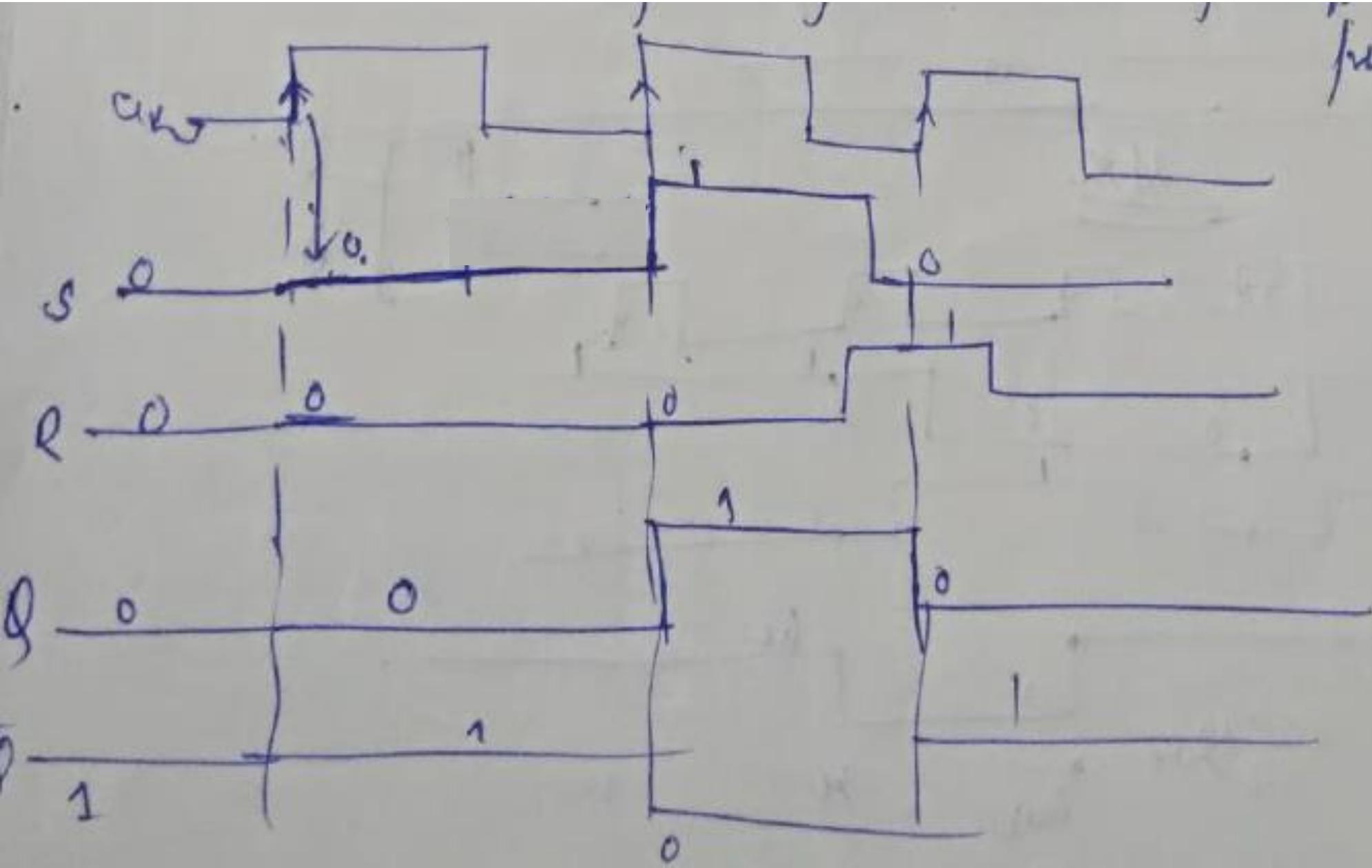
$$R = Q_n K$$



Draw the output waveform for the positive edge triggered D flip flop, if the clock and D input input waveform are follows:



Draw the output waveform for the positive edge triggered SR flip flop, if the clock and SR input input waveforms are follows:



Timing Waveform for JK Flip Flop

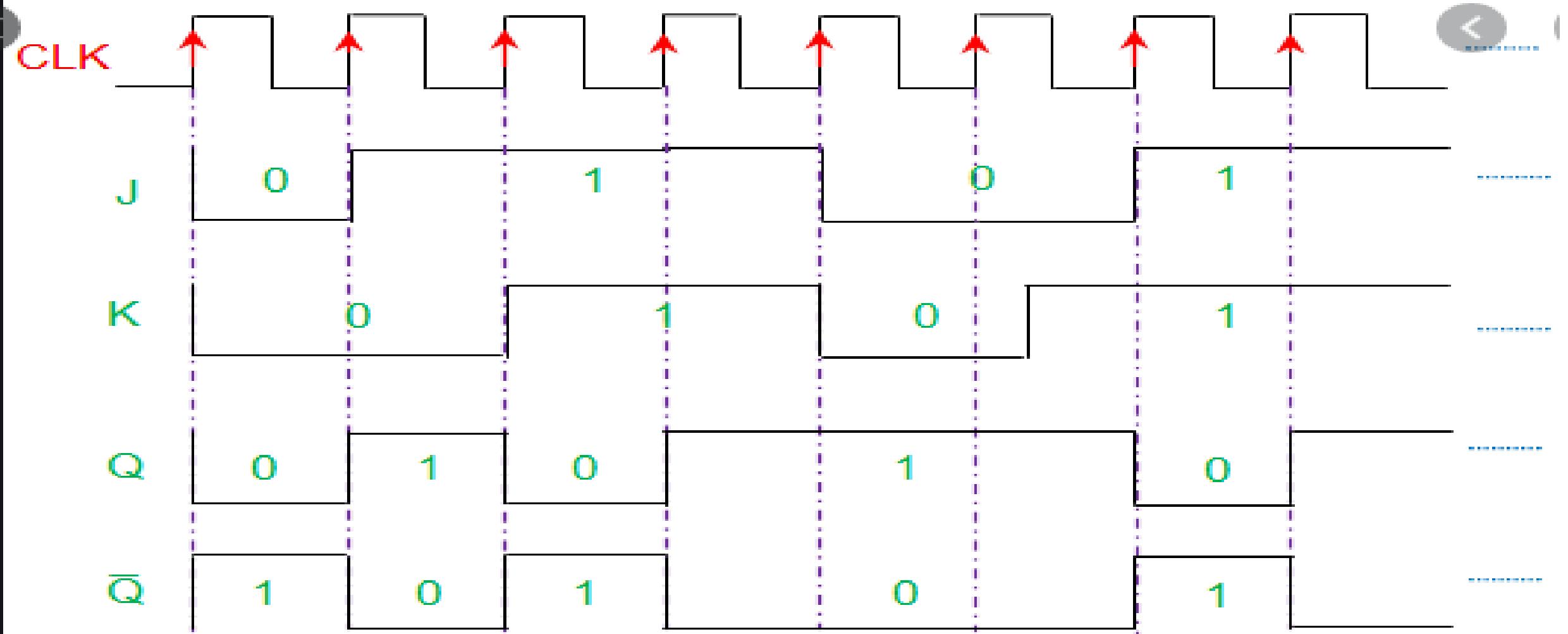


Figure 3 Timing diagram for positive edge-triggered JK flip-flop

3. The truth table for an S-R flip-flop has how many VALID entries?

- a) 1
- b) 2
- c) 3
- d) 4

3. The truth table for an S-R flip-flop has how many VALID entries?

- a) 1
- b) 2
- c) 3
- d) 4

 [View Answer](#)

Answer: c

Explanation: The SR flip-flop actually has three inputs, Set, Reset and its current state. The Invalid or Undefined State occurs at both S and R being at 1.

7. The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called _____

- a) Combinational circuits
- b) Sequential circuits

.....

12. In S-R flip-flop, if $Q = 0$ the output is said to be _____

- a) Set
- b) Reset
- c) Previous state
- d) Current state

12. In S-R flip-flop, if $Q = 0$ the output is said to be _____

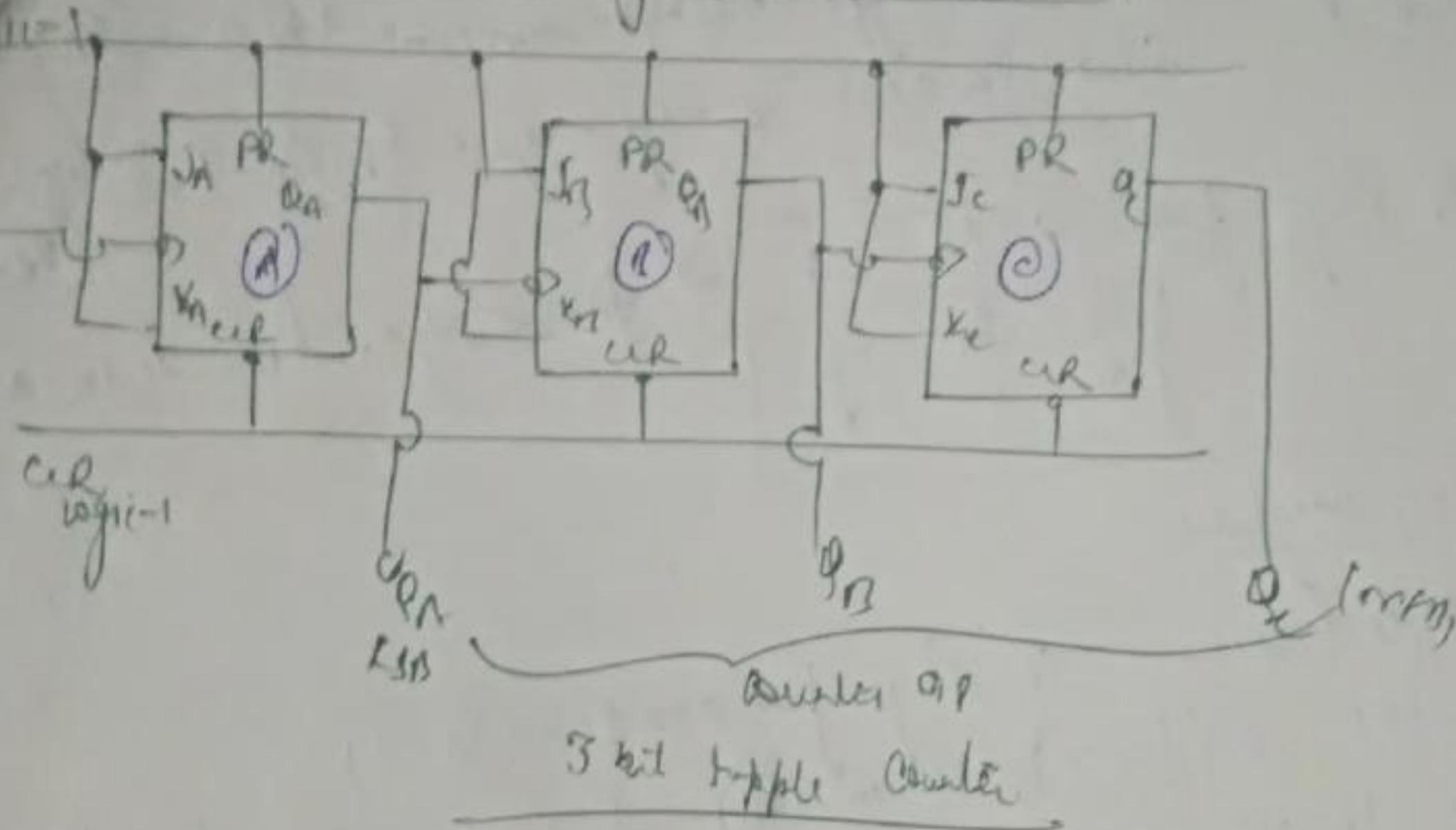
- a) Set
- b) Reset
- c) Previous state
- d) Current state

 [View Answer](#)

Answer: b

Explanation: In S-R flip-flop, if $Q = 0$ the output is said to be reset and set for $Q = 1$.

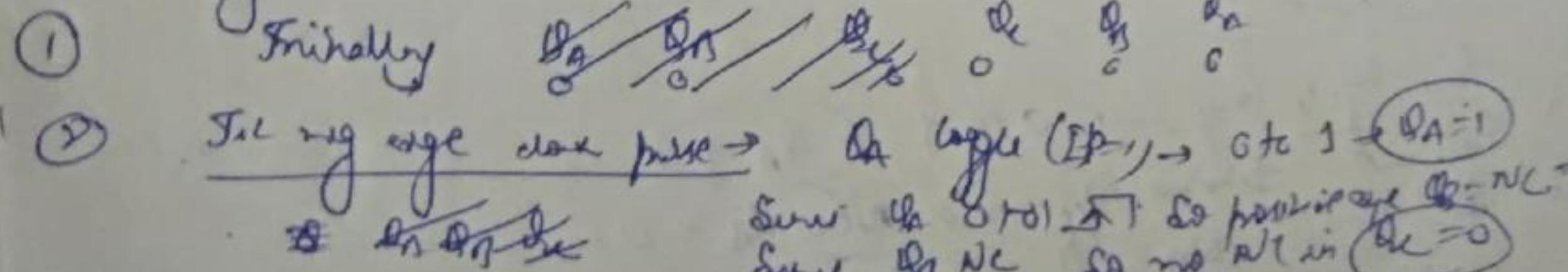
3 Bit Asynchronous Counter



①

Truthly	Q_c	Q_B	Q_A	4th State	Neural
Front	0	0	0	1	0
1's ↓	0	0	1	2	1
2nd ↓	0	1	0	3	2
3rd ↓	0	1	1	4	7
4th ↓	1	0	0	5	8
5th ↓	1	0	1	6	5
6th ↓	1	1	0	2	6
7th ↓	1	1	1	8	2
8th ↓	0	0	0	1	0

No. of State $\rightarrow 2^n \rightarrow 2^{\binom{n}{2}}$ | max count = $2^n - 1 \rightarrow 2^7 - 1 \rightarrow 7$



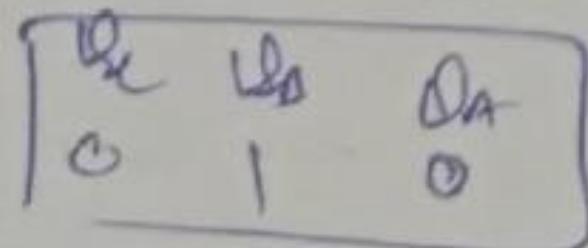
Since the total set so possibility $\binom{6}{3} = 20$

Since $\binom{6}{3} = 20$ so no all in $\binom{6}{3} = 0$

\emptyset	\emptyset	\emptyset	\mid
$\textcircled{0}$	$\textcircled{0}$	$\textcircled{0}$	\mid

2nd mag edge dark fate Ω_A larger ($\omega_A > \omega_B > 1$) $\rightarrow 1 \rightarrow 0 \rightarrow \Omega_A$
Same $\Omega_A > 0$ \nexists negative eye + $T_{\text{out}} T_B = 1$ so Ω_A ~~very~~

Since Ω_A change from 0 to 1 \nexists do positive eye; here $T_{\text{out}} T_B = 0$



and only clear pulse

①

②

③

Q_A agree ($\text{negative} \rightarrow$) Q_A change from 0 to 1 \Rightarrow Q_A = 1
Q_A 0 to 1 \leftarrow F (positive); NC is in Q_B = -1 if weak pulse during no days
Since Q_B = NC so Q_C = NC \Rightarrow Q_C = -1 \leftarrow low

the	Q _B	Q _A
0	-1	1

H^m dark future

1

Φ_A $\xrightarrow{\text{apply}}$ 1 to 0 \rightarrow

$$\boxed{\Phi_A = 0}$$

2
?

Φ_B $\xrightarrow{\text{negate}}$ mean Φ_B $\xrightarrow{\text{apply}}$ 1 to 0

$$\boxed{\Phi_B = 0}$$

Φ_C 1 to 0 $\xrightarrow{\text{negate}}$ mean Φ_C $\xrightarrow{\text{apply}}$ 0 to 1

$$\boxed{\Phi_C = 1}$$

$$\boxed{\begin{matrix} \Phi_C & \Phi_B & \Phi_A \\ 1 & 0 & 0 \end{matrix}}$$

5th dark fringe

①

So $\omega_{1,2}$ (ray) \rightarrow 0 to 1

$$q_A = 1$$

②

So $\omega_{1,2}$ prime edge no NC $q_A = 0$

③

So NC in Dn Dense then $\Rightarrow 1$

$\int \frac{dx}{l} \text{ as } q_A$
0 1

check face

(3)

On sign from 1 to 0 $\boxed{Q_0 = 0}$

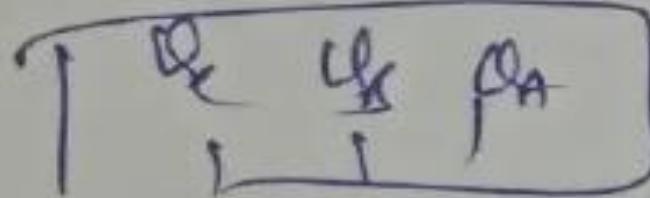
On negative sign from 1 to 0; $Q_0 = 0$, $Q_1 = 0$ or $Q_1 = 1$

On 0 to 1 \rightarrow positive sign from 1 to 0 $\rightarrow Q_0 = NR$ ~~or 1~~

Q_0	Q_1	Q_A
1	1	0

$Q_0 = 1$

7^m dark fringes

- ① DA toggle from 0 to 1 $\xrightarrow{0} \xrightarrow{1}$ prime edge generate
- ② NC in \bullet $Q_B = 1$
- ③ NC in \bullet $Q_C = 1$


B¹² new bubble

①

On wiggles from 1 to 0

$$B_{12} = 0$$

↓ negative

②

On little from 1 to 0

$$B_{12} \approx 0$$

mg sy. ↓

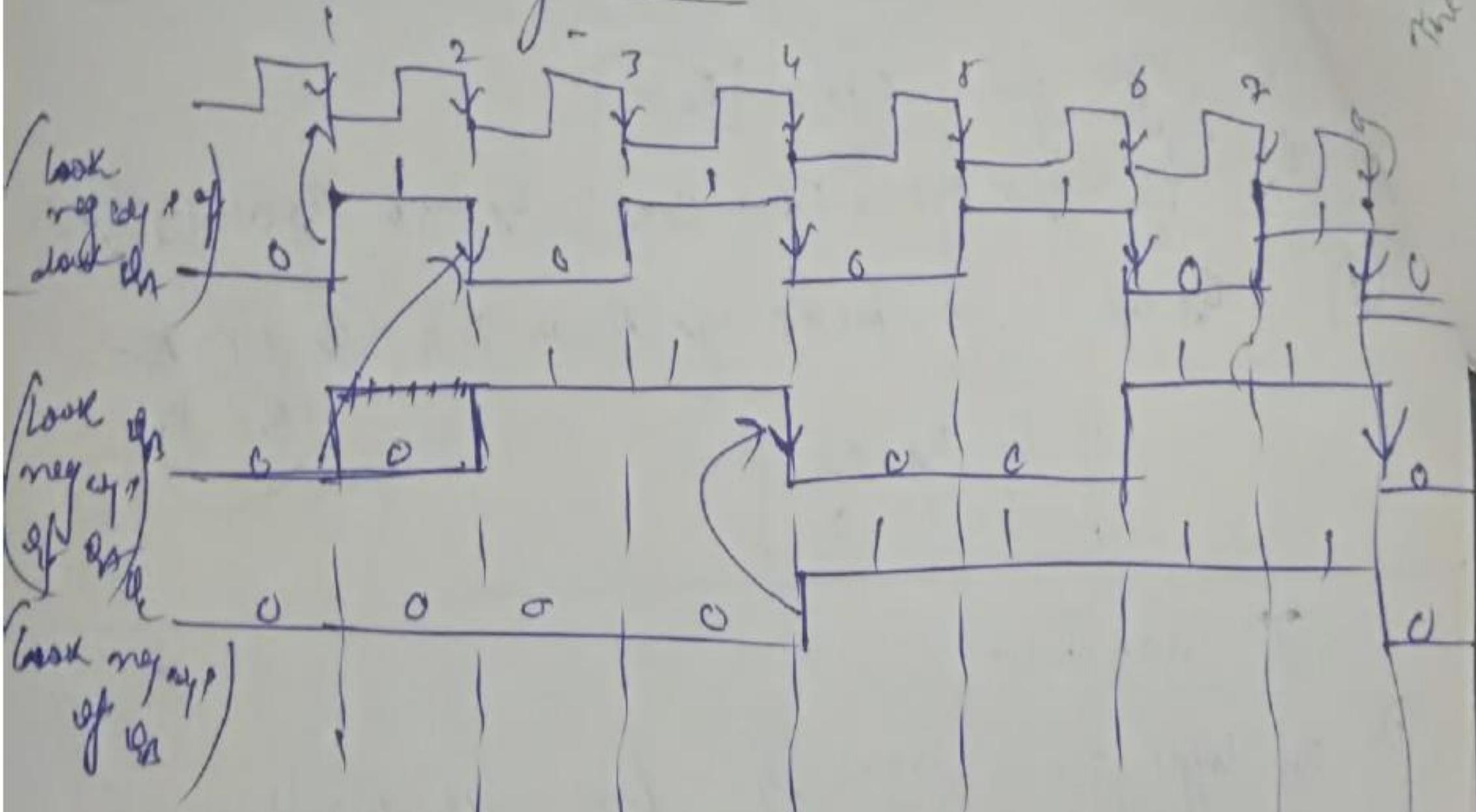
?

On coffee from 1 to 0

$$B_{12} \approx 0$$

↓ the B_{12} chg
o o o

Amij diagram



Poll

2. In a J-K flip-flop, if $J=K$ the resulting flip-flop is referred to as _____
- a) D flip-flop
 - b) S-R flip-flop
 - c) T flip-flop
 - d) S-K flip-flop

Poll

2. In a J-K flip-flop, if $J=K$ the resulting flip-flop is referred to as _____
- a) D flip-flop
 - b) S-R flip-flop
 - c) T flip-flop
 - d) S-K flip-flop

 [View Answer](#)

Answer: c

Explanation: In J-K flip-flop, if both the inputs are same then it behaves like T flip-flop.

Poll

9. The flip-flops which has not any invalid states are _____
- a) S-R, J-K, D
 - b) S-R, J-K, T
 - c) J-K, D, S-R
 - d) J-K, D, T

Poll

9. The flip-flops which has not any invalid states are _____

- a) S-R, J-K, D
- b) S-R, J-K, T
- c) J-K, D, S-R
- d) J-K, D, T

 View Answer

Answer: d

Explanation: Unlike the SR latch, these circuits have no invalid states. The SR latch or flip-flop has an invalid or forbidden state where no output could be determined.

Poll

4. How is a $J-K$ flip-flop made to toggle?

A. $J = 0, K = 0$

B. $J = 1, K = 0$

C. $J = 0, K = 1$

D. $J = 1, K = 1$

Poll

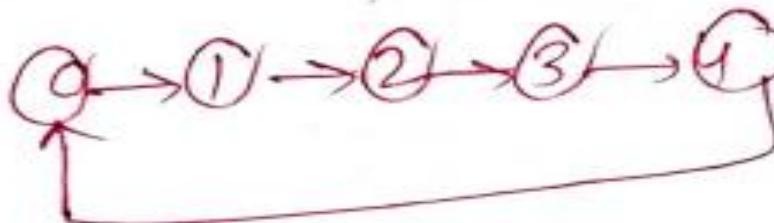
4. How is a $J-K$ flip-flop made to toggle?

- A. $J = 0, K = 0$
- B. $J = 1, K = 0$
- C. $J = 0, K = 1$
- D. $J = 1, K = 1$

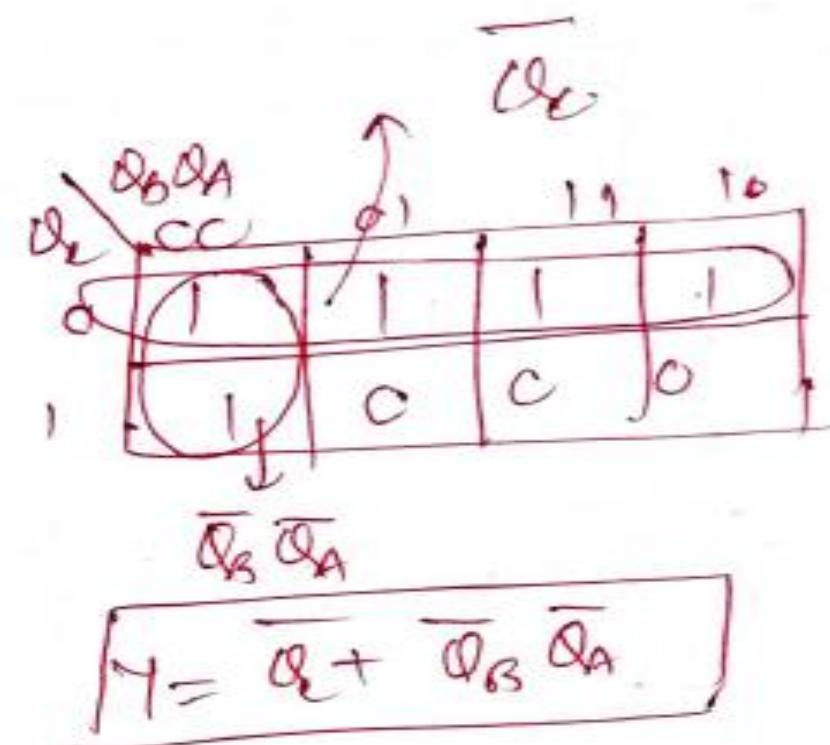
Answer: Option D

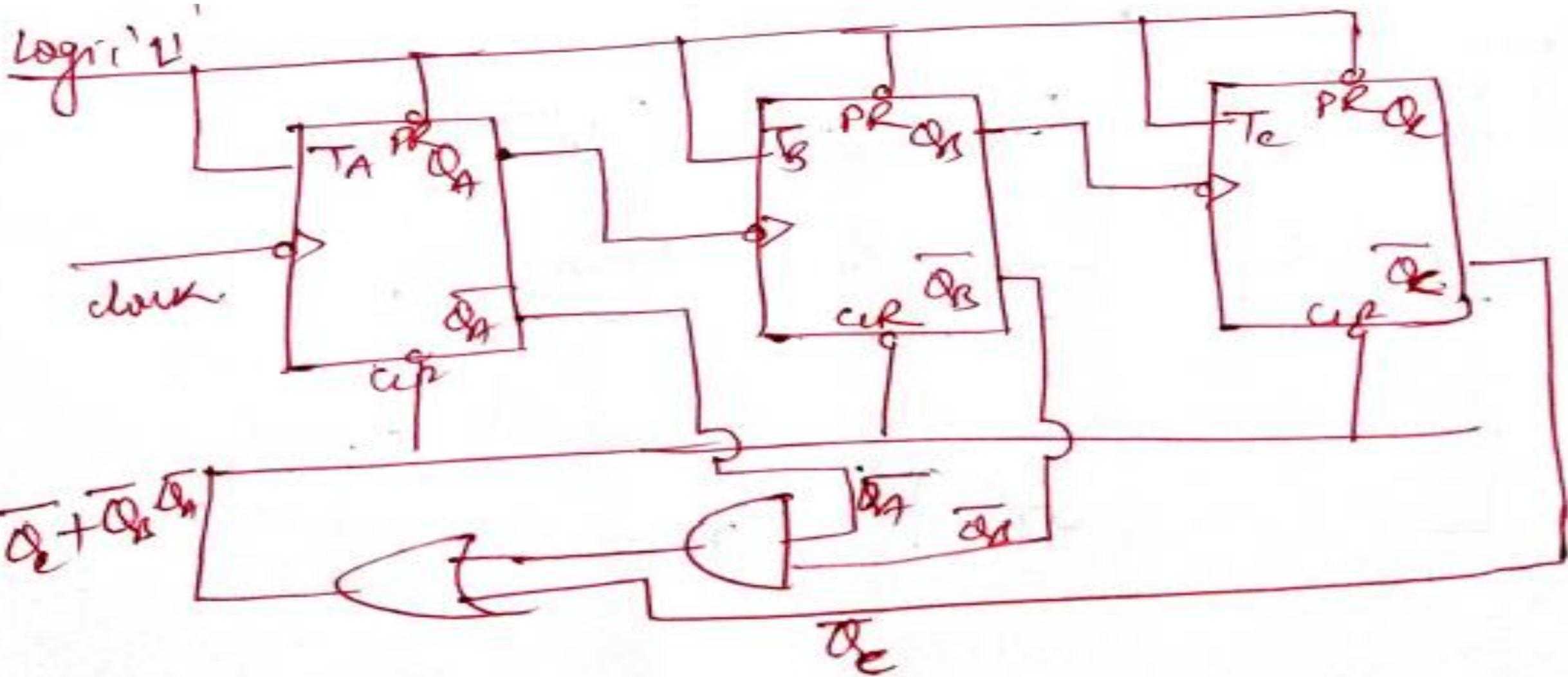
Q:- Design a modulus 5 ripple counter using a 3 bit ripple counter?

Solution:-



State	Q_2	Q_1	Q_0	γ
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	0
6	1	1	0	0
7	1	1	1	0





Poll

70. If both inputs of an S-R flip-flop are low, what will happen when the clock goes HIGH?

- A. An invalid state will exist.
- B. No change will occur in the output.
- C. The output will toggle.
- D. The output will reset.

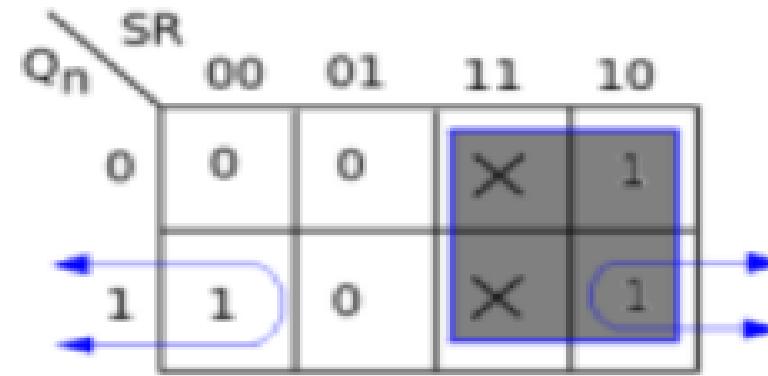
Poll

70. If both inputs of an S-R flip-flop are low, what will happen when the clock goes HIGH?

- A. An invalid state will exist.
- B. No change will occur in the output.
- C. The output will toggle.
- D. The output will reset.

Answer: Option B

7) What would be the characteristic equation of SR latch corresponding to the K-map schematic shown below?



- a. $S + RQ_n$
- b. $S + \overline{R}Q_n$
- c. $\overline{S} + RQ_n$
- d. $\overline{S} + \overline{R}Q_n$

ANSWER: S + $\bar{R}Q_{II}$

4. A flip-flop changes its state during the

- a. complete operational cycle
- b. falling edge of the clock pulse
- c. rising edge of the clock pulse
- d. both answers (b) and (c)

4. A flip-flop changes its state during the

- a. complete operational cycle
- b. falling edge of the clock pulse
- c. rising edge of the clock pulse
- d. both answers (b) and (c)

Answer

Answer. d

6. For an edge-triggered D flip-flop,

- a. a change in the state of the flip-flop can occur only at a clock pulse edge
- b. the state that the flip-flop goes to depends on the D input
- c. the output follows the input at each clock pulse
- d. all of these answers

6. For an edge-triggered D flip-flop,

- a. a change in the state of the flip-flop can occur only at a clock pulse edge
- b. the state that the flip-flop goes to depends on the D input
- c. the output follows the input at each clock pulse
- d. all of these answers

Answer

Answer. d

7. A feature that distinguishes the J-K flip-flop from the D flip-flop is the

- a. toggle condition
- b. preset input
- c. type of clock
- d. clear input

7. A feature that distinguishes the J-K flip-flop from the D flip-flop is the
- a. toggle condition
 - b. preset input
 - c. type of clock
 - d. clear input

Answer

Answer. a

8. A flip-flop is SET when

- a. J = 0, K = 0
- b. J = 0, K = 1
- c. J = 1, K = 0
- d. J = 1, K = 1

8. A flip-flop is SET when

- a. $J = 0, K = 0$
- b. $J = 0, K = 1$
- c. $J = 1, K = 0$
- d. $J = 1, K = 1$

Answer

Answer. c

22. When a flip-flop is reset, its output will be

- a. $Q = 0; \overline{Q} = 1$
- b. $Q = 1; \overline{Q} = 0$
- c. $Q = 0; \overline{Q} = 0$
- d. $Q = 1; \overline{Q} = 1$

22. When a flip-flop is reset, its output will be

- a. $Q = 0; \bar{Q} = 1$
- b. $Q = 1; \bar{Q} = 0$
- c. $Q = 0; \bar{Q} = 0$
- d. $Q = 1; \bar{Q} = 1$

Answer

Answer. a

23. In the toggle mode, a JK flip-flop has

- a. $J = 0; K = 1$
- b. $J = 1; K = 0$
- c. $J = 0; K = 0$
- d. $J = 1; K = 1$

23. In the toggle mode, a JK flip-flop has

- a. $J = 0; K = 1$
- b. $J = 1; K = 0$
- c. $J = 0; K = 0$
- d. $J = 1; K = 1$

Answer

Answer. d