10_100_1000 Mbps Tri-mode Ethernet MAC Specification

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Rev. 0.1

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Revision History

Rev.	Date	Author	Description
0.1	11/28/05	Jon Gao	First Draft

Contents

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Introduction

10_100_1000 Mbps tri-mode ethernet MAC implements a MAC controller conforming to IEEE 802.3 specification. It is designed to use less than 2000 LCs/LEs to implement full function. It will use inferred RAMs PADs to reduce technology dependance.

functional description:

- Implements the full 802.3 specifiction.
- half-duplex support for 10 100 Mbps mode
- FIFO insterface to user application
- support pause frame generation and termination
- transmitting frames souce MAC address insertion
- receiving frames destination MAC address filter
- receiving broadcast frames throughout constraint
- support Jumbo frame 9.6K
- RMON MIB statistic counter

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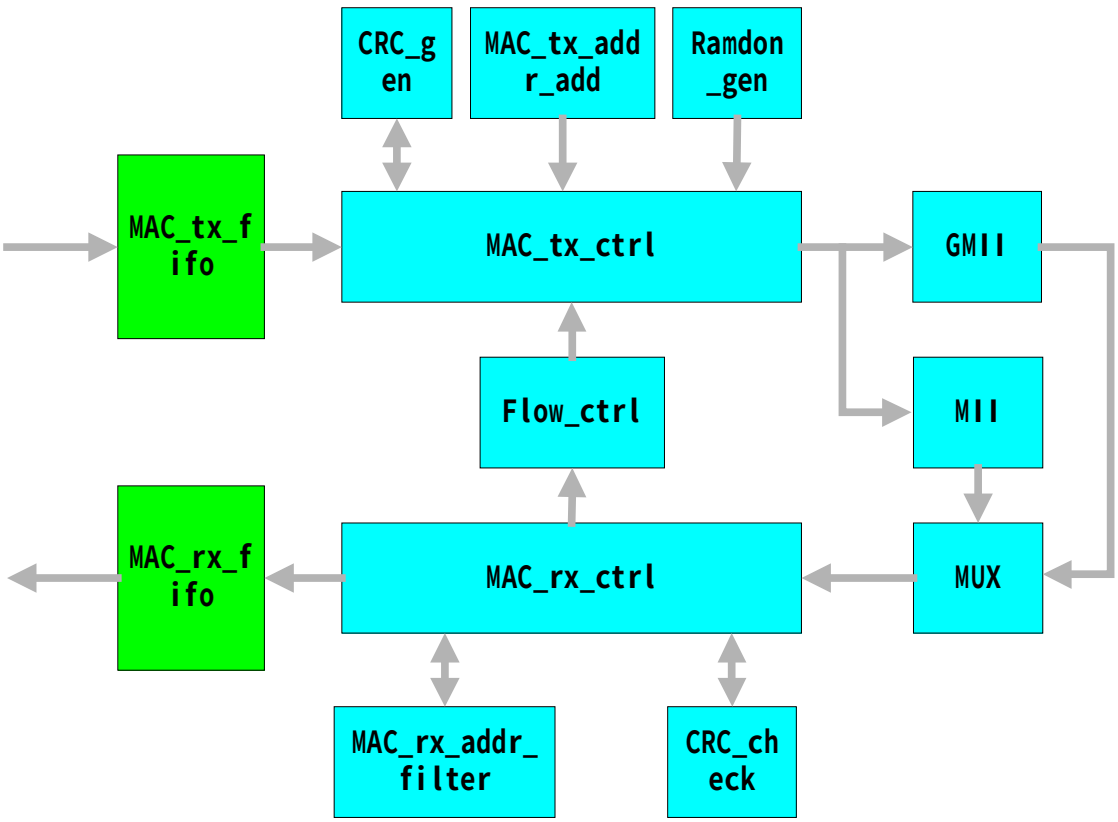
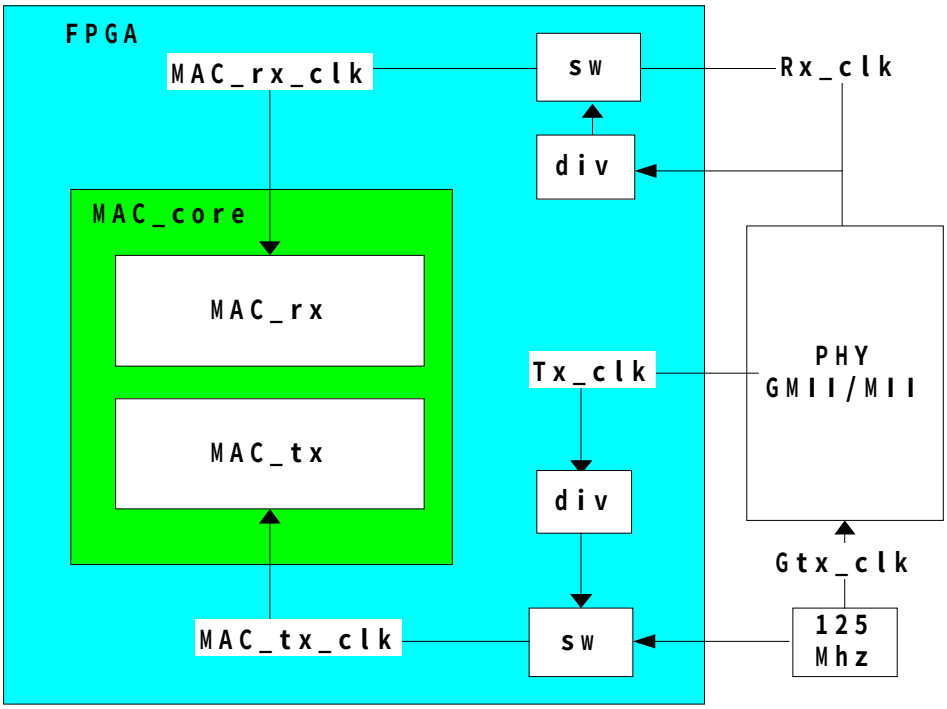
Architecture

block diagram



clock distribution



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Operation

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Clocks

This section specifies all the clocks. All clocks, clock domain passes and the clock relations should be described.

Name	Source	Rates (MHz)			Remarks	Description
		Max	Min	Resolution		
clk_pad_i	Input Pad	10	4	0.1	Duty cycle 70/30.	For external interface.
wb_clk_I	PLL	200	-	-	Must be synchronized to sm_clk_i	System clock.
sm_clk_i	Input port	55	40	1	There are multi-clocks paths.	Clock 55MHz for State machine.

Table 1: List of clocks

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IO Ports

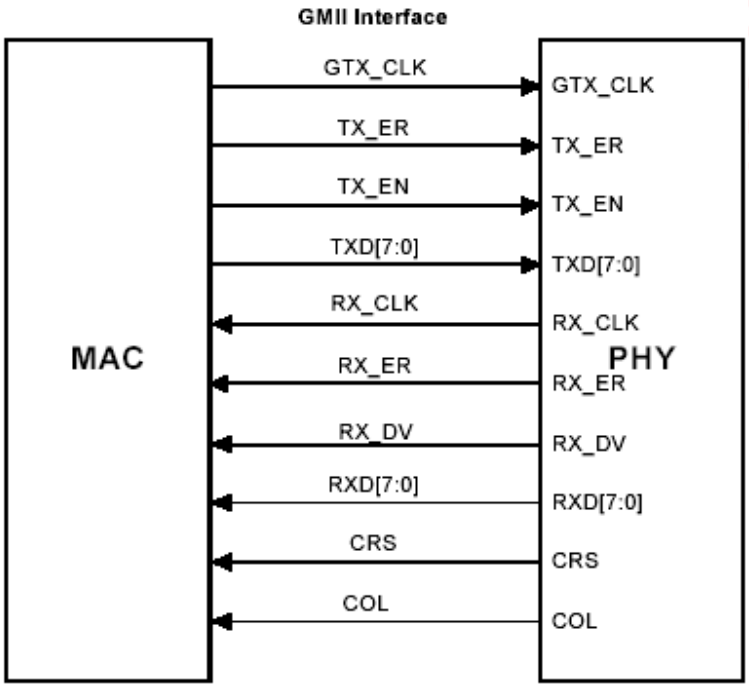
PHY interface

Gigabit Media Independent Interface (GMII/MII)

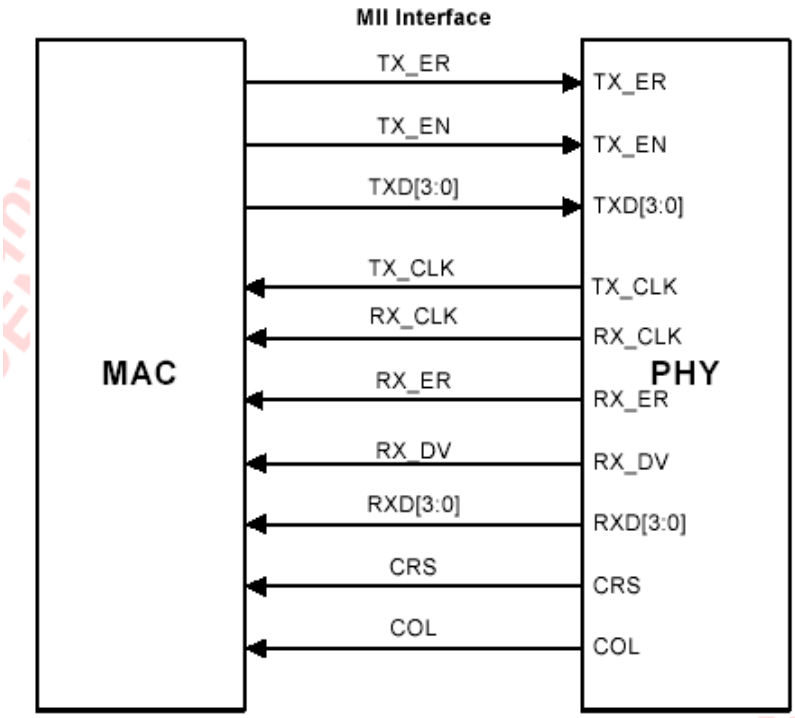
signal mapping

88E1111 Device Pins	GMII	MII
GTX_CLK	GTX_CLK	-
TX_CLK	-	TX_CLK
TX_ER	TX_ER	TX_ER
TX_EN	TX_EN	TX_EN
TXD[7:0]	TXD[7:0]	TXD[3:0]
RX_CLK	RX_CLK	RX_CLK
RX_ER	RX_ER	RX_ER
RX_DV	RX_DV	RX_DV
RXD[7:0]	RXD[7:0]	RXD[3:0]
CRS	CRS	CRS
COL	COL	COL

gmii signal diagram


GMII Interface
MAC
PHY
GTX_CLK
TX_ER
TX_EN
TXD[7:0]
RX_CLK
RX_ER
RX_DV
RXD[7:0]
CRS
COL

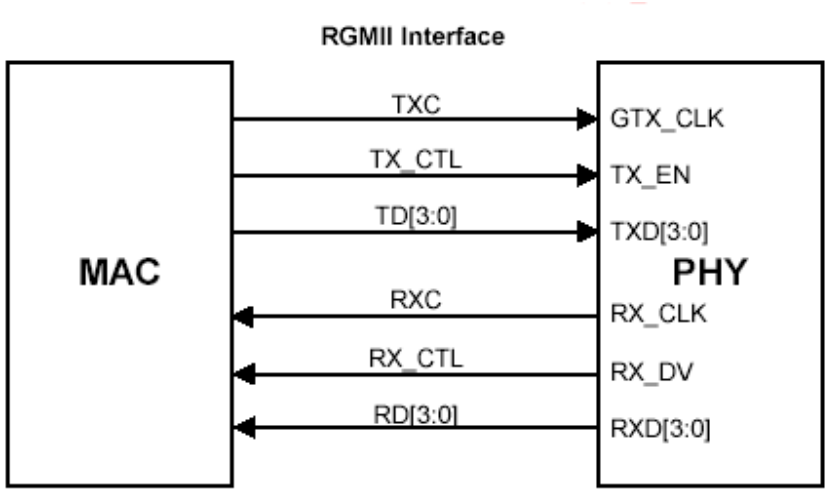
mii diagram


MII Interface
MAC
PHY
TX_ER
TX_EN
TXD[3:0]
TX_CLK
RX_CLK
RX_ER
RX_DV
RXD[3:0]
CRS
COL

Reduced Pin Count GMII (RGMII)

signal mapping

88E1111 Device Pin Name	RGMII Spec	Pin Name Description
GTX_CLK	TXC	125 MHz, 25 MHz, or 2.5 MHz transmit clock with ±50 ppm tolerance based on the selected speed.
TX_EN	TX_CTL	Transmit Control Signals. TX_EN is encoded on the rising edge of GTX_CLK, TX_ER XORed with TX_EN is encoded on the falling edge of GTX_CLK.
TXD[3:0]	TD[3:0]	Transmit Data. In 1000BASE-T and 1000BASE-X modes,TXD[3:0] are presented on both edges of GTX_CLK. In 100BASE-TX and 10BASE-T modes, TXD[3:0] are presented on the rising edge of GTX_CLK.
RX_CLK	RXC	125 MHz, 25 MHz, or 2.5 MHz receive clock ± 50 ppm tolerance derived from the received data stream and based on the selected speed.
RX_DV	RX_CTL	Receive Control Signals. RX_DV is encoded on the rising edge of RX_CLK, RX_ER XORed with RX_DV is encoded on the falling edge of RX_CLK.
RXD[3:0]	RD[3:0]	Receive Data. In 1000BASE-T and 1000BASE-X modes,RXD[3:0] are presented on both edges of RX_CLK. In 100BASE-TX and 10BASE-T modes, RXD[3:0] are presented on the rising edge of RX_CLK.



user interface

output		Rx_mac_ra	//
input		Rx_mac_rd	

output	[31:0]	Rx_mac_data	
output	[1:0]	Rx_mac_BE	
output		Rx_mac_pa	
output		Rx_mac_sop	
output		Rx_mac_eop	
			//
output		Tx_mac_wa	
input		Tx_mac_wr	
input	[31:0]	Tx_mac_data	
input	[1:0]	Tx_mac_BE	//
input		Tx_mac_sop	
input		Tx_mac_eop	

Appendix A

Name

This section may be added to outline different specifications.

Index

This section contains an alphabetical list of helpful document entries with their corresponding page numbers.