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HIBI v3 resource usage and performance

DATASHEET

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List of Abbreviations

fifo first in, first out

FPGA Field Programmable Gate Array

HIBI Heterogeneous IP Block Interconnect

SoC System-on-Chip

# Version history

## Documentation

|  |  |  |  |
| --- | --- | --- | --- |
| Date | Version | Change description | Author |
| 04.11.2011 | 0.1 | Datasheet documentation started | Juha Arvio |

# Performance and resource usage

The main resource the HIBI uses is it's wrappers. HIBI version 3 has three of them which include R1, R3 and R4. Figure shows how a R3 wrapper is constructed of a R1 wrapper which in itself has four separate fifos.



*Figure* *2-1 HIBI R3 wrapper block diagram*

## Resource usage

The resource usage for invidual HIBI wrappers was acquired from a SoC that was synthesized to a Arria II GX FPGA on a Arria II GX development board. The SoC had two HIBI components with both attached to a R3 HIBI wrapper. The size of the fifos on these wrappers was set to 4 words which amounts to 128 bits on each fifo. Figure shows the resource usage layout of the entire HIBI segment on the FPGA as seen on the Chip Planner in Quartus II. The two wrappers are highlighted in blue.

*Figure* *2-2 HIBI segment resource usage*

Table shows the combinatorial alut counts, register counts and other resource data pertaining to the two wrappers. Both alut and register counts have minimum and maximum values gathered from the SoC. The combinatorial alut and register counts can be significantly reduced for the wrappers if the fifos are implemented as onchip memories (m9k blocks in Arria II GX).

|  |  |  |
| --- | --- | --- |
| wrapper part | measure | value |
| HIBI wrapper R3 | combinatorial aluts | 724-763 |
| registers | 1039-1168 |
| HIBI wrapper R1 | combinatorial aluts | 466-533 |
| registers | 825-935 |
| wrapper fifo | word width | 38 bits (data 32, address\_valid 1, comm 5) |
| size | 4 words |
| comb. aluts | 76-104 |
| registers | 155-167 |

Table 2- HIBI R3 wrapper resource usage

## Simulated performance

The throughput was measured in Modelsim for a HIBI segment with two components, both of which were connected to the segment with a R3 wrapper. The sender transmitted a continuous stream of 1024 words to a single address. And as the HIBI segment had the data and address buses muxed together, the minimum time to send the stream was 1025 cycles. Figure shows the calculated throughput at a clock rate of 200 MHz, a typical clock rate achieved on an Arria II GX FPGA. The X-axis on the figure is logarithmic.

 *Figure* *2-3 HIBI troughput between two components*