

Juha Arvio

HIBI v3 resource usage and performance

DATASHEET

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List of Abbreviations

fifo first in, first out

FPGA Field Programmable Gate Array

Gbps Giga bits per second

H2P HIBI to PC

HDL Hardware Design Language

HIBI Heterogeneous IP Block Interconnect

HW Hardware

ID Identification

I/O Input / Output

IP Intellectual Property

IRQ Interrupt Request

P2H PC to HIBI

PC Personal Computer

SoC System-on-Chip

SW Software

tbd to be decided

TLP Transaction Layer Protocol

TUT Tampere University of Technology

VHDL VHSIC Hardware Description Language

VHSIC Very High Speed Integrated Circuit

# Identification

Vendor: TTY

Library: ip.hwp.cpu

Name: PCIe\_to\_HIBI

Version: 0.1

Author(s): Juha Arvio

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# Version history

## Documentation

|  |  |  |  |
| --- | --- | --- | --- |
| Date | Version | Change description | Author |
| 04.11.2011 | 0.1 | Datasheet documentation started | Juha Arvio |

# Performance and resource usage

The main resource the HIBI uses is it's wrappers. HIBI version 3 has three of them which include R1, R3 and R4. Figure shows how a R3 wrapper is constructed of a R1 wrapper which in itself has four separate fifos.



*Figure* *3-1 HIBI R3 wrapper block diagram*

## Resource usage

The resource usage for invidual HIBI wrappers was acquired from a SoC that was synthesized to a Arria II GX FPGA on a Arria II GX development board. The SoC had two HIBI components with both attached to a R3 HIBI wrapper. The size of the fifos on these wrappers was set to 4 words which amounts to 128 bits on each fifo. Figure shows the resource usage layout on the FPGA as seen on the Chip Planner in Quartus II. The two wrappers are highlighted in red.

|  |  |  |
| --- | --- | --- |
| wrapper part | measure | value |
| HIBI wrapper R3 | comb. aluts | 32kB |
| registers | 32kB |
| Cyclone II | c2\_onchip | 8kB |
| c2\_onchip\_debug | 8kB |

Table 4- FPGA family specific Nios II microcontrollers

## Simulated performance

The throughput was measured for a HIBI segment with two components, both of which were connected to the segment with a R3 wrapper. The sender transmitted a continuous stream of 1024 words to a single address. And as the HIBI segment had the data and address buses muxed together, the minimum time to send the stream was 1025 cycles.