# M2H2 / Sdram controller comparison

ver. 0.1

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# Document history

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| Author | Version | Project | Date | Description |
| Juha Arvio | 0.1 | Funbase | 18.01.2010 |  |

## Memory to HIBI component

An adapter component with DMA functionality to interface memory controllers to Hibi network. Only Altera’s DDR memory controllers created with the Megawizard are supported at the moment.

## Adding a custom Altera memory controller

Memory controllers for the Stratix III development board will be supplied but it’s possible to add any Altera memory controller to use with this adapter by creating it in the Altera’s Megawizard.

## Example system



## Write configuration data:

Word 0:

|  |  |  |  |
| --- | --- | --- | --- |
| Bit | 31\*1 | 30...27\*2 | 26...00 |
|  | Post\_rw\_cmd | Byte enable for the write | Write length in words |

Word 1:

|  |  |  |
| --- | --- | --- |
| **Bit** | 31...28 | 27...00 |
|  | - | Write address |

## Read configuration data:

Word 0:

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit** | 31\*1 | 30...27 | 26...00 |
|  | Post\_rw\_cmd | - | Read length in words |

Word 1:

|  |  |  |
| --- | --- | --- |
| **Bit** | 31...28 | 27...00 |
|  | - | Read address |

Word 2:

|  |  |
| --- | --- |
| **Bit** | 31...00 |
|  | Hibi Read address |

\*1 set to 0

\*2 byte enable has a width of 4 in this example

## Functional model

A data write operation can be divided into two parts:

1. Send the two configuration words to the memory to hibi controller with the hibi\_cmd bus set to write\_data (0x2) and the memory offset of the hibi address set to 0x010
2. Send the words to be written to the memory to hibi controller

A data read operation can be divided into two parts:

1. Send the three configuration words to the memory to hibi controller with the hibi\_cmd bus set to read\_rq (0x4) and the memory offset of the hibi address set to 0x010
2. Words read from the memory are sent to the address defined in read configuration word 2

Write operation:

**offchip\_mem**

**alt\_mem\_ctrl**

**n2h2**

**m2h2**

**hibi**

first word

6:

last word

10:

configuration data

1:

write data start

3:

write data end

7:

first word

5:

last word

9:

configuration data

2:

write data start

4:

write data end

8:

Read operation:

**offchip\_mem**

**alt\_mem\_ctrl**

**n2h2**

**m2h2**

**hibi**

first word

5:

last word

11:

first addr

4:

last addr

10:

first word

6:

last word

12:

configuration data

1:

first addr

3:

last addr

9:

read data start

7:

read data end

13:

configuration data

2:

read data start

8:

read data end

14:

# Synthesis

Synthesizing the Memory to HIBI adapter with one of the DDR2 sdram chips on the Stratix III development board require the following files:

1. verilog/m2h2.v, verilog/m2h2\_s3\_ddr2/m2h2\_conf.v, vhd/fifo.vhd
2. from the directory alt\_mem\_ctrl/stratix\_III\_MT47H32M8BP\_3B: stratix\_III\_MT47H32M8BP\_3B.v, stratix\_III\_MT47H32M8BP\_3B\_mem\_model.v, stratix\_III\_MT47H32M8BP\_3B\_controller\_phy.v, stratix\_III\_MT47H32M8BP\_3B\_auk\_ddr\_hp\_controller\_wrapper.v, auk\_ddr\_hp\_controller.vhd, stratix\_III\_MT47H32M8BP\_3B\_phy.v, stratix\_III\_MT47H32M8BP\_3B\_phy\_alt\_mem\_phy.v, stratix\_III\_MT47H32M8BP\_3B\_phy\_alt\_mem\_phy\_seq\_wrapper.v, stratix\_III\_MT47H32M8BP\_3B\_phy\_alt\_mem\_phy\_seq.vhd, stratix\_III\_MT47H32M8BP\_3B\_phy\_alt\_mem\_phy\_pll.v

# Verification

Verification of the controller can be done on ModelSim. The files needed to simulate the Memory to HIBI adapter with one of the DDR2 sdram chips on the Stratix III development boards require the following files:

1. verilog/m2h2.v, verilog/m2h2\_s3\_ddr2/m2h2\_conf.v, vhd/fifo.vhd
2. from the directory tb: m2h2\_tb.v, 220model.v, altera\_mf.v altera\_primitives.v, sgate.v stratixiii\_atoms.v\*
3. from the directory alt\_mem\_ctrl/stratix\_III\_MT47H32M8BP\_3B: stratix\_III\_MT47H32M8BP\_3B.v, stratix\_III\_MT47H32M8BP\_3B\_mem\_model.v, stratix\_III\_MT47H32M8BP\_3B\_controller\_phy.v, stratix\_III\_MT47H32M8BP\_3B\_auk\_ddr\_hp\_controller\_wrapper.vo, stratix\_III\_MT47H32M8BP\_3B\_phy.v, stratix\_III\_MT47H32M8BP\_3B\_phy\_alt\_mem\_phy.v, stratix\_III\_MT47H32M8BP\_3B\_phy\_alt\_mem\_phy\_seq\_wrapper.vo, stratix\_III\_MT47H32M8BP\_3B\_phy\_alt\_mem\_phy\_pll.v

To simulate this example design you need compile all of the above files except m2h2\_conf.v which is a header file to m2h2.v. Path verilog/m2h2\_s3\_ddr2/ has to be added as a include directory on the compiler options on ModelSim. M2h2\_tb.v is the top level file which has to be simulated. The clk and reset signals of the test bench are automatically generated but you have to manually toggle the signals coming from the Hibi wrapper. Use test.do to simulate the initialization phase of the Altera memory controller and test the writing and reading of the DDR2 memory with the Memory to HIBI adapter.