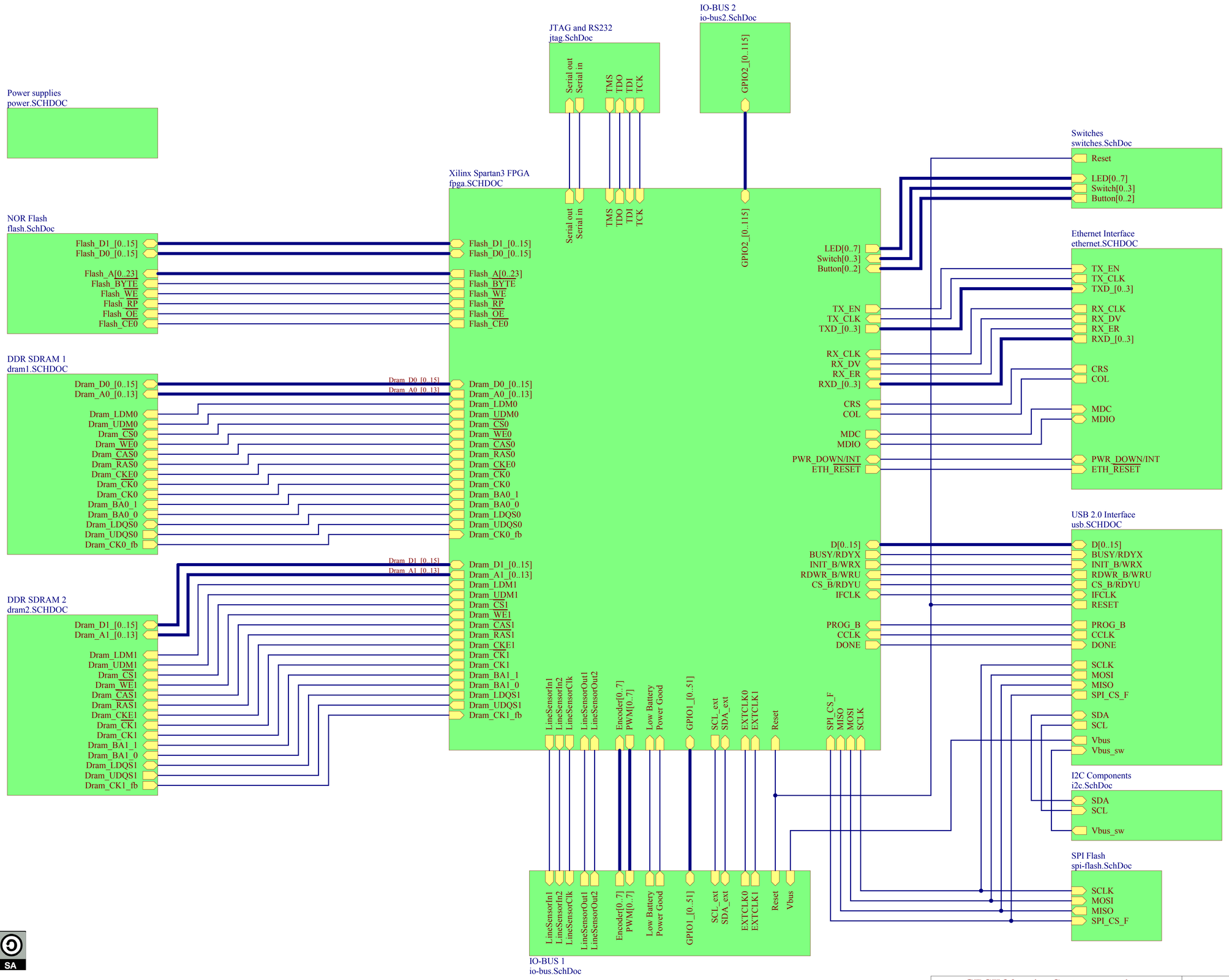
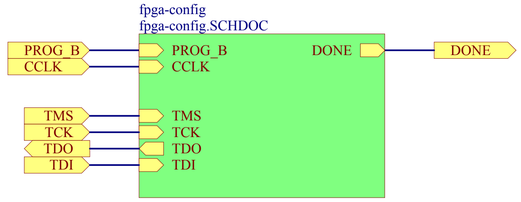


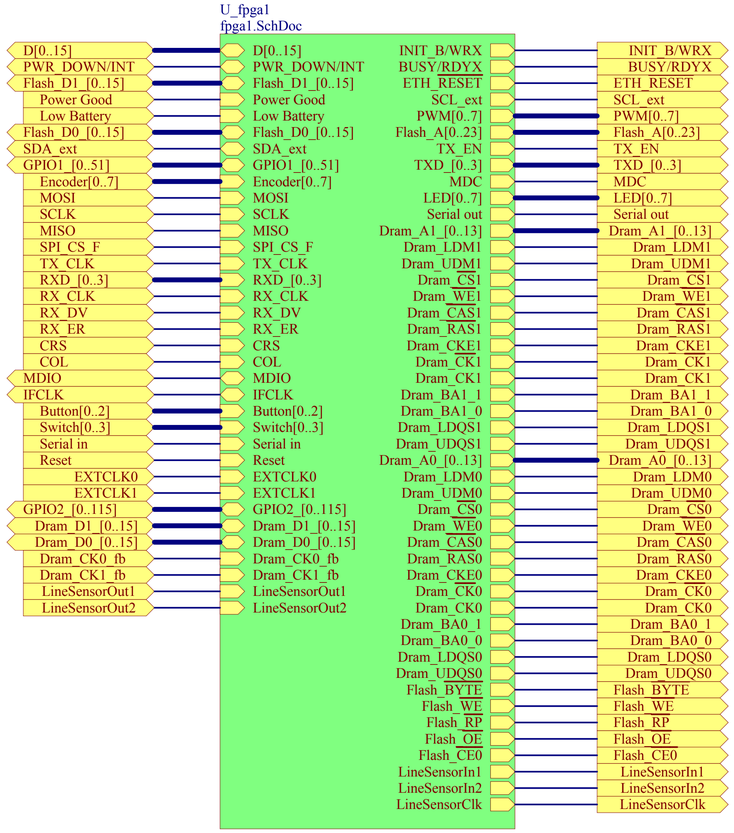
BY NC SA

For more information:
http://labs.ti.bfh.ch/gecko/wiki/gecko/license

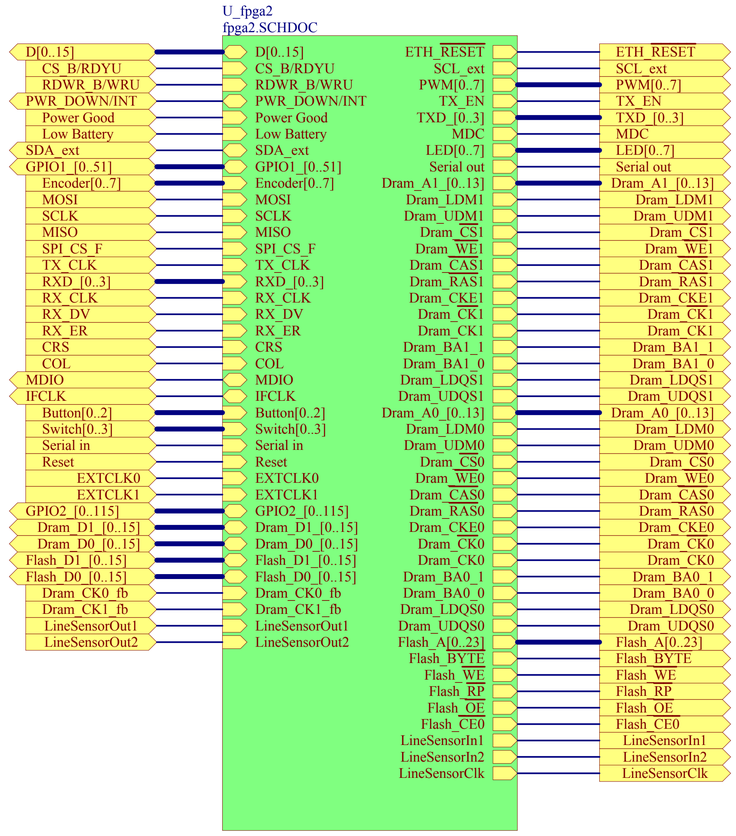
Title:	***GECKO3main: System overview***		**Berne University of Applied Science**
Size: A3_L	Author: zac1	Revision: 1.0	*School of Engineering and Information Technology*
Date: 23.07.2008	Time: 13:50:40	Sheet 1 of 19	*Quellgasse 21*
File: top.SchDoc			*CH-2501 Biel*



FPGA Banks 0,2,4,6

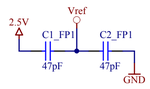


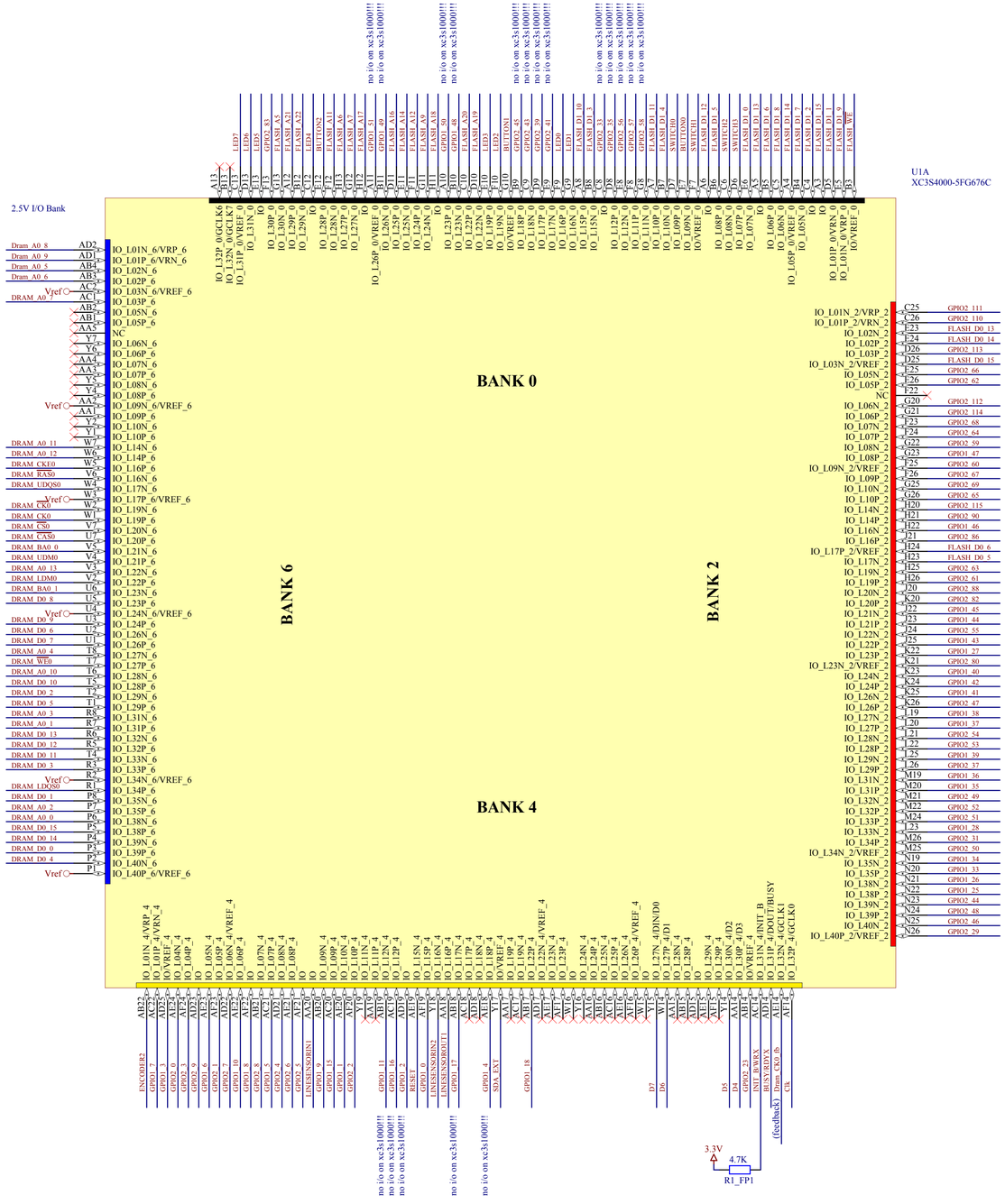
FPGA Banks 1,3,5,7



Title: ***FPGA Parts***		**Berne University of Applied Science**
Size: A3_L	Author: zac1	Revision: 1.0
Date: 23.07.2008 Time: 13:50:40		Sheet 2 of 19
File: fpga.SCHDOC		

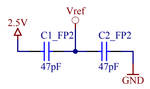
School of Engineering and Information Technology
Quellgasse 21
CH-2501 Biel

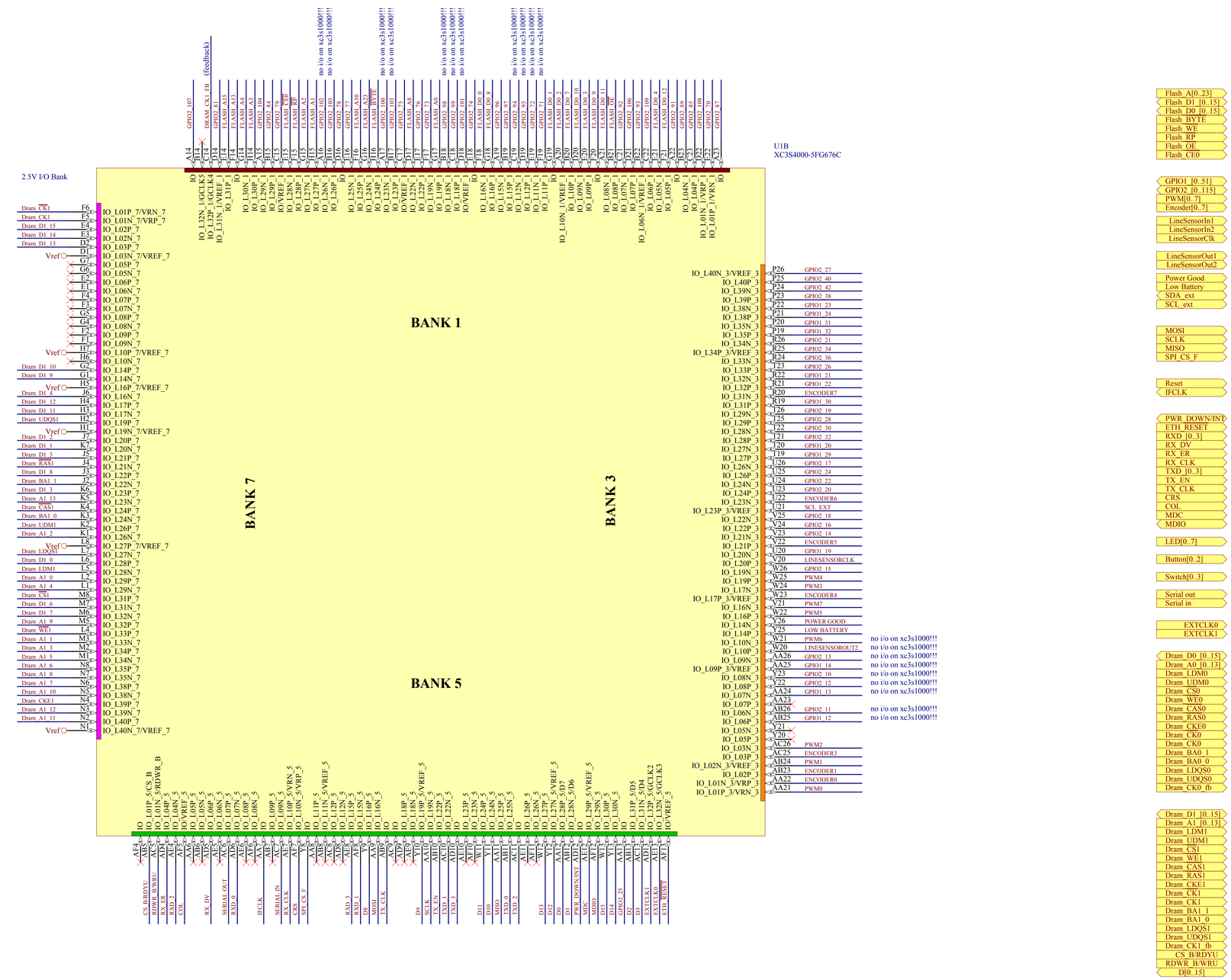




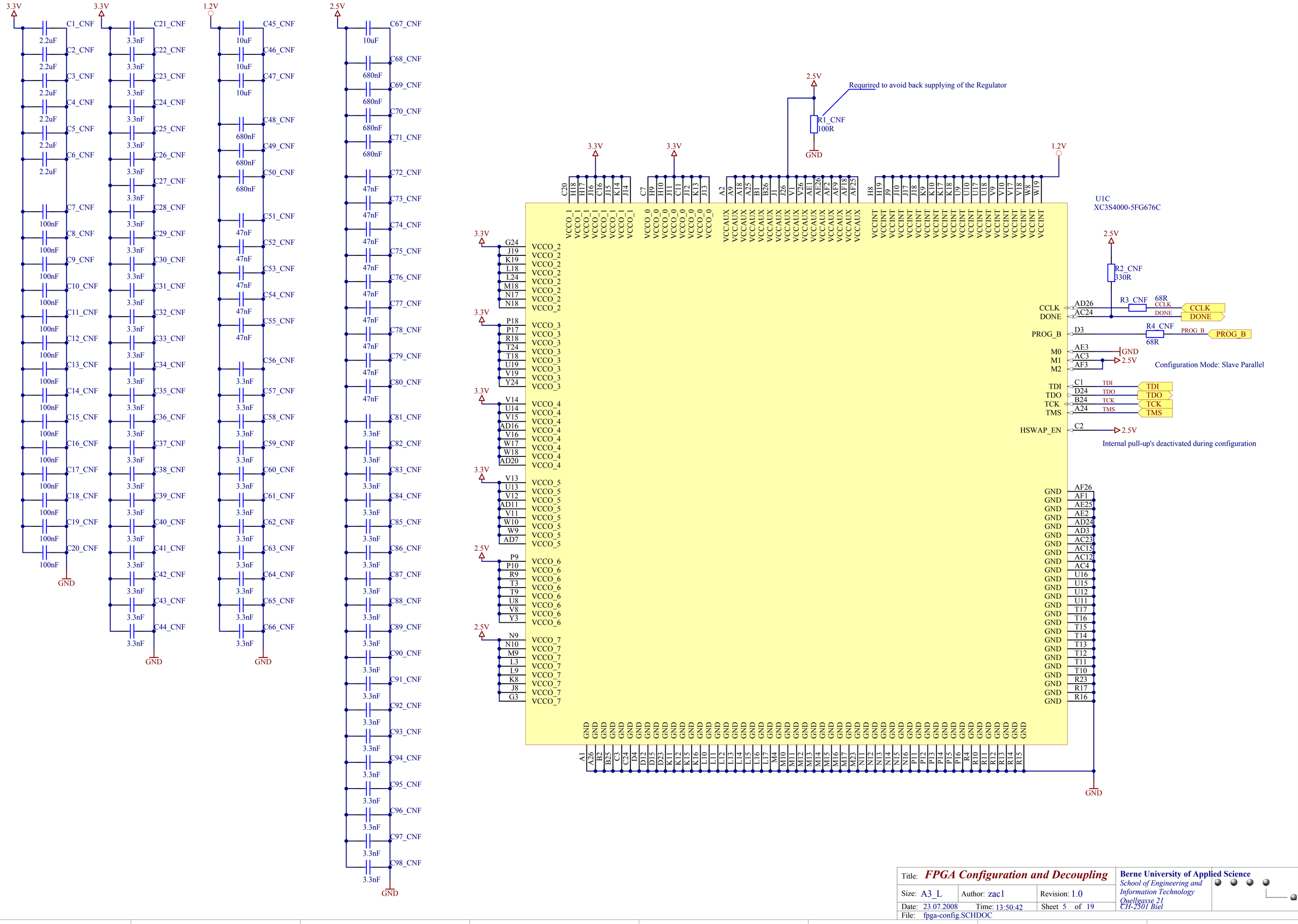
Title:	FPGA First Part
Size: A2_L	Author: zac1
Date: 23.07.2008	Time: 13:50:41
File: fpga1.SchDoc	Revision: 1.0
	Sheet 3 of 19

Berne University of Applied Science
School of Engineering and Information Technology
Quellgasse 21
CH-2501 Biel



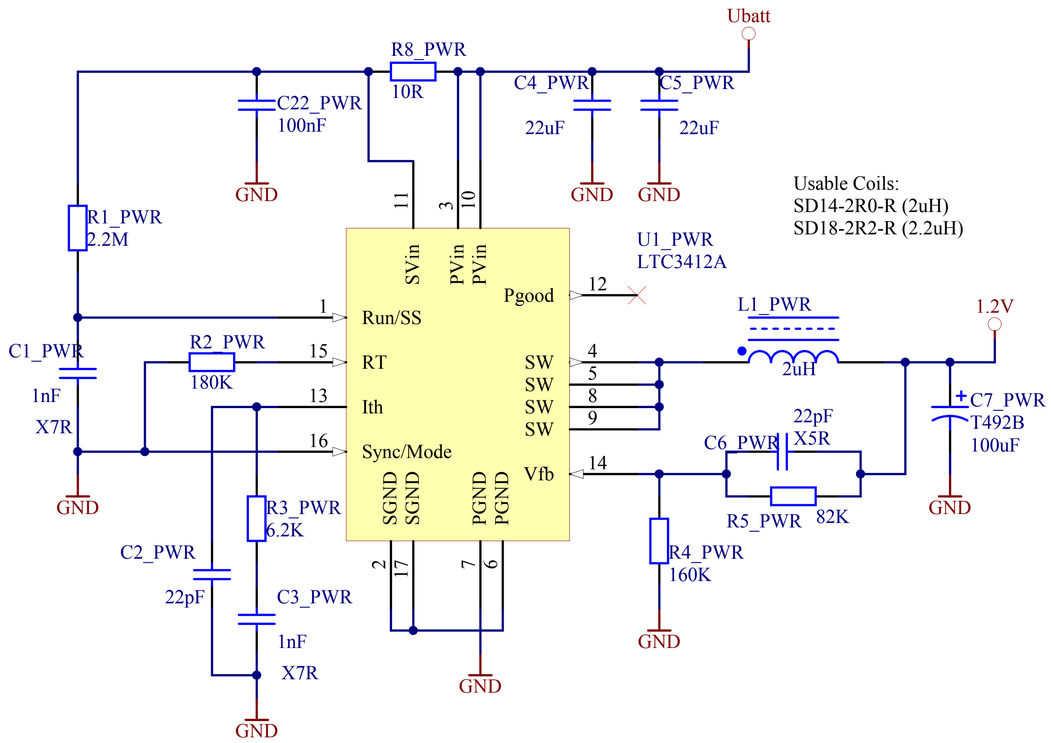


Title: *FPGA Second Part*			**Berne University of Applied Science**
Size: A2_L	Author: zac1	Revision: 1.0	*School of Engineering and Information Technology*
Date: 23.07.2008	Time: 13:50:41	Sheet 4 of 19	*Quellgasse 21*
File: fpga2.SCHDOC			*CH-2501 Biel*

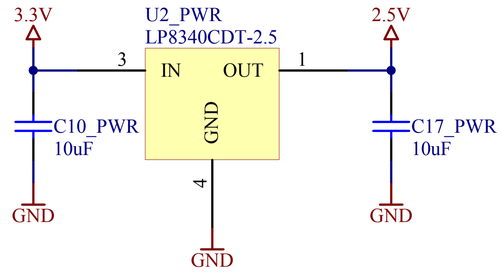


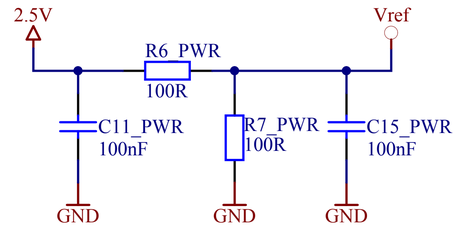
Title:	*FPGA Configuration and Decoupling*	**Berne University of Applied Science**	
Size: A3_L	Author: zac1	Revision: 1.0	*School of Engineering and Information Technology*
Date: 23.07.2008	Time: 13:50:42	Sheet 5 of 19	*Quellgasse 21*
File: fpga-config.SCHDOC			*CH-2501 Biel*

DC/DC Converter for the FPGA Core Supply, 1.2 V, 2.5 A

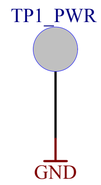


2.5 V, 0.5 A and 1.25 V Refernce Supply

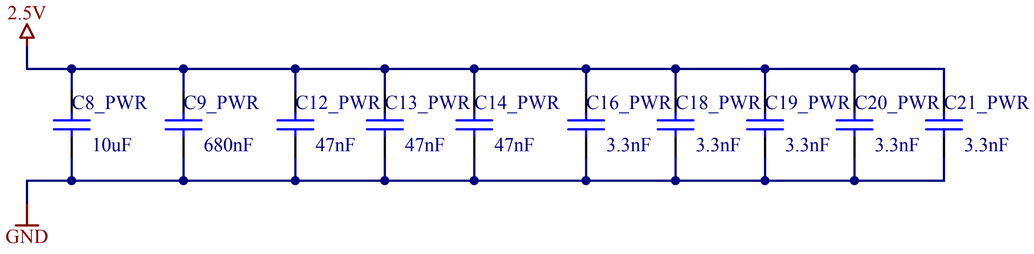




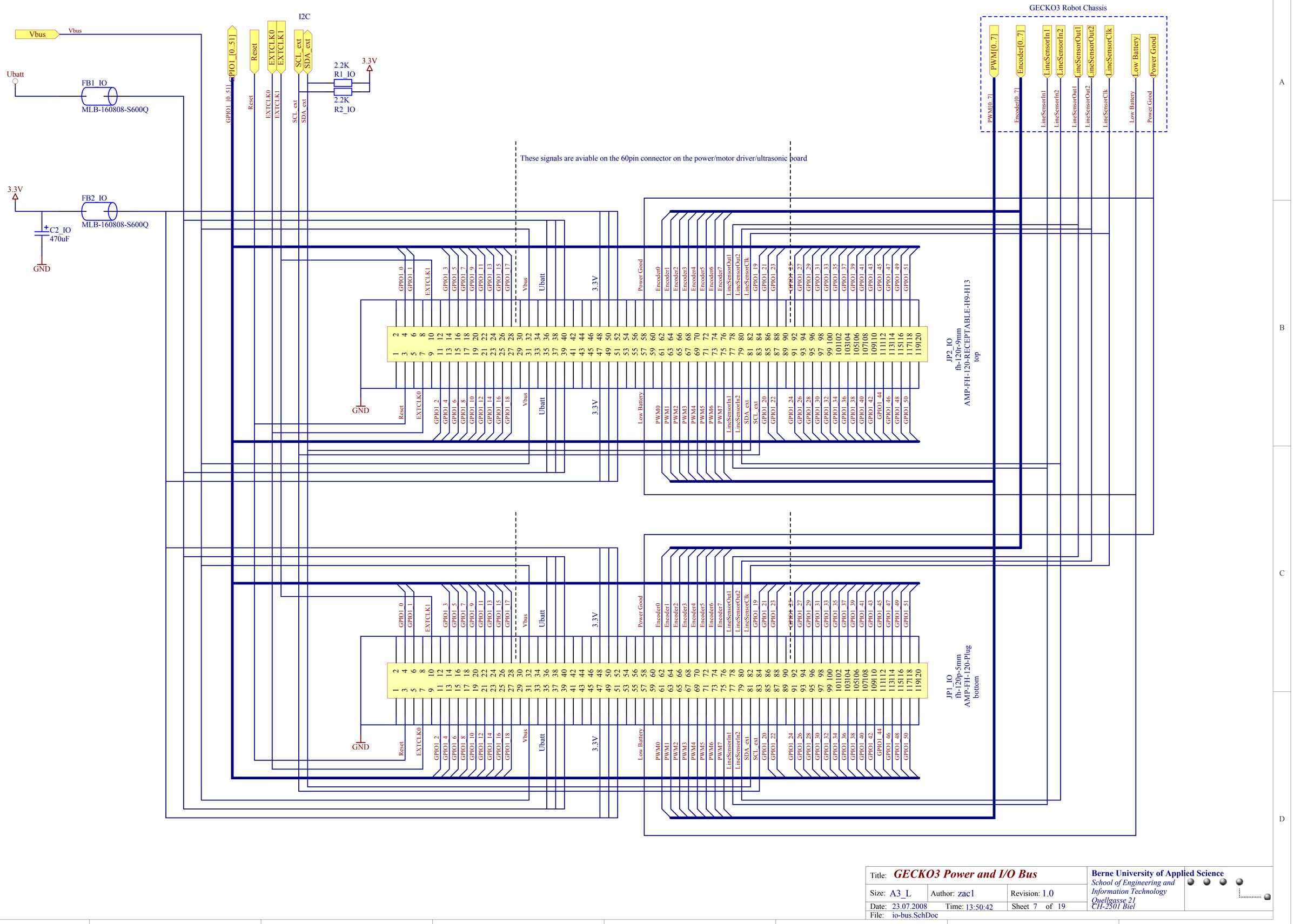
GND Testpad for Probes



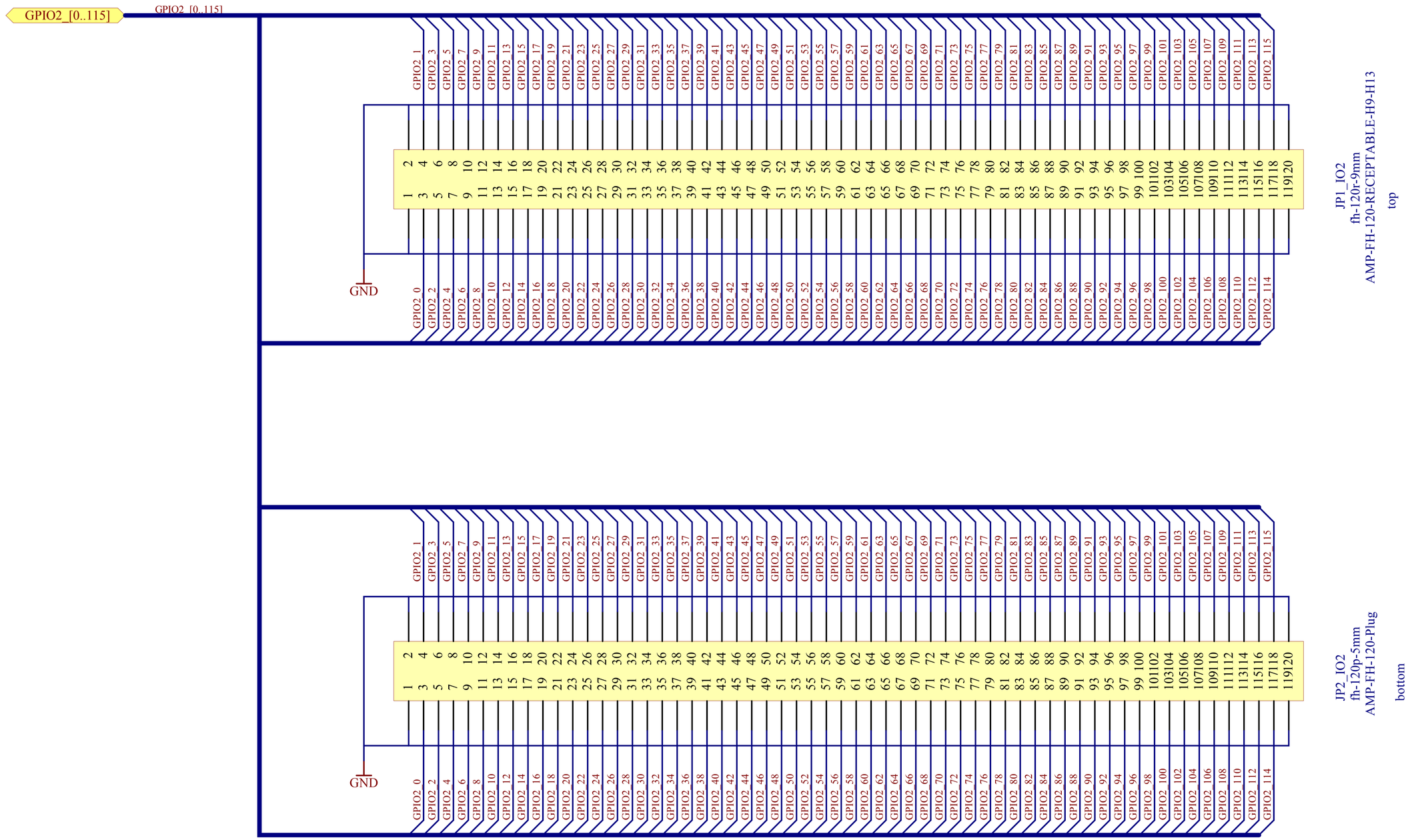
DDR SDRAM Decoupling



Title: ***Power Suplies***			**Berne University of Applied Science**
Size: A4_L	Author: zac1	Revision: 1.0	*School of Engineering and Information Technology*
Date: 23.07.2008	Time: 13:50:42	Sheet 6 of 19	*Quellgasse 21*
File: power.SCHDOC			*CH-2501 Biel*

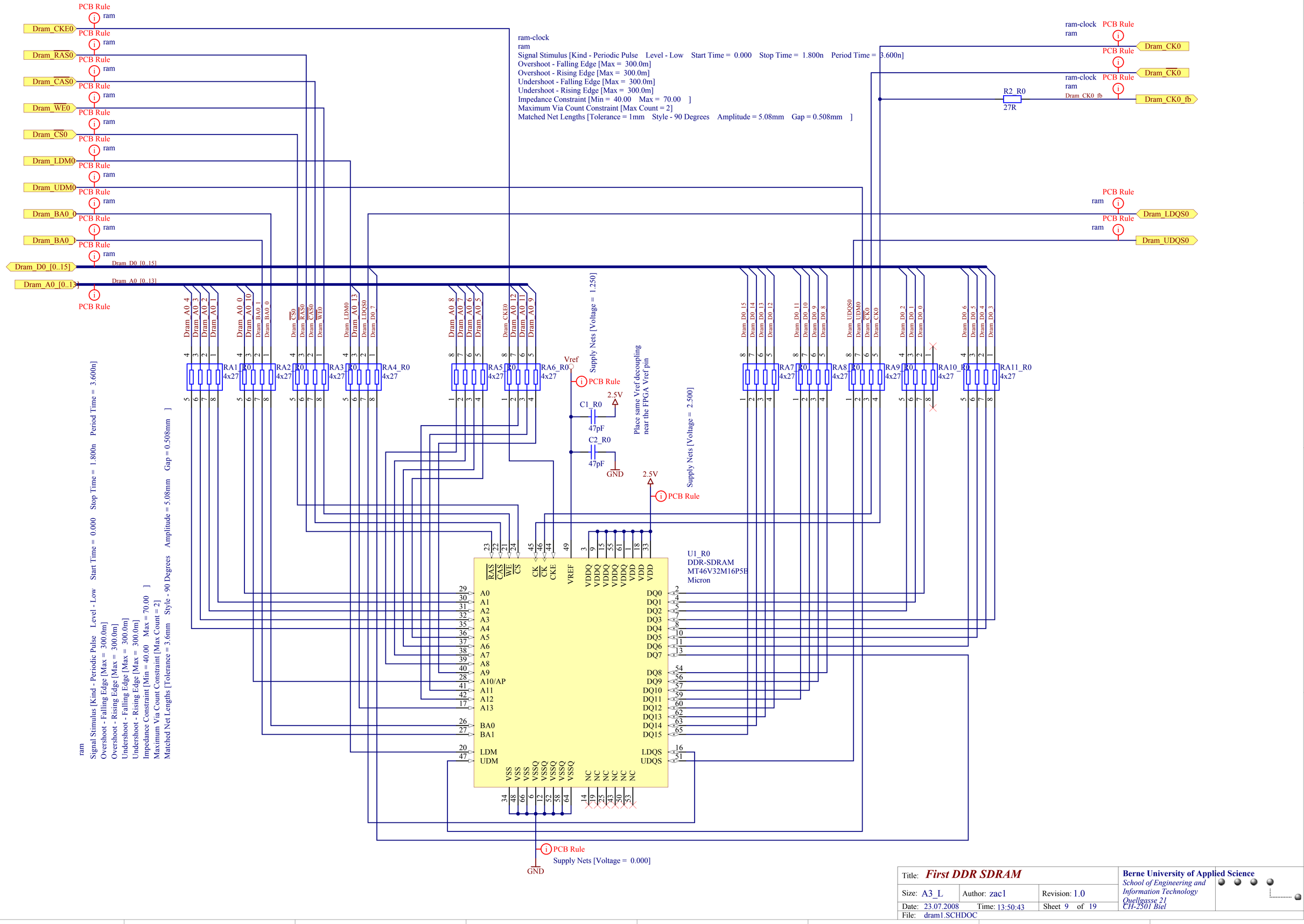


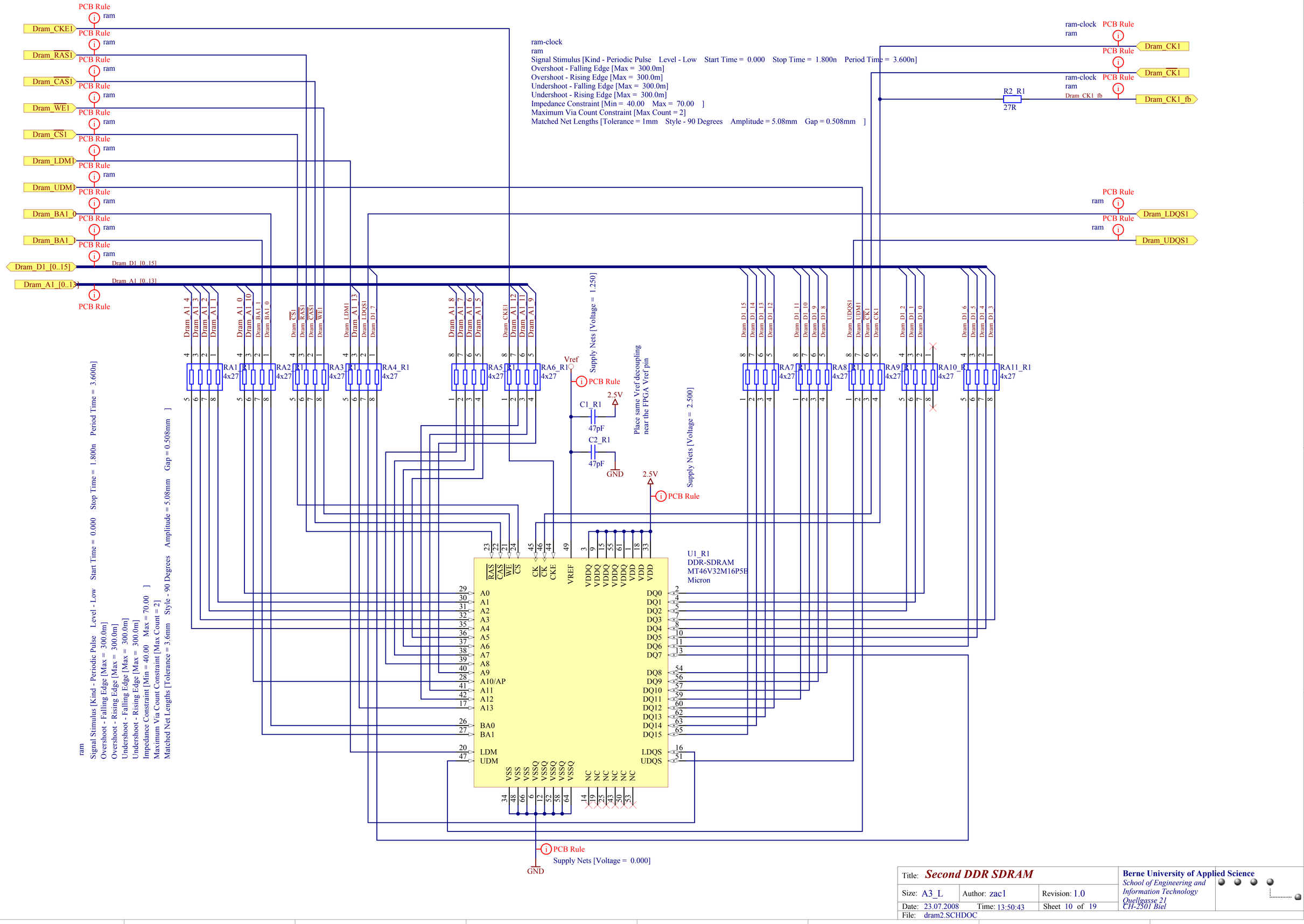
Title:	***GECKO3 Power and I/O Bus***		**Berne University of Applied Science**
Size: A3_L	Author: zac1	Revision: 1.0	*School of Engineering and Information Technology*
Date: 23.07.2008	Time: 13:50:42	Sheet 7 of 19	*Quellgasse 21*
File: io-bus.SchDoc			*CH-2501 Biel*



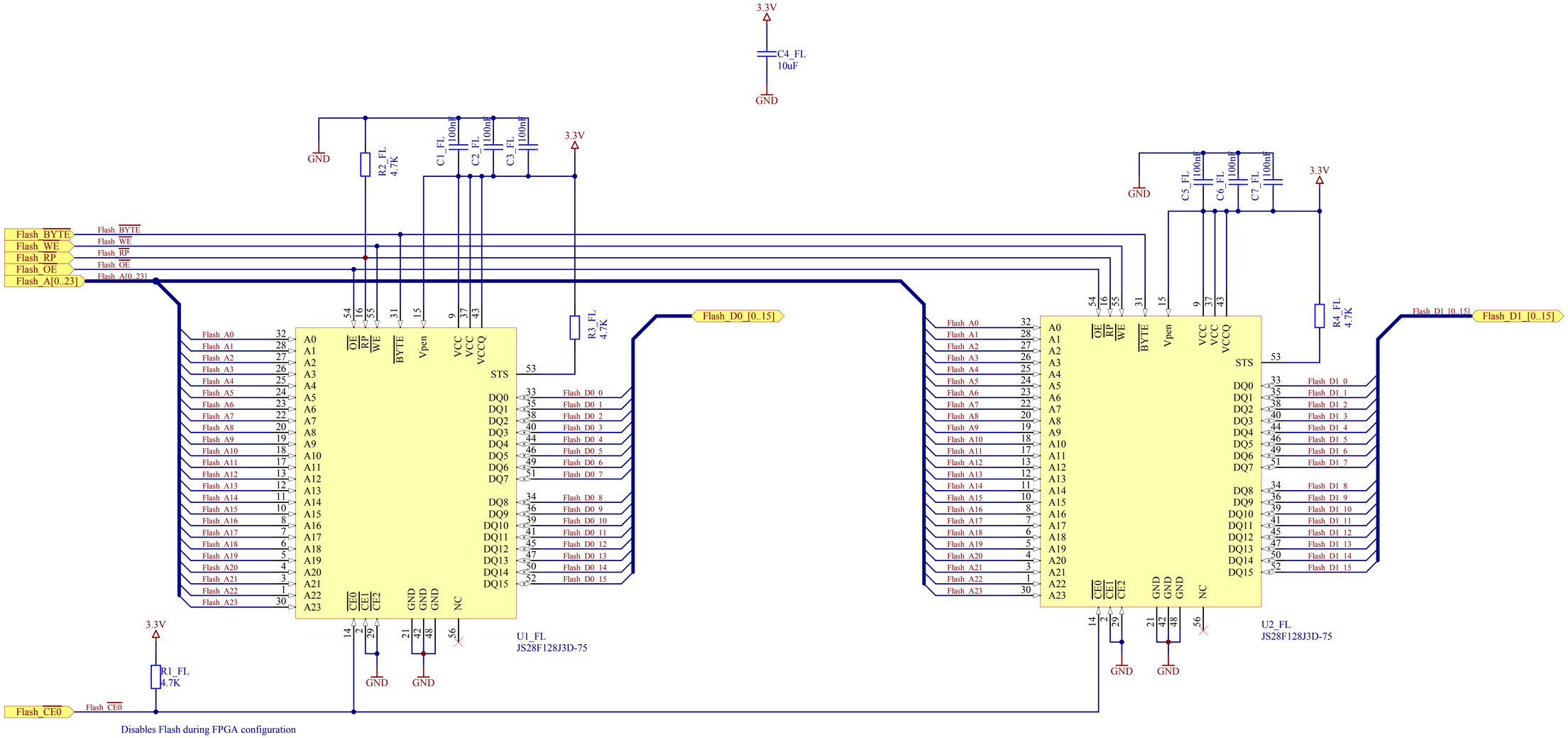
Title: *GECKO3 System and I/O Bus*		**Berne University of Applied Science**
Size: A4_L	Author: zac1	Revision: 1.0
Date: 23.07.2008 Time: 13:50:43		Sheet 8 of 19
File: io-bus2.SchDoc		

School of Engineering and Information Technology
Quellgasse 21
CH-2501 Biel

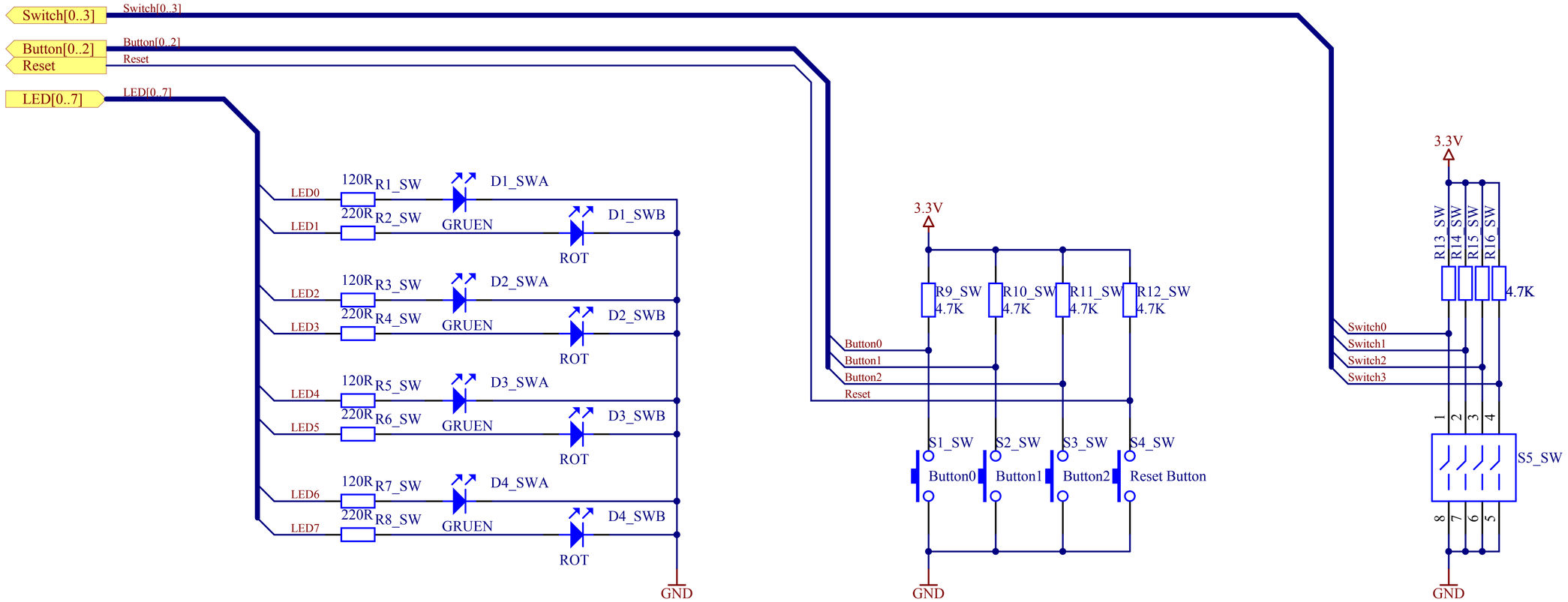

ram-clock
ram
Signal Stimulus [Kind - Periodic Pulse Level - Low Start Time = 0.000 Stop Time = 1.800n Period Time = 3.600n]
Overshoot - Falling Edge [Max = 300.0m]
Overshoot - Rising Edge [Max = 300.0m]
Undershoot - Falling Edge [Max = 300.0m]
Undershoot - Rising Edge [Max = 300.0m]
Impedance Constraint [Min = 40.00 Max = 70.00]
Maximum Via Count Constraint [Max Count = 2]
Matched Net Lengths [Tolerance = 1mm Style - 90 Degrees Amplitude = 5.08mm Gap = 0.508mm]
Dram_CKE0
Dram_RAS0
Dram_CAS0
Dram_WE0
Dram_CS0
Dram_LDM0
Dram_UDM0
Dram_BA0_0
Dram_BA0_
Dram_D0_[0..15]
Dram_A0_[0..13]
Dram_CK0
Dram_CK0
Dram_CK0_fb
Dram_LDQS0
Dram_UDQS0
R2_R0
27R
RA1_R0 4x27
RA2_R0 4x27
RA3_R0 4x27
RA4_R0 4x27
RA5_R0 4x27
RA6_R0 4x27
RA7_R0 4x27
RA8_R0 4x27
RA9_R0 4x27
RA10_R0 4x27
RA11_R0 4x27
Vref
Supply Nets [Voltage = 1.250]
Supply Nets [Voltage = 2.500]
Supply Nets [Voltage = 0.000]
Place same Vref decoupling near the FPGA Vref pin
C1_R0
47pF
C2_R0
47pF
2.5V
GND
U1_R0
DDR-SDRAM
MT46V32M16P5B
Micron
RAS
CAS
WE
CS
CK
CK
CKE
VREF
VDDQ
VDDQ
VDDQ
VDDQ
VDDQ
VDD
VDD
VDD
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12
A13
BA0
BA1
LDM
UDM
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
LDQS
UDQS
VSS
VSS
VSS
VSSQ
VSSQ
VSSQ
VSSQ
VSSQ
NC
NC
NC
NC
NC
NC
PCB Rule
ram
ram-clock
Title: First DDR SDRAM
Size: A3_L
Author: zac1
Revision: 1.0
Date: 23.07.2008
Time: 13:50:43
Sheet 9 of 19
File: dram1.SCHDOC
Berne University of Applied Science
School of Engineering and Information Technology
Quellgasse 21
CH-2501 Biel


ram-clock
ram
Signal Stimulus [Kind - Periodic Pulse Level - Low Start Time = 0.000 Stop Time = 1.800n Period Time = 3.600n]
Overshoot - Falling Edge [Max = 300.0m]
Overshoot - Rising Edge [Max = 300.0m]
Undershoot - Falling Edge [Max = 300.0m]
Undershoot - Rising Edge [Max = 300.0m]
Impedance Constraint [Min = 40.00 Max = 70.00]
Maximum Via Count Constraint [Max Count = 2]
Matched Net Lengths [Tolerance = 1mm Style - 90 Degrees Amplitude = 5.08mm Gap = 0.508mm]
R2_R1
27R
Dram_CK1_fb
Dram_CK1
Dram_LDQS1
Dram_UDQS1
Dram_CKE1
Dram_RAS1
Dram_CAS1
Dram_WE1
Dram_CS1
Dram_LDM1
Dram_UDM1
Dram_BA1_0
Dram_BA1_1
Dram_D1_[0..15]
Dram_A1_[0..13]
RA1_R1 4x27
RA2_R1 4x27
RA3_R1 4x27
RA4_R1 4x27
RA5_R1 4x27
RA6_R1 4x27
RA7_R1 4x27
RA8_R1 4x27
RA9_R1 4x27
RA10_R1 4x27
RA11_R1 4x27
Vref
Supply Nets [Voltage = 1.250]
Place same Vref decoupling
near the FPGA Vref pin
C1_R1
47pF
C2_R1
47pF
2.5V
GND
Supply Nets [Voltage = 2.500]
U1_R1
DDR-SDRAM
MT46V32M16P5B
Micron
RAS
CAS
WE
CS
CK
CK
CKE
VREF
VDDQ
VDD
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12
A13
BA0
BA1
LDM
UDM
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
LDQS
UDQS
VSS
VSSQ
NC
Supply Nets [Voltage = 0.000]
Title: Second DDR SDRAM
Size: A3_L
Author: zac1
Revision: 1.0
Date: 23.07.2008
Time: 13:50:43
Sheet 10 of 19
File: dram2.SCHDOC
Berne University of Applied Science
School of Engineering and
Information Technology
Quellgasse 21
CH-2501 Biel

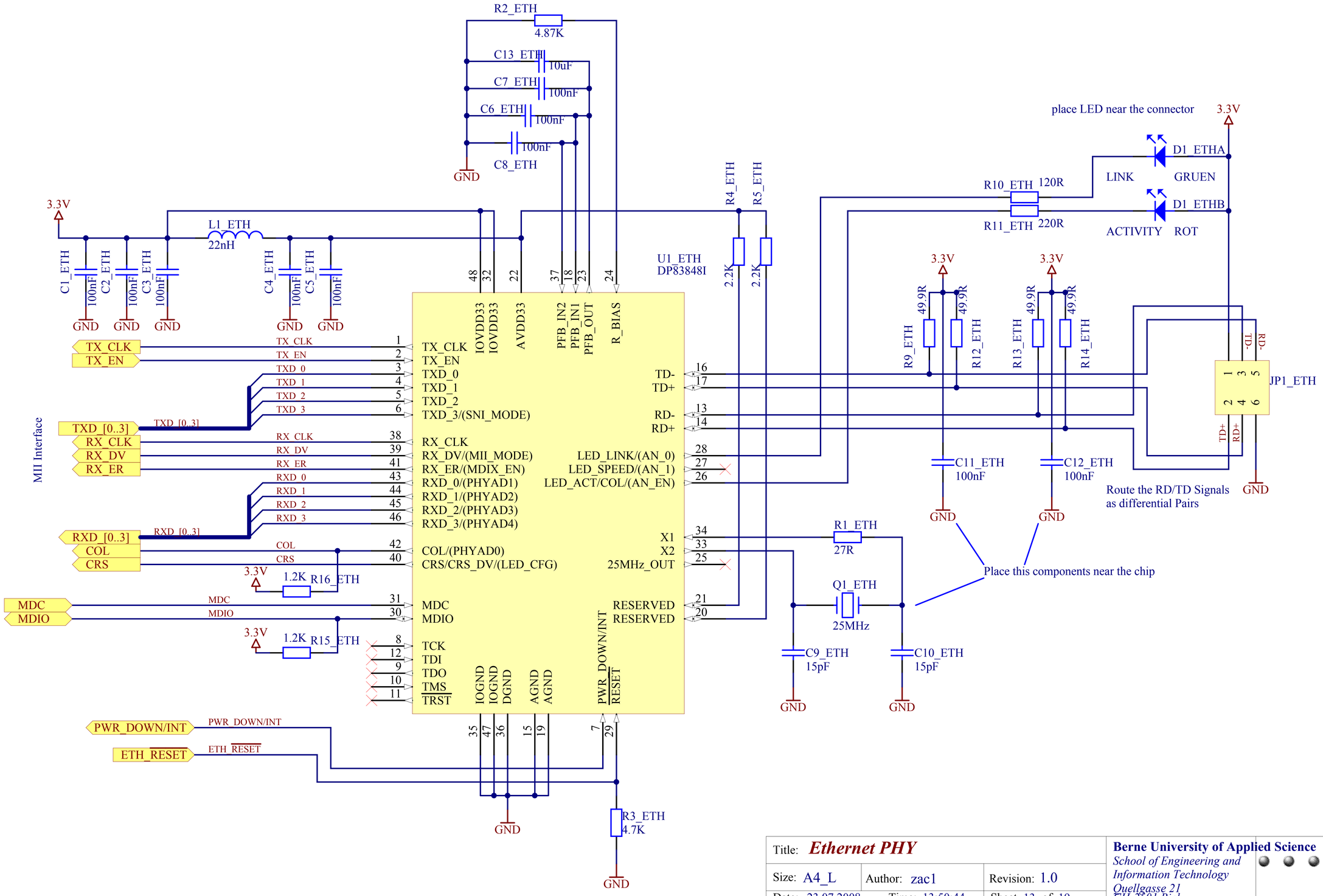
Bulk Capacitor for both Flash Chips



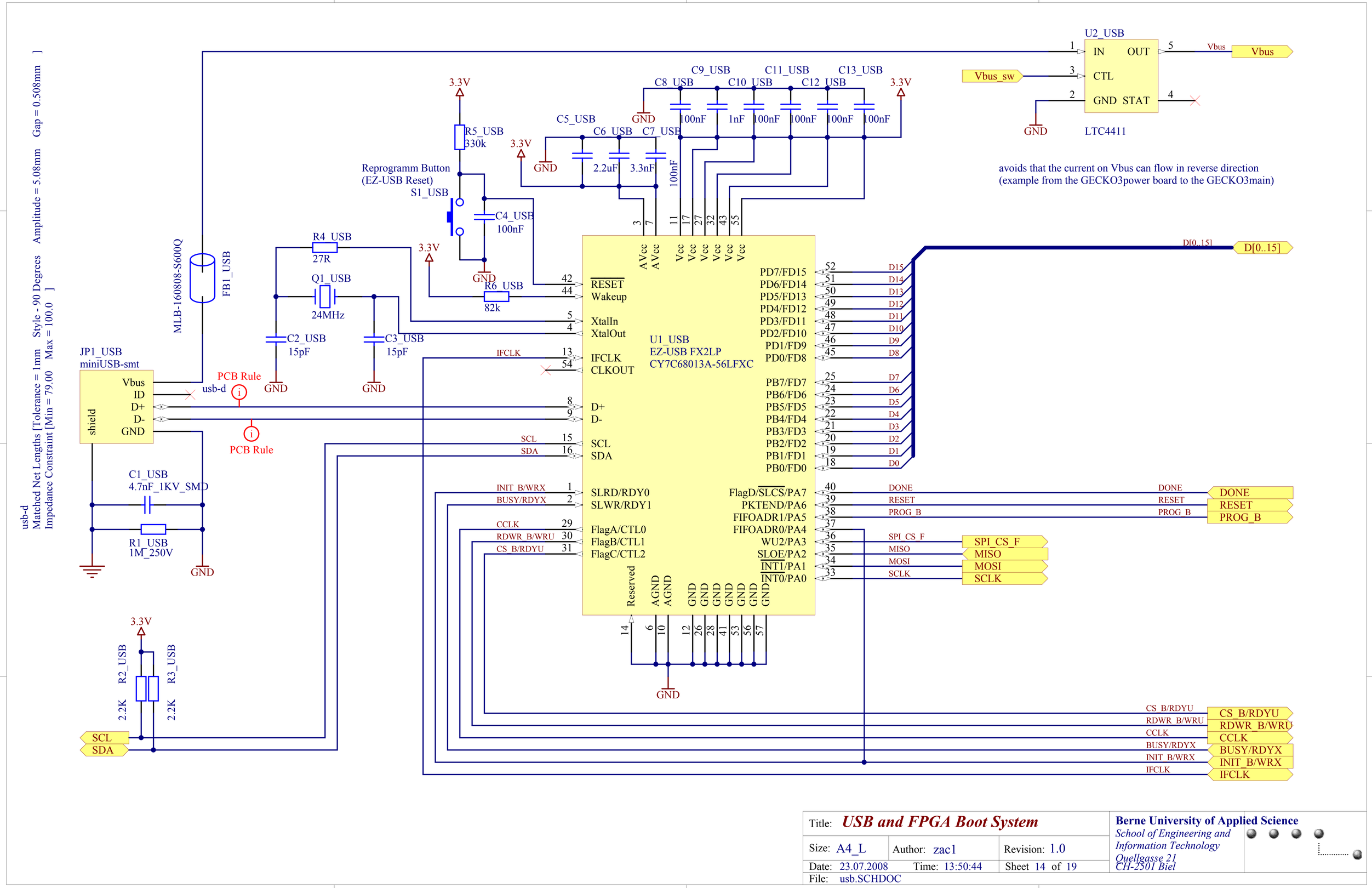
Title: ***NOR Flash***			**Berne University of Applied Science**
Size: A3_L	Author: zac1	Revision: 1.0	*School of Engineering and Information Technology*
Date: 23.07.2008	Time: 13:50:44	Sheet 11 of 19	*Quellgasse 21*
File: flash.SchDoc			*CH-2501 Biel*



Title:	***Switches and LEDs***		**Berne University of Applied Science**
Size: A4_L	Author: zac1	Revision: 1.0	*School of Engineering and Information Technology*
Date: 23.07.2008	Time: 13:50:44	Sheet 12 of 19	*Quellgasse 21*
File: switches.SchDoc			*CH-2501 Biel*

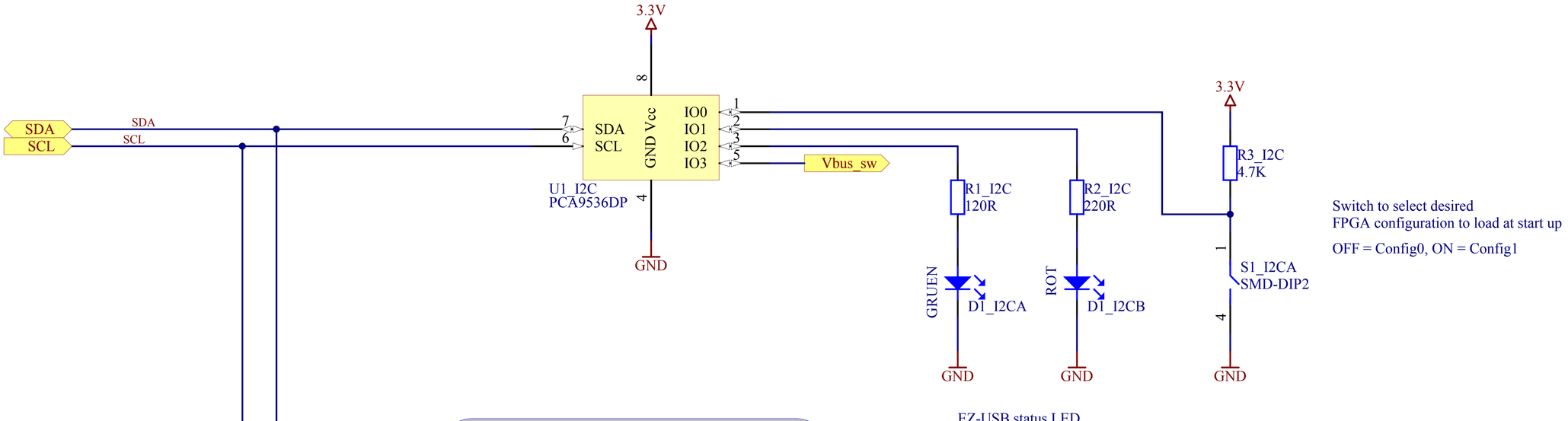


Title:	***Ethernet PHY***		**Berne University of Applied Science**
Size: A4_L	Author: zac1	Revision: 1.0	*School of Engineering and Information Technology*
Date: 23.07.2008	Time: 13:50:44	Sheet 13 of 19	*Quellgasse 21*
File: ethernet.SCHDOC			*CH-2501 Biel*



Title: *USB and FPGA Boot System*			**Berne University of Applied Science**
Size: A4_L	Author: zac1	Revision: 1.0	*School of Engineering and Information Technology*
Date: 23.07.2008	Time: 13:50:44	Sheet 14 of 19	*Quellgasse 21*
File: usb.SCHDOC			*CH-2501 Biel*

I2C GPIO expander

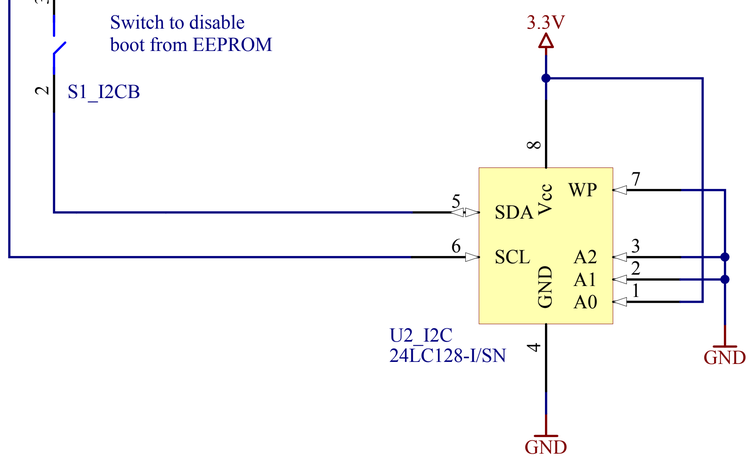


Switch to select desired
FPGA configuration to load at start up

OFF = Config0, ON = Config1

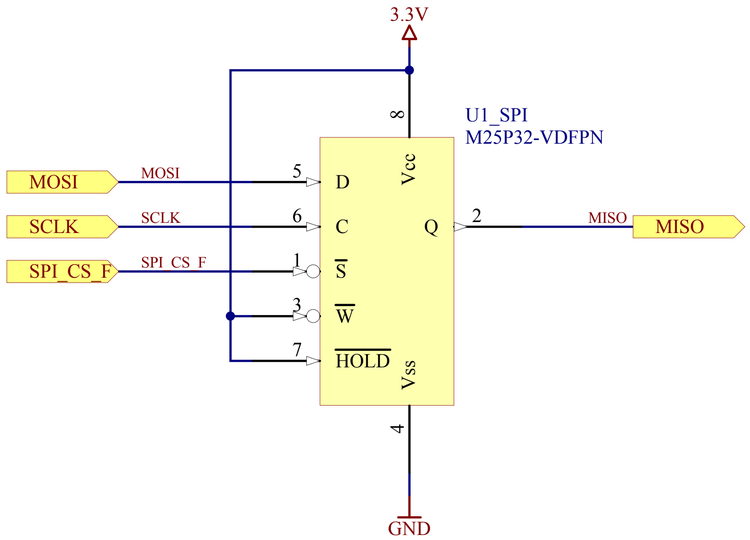
EZ-USB status LED

EEPROM to store the EZ-USB firmware



Title: ***I2C Devices***			**Berne University of Applied Science** *School of Engineering and Information Technology Quellgasse 21 CH-2501 Biel*
Size: A4_L	Author: zac1	Revision: 1.0	
Date: 23.07.2008	Time: 13:50:45	Sheet 15 of 19	
File: i2c.SchDoc			

SPI Flash to store FPGA configurations



The SPI Flash is used to store the configuration bit file for the FPGA.

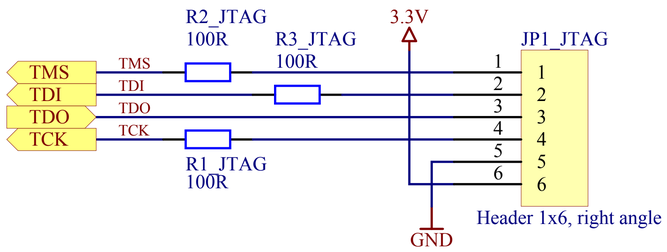
The EZ-USB configures the FPGA in the case of a stand-alone system. With this solution no Xilinx plattform flash is required.

The memory size of the SPI Flash is twice the size of a configuration bit file. This allows to store a backup/fallback FPGA configuration file onboard.
So also after a wrong update the system is still usable.
The second configuration file space could also be used to store a selftest programm.

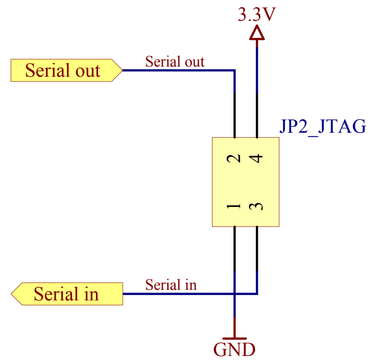
Which configuration is loaded on start-up is selected by the user with one of the DIP switches.

Title: ***SPI Serial Flash***			**Berne University of Applied Science**
Size: A4_L	Author: zac1	Revision: 1.0	*School of Engineering and Information Technology*
Date: 23.07.2008	Time: 13:50:45	Sheet 16 of 19	*Quellgasse 21*
File: spi-flash.SchDoc			*CH-2501 Biel*

JTAG Connector for the Digilent Programming Cables



Connector for serial communication like RS232



Title: *JTAG and RS232 Connector*			**Berne University of Applied Science** *School of Engineering and Information Technology* *Quellgasse 21* *CH-2501 Biel*
Size: A4_L	Author: zac1	Revision: 1.0	
Date: 23.07.2008	Time: 13:50:45	Sheet 17 of 19	
File: jtag.SchDoc			