Active-HDL PDF Export
design0 design

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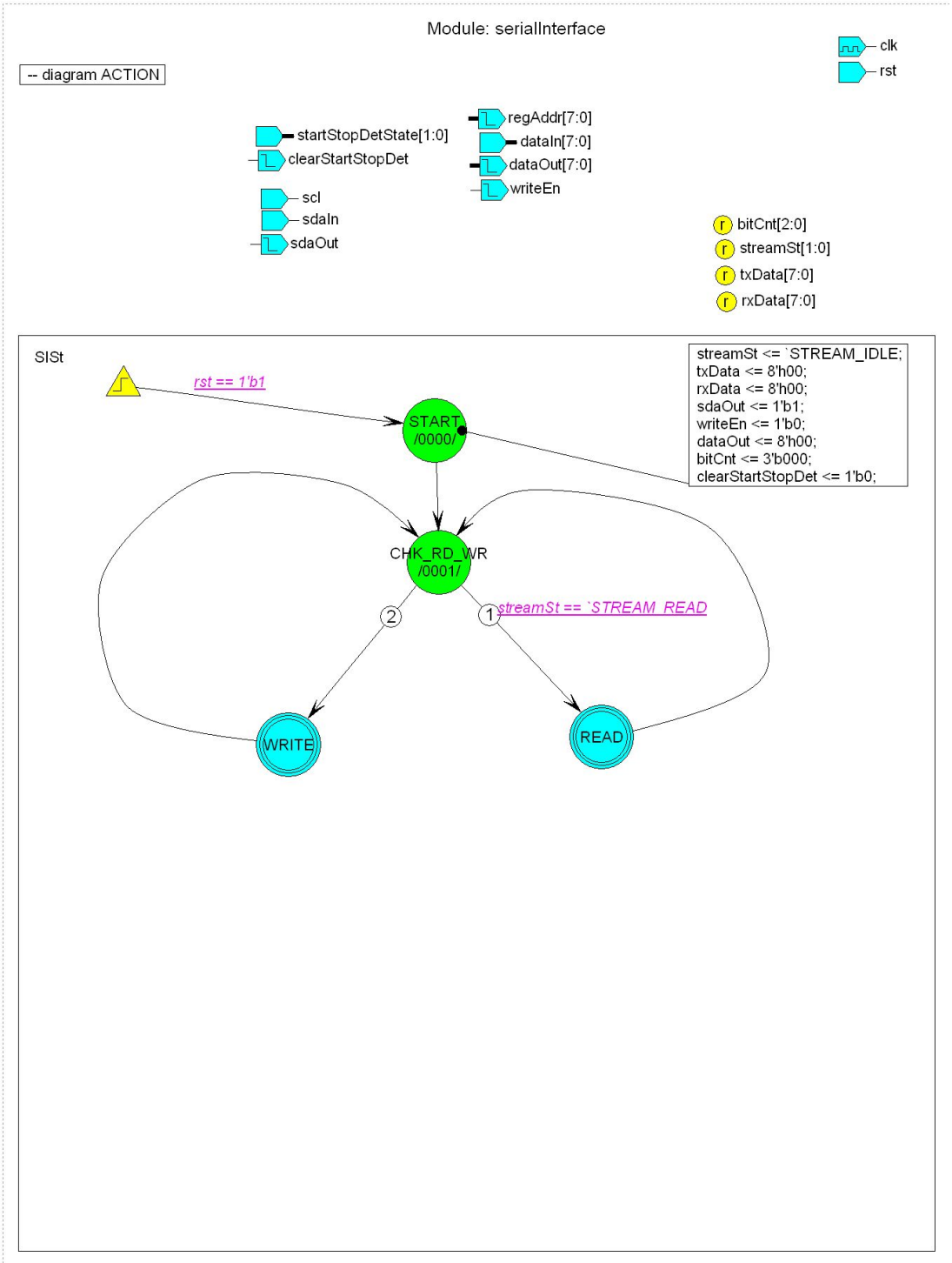
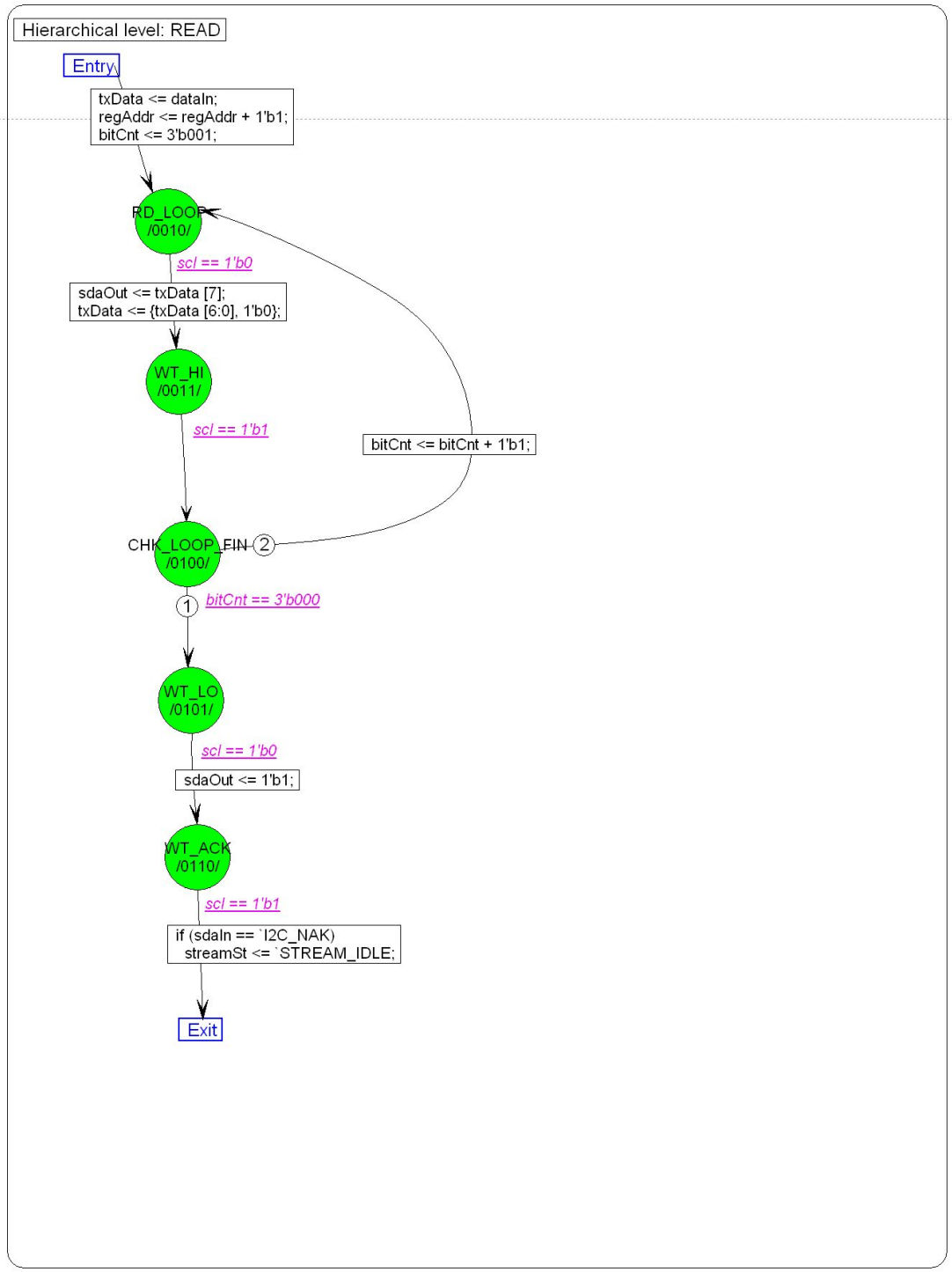
2 design0

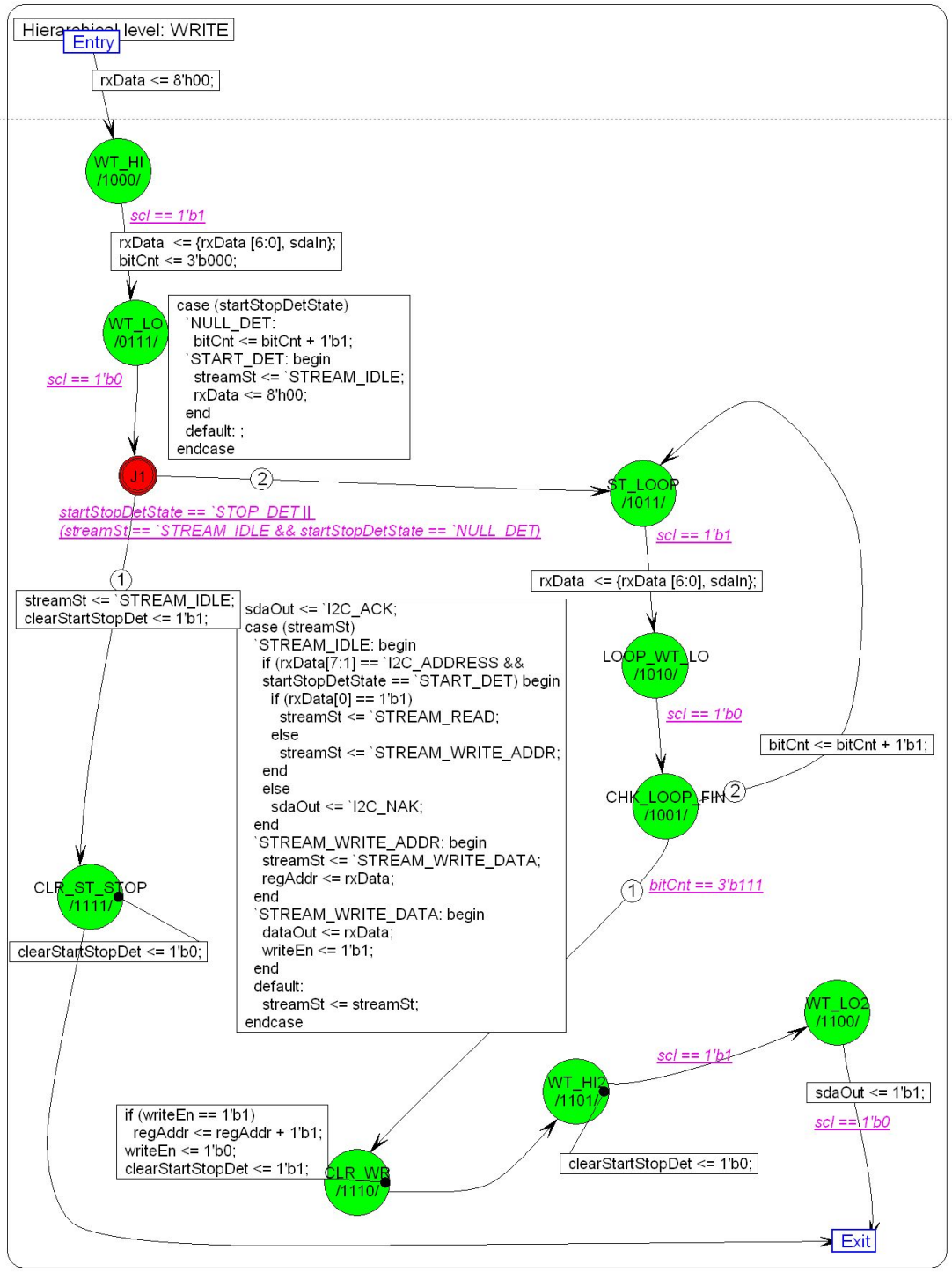
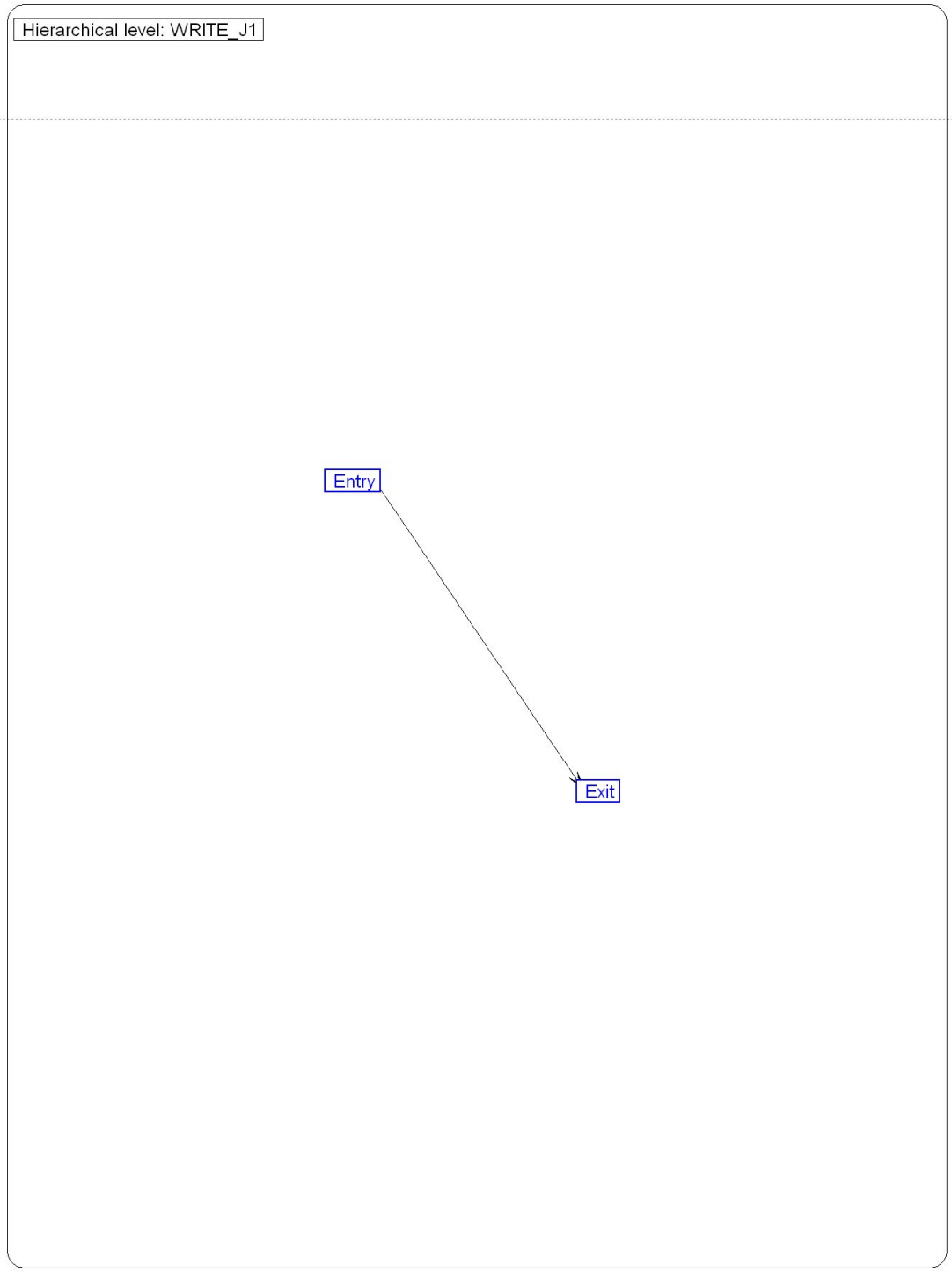
2.1 serialInterface.asf



2.1.1 READ


Hierarchical level: READ
Entry
txData <= dataIn;
regAddr <= regAddr + 1'b1;
bitCnt <= 3'b001;
RD_LOOP
/0010/
scl == 1'b0
sdaOut <= txData [7];
txData <= {txData [6:0], 1'b0};
WT_HI
/0011/
scl == 1'b1
bitCnt <= bitCnt + 1'b1;
CHK_LOOP_FIN
/0100/
2
1
bitCnt == 3'b000
WT_LO
/0101/
scl == 1'b0
sdaOut <= 1'b1;
WT_ACK
/0110/
scl == 1'b1
if (sdaIn == `I2C_NAK)
streamSt <= `STREAM_IDLE;
Exit

2.1.2 WRITE


Hierarchical level: WRITE
Entry
rxData <= 8'h00;
WT_HI
/1000/
scl == 1'b1
rxData <= {rxData [6:0], sdaIn};
bitCnt <= 3'b000;
WT_LO
/0111/
case (startStopDetState)
`NULL_DET:
bitCnt <= bitCnt + 1'b1;
`START_DET: begin
streamSt <= `STREAM_IDLE;
rxData <= 8'h00;
end
default: ;
endcase
scl == 1'b0
J1
2
ST_LOOP
/1011/
startStopDetState == `STOP_DET ||
(streamSt == `STREAM_IDLE && startStopDetState == `NULL_DET)
scl == 1'b1
1
streamSt <= `STREAM_IDLE;
clearStartStopDet <= 1'b1;
sdaOut <= `I2C_ACK;
case (streamSt)
`STREAM_IDLE: begin
if (rxData[7:1] == `I2C_ADDRESS &&
startStopDetState == `START_DET) begin
if (rxData[0] == 1'b1)
streamSt <= `STREAM_READ;
else
streamSt <= `STREAM_WRITE_ADDR;
end
else
sdaOut <= `I2C_NAK;
end
`STREAM_WRITE_ADDR: begin
streamSt <= `STREAM_WRITE_DATA;
regAddr <= rxData;
end
`STREAM_WRITE_DATA: begin
dataOut <= rxData;
writeEn <= 1'b1;
end
default:
streamSt <= streamSt;
endcase
rxData <= {rxData [6:0], sdaIn};
LOOP_WT_LO
/1010/
scl == 1'b0
bitCnt <= bitCnt + 1'b1;
CHK_LOOP_FIN
/1001/
2
1
bitCnt == 3'b111
CLR_ST_STOP
/1111/
clearStartStopDet <= 1'b0;
WT_LO2
/1100/
scl == 1'b1
WT_HI2
/1101/
sdaOut <= 1'b1;
scl == 1'b0
if (writeEn == 1'b1)
regAddr <= regAddr + 1'b1;
writeEn <= 1'b0;
clearStartStopDet <= 1'b1;
CLR_WE
/1110/
clearStartStopDet <= 1'b0;
Exit

2.1.2.1 J1