## mod\_sim\_exp\_core memory mapping

(Word adressing)

	1FFh
unused space	140h
M 2048 bits	100h
OP3 2048 bits	
OP2 2048 bits	rw_ad
OP1 2048 bits	080h
OP0	040h
2048 bits	000h

M / OP	OPE	RAND	WORD ADDRESS				1		
8	7	6	5	4	3	2	1	0	7

address structure:

bit: 8 -> '1': modulus

'0': operands

bits: 7-6 -> operand select in case of bit 8 = '0' don't care in case of modulus

don't care in case of modulus

bits:  $5-0 \rightarrow modulus addr / operand addr resp.$