A VERTICALLY INTEGRATED TEST METHODOLOGY BASED ON JTAG IEEE 1149.1 STANDARD INTERFACE

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Abstract

A vertically integrated test methodology has been developed for ASIC testing based on the IEEE 1149.1 Standard Test Interface. A common interface is used to test at the wafer, packaged-chip and board/system levels. The Boundary Scan JTAG interface is combined with an internal full scan based test technique to provide a uniform test procedure at all stages of testing. At the prototype debug phase, the test circuitry is configured to test for design and process faults. At the manufacturing stage, it allows for efficient wafer sorting and packaged chip testing. At the board/system level, the same test set used at the wafer and package levels can be employed for Incoming-Inspection of parts and In-Circuit-Testing. In addition to basic scan testing, the protocol can perform AC/Delay-fault testing. For embedded megacell and RAM module testing it is configured to control and operate an independent BIST scheme inside the ASIC device to achieve At-Speed testing. This test methodology has been implemented on practical ASIC parts. The area overhead for the Boundary Scan architecture is on the order of a few percent for 30-50K gate designs, and depending on the type of implementation, peformance overhead varies from minimal to no penalty at the I/O cells.

I. Introduction

This paper presents a vertically integrated test methodology developed for ASIC testing based on the IEEE 1149.1 Standard Test Interface. The JTAG test protocol is augmented to accomplish testing at the wafer, packaged chip and the board/system levels. Since JTAG is primarily a board-level test solution, in order to encompass a broader spectrum of test features, the JTAG instruction set was expanded and the internal test logic circutry redesigned. The test methdology uses an internal full-scan based DFT technique and a robust I/O level testing procedure using the Boundary Scan Ring. In order to allow for Delay-fault testing, AC testing functions are included in the test protocol. For embedded megacells and RAM module testing, a Built-In Self Test (BIST) scheme is developed to provide for At-Speed testing and high fault coverage.

The following is a description of the test objectives & techniques used at all 3 phases of a chip's life cycle and the design/implementation of various chip-level test functions using the JTAG test protocol. Section II describes design enhancements to the protocol and the functional operation of scan test. Sections III, IV and V present the scan test procedures used at the wafer, package and board/system levels. The RAM BIST operations and megacell testing are described in Section VI. The practical results obtained over several implementations on various gate array families are discussed in Section VII. Finally, the conclusion is presented in Section VIII.

II. Enhanced Test Protocol

The Vertex ASIC design flow is based on a rigorous test methodology. The test protocol involves a full internal scan DFT methodology coupled with extensive features at the pin I/Os to perform a thorough wafer and package test sequence. An internally developed program, the Test-Logic-Insertion (TLI) software, automatically inserts the scan FFs in the core design so as to make the scan design process completely transparent to the customer. All Vertex chips include a ring oscillator function, controlled by the test macro, formed out of the external and internal scan chains for performance characterization of the part. For megacells and RAM modules, a BIST structure is provided which is also controlled by the test macro. Additionally, a patented master-scan latch design that allows for delay-fault testing is also provided. All these features have been designed into the JTAG protocol in order to maintain a uniform test interface at all levels of chip testing. This was achieved by adding private instructions to the JTAG basic instruction set and enhancing the boundary scan cell design.

Instruction	Description
BYPASS	Required by 1149.1
EXTEST	Required by 1149.1
SAMPLE/PRELOAD	Required by 1149.1
INTEST	Optional
IDCODE	Optional
INTSCAN(M)	Chip-on-Board Internal Scan
INPLACEIN	Chip-on-Board BSR Scanin
INPLACEOUT	Chip-on-Board BSR Scanout
WFRINTSCAN(M)	Wafer Internal Scan
WFRSCANIN	Wafer BSR Scanin
WFRSCANOUT	Wafer BSR Scanout
INTSCANP(M)	Package Internal Scan
INTROSC	Internal Scan Ring Oscillator
EXTROSC	External Scan Ring Oscillator

Table 1: Vertex Test Instructions

A total of 12 private instructions (9 + 3 for Master Scan), as shown in Table 1 were added. The instruction register size was expanded to 5 bits. (It is assumed that the readers are familiar with the operation and functionality of the JTAG protocol and hence no attempt has been made to describe the logic details of the protocol. Please refer to the JTAG spec for details [3].) For purposes of internal scan testing, a set of 3 individual instructions are required at the wafer and chip-on-board levels. At the wafer level, these are WFRSCANIN, WFRINTSCAN(M) and WFRSCANOUT. At the board level, these are INPLACEIN, INTSCAN(M) and INPLACEOUT. The requirement for internal scan testing dictates the use of only the *update* function during the external ring scanin and the use of only the *capture* function during the external ringscanout. Since the TAP controller state diagram requires passing through both the *capture-DR* and *update-DR* during any single TDR sequence, separate intructions were devised to handle the *capture* and *update* functions in different sequences. The difference between wafer scan test and chip-on-board scan test instructions is as follows: during wafer test, the signal is driven and observed through the I/O pads thereby providing a rigorous coverage of the I/O drivers, buffers and their control signals; during chip-on-board scan test, the signal is driven into the chip directly from the *update* stage and captured directly into the *capture* stage of the boundary scan cell, thereby bypassing the I/O area completely. Figure 1 shows the logic diagram of a generic Vertex Boundary Scan cell. At the package level, since the tester provides a broadside stimulus to the primary inputs and outputs, only one instruction, INTSCANP(M), is required to achieve internal scan testing.

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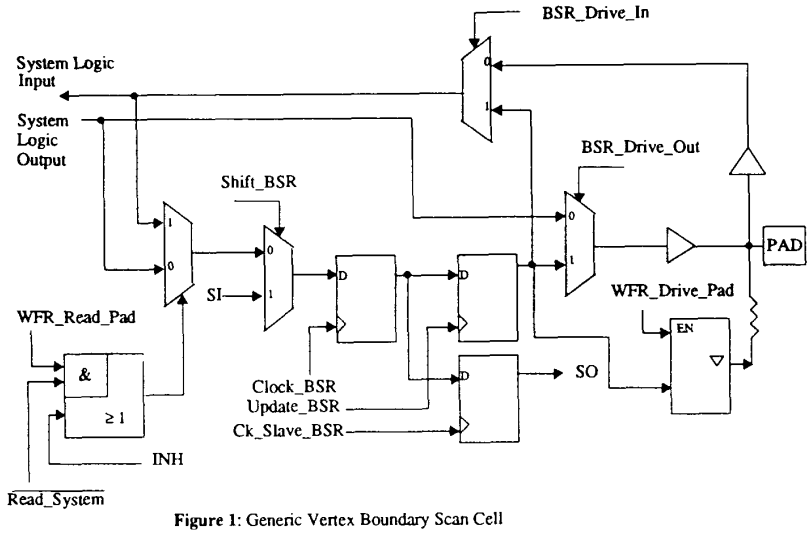

Figure 1: Generic Vertex Boundary Scan Cell

In addition to scan testing, the three internal scan instructions, WFRINTSCAN(M), INTSCAN(M) and INTSCANP(M), are also used to control the BIST circuitry for megacells and RAM modules in the Run-Test/Idle state. The INTROSC and EXTROSC instructions are used to configure the scan chains into ring oscillator functions for performance characterization.

III. Wafer Testing/Sorting

The scan test is essentially achieved by use of the 3 wafer scan test instructions as mentioned in the previous section. At WFRSCANIN, the stimulus loaded into the update stage of boundary scan cells is driven through the pad by use of the *wfr_drive_pad* signal shown in Figure 1. The cell configuration allows for the stimulus to be received by the core logic directly from the pad. The control is held in this state until the TAP controller is brought to the Run-Test/Idle state in the WFRSCANOUT instruction. After WFRSCANIN, the internal scan ring is loaded using the WFRINTSCAN(M) instruction. This is followed by the WFRSCANOUT instruction when the *wfr_read_pad* signal is activated to capture the value on the pad being driven out of the core logic due to the vector loaded into the internal scan chain. The capture takes place in the *capture-DR* state, by which time the *wfr_drive_pad* signal has long been turned off. The TAP controller is then shifted into the *shift-DR* state and the response vector scanned out. After returning to the Run-Test/Idle state, a system clock pulse is applied to capture the test response in the internal scan chain. The sequence is repeated for all the scan test vectors.

A special test sequence, ***dynamic clocking***, has been devised to detect the faults at the tri-statable I/O drivers and their control signals for Bi-directional and 3-state output pins at wafer test. The technique of ***dynamic clocking*** has been incorporated into the ATPG tool developed in-house at Vertex. In this test sequence, during tri-state testing, the I/O pad is driven to a certain value at WFRSCANIN through a weak driver, specially designed for this purpose. Since the output driver is in the tri-state mode, the same logic value should be captured during WFRSCANOUT for the good machine. A different value captured will detect the faulty operation of the tri-state function on the output driver. The output driver function is tested by charging the pad with an opposite value through the weak driver at WFRSCANIN. At WFRSCANOUT, the value captured for a good machine should reveal the value driven by core logic through the output driver. In the addition to the regular scan testing, the wafer test procedure also involves testing the internal and external scan chains in ring oscillator modes for performance characterization. A small parametric sampling is also done at this time. For instance, input leakage, input threshold and output drive test are also performed.

In the manufacturing environment, the benefits of a low pin count test interface are numerous. For example, a typical probe card consisting of approximately 256 probes can easily exceed several thousands of dollars. With this test methodology, the probe card costs are significantly reduced to below a few hundred dollars. The cost savings are also quite evident for repair and planerization of the probe cards. Another advantage of the low pin count interface is the ease of alignment, which can account for significant savings in test time overhead. With all pads probed, pad damage can be incurred due to repetitive probing making the packaging bond process far more costly. Other benefits lie in the cabling interface. By reducing the quantity of lines the mechanical interface is far more robust. Cable impedance qualification time (time-domain-reflectometry techniques) is also reduced thereby guaranteeing signal integrity to the DUT.

IV. Package Testing

At the package level, scan testing is accomplished with the use of only one instruction: INTSCANP(M). During package test, all boundary scan cells except the *inhibit* (enable) cell operate in a transparent mode. The major difference between the INTSCANP(M) and its wafer and chip-on-board counterparts [INTSCAN(M) & WFRINTSCAN(M)] is that in the latter cases, ATPG determines the value of the *inhibit* cell. For package test, the value in the *inhibit* cell is set manually and used to avoid conflicts at Bi-directional I/O cells that switch their direction between consecutive patterns.

Initially, the SAMPLE/PRELOAD instruction is used to load a dummy pattern with specified values at the *inhibit* cells. A dummy pattern is then applied by the tester at the device. The INTSCANP(M) instruction is then loaded and a test pattern scanned into the internal scan chain. The TAP controller is moved to the Run-Test/Idle state. In this state, a test pattern through the tester is applied at the primary inputs and outputs of the device, followed by a system clock sequence. The sequence from application of a dummy pattern to system clock application is then repeated for each scan vector. The dummy pattern is applied to protect the device from: (a) conflicts at the I/O pin due to a direction switch of a Bi-directional I/O cell caused by the change in core logic due to the system clock pulse, and/or (b) stray currents that may occur during the

internal scan sequence.

The boundary scan architecture provides for several other types of testing not otherwise easily possible at the device level. By using the *update* stage of the boundary scan cell, it is possible to test for power and ground bounce severities for several outputs switching simultaneously. Furthermore, many standard tests, such as continuity tests for opens/shorts and leakage tests can be performed by simply setting the appropriate values in the boundary scan ring without the need for an ATPG tool to figure out a correct pattern to be applied at the input of the combinational island that drives the primary I/O pins. Due to the simplicity of the interface, wafer sort tests can be cross correlated in the package environment.

V. Board/System Testing

The JTAG standard [3] specifies only the INTEST instruction to perform a broadside functional test for chip-on-board applications so as not to disturb other parts on the board. The INTEST instruction requires a special multiplexer (between the I/O pin and the core logic) that, in some implementations, can cause unacceptable performance penalties. The scan test instructions INPLACEIN and INPLACEOUT also require the presence of this multiplexer to allow internal scan testing of the device on board. However, the same set of test vectors that are used to test and qualify a part at the wafer and package levels is used at the board level in order to maintain a vertically integrated test philosophy.

Such a philosophy enables Incoming-Inspection of parts which could be essentially package level testing at the customer site. As mentioned in section III, the test signals do not flow through the I/O pad and I/O drivers at the board scan test level. Therefore, there is some loss of coverage over the faults on the control and data lines of the I/O drivers and buffers. However, due to the EXTEST instruction, this loss is compensated by any board level interconnection test sequence that would test for these faults.

The scan test sequence at this level is identical to that at the wafer level except for the use of different instructions. The initial boundary scan ring is loaded with the INPLACEIN instruction which only allows an *update* operation and no action takes place in the *capture-DR* state. The INTSCAN(M) instruction is then used to load the internal scan chain. The primary outputs' response is then *captured* using the INPLACEOUT instruction in the *capture-DR* state with no action taking place in the *update-DR* state. This is followed by a system clock pulse to capture reponses in the internal scan chain. The procedure is repeated for each scan vector for the device.

In addition to the above, the protocol offers all the advantages of rigorous testing at the board level, such as interconnection testing, glue-logic island testing, etc. for which it is designed. Moreover, the test methodology used for the board level is fully applicable to an Multi-Chip Module (MCM) scenario.

VI. Megacell/RAM and AC/Delay-fault Testing

A specially developed automation software generates BIST circuitry around the periphery of a megacell or RAM module. The BIST logic control is part of the internal scan chain, thereby enabling full control of its operation through the internal scan chain and the test macro. The BIST logic is operated in the Run-Test/Idle state of the internal scan instructions: INTSCAN(M), INTSCANP(M) and WFRINTSCAN(M). The control signals *jtst* and *jbyp* are provided through two extra scan FFs located in the BIST logic. In the functional operation mode, these FFs default to values that allow the RAM to operate in the normal mode. During regular scan test, the RAM is put in a bypass mode and during RAM test, appropriate values in these FFs allow independentmodule testing. The use of special FFs to control the test operation for each RAM module allows flexibility to perform individual module debug as well as parallel testing of several modules simultaneously. For RAM modules, the 13N algorithm [1] is used to generate the test vectors. It has been shown [2] that this algorithm detects all stuck-at, transition, state-coupling, multiple-access and stuck-open faults. The BIST logic is operated to achieve At-Speed testing of the RAM modules.

For AC performance characterization, the INTROSC and EXTROSC instructions configure the internal and external scan chains, respectively, into ring oscillators. Since the internal scan ring consists of several thousands of latches, the results obtained from the ring oscillator measurements provide excellent correlation to actual performance of the parts. For delay-fault testing, a special patented master-scan latch design is used to control the operation of a smooth 1-to-0 and 0-to-1 transition capture and measurement. (The discussion of the design and operation of the master-scan latch is beyond the scope of this paper.)

VII. Results

The test methdology presented in this paper has been implemented on practical ASIC parts. Tables 2 & 3 show various area overheads over two generations and different sizes of Vertex gate arrays. In the V25 series, the JTAG boundary scan cells were designed and placed in the core logic area. As can be seen from the table, this proved to be a costly process for lower than 10K available-gate designs. Due to the INTEST performance penalty being more than a nanosecond, the V25 series offers both versions of boundary scan cells: with and without INTEST. In the V50 series, this was optimized to include the boundary scan logic in the I/O cell area, reducing the performance penalty to less than 0.1 nanoseconds. This is because, in the V50 series, a novel circuit design with custom layout was implemented to place the multiplexer before the input buffer/driver. It can be seen from the table that the JTAG area overhead incurred for the V50 gate arrays is only due to the test macro, which consists of only a few hundred gates. Realistic assumptions were made over the number of functional I/Os and RAM modules used for each gate-array size. For RAM modules, the following assumptions were made: 1 2K-bit RAM module for less than 30K used-gates design, 2 modules for designs between 30K and 100K used-gates and 3 modules for designs greater than 100K used-gates. The area overhead for the JTAG boundary scan cells makes a significant impact (on the order of few percent) when a comparison between the V25 and V50 series is made.

Figures 2 and 3 show the area overhead plots for the two families V25 and V50 with respect to the impact of size of gate array (used gates) and the type of routing technology used (double-level-metal vs. triple-level-metal). The overhead numbers include both JTAG and internal scan penalties. As the number of used gates increases, the impact of scan and JTAG overheads decrease significantly. The same trend is seen for routing technologies owing to an increase in usable gates for each gate-array size for the triple -level-metal scenario.

Since Vertex uses a full internal scan methodology, all parts are tested for greater than 99% stuck-at fault coverage. The test vectors are generated from a powerful ATPG tool developed internally and well-proven through years of refinement over the course of many designs. A patented design allows for zero performance penalty due to the scan latch. Due to an optimized physical design/layout flow, which entails a post-layout scan chain connection and rigorous timing analysis/optimization, the performance penalty due to scan chain routing is negligible. The test pin overhead is only the 4 (+1 optional) pins required for the JTAG interface.

VIII. Conclusion

A vertically integrated test methodology based on the standard JTAG test interface has been developed and presented in this paper. The protocol was implemented on two generations of

V25 Family Size	Utilized Gates	Functional I/O	Test Macro Overhead	BS Cell Overhead	Internal Scan Cell Overhead	No. of 2K-bit RAM Modules	BIST Logic Overhead	Total Overhead	%age Overhead
37K	25900	168	700	1512	1701	1	1017	4930	19%
54K	37800	204	700	1836	2847	1	1017	6400	17%
89K	62300	260	700	2340	4062	2	2034	9136	15%
129K	90300	312	700	2808	7305	2	2034	12847	14%
172K	120400	360	700	3240	9598	2	3051	16589	14%

Table 2: Area Overhead over Used Gates for the V25 Gate-Array family with RAM

V50 Family Size	Utilized Gates	Functional I/O	Test Macro Overhead	BS Cell Overhead	Internal Scan Cell Overhead	No. of 2K-bit RAM Modules	BIST Logic Overhead	Total Overhead	%age Overhead
24K	16800	120	700	0	950	1	1017	2667	16%
30K	21000	168	700	0	1366	1	1017	3083	15%
41K	28700	204	700	0	2128	1	1017	3845	13%
54K	37800	204	700	0	2385	2	2034	5119	14%
86K	60200	260	700	0	4603	2	2034	7337	12%
107K	74900	312	700	0	6058	2	2034	8792	12%
146K	102000	360	700	0	8097	3	3051	11848	12%
198K	138600	360	700	0	11720	3	3051	15471	11%
256K	179200	360	700	0	15740	3	3051	19490	11%

Table 3: Area Overhead over Used Gates for the V50 Gate-Array family with RAM

gate-array families: V25 and V50. It was shown that by incorporating the JTAG boundary scan cells inthe I/O area significant advantages in area overhead and performance were obtained. The results presented from realistic experiments over a wide variety of gate-array sizes and different routing technologies show that complete device testing at all levels can be achieved with very reasonable silicon overhead and minimal performance impact.

The test methodology accomplishes testing at all levels ranging from the wafer level up to the board and system levels. At the prototype debug stage, test circuitry and functions are provided to achieve efficient testing of design and process faults. At the manufacturing stage, the procedures provide for quick wafer sorting without the need to probe all pins and efficient package testing using internal full scan based test techniques. A uniform test pattern set that is used at the wafer and package phases can also be used for Incoming-Inspection of parts and chip-on-board scan test applications. The test methodology demonstrates a powerful and standard way to achieve most of the ASIC testing objectives with acceptable area and performance overheads.

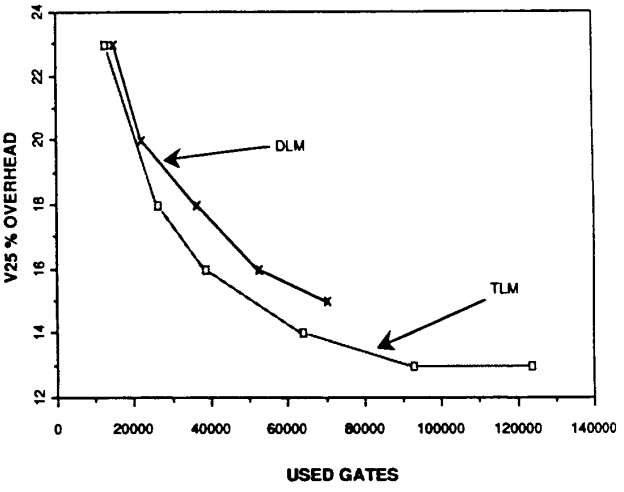

Figure 2: Area Overhead Plots for the V25 family with double and triple level metal without RAM

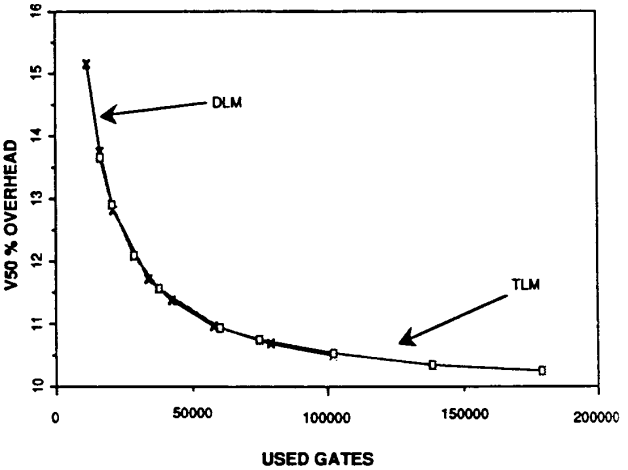

Figure 3: Area Overhead Plots for the V50 family with double and triple level metal without RAM

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