Educational Design of High-Performance Arithmetic Circuits on FPGA

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I. Summary

In many courses of digital system design, a large amount of time is spent introducing the students to architectural and circuit design. A typical laboratory application is the design of arithmetic digital circuits. In the past, as a hardware platform for educational digital design, programmable logic arrays (PLA's) have been widely used. Today, the field programmable gate arrays (FPGA's), seem to be the most suitable technology for this purpose. In this paper, among the many possible design examples, the authors have chosen the implementation of the radix-4 SRT algorithm for division. As convenient tradeoff between area cost and performance, SRT division implementation is being used in many recent general-purpose processors. The circuit offers a sufficient complexity to give practice to the students and to stimulate useful classroom discussions. Moreover, a system for rapid circuit prototyping and testing has been carried out. The prototyping-board allows the transfer of student designs into an SRAM-based FPGA chip and the performance of functional tests of the circuit. The prototyping system is directly controlled by a personal computer via ISA-Bus, and it allows students concentrate their attention on elaborating the digital design rather than striving with board assembly and PC-to-board communication.

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