A 3.3-V Programmable Logic Device that Addresses Low Power Supply and Interface Trends

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ABSTRACT

This paper discusses a 3.3V programmable logic device family which provides up to 130K gates. It blends a multi-dimensional interconnect scheme, logic array block approach consisting of 6,656 logic elements and circuit techniques to address low power supply and interface trends. It is designed on a 0.35um triple metal - dual oxide process to operate in a 3.3V only, 5V only or 3.3V-5V systems. Under worst case operating conditions it was observed to have a typical system operating frequency of 90MHz. The EPF10K50V is the first member of the second-generation FLEX 10K family.

INTRODUCTION

The integrated circuit business is continuously driven to reduce cost. Price reduction is strongly driven by migrating to scaled processes, which reduce die sizes and increase yields. Replacing prior generation ICs with their smaller - less expensive current generation duplicates is essential for reducing the component cost.

As silicon feature sizes scale - power supply voltages are required to follow suit and avoid reliability problems [1-3]. Generally processes that are at or around 0.35um channel length (commonly used parameter in evaluating the process capability) have reduced the operating voltage to 3.3V. This would require system supply voltage level changes, in order to utilize the lower cost current generation product. It is thereby expected that there may be a transition period for the standard power supply to switch over to 3.3V [4,5]. During the transition period, mixed voltage systems have become necessary. The mixed voltage system is acting as the intermediate platform for the market as it struggles to completely switch over to the lower power supply standard. Other benefits for adopting the new process and power supply standard are: i) power reduction from parasitic scaling and lower operating voltages, ii) performance improvement from process enhancements, parasitic scaling and lower operating voltages and iii) improved reliability from reduced heat generation and noise reduction [6-8].

The purpose of this paper is to present a device which addresses low power supply and interface trends. The device provides a single power supply solution or a mixed/multiple supply power solution. The device requires a multi-purpose I/O pre-driver and driver circuitry, a voltage converting circuit and a multiple power supply scheme to achieve the desired flavor. The paper will also cover solutions to the next transition period, namely the 3.3V to 2.5V standard switch.

ARCHITECTURE

The FLEX 10KV architecture consists of multiple rows and columns of LABs. Each LAB consists of 8 Look Up Table Logic Elements. Additional details of this architecture can

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be found in [9]. The FLEX 10KV family has added a multi-purpose I/O pre-driver and driver circuitry and a voltage converting circuit to provide the desired power supply and interface solution. The solutions available are to have a single power supply with a TTL and/or CMOS interface or a multi-supply with TTL/CMOS interface.

POWER SUPPLY AND INTERFACE OPTIONS

Single Power Supply Solution

This alternative can be used to satisfy two different customer bases, one that requires: i) a 3.3V only solution and ii) one that requires a 5V only or 5V substitute solution with a 5V-tolerant interface.

To satisfy the first case, one needs a standard CMOS output driver and a standard TTL or CMOS input driver. The second case, while taking advantage of the 0.35um technology, requires the device to provide a power supply voltage converter, a level shifting output driver and a 5V-tolerant TTL or CMOS input driver and output driver.

Multiple/Mixed Power Supply Solution

This alternative can be used to satisfy three different customer bases, one that requires: i) a 3.3V solution with a 5V-tolerant interface, ii) one that requires a 3.3V solution with a 2.5V interface and iii) a 2.5V solution with a 3.3V interface.

To satisfy the first case one needs an output driver that has its PMOS well tracking[1] the input pin as it exceeds Vcc and a 5V-tolerant TTL or CMOS input driver and output driver. The second case requires a hybrid I/O driver [10]. Lastly, for an optimum design the third requires a 2.5V process, a level shifting output driver and a 3.3V-tolerant 2.5V interface or TTL input driver and output driver.

As we continue to follow the technology road map - 0.25um or less, we will, in addition to the power supply reduction to 2.5V at the 0.25um [6], be forced out of the traditional TTL Vih and Voh levels. This will present a challenge for I/O communications between devices operating at 2.5V and 3.3V. In this mixed voltage environment, it would be advantageous for the 2.5V devices to deliver output levels or receive input levels that comply with 3.3V devices. The 2.5V supply is presently the next available standard "beyond TTL" that address the I/O characteristics for devices operating below 3.3V [11]. This family in particular does not support the 2.5V interface standards. These standards will be visited in the next generation product family.

CIRCUITS

I/O pre-driver and driver

The pre-driver and driver shown in figure 1 can be configured to perform as a typical CMOS, hybrid, level correcting and/or well tracking driver. The level correcting configuration is applicable when the device is required to drive other devices which require performance and are powered by a higher supply. The well tracking scheme is required to avoid turning on the PO1 drain to substrate diode or the PO1 itself. The turn on occurs when the pin voltage exceeds the power supply voltage. Turn on is avoided by allowing the well to follow the pin voltage beyond the supply volt-

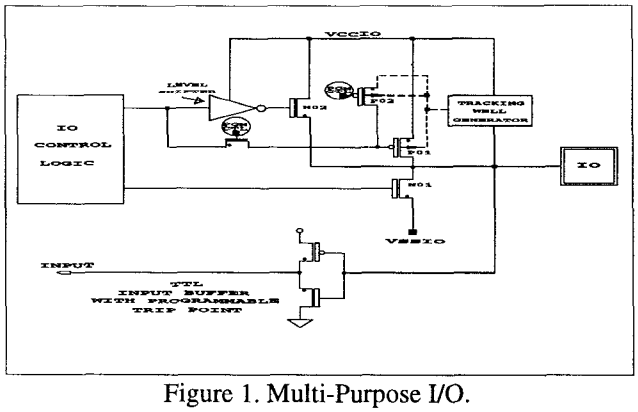

Figure 1. Multi-Purpose I/O.

1. Patent pending

age, see figure 2.

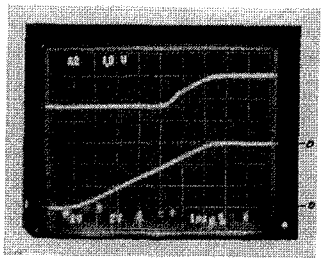

Figure 2. Tracking Well.

To avoid oxide stress concerns when the I/O is exposed to voltages greater than Vcc - NO1, NO2, PO1 and PO2 transistors are designed using greater than the normal gate oxide thickness. The additional steps required to do this were at a minimum incremental cost which was traded off for performance and reliability. Other approaches use transistors in series to divide the voltage and isolation transistors to reduce the voltage seen by the oxide [12-14].

The hybrid scheme combined with the circuits mentioned provides for a rich interface capability. The I/O driver structure supports an input leakage specification of 10uA, ESD immunity of greater than 5KV and latch-up immunity of greater than 300mA injected current. Figure 3 shows 25% less ground bounce noise than its 5V-counterpart for

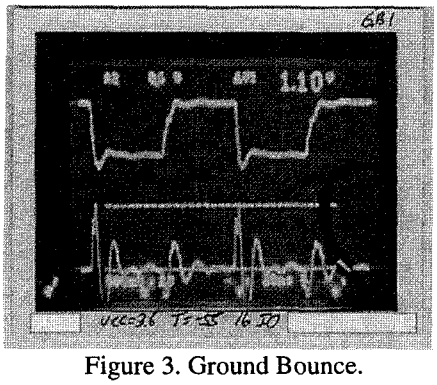

Figure 3. Ground Bounce.

the I/O.

Voltage supply converter

The voltage supply converter is most favorably applied in cases where the system power supply scheme does not track the technology scaling road map. In this case, the advantages of the scaling are utilized by providing an "on-chip" interface solution that accepts the present voltage standard and translates this via the Voltage Supply Converter (VSC) to the voltage needs of the scaled technology, see figure 4. Existing VSC circuits are not required to operate over a wide range of current demand while maintaining performance specifications [15-16]. This is a requirement that needs to be met for PLDs. This is because a PLD is designed to be able to perform multiple logic functions

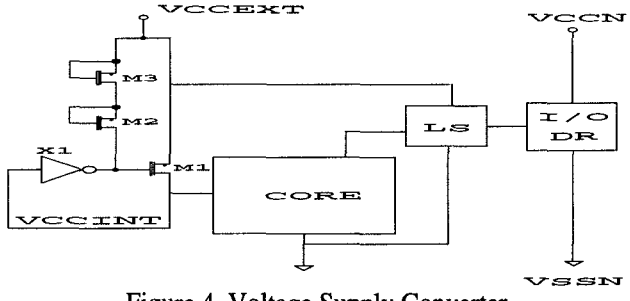

Figure 4. Voltage Supply Converter.

which would have different power requirements.

The VSC used here is designed to insure that the internal supply voltage does: i) not sag below the worst case operating Vcc to avoid performance variations and ii) not drift above the highest acceptable voltage that the oxide can tolerate. The current required to violate case one above was observed to be greater than 2A. The design used to consume 2A utilized 83% of the available logic elements as T-flip flops switching at 42MHz. Note, that at this current level IR drop will also start to play a significant role in the internal Vcc translating to reduced performance.

The VSC with the 0.35um technology provides a 5V alternative which has no performance penalty and 46% less power consumption when compared to the prior generation 5V product - see table 1 below:

Table 1: Performance and power comparison for the VSC device option.

	10K50V-0.35um(VSC)	10K50-0.5um(5V)
tdrr*	15.3ns	17.4ns

Icc	1.18A	2.2A

* tdrr measures register to register delays using multiple Logic Elements and interconnect lines.

PERFORMANCE EVALUATION

The data shown below was collected under the worst case commercial operating conditions. The data corresponds to the 3.3V only with 5V-tolerant capability device option.

	10K50V Measured	10K130V Simulated
Clock to I/O reg. output, tco	6.8ns	7.7ns
Input to output delay, tpd	13.4ns	21.0ns
Icc*	1.0A	-------

* Measured under typical conditions using 16-bit counters to fill up the device.

TECHNOLOGY EVALUATION

Die Size	240K mils sq
Minimum Feature Size	0.35um
Vtn/Vtp	0.6V/-0.7V
tox1	70A
Metal 1/2/3 pitch	0.95um/1.1um/1.2um

The die photograph is shown in figure 5.

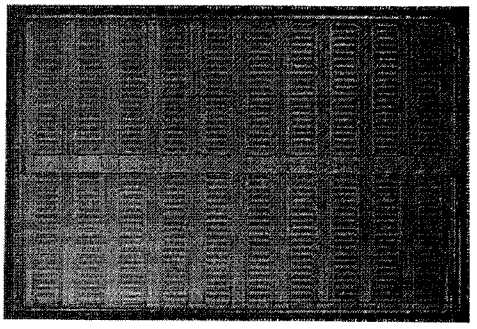

Figure 5. Die Photograph.

CONCLUSION

The FLEX 10KV is a family of PLDs that provides a flexible solution to address the low power supply and interface trends we are encountering and will continue to encounter as we travel the technology migration path. It does this without sacrificing performance or reliability.

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