TEST STANDARDS (WITH FOCUS ON IEEE1149.1)

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ABSTRACT

Testing systems using a standard test bus is presently the best method to guarantee the necessary test compatibility between IC manufacturers. A first action to promote a test bus started in 1985 in Europe with the Joint Test Action Group, JTAG. A test bus called IEEE1149.1 is now widely supported by most semiconductor companies, system test *companies and a growing number of system designers. The success of this action and the increasing need in testing mixed-signal and state-of-the-art systems has accelerated the process development of new standard test busses. Therefore, since Boundary-Scan is a Design-for-Test technique, IC designers are responsible of test implementation on chips.*

INTRODUCTION

In the eighties, a proposal of a universal standard testability bus serving all types of electronic systems have been started. Considered too ambitious, this proposition was split into several standards, each dealing with a different aspect of the original system test problem. The name of this set of test busses is 1149.X where X is a number associated with each subsystem test aspects.

In 1985, Bull, British Telecom, Ericsson, Philips, Siemens, Thomson and other European companies formed the JETAG (Joint European Test Action Group). Rapidly, the action became world-wide changing the group name to JTAG.

Recent advances in the electronic industry present, to the Design-for-Test community, a challenge of testing systems where observability and controllability are dramatically reduced. This challenge consists in replacing traditional physical access test technology, that became obsolete, by a non-contact test method. The main motivation is due to advances in technology like device miniaturization, Surface Mounted Devices (SMD) with fine-pitch connectors, Multi-Chip Modules (MCM), Multi-Layer Printed Circuit Boards (PCB) with components on both sides, etc. Test cost reduction is another important motivation of providing a new technique of testing boards.

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TRADITIONAL SOLUTIONS

In-circuit test technique of a PCB (figure 1), consists in providing observability and controllability through physical node access via a matrix of pins. This operation is performed with a bed-of-nails on a vacuum fixture.

The goal of this interconnect test technique is to detect manufacturing defects of mechanical, thermal and electrical type. It is often necessary to readapt and sometime fabricate a dedicated bed-of-nails support for each new board, therefore increasing test cost.

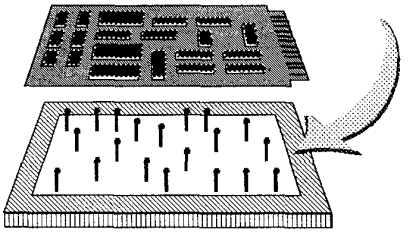


Figure 1 - In-circuit test technique with bed-of-nails

As a complement to in-circuit test, a functional test checks for faults affecting the board at the logical and functional levels (figure 2). Specific testers are often necessary to apply test vectors to the board. These testers are often very expensive and require specialists.

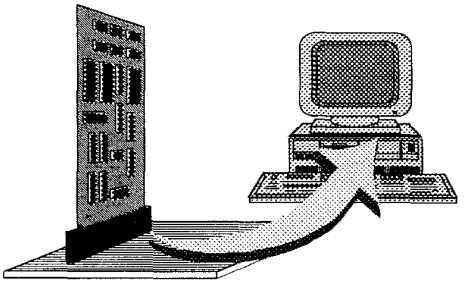


Figure 2 - PCB functional test from board connector

BOUNDARY-SCAN PRINCIPLE

Inspired from the Scan Path technique [1], Boundary-Scan consists in insuring observability and controllability of a board through its edge connector using non-contact methods. A collection of IC and board Design-for-Test rules transforms the hardware PCB in-circuit test method into a software based technique. A set of patterns are then presented through dedicated test inputs allowing full observability and controllability on every pin of every circuit on the board.

1149.X FAMILY

Table 1 gives a short presentation of the 1149.X family. The prefix IEEE designates an approved proposal by the IEEE Computer Society, whereas the prefix P stands for proposal and designates an unapproved draft, subject to change.

Number	Title	Status
IEEE1149.1	Standard Test Access Port and Boundary-Scan Architecture	Published in Feb. 1990. 2 revisions: 1149.1a & 1149.1b
P1149.2	Extended Digital Serial Access Port	under development
P1149.3	Real Time Test Bus	discontinued
P1149.4	Mixed-Signal Test Bus	Nearing completion
IEEE1149.5	Module Test and Maintenance Bus	Standard in may 1995
P1149	Overview Document	Not yet started

Table 1 - 1149.X test bus family

IEEE1149.1 Standard Test Access Port and Boundary-Scan Architecture

This is the first and best established standard. It is better known as JTAG, even though the Joint Test Action Group don't exist any more since it has reached its objective in February 1990 when the IEEE approved the standard. More details on this standard are given later in this paper. Several documents give more details [2] [3]. A Boundary-Scan Description Language (BSDL), a subset of VHDL, has been recently added to the standard [4], now called IEEE1149.1b.

Furthermore, most of electronics companies have added products addressing the Boundary-Scan approach at the component, CAD tools and the ATE system levels, thus proving the commercial success of the test standard.

P1149.2 extended digital serial access port

This proposal offers test features similar to those provided by the IEEE1149.1, but with two main differences [5]. First, it has fewer constraints on the test register design. Second, it uses a direct parallel access method instead of the serially programmed instruction register required by the IEEE1149.1 standard. P1149.2 has a more flexible approach than IEEE1149.1, which is probably better for IC manufacturers and designers, but on the other hand, it will reduce compatibility between IC manufacturers which implies that components obtained from different suppliers would not always interwork correctly. Not date has been fixed yet for ballot of the P1149.2.

P1149.3 real time test bus

The objective of this proposal was to allow Automatic Test Equipment, ATE, to control and monitor digital signals on a loaded board in real time, through test access paths built into the system. This proposal has been terminated in 1992 due to insufficient company support.

P1149.4 mixed-signal test bus

This standard proposal will allow the test of boards containing mixed-signal and digital circuits. P1149.4 could be defined as including the IEEE1149.1 plus the ability of performing continuous time and continuous voltage/current access as well as the measurement ability of resistors, capacitors, inductances and time delays. Test of pull-ups, pull-downs and coupling impedances not feasible with the digital test bus are made possible in this standard. Present status of P1149.4 is described in [6].

IEEE1149.5 module test and maintenance bus

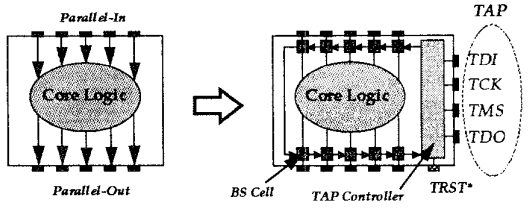
Subsystem level aspect of testability is dealt with this standard proposal, called MTM bus. MTM bus is basically intended for use as a backplane serial test bus, it could also be used in parallel or in hierarchy with other test busses. Its main objective is the ease of in-situ testing and 'hot-swapping' of PCBs during field maintenance enabling a PCB to be removed from the backplane without breaking the communication link between the remaining modules. MTM-bus features a master-slave communication protocol implementing the ISO-7 layer model [7] [8]. MTM bus is mainly dedicated to applications in fields like telecommunications, military computers, and avionics systems.

P1149 Overview document

This overview document will be the last member to be standardized since it will be a guide to the use of the other IEEE1149.X standards. It will also give examples on how to produce a testable system design using testable ICs.

IEEE1149.1 TEST BUS STANDARD

To produce an IEEE1149.1 testable board, every digital circuit on it has to include the necessary logic circuitry allowing its conformity to the standard (figure 3).

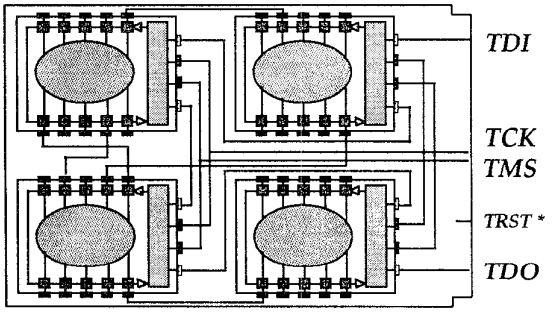


* *TRST (Test Reset) is optional*

Figure 3 - Digital chip without (a) and with (b) IEEE1149.1 Boundary-Scan test bus

A minimum of 4 mandatory test pins should be added to the functional pins, plus one optional. These pins are called 'Test Access Port', TAP, their role is as follows:

TDI (Test Data Input) is a serial input pin. At the circuit level, instructions and data are shifted serially through TDI and collected at the TDO pin (Test Data Output). TDO is a serial output pin linked to the TDI of another circuit (figure 4) forming a chain of scan paths at the boundaries of the circuits on a board. One or several serial paths could be provided on the same board depending on its complexity. TCK (Test ClocK) should be kept separate from any system clocks. TCK samples the state of TMS (Test Mode Select) therefore controlling the mode of operation. TRST (Test ReSeT) is an optional input that resets the TAP controller asynchronously.



* *TRST is optional*

Figure 4 - Digital board with Boundary-Scan test bus

The edge connector of a Boundary-Scan board has the same 4 (or 5) TAP pins. In normal mode, TDI, TCK, TMS and TRST are pulled-up, whereas TDO is in Hi-Z state.

BOUNDARY-SCAN ARCHITECTURE

A Boundary-Scan architecture is devided in two parts: a control part called 'TAP controller' and a data path composed of several registers accessible serially through TDI (control) and TDO (observation).

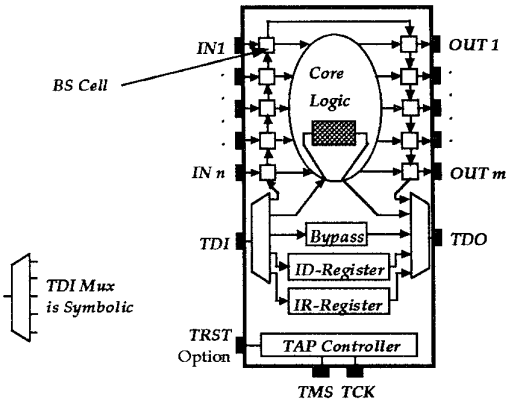


Figure 5 - Test architecture of the IEEE1149.1 standard

Three registers of the data path are mandatory: the instruction register (IR), the bypass register and the data Boundary-Scan register. Other registers are optional like the identification register (ID) and user specific registers.

TAP CONTROLLER

The Test Access Port Controller is a finite state machine with two input signals TMS and TCK (figure 6).

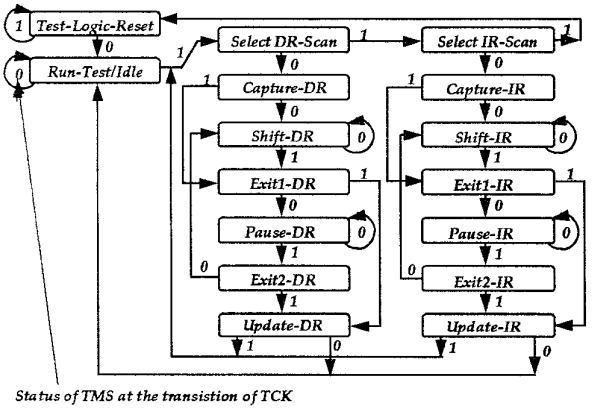


Figure 6 - TAP Controller States diagram

When the controller is in the 'Test-Logic-Reset' state (TMS at 1) the circuit is in its normal mode. In the test mode, instructions decoded in the instruction register are executed with respect to the TAP controller. Three instructions are although mandatory:

- EXTEST, tests for external interconnection short/opens
- BYPASS, holds the chip logic out of the scan chain
- SAMPLE/PRELOAD: SAMPLE takes a "snap-shot" of the I/O logic-levels, PRELOAD allows preconditioning of output cells.

Other instructions are optional:

- INTEST, tests the core logic function of the circuit
- IDCODE, shifts out the content of the identification register, locating the chip on the board and recognizing it.
- RUNBIST, stimulates and reads self-test registers
- USERCODE, Used to Identify PLDs Mainly
- CLAMP, Used to Avoid Bus Contention by Presetting Output Values. Sets Bypass Register between TDI & TDO
- HIGHZ, Similar to CLAMP but Leaves Outputs in High-Impedance State

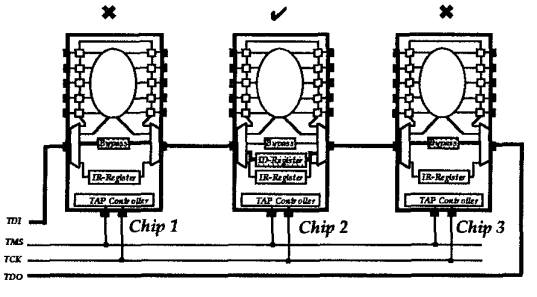


Figure 7 - Example of the identification operation

Figure 7 shows the operation of identification of chip2 (IDCODE), while chip1 and chip3 are bypassed (BYPASS).

BOUNDARY-SCAN TEST STRATEGY

Execution of a Boundary-Scan test on a board could be presented as a sequence of three steps:

Step1: Integrity test, where the test path is 'tested' before using it. It consists in capturing in the instruction register, IR, of every circuit in the chain the 'checkerboard' 01 sequence. If this test passes then the test of interconnections can start. Extra test sequences could also be applied to check the other registers and operation of the architecture. BYPASS and IDCODE instructions are used here.

Step2: Interconnect test is then applied for checking for opens, shorts and other defects between the circuits on the board. EXTEST is used here

Step3: This optional step is basically dedicated to internal test of the circuits. INTEST and/or RUNBIST instructions could be applied here.

CONCLUSION

Boundary-Scan technique answers the test problem at the IC, Multi-Chip Module, PCB, and complete hardware system levels. More recently, it has addressed module test and maintenance. A mixed analog-digital system test is coming soon. By its standard feature, the Boundary-Scan architecture can be easily automatically included in designs by synthesis tools, even at high levels of abstraction.

The benefit of this technique will reach its maximum when all chips in the system to test are 100% Boundary-Scan compatible. Although, many techniques mixing Boundary-Scan with non Boundary-Scan chips have been proved technically feasibility and cost effective.

Finally, the transition from in-circuit to Boundary-Scan test is already a success. The rapidly growing Boundary-Scan market testifies, if necessary, to all the benefits of the Boundary-Scan technique.

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