An FPGA-based Digital Camera System Controlled from an LCD Touch Panel

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***Abstract*— Field Programmable Gate Arrays (FPGAs) are in use to build high performance image processing systems. This paper presents the design and implementation of such an open FPGA-based Digital Camera System for image capturing and real-time image processing. Images captured with a CMOS sensor are initially stored in the system's memory and then they are displayed on an LCD Touch Panel. The main goal of this proposed architecture is to be used as a platform to implement and test advance image processing algorithms. Apart of this, the system supports the control of the image sensor, through the LCD Touch Panel. In addition, has the ability to communicate with a PC through a JTAG interface for storing the images on it. The structural element for this proposed architecture was chosen to be the low cost and widely used at universities, Altera's DE2 development board.**

I. INTRODUCTION

The constant reduction both of cost and size of image sensors and the increasing complexity of FPGA circuits let us to design and implement an FPGA-based Digital Camera System. Also, due to the appearance of the LCD Touch Panels this system could be able to be controlled from such a panel. Furthermore, the flexibility of FPGAs gives us the possibility to integrate additional applications and image processing algorithms to the system without any cost in hardware [1-3]. It's worth mentioning that the hardware image processing algorithms could be faster than the corresponding algorithms in C/C++.

For the implementation of this system the development platform DE2 by Altera, the TRDB-D5M Camera and the TRDB-LTM LCD Touch Panel by Terasic have been chosen [5-8]. Some of the DE2's I/Os have been used for the interconnection of the Camera and the LCD Touch Panel as well as for the communication between the DE2 and a PC.

Apart from the memories and the I/Os, the DE2 has a Cyclone II EP2C35 FPGA by Altera. This FPGA has 33216 logic elements, 483840 memory bits, 70 embedded multipliers and 4 Phase Locked Loops (PLL). The interfacing of all DE2's hardware components can be achieved through the FPGA. For the implementation of the system which is presented in block diagram in Fig. 1, the following subsystems have been designed in Verilog HDL [9, 10]:

- Camera Sub-System
- LCD Touch Panel Sub-System
- JTAG Sub-System

This system which is designed using the Altera's QuartusII v.7.2, takes up to 7% of the FPGA's logic elements, 12% of the total memory bits, 0% of the embedded multipliers and 25% of the PLLs. Consequently the FPGA has enough free space for the implementation of image processing algorithms.

II. CAMERA SUB-SYSTEM

The Camera Sub-System which is presented in block diagram in Fig.2, captures the image from the sensor,

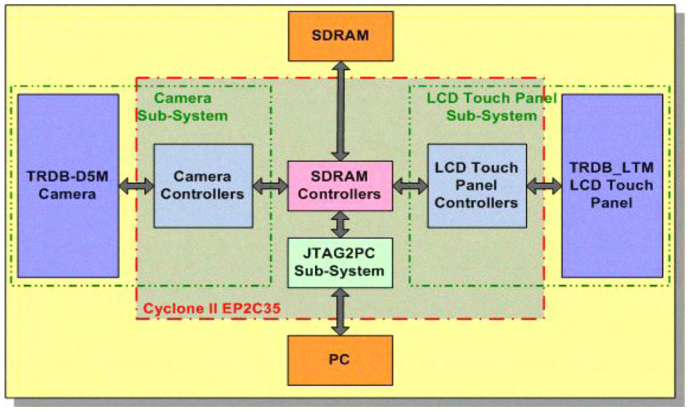

Figure 1. Block diagram of the FPGA-based Camera System

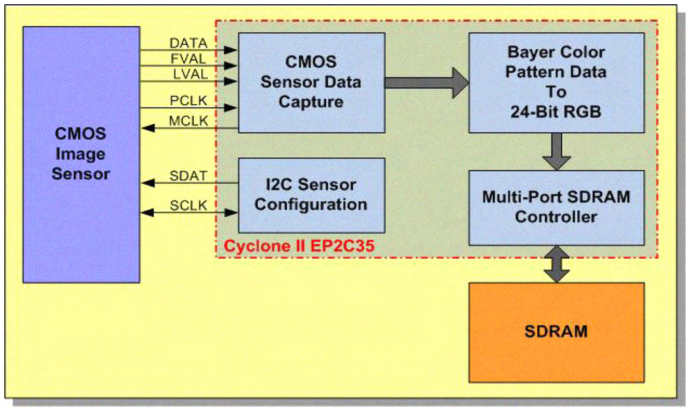

Figure 2. Block diagram of the Camera Sub-System

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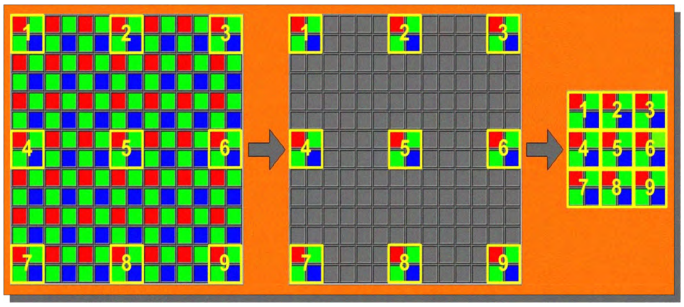

Figure 3. The skipping method

transforms it into RGB format and stores it in the SDRAM of DE2. The Camera Sub-System has two parts, the TRDB-D5M Camera and the Camera Controllers.

A. The TRDB-D5M Camera

The TRDB-D5M Camera by Terasic incorporates a CMOS image sensor with resolution up to 5 mega pixels (2592H X 1944V) [8]. The image sensor exports its data according to the Bayer Pattern format. Hence, the odd pixel lines of the image sensor contain the Green and Blue color components, whilst the even lines the Red and Green color components.

This Camera manages the Green pixels as two different color components depending on which line they come from, despite the fact they have come from the same color filter array. Consequently, the final number of the color components is four: Red, Green1, Green2 and Blue (R, G1, G2 and B).

The image sensor has 256 registers whose values are determined for the Camera's operation. The access to the Camera's registers is achieved via a serial i2c (inter-integrated circuit) interface.

The data that are exported from the Camera to the DE2 are 12-bit per pixel. In this particular application the captured images have VGA resolution (640Hx480V). This is achieved using the skipping method as presented in Fig.3. This method allows the image sensor to capture images in Bayer Pattern format with a frame rate up to 150 frames per second.

Finally, the communication of the Camera and the FPGA is achieved through a 40-pin expansion header.

B. Camera Controllers

The control and the communication between the Camera and the DE2 are achieved through the following Camera Controllers which were designed in Verilog HDL and implemented into the FPGA [8-10]:

- CMOS Sensor Data Capture Controller
- i2c Sensor Configuration Controller
- Bayer Color Pattern Data to 24-bit RGB Controller
- Multi-Port SDRAM Controller

The CMOS Sensor Data Capture Controller is responsible for the control of the Camera's operation as well as for the output of the pixel data through a 12-bit data bus. The pixel's data come out of the Camera for every clock cycle starting from the pixel in the upper left corner of the image sensor. When the process of exporting the data of a full image has completed, the transmission of the next one starts. It is also responsible for the start and stop of the TRDB-D5M Camera's operation through the start capture and stop capture signals. These signals are enabled every time the corresponding area in the LCD Touch Panel is activated.

The i2c Sensor Configuration Controller is used to generate the i2c signals necessary for the control of Camera's registers. Through these registers, parameters like exposure time, zoom mode, H_Blanking, V_Blanking, gains of color components and the active area of the image sensor are determined.

The Bayer Color Pattern Data to 24-bit RGB Controller is responsible for the conversion of the captured image from Bayer Pattern format to RGB format. In this controller data are inserted from the CMOS Sensor Data Capture Controller through a 1280 depth 12-bit line buffer. The Bayer Color Pattern Data to 24-bit RGB Controller in order to convert the data from Bayer Pattern format to RGB format calculates the two missing color components for every pixel by using the values of the neighbouring pixels and calculating their average [4]. A reduction of pixel data size is necessary because the Camera exports 12-bit data per color component but the LCD Touch Panel supports 8-bit data. For this reason the Bayer Color Pattern Data to 24-bit RGB Controller removes from the data of every color component the 4 LSBs (Least Significant Bits). This reduction does not significantly affect the content of the final image since the LSBs are responsible for the details of the image. Finally, the Bayer Color Pattern Data to 24-bit RGB Controller sends the data for every pixel in RGB format, to the Multi-Port SDRAM Controller through a 24-bit Data Bus.

The Multi-Port SDRAM Controller is responsible for sending the data which come from the Camera to the SDRAM. It also undertakes to read the data from the SDRAM and to send them to the LCD Touch Panel. The size of the data that arrive to the Multi-Port SDRAM Controller as well as those which are sent by it are 24-bit. Finally, the Multi-port SDRAM Controller incorporates a logical circuit which creates the timing signals of SDRAM.

III. LCD TOUCH PANEL SUB-SYSTEM

Fig.4 presents in block diagram the LCD Touch Panel Sub-System which displays the contents of the SDRAM on the

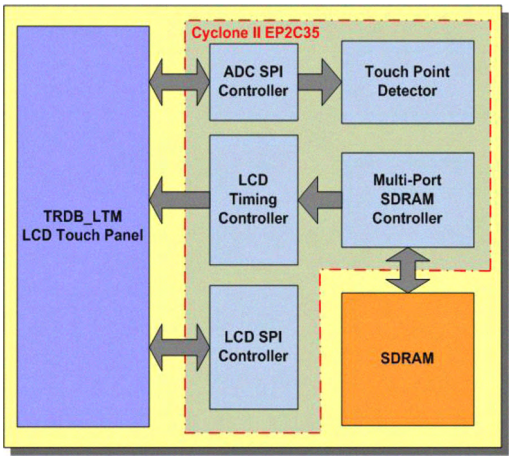

Figure 4. Block diagram of the LCD Touch Panel Sub-System

LCD Touch Panel. Equally, it is responsible for the touch detection on the Panel. This sub-system consists of two parts, the LCD Touch Panel and the LCD controllers.

A. The LCD Touch Panel

The LCD Touch Panel which has been chosen in this system is the TRDB_LTM by Terasic [6, 7]. Through the LCD Timing Controller the 24-bit data which are stored in the SDRAM are displayed on the LCD Touch Panel. The values of the control registers of the LCD Touch Panel which are related to its function are determined by the LCD SPI Controller.

Every time touching is being detected at any spot of the LCD Touch Panel, the corresponding analog coordinates are created. The Analog Devices AD7843 ADC transforms the analog coordinates into the corresponding digital data which are sent to the FPGA through the second 40-pin expansion header of DE2.

It is worth noting that because of the limited number of I/Os of the expansion header, the LCD Touch Panel and the ADC share the same clock and chip enable signals. Consecutively, during the design of the LCD SPI Controller there should have been given more attention to the control of these signals in order to avoid the simultaneous use of the serial port interface by both the LCD Touch Panel and the ADC.

Finally, it should be noted that the resolution of the LCD Touch Panel is 800Hx480V. Because the image that captured from the Camera Sub-system has resolution 640Hx480V, two black bars are created in the sides of the LCD Touch Panel. In these bars the LCD Timing Controller draws the four buttons for the Camera control.

B. LCD Touch Panel Controllers

The following LCD Touch Panel Controllers which are responsible for the control of the LCD Touch Panel and the data transfer from DE2's SDRAM, were designed in Verilog HDL [9, 10]:

- ADC SPI Controller
- Touch Point Detector Controller
- LCD Timing Controller
- LCD SPI Controller

The ADC SPI controller receives the digital signals from the LCD Touch Panel's ADC every time an area on the Panel is activated through touching. Then, it exports two 12-bit numbers which represent the x and y coordinates of the area that has been activated.

The Touch Point Detector Controller receives the coordinates of the activated areas and sends them to the 7-Segment displays of the DE2 in order to be displayed. It also controls if the x and y coordinates reflect a point in one of the predefined active area. These areas are represented by the buttons of the LCD Touch Panel and activate one of the following control signals of the Camera:

- **Start Capture** which activates the Camera
- **Stop Capture** which deactivates the Camera
- **Exposure Mode** which decides the increase or decrease of the exposure time
- **Change Exposure** which increases or decreases by 32(Hex) the exposure time depending on the exposure mode

The LCD Timing Controller is responsible for the formation of the image that will be displayed on the LCD Touch Panel. The whole process is based on the use of a counter with values from 0 to 800x480-1 (LCD Touch Panel's resolution). For every value of the counter the LCD Timing Controller sends a 24-bit number to be displayed in the corresponding position on the LCD Touch Panel. Depending on the value of the counter this number will be either 24-bit data from the SDRAM or 24-bit data from the Controller. The LCD Timing Controller generates the data which represent the four buttons and the two black frames on the right and left sides of the image.

The values of the registers of the LCD Touch Panel are chosen by the LCD SPI Controller. These values are specific and are received from a look-up table every time the system is activated. The LCD SPI Controller also generates the appropriate signals for the timing of the LCD Touch Panel.

IV. JTAG2PC SUB-SYSTEM

The DE2 development board supports the communication with a PC through the JTAG interface. For this reason Altera has developed the respective software, the DE2 control panel [5]. This software supports the transfer of data from DE2's SDRAM to PC and vice versa through the JTAG2PC Sub-System. Fig. 5 presents the block diagram of the JTAG2PC Sub-System which comprises of the following components:

- USB_JTAG Controller
- CMD
- JTAG2SDRAM Controller

The USB_JTAG Controller transforms from parallel to serial the data that coming from the SDRAM through the JTAG2SDRAM Controller, in order to send them to the PC.

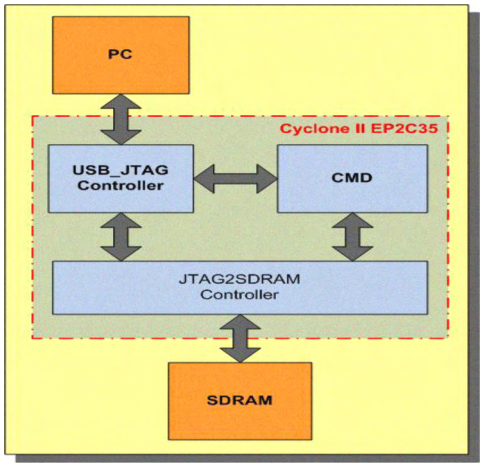

Figure 5. Block Diagram of the JTAG2PC sub-system.

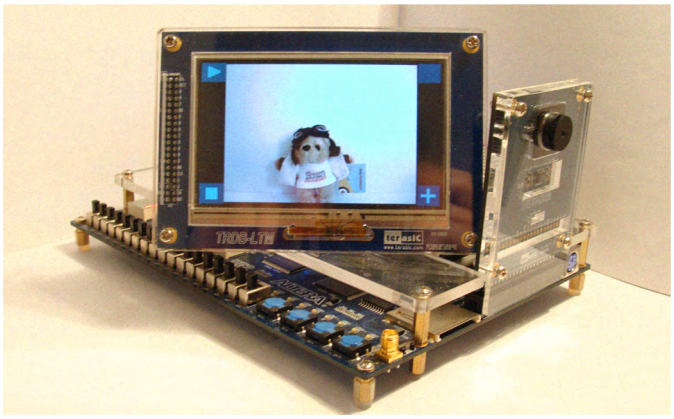

Figure 6. The captured image when the exposure time has the default value.

It also transforms the data that the DE2 receives from serial to 8-bit parallel.

The CMD is a decoder that undertakes the handle of the JTAG2PC sub-system. It receives specific instructions from PC and generates the appropriate signals for the control of the JTAG2SDRAM Controller and the USB_JTAG Controller.

Finally the JTAG2SDRAM Controller undertakes the transfer of the data from the USB_JTAG Controller in the SDRAM and vice versa creating the appropriate timing signals.

V. EXAMPLES

At the system start up the default value of the exposure time register is 7C0 (Hex). Each time the user activates the change exposure button the value of the appropriate register is increased or decreased by 32 (Hex) depending on the status of the exposure mode button. In the following Figures is evident the difference in brightness of the displayed images.

Fig.6 presents the captured image when the exposure time has the default value. Fig. 7 and Fig. 8 show the captured images when the exposure time is increased or decreased by 96 (Hex) respectively.

VI. CONCLUSIONS

The proposed FPGA-based Digital Camera System, due to the FPGAs' flexibility, is mainly targeting to be used as an open and low cost platform for implementing and testing real-time image processing algorithms. In addition the exploitation of LCD Touch Panel can effectively assist in the control of more camera's parameters. Image processing algorithms can take place before or after the data storing and because of the FPGA's presence, system has the ability to be easily modified. Future plans are to embed and test more advance image processing algorithms due to the fact that there is enough space left in the FPGA. In addition we intend to create an extended menu for the LCD touch panel. Developing such a menu the user can fully and in a friendly manner control Camera's functionality. Through this menu the user can also easily select the execution of the desirable image processing algorithm.

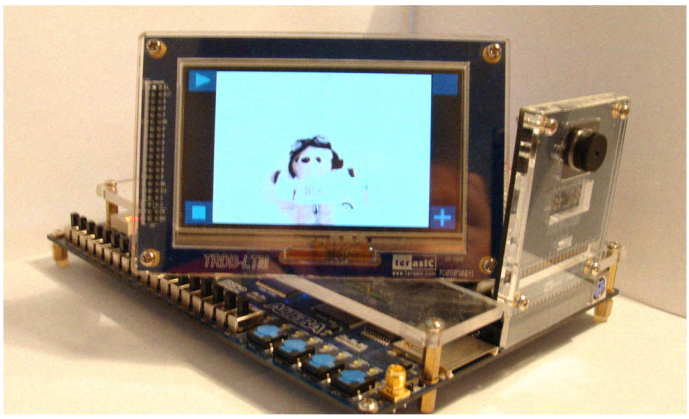

Figure 7. The captured image when the exposure time is increased by 96 (Hex).

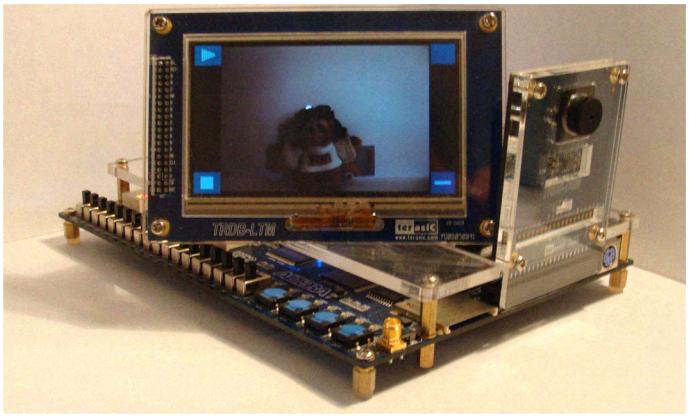

Figure 8. The captured image when the exposure time is decreased by 96 (Hex).

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