Building an Evolvable Low-Cost HW/SW Educational Platform – Application to Virtual Instrumentation*

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Abstract

This paper describes a hardware/software FPGA-based platform. Its goal is to provide a reusable low-cost system for teaching system-level design, with an emphasis on design reuse as an effective mean to cope with an ever growing design complexity. An open source strategy promotes cross-university collaboration by relying on previously developed software. The first implementation examples target the area of Reconfigurable Virtual Instrumentation (RVI), which in turn provides a low-cost solution for teaching electronic instrumentation.

1. Introduction

FPGA-based platforms are increasingly becoming an attractive solution for teaching design methodologies of complex digital systems. Moreover, some of the exciting new educational uses of such platforms go beyond the area of digital logic, and also harness most FPGA architectures as a low-cost general-purpose computation medium [1]. In this paper, we show how the proposed RVI platform can be used in teaching experimental physics by emulating custom and general purpose instrumentation such as waveform generators and logic analyzers.

In the following sections we explain the strategy used in building the RVI platform. We then describe the hardware and software architectures, followed by a few actual educational use cases.

2. Design reuse and open source approach

One important element for the success of the RVI platform in the instrumentation field is the availability of a strong, shared open-core/open source library of modular components. The platform, based essentially on FPGA devices and standard personal computers is of a particular interest to the academic and scientific community, as it represents a low-cost educational solution. This is particularly the case in developing countries where financial constraints are extremely tight making it very difficult to afford the cost of expensive instruments.

By requesting from students to follow a modular block-based design for reuse methodology, we teach them how to cope with the complex mix of skills and design effort required in complex designs. This approach also promotes a future expansion of the project since building adds-on incremental solutions can be reutilized by a large community of developers. It represents one of the major concepts behind this project. The approach is enforced through the use of the public Wishbone IP interconnection standard, which is present in many of the IP cores offered by the OpenCores organization [2]. It implies that the solution needs to be open source [3] allowing a constructive synergy among all developers.

3. System architecture

A high-level description of the system architecture comprises both hardware and software sub-systems. The hardware includes a standard personal computer connected to a reconfigurable board through a physical connection. In our application, the board represents the *Reconfigurable Instrument* (RI); that is a versatile hardware device that can be reconfigured into different electronic instruments using a software tool. The RI includes one mother board built around a medium to large capacity FPGA device (ACTEL A3PE600 [4]) and four main blocks, namely: communication ports, extension memory, debugging facilities, and two high quality board-to-board connectors with 54 pins directly connected to the FPGA general purpose I/Os. Four standard communication ports are logically connected to the FPGA: RS232, USB1.2, USB2.0, and Ethernet

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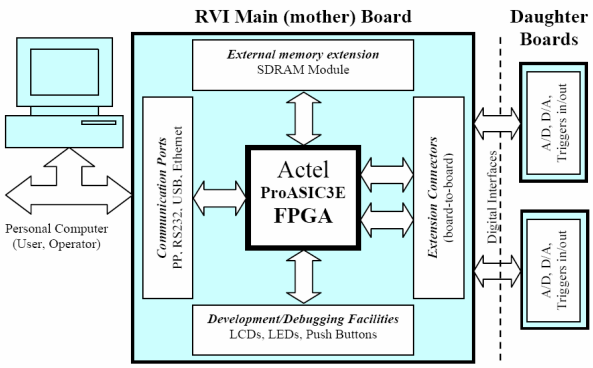

Figure 1. Hardware architecture

10/100. The main board has a SODIMM 144STD socket for SDRAM modules from 128 MB to 512MB. Figure 1 shows a board-level description of the hardware sub-system.

Two daughter boards are also included in the RI. The first, a Low Performance (LP-DB), contains a dual channel 10-bits 20 MSPS Digital-to-Analog Converter (AD9201, Analog Devices), a dual channel 14-bit 1 MSPS Digital-to-Analog Converter (LTC1654, Linear) and the second, a High Performance (HP-DB), contains a single channel 14-bits 125 MSPS Digital-to-Analog Converter (LTC2255, Linear), a single channel 16-bit 50 MSPS Digital-to-Analog Converter (LTC1668, Linear).

The software on the PC is a collection of generic and independent modules organized hierarchically. It provides a graphical and textual user interface, a library of virtual instruments with custom user interfaces, data storage facilities, and communication drivers.

The code corresponding to the FPGA is a re-usable synthesis friendly VHDL description divided into four basic blocks: A port communication, a dual port memory and registers, the instrument core, and an FPGA port assignment description file.

4. Design examples

To be integrated in the system, a reconfigurable instrument core must comply with the standard interfaces of the PC-FPGA communication block and the external hardware specific interface block. It should also comply with a common mechanism of interaction. If the three main blocks: PC-FPGA communication block, instrument core, and the external hardware interface respect both previous conditions, then each block can be updated or upgraded independently and can be reused in different contexts. Hereafter, we describe a few examples that were implemented according to the principles described in this paper.

The first implementation is a third order Sigma-Delta demodulator using the architecture in [3] due to its suitability for FPGAs. The goal is to run at a clock frequency of 80 MHz for a total of approx. 8 x 10^9 16-bit arithmetic operations per second, which is clearly beyond the capacity of most modern processors.

The second implementation is an arbitrary waveform generator capable of generating standard waveforms such us triangular, square, ramp, etc. It also contains a custom 14-bit CORDIC block for the generation of sine waves through the 14-bits 1 MSPS digital-to-analog converter working at 1 MSPS.

5. Conclusion

By promoting an open source/open core approach, we allow a large community of users/contributors to rely on all developed materials, saving important costs of commercial IP blocks, highly useful for universities and research institutions in developing countries. While the cost of the hardware is expected to remain approximately constant, its value will strongly increase with each new virtual instrument that can be implemented.

The main board has been manufactured as well as the two daughter boards. We should be able to couple the presentation with a demo during the MSE conference using the examples mentioned in this paper.

6. Acknowledgment

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