An Embedded JTAG, System Test Architecture

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1. Abstract

IEEE 1149.1, *The Standard Test Access Port and Boundary-Scan Architecture*[1] (JTAG) was written to provide standardized test access to surface mounted integrated circuits (ICs) whose high density packaging restricted physical test access. Although the four-wire (optionally five-wire) test port defined within the standard is commonly applied to test printed circuit boards (PCBs) in a factory, there is not yet a standard method for testing modules once they are installed in a system. This paper describes an architecture for extending the application of JTAG to system-level testing. It assumes reader familiarity with IEEE 1149.1.

2. Goals for JTAG Embedded System Test

Motivation for rerunning factory tests on a complete system is provided, in part, by common experience with no-fault-found failing systems. When system-level functional tests are fault graded, they commonly can detect between 50 and 75% of all possible structural defects. Structural tests run in a factory on PCBs and ICs can frequently detect in excess of 95% of all possible structural defects. This alone could inspire rerunning factory tests in the field to improve defect diagnosis and to reduce the total number of no-fault-found events.

JTAG has not found widespread use as a backplane test bus. If a single 1149.1 test bus were used, the simplest implementation with TDI entering each module and TDO exiting to serially weave through each module presents several limitations: First, if any module is removed, then the entire test ring is open and no tests can be run. Second, with several modules in series the scan ring length may become awkwardly long and again, if any module has a defect that prevents the scan chain from working, then all testing is frustrated. Methods requiring multiple, multiplexed JTAG signals have been proposed, but because they require additional backplane pins and do not easily scale to large backplanes, they have not been widely used.

This paper describes a method that allows 1149.1 to be used as a multidrop backplane test bus. It avoids the complications of introducing another communications protocol. The most challenging requirement for a slave module interface is to provide simple multi-drop access to each 1149.1-testable module that supports backplane module interconnect testing. Because 1149.1 does not support multidrop access, small extensions are defined to allow the same protocol to be used for backplane testing that is already used for PCB and IC test access.

Our embedded test architecture requires one interface IC to convert a parallel computer bus to a serial JTAG backplane test bus. We call this bus master interface a parallel-to-serial converter[2]. In addition, each printed circuit board requires an addressable slave interface to allow the test bus master to select each module in turn and to deliver the test vectors originally written for stand-alone, factory test. We call this second IC a Scan Bridge[3].

3. JTAG Bus Master - A Simple Parallel-to-Serial Converter.

The JTAG backplane test bus master (see Figure 1) converts 1149.1-based test vectors developed for factory tests into a serial 1149.1 bit stream. These vectors stored in parallel byte format in the diagnostic processor are converted into a serial test stream much like an RS232 interface chip converts processor byte data into serial signals. This is the same function performed within a factory tester.

The parallel-to-serial converter IC has a flexible CPU interface with addressable data and control/status registers for attachment to any memory-mapped computer I/O bus. The parallel bus interface is kept to eight-bit width to minimize required package lead-count. The parallel-to-serial converter test data registers are double-buffered to allow communications with the backplane test bus to continue from one of the buffers while the empty TDO buffer or the full TDI buffer is being serviced by the diagnostic processor.

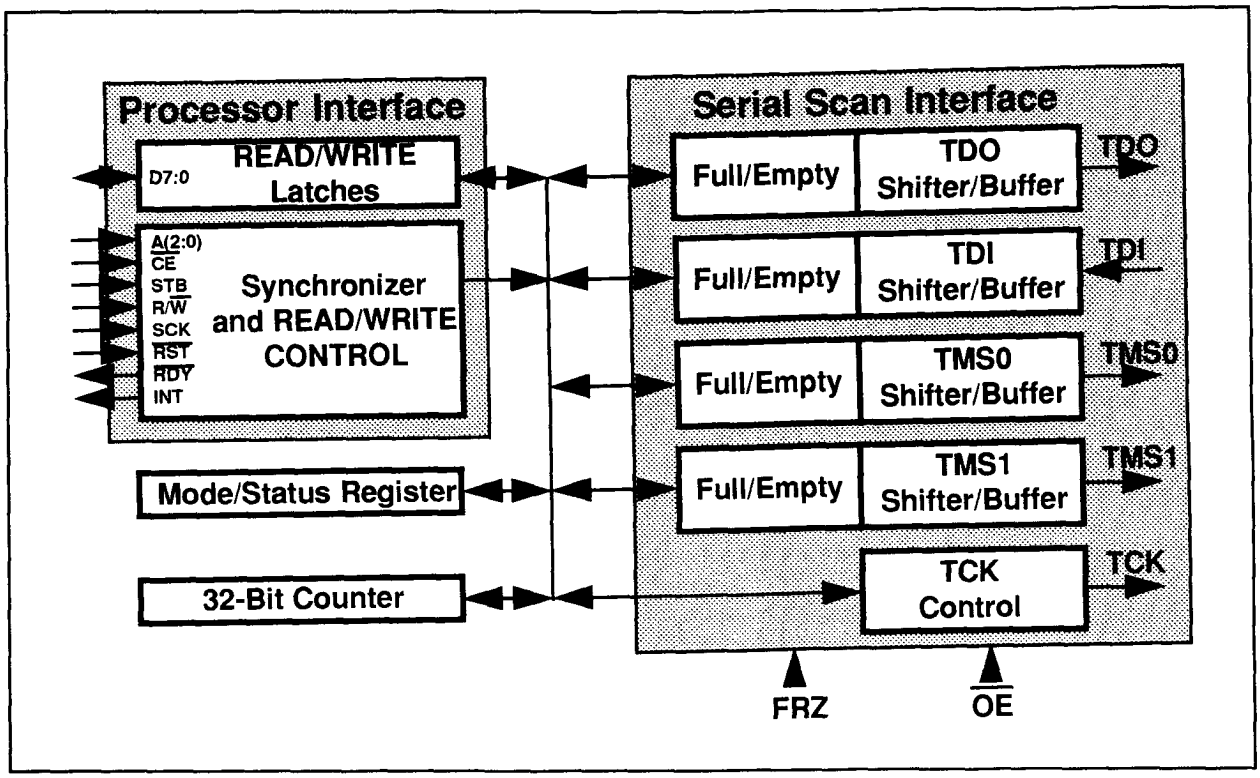

Figure 1 *Parallel-to-Serial Converter, JTAG Bus Master*

Allowing the diagnostic processor to serve other roles means that it may not always be ready to immediately respond to data transfer requests from the JTAG test port. Three user-selectable data flow control methods are provided: interrupt, polling, and wait-state-generation. The 1149.1 backplane test bus must be able to pause when the diagnostic processor is unavailable.

Although IEEE 1149.1 has been defined with pause states that would allow the flow of data to be paused, using this feature requires providing control for complex movements around the state diagram of the test access port (TAP). A simpler mechanism has been defined within the IEEE standard. It allows the test clock, TCK, to be stopped indefinitely at a logic ZERO. Using this option for flow control of the 1149.a test port, a rather simple flow control method can be defined. Whenever the CPU is not ready to transfer data to TDI, or from TDO, the parallel-to-serial converter, TCK will simply pause.

TMS, JTAG's singular control line, spends most of its time either HIGH, when in Test-Logic-Reset state, or LOW, when in one of the other five stable states (Run-Test/Idle, Shift-Dr, Shift-IR, Pause-DR, or Pause-IR) of the TAP state diagram. TMS only changes to control movement between stable states in the TAP state diagram. In order to move between stable states, the TMS I/O interface needs to generate short strings of ONEs and ZEROes, but never more than can be contained in one byte of information. Thus, it is possible to generate the needed control of the TMS signal with a parallel-to-serial converter much like the converters used to interface TDI and TDO to the processor bus. The TMS generator can fill the long time intervals when TMS is HIGH or LOW, by simply holding the last value shifted to its output as a static value on the TMS pin.

Once pausing TCK was chosen as the basic strategy for controlling data flow to the JTAG port, TCK pausing was extended to control other parallel-to-serial converter operations. For example, to align the serially shifted data and hence terminate shifting data through the serial scan path, a TCK counter was include which is preloaded with the length of the currently selected PCB scan ring. Once this counter has reached terminal count, it pauses TCK. At that time the data shifted into the scan chain should be aligned and ready for parallel transfer during an Update operation. Because TCK is paused, the next micro-operation can be loaded at leisure.

The selected mechanism for controlling movement through the TAP state diagram is to complete movement in small steps and to pause TCK at the end of each operation. The number of required TCK pulses is

loaded into the TCK counter. Each operation always ends with a paused TCK. Once stopped, the next operation is loaded into the parallel-to-serial converter registers. The TCK counter is loaded last.

The TCK counter can be exploited to support other features such as counting BIST clock pulses. Further, if a system has a closely controlled phase alignment between TCK the system clock, it is possible to consider repeatedly reloading and running a diagnostic and using the TCK counter to trigger a system state sampling. If the value loaded into the TCK counter is incremented for each repetition of the diagnostic test, then the system state may eventually be capture for each clock cycle of the test. If each of these captured system states is continuously saved this data would permit a pseudo logic analyzer-like display to be produced. Thus a PCB with little physical test access can be monitored or debugged with support tools that normally require attachment of physical logic probes. Even the state of ASIC internal registers could be captured for analyses.

The parallel-to-serial converter bus interface that serves as a 1149.1 test bus master could be used to enhance either an embedded system diagnostic processor or it could be used to enhance a portable computer to convert it into a portable JTAG tester. In either case, the JTAG test vectors developed for factory tests could be exported to test a module in the field, as long as the PCB could be connected to an embedded test bus.

3.1 Software Interface to the Bus Master.

To integrate the parallel-to-serial converter to the embedded processor requires a library of I/O macros. Each macro would support a minimum test operation. For example, one macro could be used to initially configure the converter. It would define the CPU handshaking method. Another could be used to preload the mode registers and to load the TCK counter before shifting TDI and TDO. This means that the command set is not inflexibly defined within the silicon of the converter but it is left as a flexible option that can be extended as desired for special applications.

4. Slave Module Interface Requirements

Directions for finding the once elusive goal of reusing 1149.1 as a simple JTAG-based backplane test bus was provided by Bhavsar[4] in his historic paper describing an addressable 1149.1 slave module interface. He proposed reusing the JTAG bus as a PCB address bus by using TDI to transmit an address upon leaving the Test-Logic-Reset state and first entering the Shift_IR state. The data shifted into the instruction register was the PCB address. However, that protocol which did not support simultaneous control of more than one module could not test backplane interconnections. That limitation has been overcome by additional extensions of the 1149.1 protocol which are contained in the Scan Bridge (See Fig 2).

These extensions provide addressability to the 1149.1 test bus by first defining a Wait-For-Address (WFA) state in which a module waits to be SELECTed or UNSELECTed. Whenever the backplane 1149.1 test bus enters the Test-Logic-Reset (TLR) state, all modules are controlled to the WFA state. (A broadcast command GOTO_WAIT can also return a module to the WFA state without the requirement to enter the TLR state.) To address, that is, to SELECT a module, an address is shifted onto the backplane test bus and into the instruction register of each module's slave interface controller.

When in the WFA state, each slave module controller will compare the contents of the address shifted into its instruction register with an address presented to a set of static input pins. Following the comparison, a module with a matching address will enter the SELECT state. Once selected, the slave module interface is connected uniquely to the test bus master. The slave module interface is now simply one more IC in the target module's scan ring. Once selected other Scan Bridge test configuration registers may be accessed and used to further control testing. They can provide local BIST support and other features such are accessing multiple local scan rings to provide access to such hardware challenges as optional mezzanine cards.

A second extension was defined to allow flexible backplane interconnect testing. This extension allows the signals forced onto the backplane by one module to be held constant while a second module is addressed and controlled to read its backplane input signals. This requirement has been met by defining a set of PARK and UNPARK commands and the supporting architecture for the scan bridge slave module interface. Because the Instruction Register of a selected slave module interface is in series with the local test ring during IR test access, an instruction can be sent to the selected module's, Scan Bridge to command it to be PARKed temporarily whist a second module is addressed.

One of the PARK instructions, park_shift_dr, when loaded into the scan bridge instruction register conditions the local scan ring TAPs to PARK and pause in the shift_dr state when the TAP controller next enters

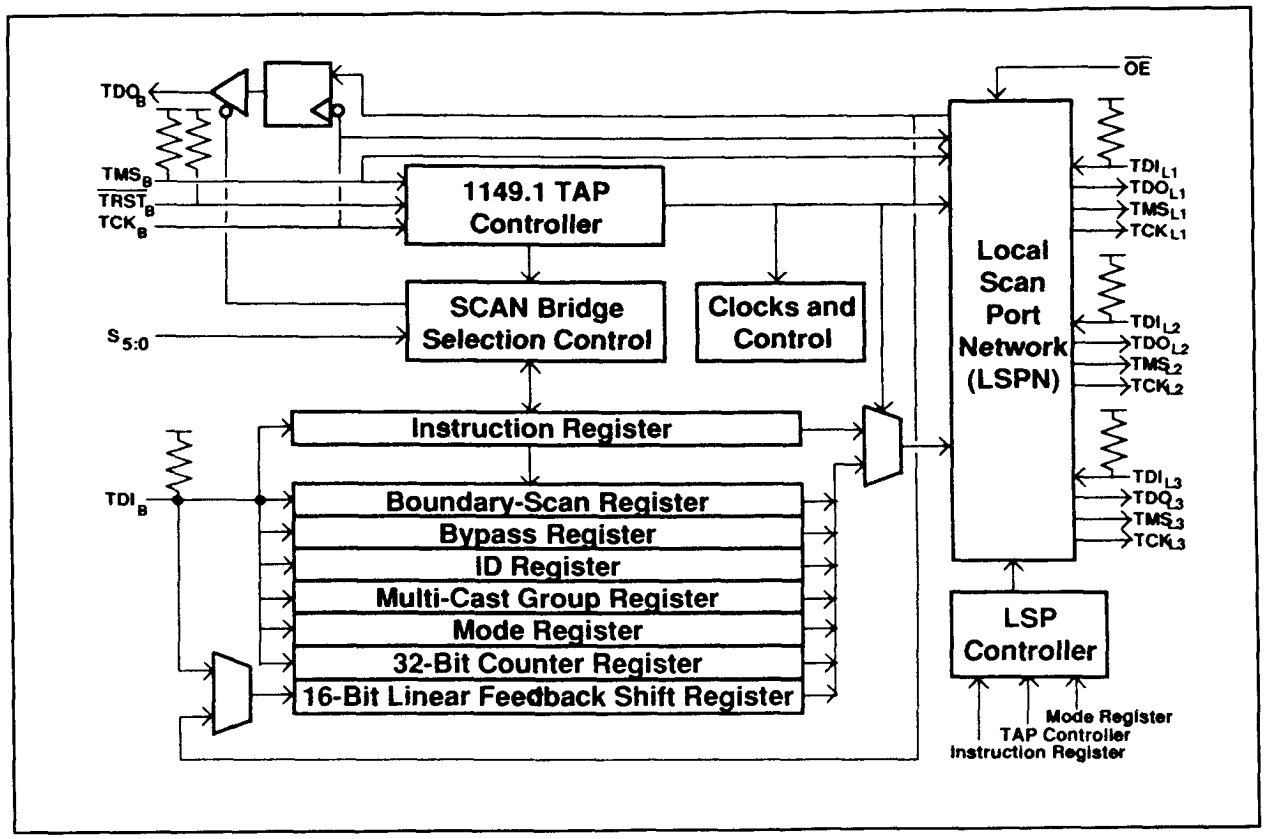

Figure 2 *Scan Bridge, Multi-Drop, JTAG Slave Module Interface.*

that TAP state. Once in that state, TCK is paused until a subsequent command is received to UNPARK that PCB's TAP controllers. While the local serial ports are frozen, the Scan Bridge backplane interface remains actively engaged with the backplane test bus.

In order to maintain synchronization between the backplane TAP state and the target module's TAP state, PARKing and UNPARKING can only change when both buses are in the same state. This means that once a PARK command has been received that many TCK clocks may intervene between the command and the operation. And after an UNPARK command has been received, the local port will not UNPARK until the backplane TAP enters the same state as the PARKed local ring. These two extensions provide a simple mechanism to control the outputs from one module while one or more other modules are controlled to read their backplane inputs.

Additional addressing modes are included in this extended 1149.1 protocol. For example, some of the slave module addresses have been allocated for broadcast and multicast addressing. Using these modes it is possible to PARK two or more modules in the same state. If more than one PCB is PARKed in Exit_DR, then they could be UNPARKed simultaneously to control several modules to inter the UPDATE-DR state at the same time. Test results could also be CAPTURE simultaneously. This simultaneous control provides embedded within a system features once requiring an external factory backplane tester.

Further, using PARK-Run-Test/Idle, it is possible to start a Built-In-Test (BIT) operation on one PCB and to then SELECT a second on PCB for BIT testing. In this manner BIT could be run simultaneously on all PCBs with the results collected once tests are complete by addressing each PCB one-at-a-time.

5. Example Application

Champlin[5] described the application of these components as they have been exploited by Motorola in its Iridium Satellite. In that application to provide fault tolerance, bus masters were sometimes co-located with the Scan Bridge to provide a master-capable slave module. By using embedded system test access Iridium is expected to be able to build and launch satellites at the rate of one-a-week. This level of embedded test access with isolation to a single component is an improvement upon the physical access once provided by bed-of-nails

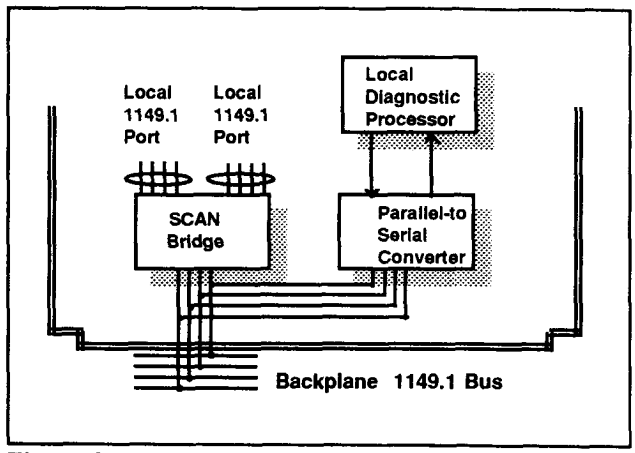

Figure 3 *Example Application: A Master-Capable Slave Module.*

fixtures. Such in circuit test methods are now possible within physically inaccessible sealed systems and even when in orbit.

6. Conclusions

JTAG has been extended to serve as a backplane test bus by defining a simple protocol extension to the 1149.1. A new protocol is not needed. This allows factory test programs to be reused in for embedded test access either at factory system test or even in the field to verify system structural integrity or to isolate defects.

7. Acknowledgements

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8. Author

John Andrews, a graduate of the University of Maine, holds seven patents for IC design, has served as a member of the IEEE 1149.1 Working Group and as chairman of the Maine and Boston Chapters of the IEEE Computer Society. He is a Licensed Maine Guide.

9. References

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