A Low Power Programmable Logic Device Reconfigurable for 3.3V or 5.0V Operation During and After Fabrication

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Abstract

A programmable logic device which is reconfigurable to operate at either a 3.3V or 5.0V supply specification has been fabricated. On-chip circuity is dynamically adjusted for 3.3V or 5.0V operation. The voltage supply configuration can be changed after fabrication by opening a fuse or writing into a selection register. The device consumes less than 500uW of power at 3.3 volts.

Introduction

The goal was to design a device that could easily be switched from 5.0V to 3.3V as the market dictated. This was particularly important for a programmable logic device where the 3.3V market is still in its infancy. With hand-held and other low power applications growing rapidly the demand for 3.3V devices could surge quickly. The flexibility of this device allows a response to the potential rapid ramp up in 3.3V applications while efficiently meeting current 5.0V demand.

Implementation

This programmable logic device device allows low power 3.3V and 5.0V operation, and is programmable for operation at either supply voltage both during and after fabrication. Voltage selection is programmed during fabrication with a metal option. The state of this metal option is decoded by on-chip circuitry to enable operation at the desired voltage. The state of the voltage selection metal option is the only difference between the the 3.3V and 5.0V version of the device at the foundry level. All circuitry necessary to operate correctly at both voltages is present on the chip.

After fabrication, it is possible to create 3.3V devices from 5.0V parts, and vice versa. This is done in one of two ways: A nonvolatile change can be made by opening an on-chip fuse with a laser. A volatile change, which allows testing to be performed prior to committing to the nonvolatile change, can be made by writing into an on-chip selection register. Figure 1 illustrates this selection circuitry. The switch represents the

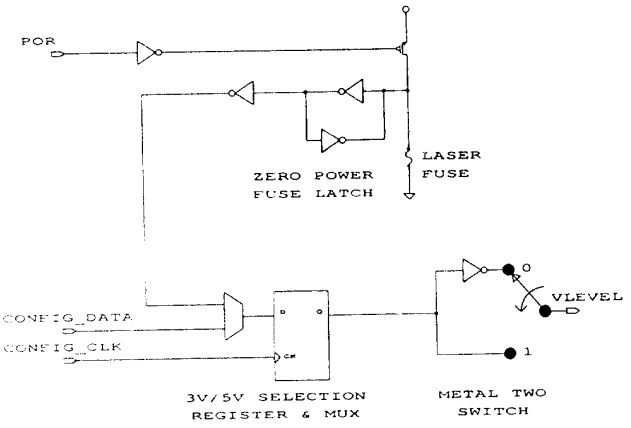

Figure 1. Selection Circuits

choice made during fabrication to create a 3.3V or 5.0V device. The fuse latch is read when the chip powers up and this data is loaded into the selection register during chip configuration. To maintain low power the fuse latch is made zero power by the POR signal returning to 0V (POR is described below) to turn off the fuse pull up. The selection register can be written into directly,

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Fuse Data (0 = intact) (1 = opened)	Metal two switch position	Chip Vcc operation
0	0	5.0V
0	1	3.3V
1	0	3.3V
1	1	5.0V

Fuse Data can be overwritten by writing directly into t selection register after the chip is configured.

Table 1. 3.3V / 5.0V Selection Table

overwriting the fuse data, to change the voltage supply choice made with the metal option. The supply voltage choices are summarized in table 1.

The architecture uses FIFO SRAM cells to retain configuration data and uses multiplexers to implement four variable function generators. Figure 2 shows both a function generator cell and detail of the SRAM cells that are used for maintaining configuration data. The SRAM cells are composed of a cross-coupled pair of inverters with a pass gate controlled by an address signal. This arrangement insures the cell is zero power once configured. An on-chip controller drives the address lines of the SRAM, loading configuration data serially. The function generator is used for the implementation of all on-chip combinatorial logic. It uses no analog circuits such as sense amplifiers or reference sources which consume D.C. power and are difficult to optimize well over the required 3.3V to 5.0V operating range. The function generators use n-channel only pass transistors to form the multiplexers and operate at supply voltages over $2V_Tn$. N-channel only pass gates are also used in the interconnect that drives the function generators. This allows for compact layout while giving good speed performance and functionality to low voltages. The performance is in fact faster than had full CMOS transmission gates been used. This is due to the increased capacitive loading that the p-channel device would present. P-channel feedback transistors are used to insure zero power operation by regenerating the Vcc-V_Tn logic high signals at the input and output of the function generator to a full Vcc level. For maximum performance the inverters that are driven through the n-channel only multiplexers are designed with an input threshold slightly lower than 1/2 Vcc.

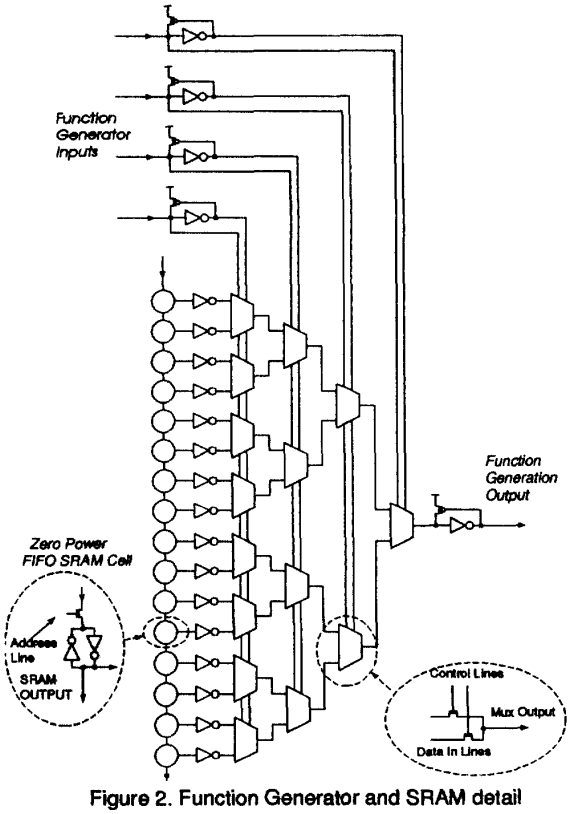

Figure 2. Function Generator and SRAM detail

The overall architecture of the chip is shown in figure 3. Function generators are paired with configurable flip-flops to form Logic Elements (LE) . Groups of eight LEs are placed into Logic Array Blocks (LAB), with fully populated local interconnect. The interconnect is programmed by SRAM architecture bits controlling n-channel pass transistors. LABs are placed into rows. LAB communication along a row is accomplished by

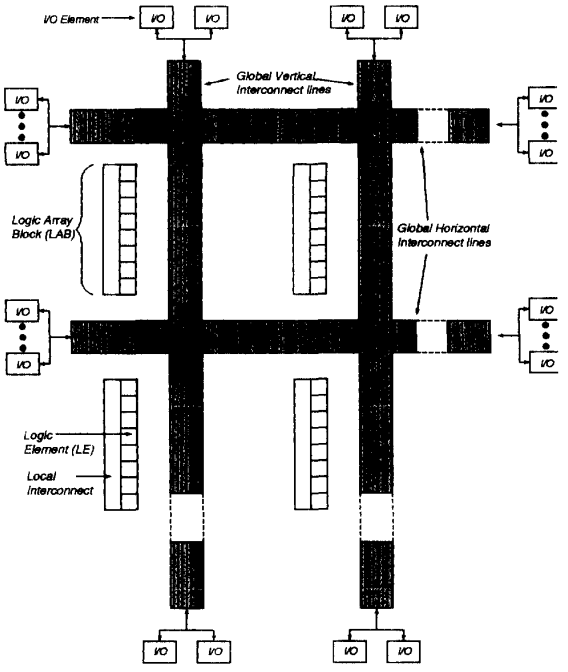

Figure 3. Chip Architecture Overview

Global Horizontal Interconnect lines, which span the entire row. Communication between rows is accomplished by Global Vertical interconnect lines which span the entire height of all of the rows of the chip. There are a total of 208 LEs organized into two rows of 13 columns. In addition the 74 I/O pins have configurable Input/Output registers.

The only analog circuit on the chip is the Power On Reset (POR) circuit. The POR circuit is used during power up to signal the start of configuration of the on-chip FIFO SRAM. The POR circuit generates a signal named POR that remains high until the supply voltage is high enough for proper SRAM operation. This voltage is designed to be safely below the minimum 3.0V power supply operating level. Figure 4 shows the POR circuit. It is composed of three copies of the SRAM cell with weak pull ups and pull downs to bias the output state to a high. For the POR circuit to signal the start of configuration the Vcc level must reach the SRAM operating level of 2.1 Volts plus approximately 0.4 Volts in order to over come the biases. Three SRAM cells are needed: The first is used to create an accurate input impedance for the second cell. The second and third cell make sure both a "1" and "0" are writable into the SRAM. The POR circuit is the only circuit that draws any D.C. power on the chip. Chip Icc standby is below 150uA. Once the POR circuit signals that Vcc is above the functionality threshold of the SRAM cells, the device begins configuration. The chip has several

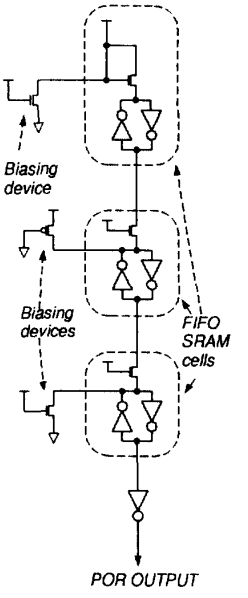

Figure 4. Power On Reset (POR) circuit

configuration modes which are controlled by mode pins. Configuration data may come from a variety of off-chip sources, including a configuration ROM or a microprocessor bus. If at any time during or after configuration a Vcc brown out occurs (Vcc drops below the SRAM operating voltage) the POR circuit will trigger the part to reinitialize and restart configuration.

The TTL input buffers are shown in figure 5. They have been optimized for 3.3V operation when signal VLEVEL is "0" and for 5.0V operation when "1". The input threshold is

adjusted by enabling the second n-channel pull down path. It is important to center the input threshold individually for the two operating voltages in order to maintain safe input noise margins. The device uses CMOS output drivers that give good performance and meet industry standard 3.3V and 5.0V output specifications without requiring alteration between operating voltages. The 3.3V Vcc input to output delay, from pad to Global horizontal line, through an LE, out onto a Global vertical line and to an output pad is under 23ns.

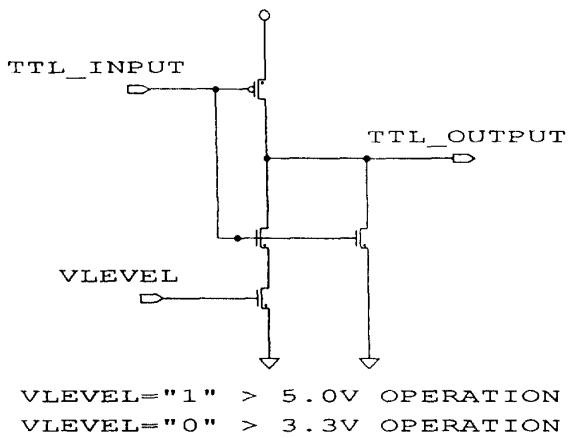

Figure 5. TTL Buffer

References

1. FLEX Family Programmable Logic Device Data sheet

2. FLEX Programmable logic Product Information Bulletin