Tool Reusable for DSP System Emulation and Board Production Testing

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INTRODUCTION

Design of a Digital Signal Processor (DSP) system requires two important tasks to be addressed for successful hardware/software integration and system verification. First, there must be a debug tool for testing code on the hardware. Standard debug capabilities for accessing on-chip emulation ports on devices must be available and allow communication with various types of architectures. This means the tool must be able to read/write memory and registers, set breakpoints, single step through code and load or save programs to one or more devices in the system. Most DSPs and Reduced Instruction Set Computers (RISC) today have a means for accessing on-chip resources via a serial interface to a debug port.

Second, there must be a tool for testing out boards for system functionality. A viable solution for addressing high pin counts, Multi-Chip Modules (MCM), surface mount technology and custom Application Specific Integrated Circuits (ASIC) is the use of a standard serial scan methodology. Therefore the tool must be able to provide a means for serially accessing N bit register cells, support 3-V or 5-V input and output pins, hopefully be portable to various computer platforms, and have some ease of use for quick generation and evaluation of test vectors for a board or system level test environment.

The increased use of the Joint Test Action Group (JTAG) serial port for access and control of complex system design has led to the development of a tool which has multiple use. A universal JTAG port command converter has been designed which can communicate with Motorola DSP on-chip emulation circuits as well as the serial JTAG shift register cells of devices designed into a system.

Standard JTAG controller chips on the market today are designed as a group of control and data registers with a memory for loading serial data. These controllers are state machine driven and normally have a bus interface for accessing their registers and memory. Data on these devices is serially shifted out to the target by sequencing through a data memory after hardware counters are loaded. This requires the controller chips to be driven by a host computer or a microcontroller. These JTAG controllers are dedicated and locked to specific hardware and software platforms such as Personal Computers (PC).

A universal command converter has been developed by the Motorola DSP Division Development Tools team which allows high level command packets from a host computer to be transferred to a DSP- based microcontroller which converts the command packets and data to JTAG equivalent serial bit streams. This method of high level interface provides flexibility for developing special emulation commands and board level JTAG serial test vectors in systems developed using Motorola DSP architectures.

QUICK REVIEW OF IEEE 1149.1 REQUIREMENTS

In order to understand better the design and test requirements of a DSP based system using JTAG, let's review the fundamental requirements of the Institute of Electrical and Electronics Engineers, Inc. (IEEE) Standard

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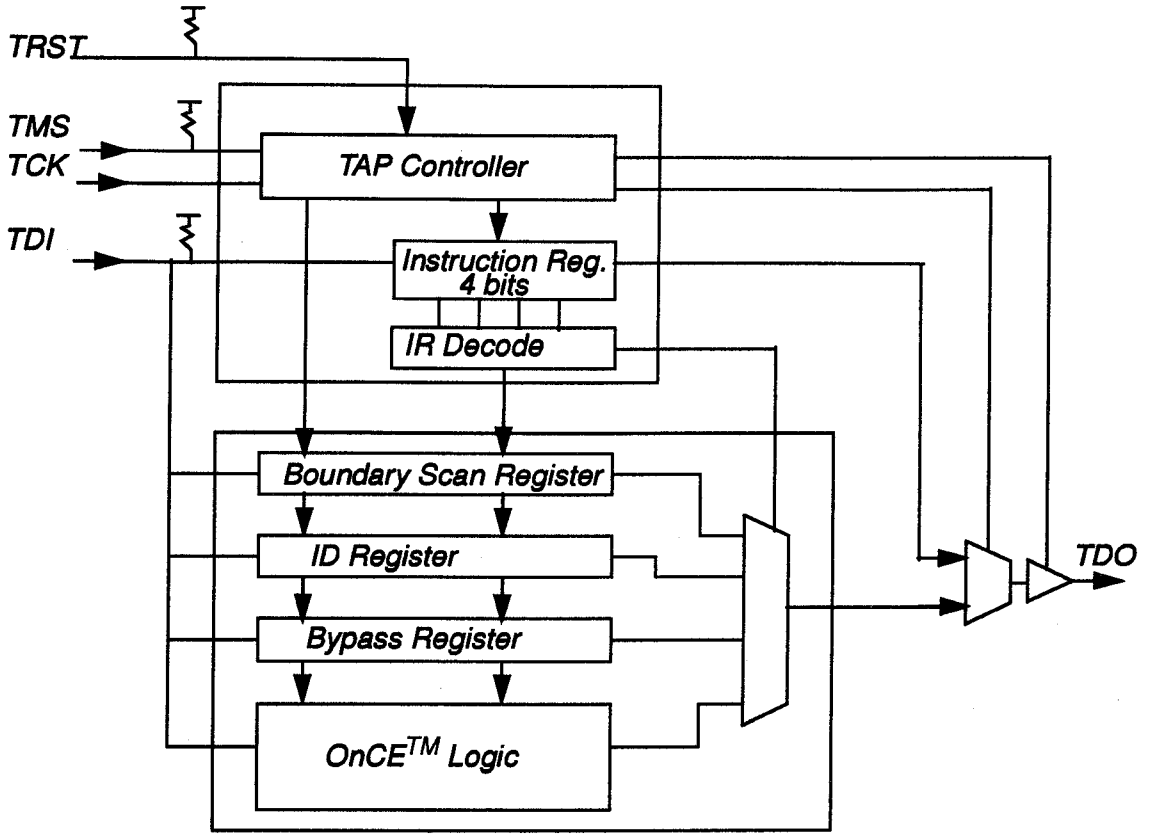

Figure 1 - JTAG/OnCE Interface on DSP56300,DSP56600 and DSP56800 Families

Test Access Port and Boundary-Scan Architecture (Std.1149.1) and how it is implemented on a Motorola DSP

Figure 1 is a block diagram of a Motorola DSP implementation of the IEEE 1149.1-1990 test logic coupled to a OnCE[1] block.

A minimum of four dedicated pins must interface to a Test Access Port (TAP) which contains a 16-state controller. The TAP contains the circuits needed for testing the interconnections between integrated circuits once they have been assembled onto a printed circuit board. This is accomplished using a boundary-scan technique. Boundary scan is a method used for observing signals at each component pin. A shift register stage is placed adjacent to each pin so pin values may be controlled or monitored. This is important for testing continuity and pins that may be stuck at one or zero.

A user defined block may also be accessible via the TAP controller. Motorola DSPs that have JTAG ports also have an on-chip emulation block accessible via the JTAG pins. This block allows users to communicate directly with the program controller in the DSP core so that machine instructions can be fed directly to the program decoder and executed. This allows users to have direct access to all on-chip resources and also provides a convenient means for dynamically testing a board or system for timing and functionality using DSP assembly language programs. The OnCE block is a user defined block and is not a required block in the IEEE 1149.1 standard.

The dedicated JTAG pins are:

TCK - Test clock input to synchronize the test logic.

1. OnCE is a trademark of Motorola, Inc. All product and brand names appearing in this article are registered trademarks or trademarks of their respective holders.

TMS - Test mode select input, with on-chip pull-up resistor, sampled on the rising edge of TCK to sequence the TAP controller's state machine.

TDI - Test data input, with on-chip pull-up resistor, sampled on the rising edge of TCK.

TDO - Three-state test data output that is actively driven in the Shift-IR and Shift-DR controller states. TDO changes on the falling edge of TCK.

TRST - Test reset input with on-chip pull-up resistor, provides an asynchronous initialization of the TAP controller and is optional.

The TAP controller is a synchronous finite state machine that responds to changes at the TMS and TCK pins. Transitions from one state to another occur on the rising edge of TCK.

There are two paths to the TAP controller state machine. The SHIFT-IR_SCAN path is used to capture and load JTAG instructions into the instruction register. The SHIFT-DR_SCAN path is used to capture and load data into the test data registers. The TAP controller executes the last instruction decoded until a new instruction is entered at the Update-IR state or until the Test-Logic-Reset state is entered.

There are three mandatory instructions required in the IEEE 1149.1 standard **(Bypass, Sample/Preload, and Extest)**. The Motorola DSP IEEE 1149.1-1990 implementation includes six public instructions (CLAMP, HIGHZ, EXTEST_ PULLUP, IDCODE, DEBUG_REQUEST, ENABLE_OnCE). The TAP controller contains a four bit instruction register which presents an instruction to be decoded during the Update-IR state. All communication with the OnCE port is conducted via the Shift-DR path after Enable_OnCE is decoded by the TAP controller.

UNIVERSAL COMMAND CONVERTER

The requirements definition of a debug and test controller were put together using customer inputs and prior experiences of the development team. It was realized that the speed of the serial transfers was important since a system could comprise of one or more DSPs. Low power applications where Vcc could be less than 3-V needed to be considered and the mobility of the tool was important since many customers used different computer platforms and operating systems.

Analysis of what was available on the market using criteria such as ease of use, availability, cost, and the requirements previously described, it was decided to use an intelligent controller instead of a dedicated state machine driven controller. Also, the generation of test vectors and control stimulus to the target DSP's debug ports needed to be flexible especially during initial system development. Implementation of the necessary blocks of a serial sequencer were achievable in software so the real task was finding a controller that could handle the tasks in the approximate time it would be performed in dedicated hardware.

HARDWARE REQUIREMENTS

A fast microcontroller with sufficient on-chip resources to handle the electrical requirements of a JTAG protocol was needed. After benchmarking several general purpose microcontrollers we concluded that the DSP56002 at sufficient speed would be an excellent fit for converting high level command packets from a host computer to serial bit streams that adhered to the JTAG protocol. The system could act as a standalone controller that was portable to the most popular computer platforms with minimal hardware and software effort.

The command converter is based on an 80 MHz DSP56002 which uses its on-chip resources to minimize and simplify the interface to the target JTAG/OnCE debug ports. Communication with a host computer is via the DSP56002 Port B in an 8-bit parallel fashion or via the Serial Communications Interface (SCI) port, while the JTAG serial interface to the target(s) is via the DSP56002 Synchronous Serial Interface (SSI) port.

Figure 2 illustrates the minimal external hardware which is required using the DSP56002. A high speed buffer was put between the DSP56002 SSI and the target JTAG chain so the voltage to the target would be dictated by the target's power supply. The DSP56002 has an on-chip Phase Lock Loop (PLL) for variable system clock frequencies and is used for software

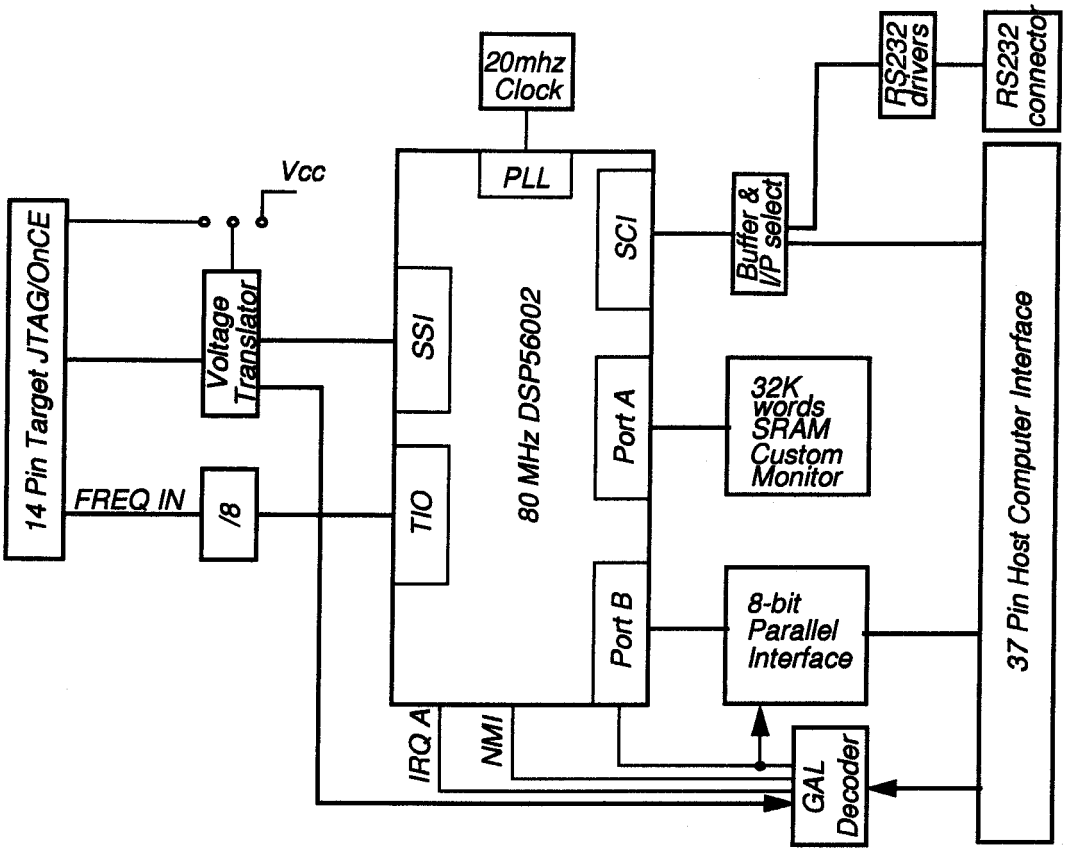

Figure 2 - Universal JTAG Command Converter based on 80MHz DSP56002

control of target systems that require slow clocks.

Although the IEEE 1149.1 JTAG specification dictates that the TCK clock must be independent of the device it is built into, there are many occasions where user defined blocks must synchronize to the TCK pin to latch the correct data. If the TCK frequency is running at a rate faster than the target's system clock, the TCK frequency must be slowed down to allow correct synchronization. The DSP56002 has an on-chip timer that may be used to measure the target's frequency to determine what clock rate is appropriate for sending and receiving serial scan information.

As the number of devices increases in a JTAG daisy chain, the capacitive loading of each device input will begin to affect the rise and fall time of TCK and TMS. It is good practice to buffer the TCK and TMS lines with a minimum of four loads per buffer to insure setup and hold times for TDI, TDO and TMS are met when clocking data into and out of the system.

The command converter provides a reset control signal on its 14 pin connector, so care should be taken during initial JTAG interface design to evaluate whether the entire system should be reset simultaneously. It should be noted that in a system that has all device reset inputs tied together, each assertion of the reset pin will force all devices to initialize. This may be undesirable during the debug process especially where devices interact and one device may need to be reset but not the others.

SOFTWARE REQUIREMENTS

Since JTAG control is now software driven, it was decided that a painless means for software upgrades or bug fixes was needed. The command converter exits reset in the bootstrap mode of operation and boot loads its monitor program into a local 32K Static RAM array over the SCI port from the host computer. The current monitor program is about 8K words in size

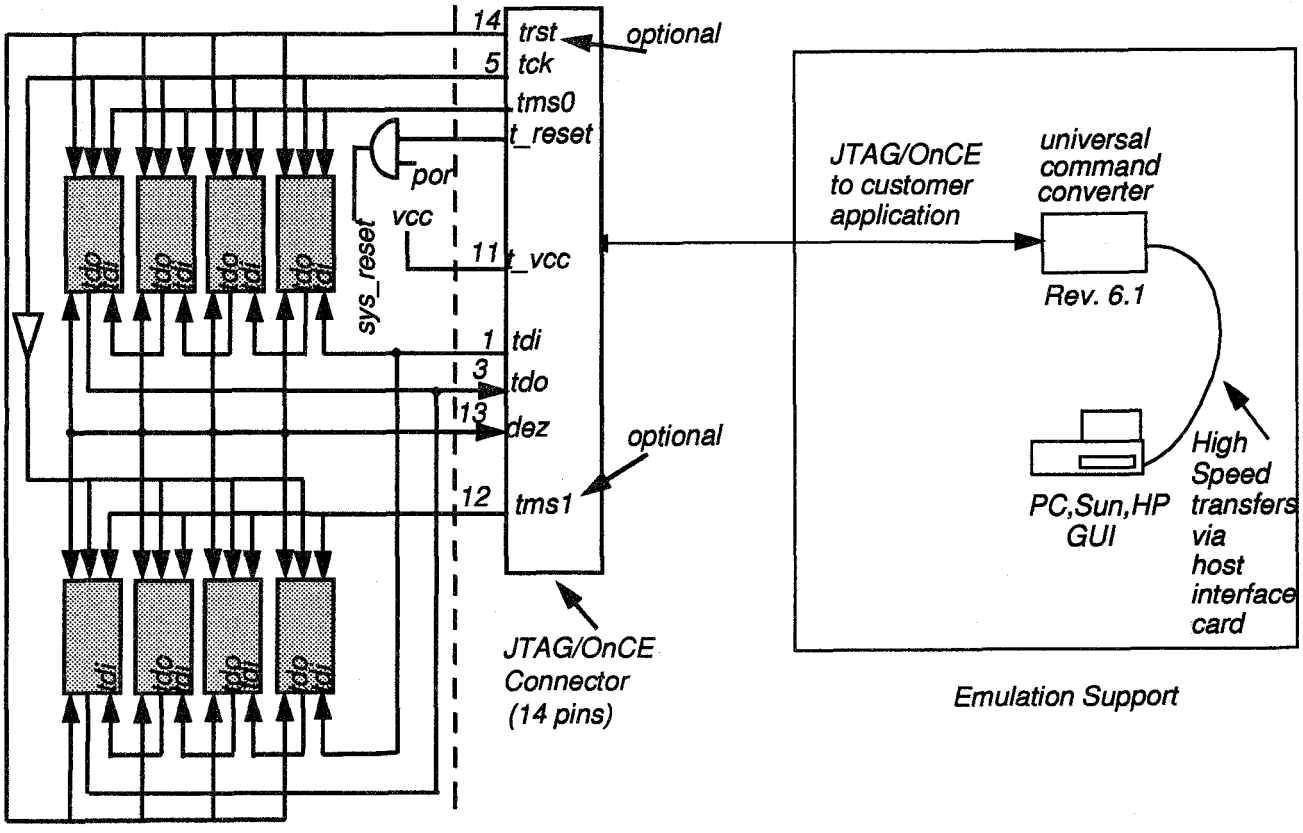

Figure 3 - Example JTAG Hookup of multiple DSPs using Universal Command Converter

so lots of storage is available for loading and running large test sequences.

The development of three Motorola DSP cores which have JTAG ports led the development tools team to design the command converter monitor program in a modular fashion so that each new architecture added would utilize the existing drivers. A set of command packets was defined to allow the host computer to be loosely coupled to the command converter local resources. The command packets were designed for emulation control and it was later realized that the same concept could extend to control of a boundary scan sequence.

A set of drivers written in the C language provide the host computer's interface to the command converter. These functions provide the command packets for reading and writing serial sequences to the target. Source code to the C drivers as well as the command converter monitor is made available to users when purchasing an Application Development System (ADS) for a Motorola DSP.

The command converter is fully supported with a Graphical User Interface (GUI) for system hardware and software debug. The GUI runs under Microsoft Windows 3.1 and Windows 95, Hewlett Packard's Unix operating system 9.x, and Sun Microsystems Solaris operating system 2.5. It provides source level debugging capabilities for single or multiple DSP based target systems.

DESCRIBING AND TESTING A SYSTEM WITH MULTIPLE DEVICES

Figure 3 illustrates a multiple DSP system and its JTAG hookup. For emulation purposes, this hookup would be described using a **DEVICE** command in the GUI so the command converter is configured properly for communicating with each device. Devices which are not DSPs can also be hooked in the serial daisy chain and information describing it's JTAG instruction bit length are entered again using the **DEVICE** command with different arguments. Designa-

tion of a device number is arbitrary as long as the device position is described correctly with respect to which command converter it is tied to and which of two TMS lines it is controlled by.

Each command converter can support emulation for as many as 24 devices in a JTAG daisy chain. Each command converter has a unique address ranging from 0 to 7 which allows users to debug multiprocessor systems where as many as 8 command converters are tied in parallel to the host computer interface port. This allows a total of 192 JTAG devices that may be controlled in a complex system.

For boundary scan cell control its not as simple as this. The user target system must be described in a hierarchical manner. Boundary-Scan Description Language (**BSDL**), which is a subset of VHDL (Very High Scale Integrated Circuit Hardware Description Language) describes the IEEE 1149.1 implementation on a device and how it operates. There is now a language extension to BSDL developed by Texas Instruments, Inc. called Hierarchical Scan Description Language (**HSDL**) which allows a complete system to be described using information from BSDL.

Once a system has been described in a hardware description language, the output of this description must be fed into the command converter. A serial vector format (**SVF**) developed by Texas Instruments, Inc. and Teradyne Inc. is becoming widely accepted as a defacto standard file format for expressing serial test stimulus and response for IEEE 1149.1 based tests. The universal command converter monitor is being modified to support the SVF file format so that test patterns generated using widely accepted industry tools may be driven onto the target JTAG port via the command converter.

Support is accomplished by reading the SVF ASCII file using software drivers written in C on a host computer, translating the information into command packets and sending these command packets to the universal command converter. The command converter will then translate these packets into boundary scan serial bit streams and send and receive the appropriate bit length defined in the SVF file. Output response from the target is stored to a file for later review.

This added capability will allow users to perform static test analysis for physical board design verification as well as production testing. Dynamic tests for DRAMS or other synchronous devices can easily be accomplished using assembly language programs downloaded and run on the target DSP.

SUMMARY

Tools that support designs that use the IEEE 1149.1 JTAG port for emulation and board test are becoming more common. These tools not only are used to debug hardware and software interaction but are now used to validate the design using sophisticated board test techniques. High level languages are now being used to describe these designs and the complex interaction of boundary scan cells and built in self-test circuits. These tools provide the necessary set of capabilities for getting the job done quickly at all levels of the product life cycle. The use of an 80MHz DSP56002 as a JTAG controller allows developers to utilize a common tool on various computer platforms using a Motorola GUI or developing their own custom built utilities using a set of readily available device drivers and libraries.

The three newest Motorola DSP core based architectures (DSP56300, DSP56600 and DSP56800) have IEEE 1149.1 JTAG ports for emulation and pin boundary scan. Development tools which support full source code emulation in the target system as well as board/system level boundary scan cell control are available for these cores.

REFERENCES

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