A Low Cost and Interactive Rapid Prototyping Platform For Digital System Design Education

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ABSTRACT

In this paper, we describe a cost-effective FPGA-based logic circuit emulation platform. It consists of a hardware engine to emulate the circuits and software for the user interface to drive the emulation and monitor the results. It is a very flexible and powerful design verification platform. Additionally, its economical price makes it possible to assign an FPGA (Field Programmable Gate Array) prototyping board to every student. This system provides an interactive verification environment using a communication protocol through bi-directional serial link, like the RS232C. Our system has the potential to meet market demands, especially in the educational field, which requires a low cost and yet powerful verification methods for digital hardware design.

1. Introduction

Verification is becoming the most critical and time consuming part of digital hardware development. In academic classrooms, verification is an inevitable part of design education. Traditionally, students just use the software-based simulation tool to verify their design correctness. But, source level functional simulation by software is too slow and not enough to confirm the correctness because of the mismatch problems between simulation and synthesis, and timing-related problems. These problems are cleared by lower (gate) level simulation/emulation after logic synthesis and mapping procedure. The software-based gate-level simulation or timing simulation is available for further verification. But, these have limitations in simulation performance.

Hardware-based emulation by FPGA prototyping board [1,2] is one of the emerging alternative approaches that accelerates digital design verification while achieving both higher accuracy and better performance. For each specific application, the different FPGA board design and implementation is required to support each verification requirement. Different board designs mean more expenses and more verification time. Even the existing general purpose rapid prototyping FPGA boards of high-end technology are not applicable for some complicated applications which need special peripherals like wireless communication links or many multimedia I/O peripherals. Furthermore, it is hard to learn how to use the generic multi-functional prototyping board for each specific demand. The "Chipscope" tool [3] from Xilinx may be an alternative to solve this limitation. However, the Chipscope has its own limitation, because it cannot provide the stimulus to the FPGA but just probes the signals in the FPGA by acting as an embedded logic analyzer.

In [4] we developed an interactive hardware-based verification platform named "LAPG (Logic Analyzer and Pattern Generator)". This platform requires only a simple FPGA board with minimum features which enables hardware emulation system economically as shown in Figure 1. This approach is based on a virtual hardware wrapper that generates the stimulus and probes the outputs of the design under test as shown in Figure 2. This eliminates the I/O restrictions and provides controllability and observability on the design. The verification procedure with LAPG is shown in Figure 3.

The hardware and the software of the LAPG on the host machine communicate with each other to verify the user design implemented with FPGA. This serial communication link provides the LAPG flexibility and the core features as a generic hardware-based verification engine. The LAPG [4] is inefficient due to the communication overhead between host machine and FPGA board.

In this paper, we develop an enhanced version of LAPG (new LAPG) by proposing a new communication protocol to minimize the communication overhead and to add more features.

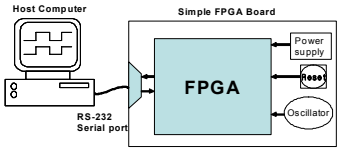

Figure 1. A simple rapid prototyping board organization consisting of an FPGA chip, serial port, and oscillator

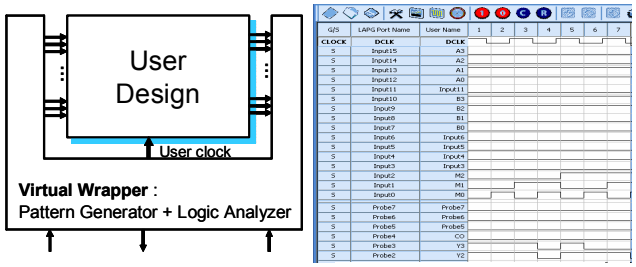

Figure 2. (a) Wrapper circuit for LAPG : wrapper is connected to the primary input and output ports of user design. (b) Software GUI part for LAPG on host computer : it captures stimulus for the circuits under test from user interactively and communicates with LAPG Virtual Wrapper to get the responses and emulation results showing the waveform to users graphically.

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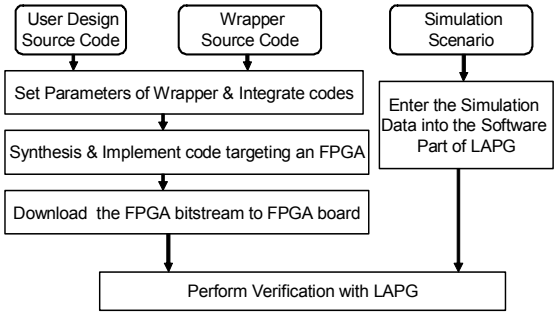

Figure 3. Verification flow with LAPG

2. Enhanced Approach: New LAPG

The enhanced communication protocol of the new LAPG gives less communication overhead and more verification capacity. For example, with new LAPG we can specify the number of clock cycles needed to get the computed results without additional input data. And, we can do experiment with different types of clocking schemes.

The new communication protocol consists of four types of packets: (1) commands, (2) ACK (Acknowledge), (3) injection data, and (4) sampling data. The commands provide the instructions from the software to the hardware on how to apply stimulus and monitor the output data. The ACK is the response from the hardware to the software which confirms that the hardware received the proper command and is ready for the next command or data from the host computer. The command packet formats are shown in Figure 4. The reset command performs configuration and execution command, which defines the following data packets. The command packet can change the LAPG execution parameters including the active clock edge type, sampling timing, the number of clocks before sampling, and the number of injection data packets following the command packets.

With the proper packet mix, we can minimize the communication overhead, thereby achieving better performance. Figure 5 shows a typical communication scenario for multiple inputs and outputs data exchange between host and FPGA. Figure 6 shows the reduced communication overhead by the new LAPG compared with the old LAPG. The circuit examples of number 5 and 8 in Figure 6 are des and 8051 core respectively. The other circuit examples in the Figure 6 are simple circuits such as ALU, counters, multiplier, booth multiplier, divider, and priority encoder.

3. Applications to Design Courses

We use the LAPG in digital system design courses for junior student laboratory experience. Students used the LAPG to prove from simple counter design to the 8-bit microcontroller design. Before we started using this platform, two or three students shared a single FPGA board for experiments. With this new platform it is possible for every student to have their own FPGA board because of its low cost. In addition, this FPGA board eliminates the restriction of the I/O environment because any special I/O peripherals are not needed. It is possible to replace logic analyzers with our LAPGs at laboratories. Students were able to perform I/O signal monitoring of design circuits without using so expensive and complex logic analyzers. Furthermore, we may save verification time since we can use the same test vectors for both software simulation and FPGA-based hardware verification.

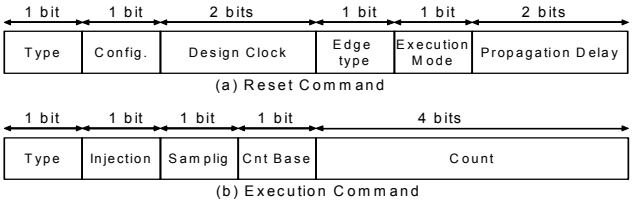

Figure 4. New LAPG command packet formats

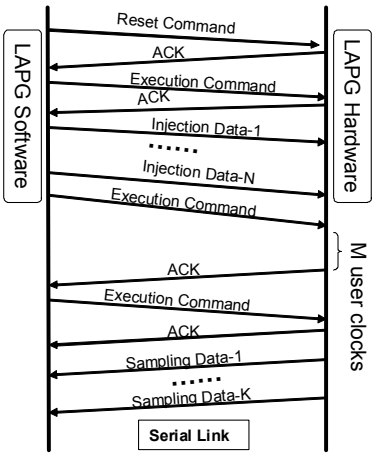

Figure 5. Simulation scenario with new LAPG (des example)

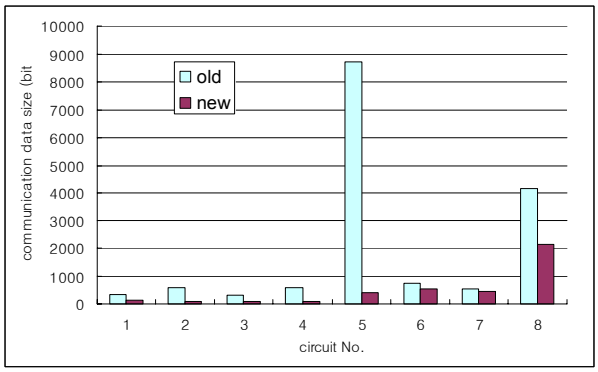

Figure 6. Communication data overhead comparison between old and new LAPG

4. Conclusion

In this paper, we proposed an efficient hardware verification platform based on a virtual wrapper and serial communication protocol. We believe that the proposed platform can meet the education market needs for an interactive and flexible design verification environment at a very low cost.

References

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