Research on Design for Testability of PCB Based on JTAG

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Abstract: Design principle and methodology of DFT in BST are discussed ,fault models of interconnect on a circuit board and equivalent exchange are done in order to simplify test process. Mathematical models of BST are established also in this thesis. Based on above principle and methodology, test stimuli generation and test response analysis of boundary scan interconnect test are studied .Two optimal boundary scan interlink age test algorithms are presented. Using DFT methodology of boundary scan, DFT of circuit board is finished, by two optimal algorithms, test effectiveness and correctness is validated.

Keywords: Boundary scan;design-for-Test;PCB;IEEE 1149.1 Standard .

1 Introduction

BST (Boundary Scan Test) is one kind of test technology based on DFT (Design For Testability) of integrate circuit[1]. It finishes the test and fault diagnose of the circuit system through the analysis to the output respond, which the test figure is inputted the test register of the IC. At present BST technology mainly has four kinds of application ways: the interconnection test of the circuit board、the completeness test of the boundary scan chain、the device function test and the device existence test. In addition, boundary test is also extensively apply to the program and debugging of the device.

2 Mathematics Model of the BST

The test matrix T formed of the certain quantity test vector will be inputted in A, then the BST diagnose the fault according to responding matrix R. In the BST circulation, the vector that is formed from the test code loading on every network is called PTV(Parallel Test Vector),write it for v_j^p （j=1，2，…，N）. Corresponding the test response vector adopting a certain PTV is called PRV(Parallel Response Vector),write it for v_j^p （j=1，2，…，N）. In fact, we should regard the tested circuit as a N input/N output system, its input vector and output vector are also bull vector. For one general N input/N output static system (the output and input is real number vector),the BST course can be expressed through a simple linear equation under the ideal situation not considering the noise[2].

$$Y=D*X \qquad (1)$$

Among them， X and Y represent separately the input matrix and the output matrix, D is the system characteristic matrix. Then, the fault diagnose problem for the N input/N output system will turn the distinguishable problem that has known the Y and X matrix and get the D, in fact, this can be summed up in the course of getting the contradictory matrix. For the BST, we can set up the similar model with the formula (1):

$$R=C(A,T) \qquad (2)$$

Among them, the R matrix represents the test matrix and the T matrix represents the response matrix, the A matrix represents the circuit board fault characteristic matrix. For the formula (2) to be established, firstly, we must construct rationally short circuit fault characteristic matrix A ,which possesses the mapping relation with short circuit fault. Then we must also construct a kind of rational operator C and establish the mapping relation

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between A , T matrix and R matrix.

The circuit board fault can be divided into the open circuit fault and the steps from physics, from logic, it can be divided into S-A-1 fault (Stuck at 1) 、S-A-0 fault (Stuck at 0)and bridge graft short circuit fault . it's fault characteristic matrix ai,j (NxN) can be expressed 1 or 0 for any inputting v_i^P in i network.

Take example for the short circuit, we can set up the N×N steps short circuit fault characteristic matrix as the following form:

$$\begin{array}{c} \\ \\ \\ \text{i row} \\ \\ \text{j row} \\ \\ \\ \end{array} \begin{array}{c} \begin{array}{cccccccc} & & & \text{i} & & \text{j} & & \\ & & & \textit{line} & & \textit{line} & & \end{array} \\ \left|\begin{array}{cccccccc} 1 & 0 & \cdots & 0 & \cdots & 0 & \cdots & 0 \\ 0 & 1 & \cdots & 0 & \cdots & 0 & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & & \\ 0 & \cdots & \cdots & 1 & \cdots & 1 & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & & \\ 0 & \cdots & \cdots & 1 & \cdots & 1 & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & & \\ 0 & \cdots & 0 & \cdots & 0 & \cdots & 0 & 1 \end{array}\right| \end{array}$$

If i network and j network of the fault circuit board short circuit, ai,j and aj,i of the fault characteristic matrix are 1, the element of the rest no fault characteristic in matrix are all 0. In addition, the diagonal element of the matrix is 1, it represents that any network shorts circuit with itself. The short circuit fault characteristic matrix belongs to the symmetrical bull matrix. The fault characteristic matrix degenerates into the unit bull matrix when the short circuit fault doesn't take place. Namely no fault characteristic matrix belongs to the unit matrix(unit bull matrix defines , δi,j =1, if i=j; δi,j =0，if i≠j). It is obvious that the fault characteristic matrix can describe accurately whether or not exist short circuit between every network ,the one-one relation exists between it and the short circuit fault.

After setting up above-mentioned fault characteristic matrix, The ones that look for one rational operator to set up the mapping between the R matrix with A and T is next job.

3 Boundary Scan Interlinkage Test Algorithms

Since the BST technology was born, a lot of scholars proposed successively some classical algorithms, for the instance MCSA algorithm[3],True/Compliment algorithm, adaptive algorithm of W step, adaptive algorithm of C step etc. The test vector that above-mentioned classical algorithms produce is simple, the code is easy and the classical adaption algorithm meets the completeness of testing, but the test time of the classical algorithm is long, the ability to diagnose the complicated circuit fault is bad. In order to remedy insufficient ,some scholars propose the test information condensation algorithm[4] and GANN test vector producing algorithms, these new algorithm that adopt new theory in optimizing the test vector have some unstableness, the test time is short, but there are more appended condition in optimizing and it is difficult to fix, so we need to analyze according to the concrete conditions and choose the suitable test algorithm.

The text selected two slices of Common Programmable Logic Device(CPLD) and design the principle demonstration board of boundary scan, as fig (1) showing. On the basis of interlinkage test algorithm, we can combine manufacture techniques of integrate circuit with concrete characteristic of PCB and optimize the test matrix, then put forward two kinds of practical boundary scan interlinkage test algorithms.

(1)The test algorithms of the whole " 0 " (or " 1 ") sequence + parallel " 01 " sequence and " 10 " sequence

The basic thought refers that the whole " 0 " (or " 1 ") vector is used firstly to test open circuit fault, we can add the whole " 0 " vector (or the whole " 0 " vector) if it need to carry on extra

languishment fault test to the signal line, this algorithm in the text is called algorithm 1 . According to the geometry information of the circuit and the analysis of mathematics model of two short circuit, we can get the following conclusion: The situation that only needs to test the short circuit of the border upon network can reach the high fault coverage rate (It is supposed that short circuit fault only happen between two or a lot of with border upon networks here). We utilize this conclusion to optimize the test. we find the fault with a specific measuring prompting first, and then orient the fault with a diagnosis prompting according to the result of measuring . Realize the step concretely as follows:

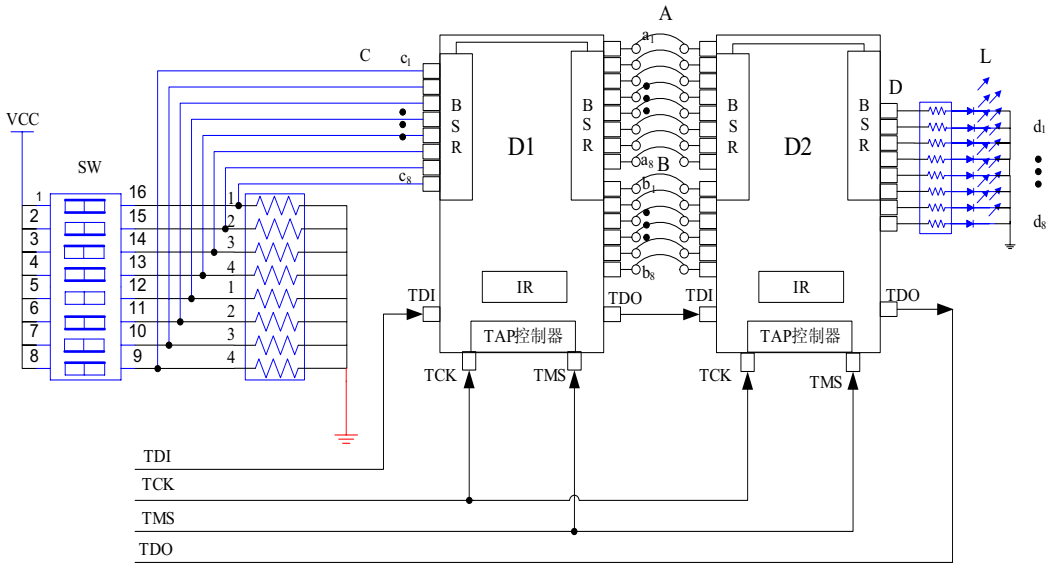

Fig.1 line sketch map of the principle demonstration board

Step one: Bring to bear the whole 0 and the whole 1 vector, then measure and diagnose all to languishment fault including open circuit fault, the short circuit fault with the power and he short circuit fault with the ground wire ;

Step two: Bring to bear the ……010101 test vector, measure the short circuit fault. If has not found the fault, the next step is step four;

Step three: Bring to bear the ……101010 test vector, orient the short circuit fault .

Step four: Over.

The diagnoses principle of the languishment fault that utilizes $v_1^P = \overline{0}$ and $v_2^P = \overline{1}$ to measure is obvious. Bring to bear the vector $v_3^P = [\cdots\cdots 0\ 1\ 0\ 1\ 0\ 1]_n$, supposing that the response vector is v_3^P. If $v_3^P = v_3^P{}'$, the circuit has no fault and the test is over. If $v_3^P \neq v_3^P{}'$, the circuit has fault and Bring to bear the vector $v_4^P = [\ldots\ldots 0\ 1\ 0\ 1\ 0\ 1]_n$, then get the response v_4^P, defining:

$$v_f = v_3^P{}' \oplus v_4^P{}' =$$

$$[\cdots \overline{v_3^P{}'(5) \oplus v_4^P{}'(5)} \ \cdots \ \overline{v_3^P{}'(2) \oplus v_4^P{}'(2)} \ \overline{v_3^P{}'(1) \oplus v_4^P{}'(1)}]$$

$v_f(i)$ is the exclusive or of $v_3^P{}'$ & $v_4^P{}'$ (equal to "exclusive nor "in logics) .Observeing v_f vector, if $\exists\, v^f(i) = 0, v^f(i+1) = 0, v^f(i+2) = 0$ under the condition of $1 < i < n$, then the network is

languishment in 0; Homoplastically, if $\exists v^f(i) \neq 0, v^f(i+1) \neq 0, v^f(i+2) \neq 0$ under the condition of $1 < i < n$, then the network is languishment in 1; If two or more than two f in succession , then the corresponding network is in short circuit or in adjoining languishment many network fault. Form 1 provides the 8 network test instance that have short circuit .

v_3^P、v_4^P can also realize the open circuit and the measuring and localization of the languishment fault, namely the test vector v_3^P、v_4^P are redundant, then the test algorithms can be optimized to remove the whole " 0 " and the whole " 1 " vector. So, algorithm 1 optimizes the diagnosis of open circuit, short circuit and languishment fault at the same time only with 01 and 10 array. The concrete test step:

Step one: Bring to bear……101010 array and 010101 array;

Step two: Measure and diagnose the fault according to the calculation result of testing and responding;

Step three: Over

The term that the algorithm above educes is that two adjoining network may short circuit and not adjoint network have open circuit. No matter what fault of open circuit, short circuit or languishment, SRV of the corresponding network observation unit is the single value vector (namely every element is the same in the vector) . For the instance of the kind of a lot of fault or a lot of adjoining network short circuit or open circuit, though this way can measure and orient the fault, but the fault diagnoses is fuzzy. For this reason, the algorithm above can be improved further. If a lot of adjoint networks have faults, in order to distinguish trouble the faults, we can increase a complementary logic value with the element of each fault network SRV as prompting, We define this vector for the fault partition the vector. Because this kind of test algorithm has exerted the 01 and 10 complementary test array, if the result of the test is a lot of adjoint network fault and can increase a complementary test prompting with SRV, so the algorithm improved from algorithm 1 is called complementary vector test algorithm in here. It has the following main characteristic: 1,The number of the test vector is 2 or 3 and does not increase with the network counts increasing; 2, the test vector and the diagnose algorithm has nothing to do with the concrete craft and is effective to the crafts , such as TTL , CMOS , or ECL ,etc; 3,For the many network fault, it can measure, make a reservation and distinguish.; 4, The complementary vector test is non- complete test algorithm, only on the premise of meeting the structure fault model of question circuit, it is complete.

(2)The application boundary scan interlinkage test algorithms

There are two slices of BS device of D1 and D2 in BST principle demonstration board, we can find out that two groups of networks of A, B exist among D1 and D2 from the principle picture of the circuit. The BS interlinkage test will test the fault situation of two groups network of A, B. Given a test stimulationon D1 output pin v_{AB1}^P =[01010101010101]14 , v_{AB2}^P = [10101010101010]14, The corresponding output can make the unit on 1 and get the response '= [01010101010101]14 , '= [01010101010101]14 from D2. According to algorithm 1 , $v_{AB1}^P = v_{AB2}^P$ ' , $v_{AB2}^P = v_{AB2}^P$ ' ,

=[00000000], then D1 and D2 interlinkage

networks have no fault.

Form 1 8 network test instance that have short circuit

networks	Parallel test vector(v_i^P)	Parallel response vector(v_i^P ')	
		' ' ' '	
n_1	1 0 1 0	1 0 1 0	0
n_2	0 1 1 0	0 1 1 0	0
n_3	1 0 1 0	1 0 1 0	0
n_4	0 1 1 0	0 0 1 0	1
n_5	1 0 1 0	0 0 1 0	1
n_6	0 1 1 0	0 1 1 0	0
n_7	1 0 1 0	1 0 1 0	0
n_8	0 1 1 0	0 1 1 0	0

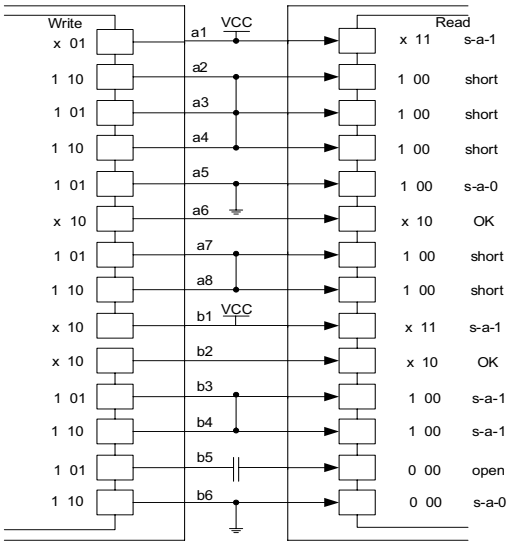

Fig. 2 interconnection fault setting of BSD principle demonstration board

As Fig. 2 shows, fault set up various kinds of fault type of open circuit, short circuit(two crunodes and many crunodes) and languishment. Known by the list of references [5], D1 and D2 are CMOS structure circuit. According to the theory of the circuit, the short circuit fault of D1 and D2 are shown as the line and, the languishment of the open circuit is 0. Exert vector 1 , 2 and get response , according to algorithm 1, network a1 , b1 are dull in 1,namely short circuit with the power, network a2 , a3 , a4 , a5, a7 , a8, b3 , b4 , b5 , b6 are short circuit or dull in 0. So far, all fault have already been measured. In order to distinguish the fault, according to the test method of the complementary vector, we can exert the fault partition vector v_{AB3}^P= [x1111x11xx1111]14(X is unconcern bit, it could be 0 or 1) and get response v_{AB3}^P'= [x1111x11xx1111]14, then a2 , a3 , a4 are short circuit , a5 is dull in 0, a7 , a8 are short circuit, b3 , b4 are short circuit, b5, b6 are dull in 0, test is over.

Use three PTVs to test the setting fault of Fig. 2, according to the preceding trouble model , we can know that the situation of the diagnose result and the real circuit are totally unanimous. The method of the complementary vector test is feasible to test the most circuit boards, but have potential completeness for some multi-layer high-speed circuit board that need to lay the electric wire interlacely. Such as the situation that a1 and a6 short circuit, The method of the complementary vector test can't be examined or diagnosed inaccurately .

4 Conclusion

This text has introduced briefly the fault and

the fault model of the circuit board, has set up the mathematics model of BST, then discussed the diagnosis method of BST, has commented the characteristics and suitable situations of several kinds of classical test algorithms briefly, on this basis, have proposed two kinds of optimization interconnections test algorithm. This text has designed a simple experiment circuit board and explain the BST of this circuit board in the application of algorithm. In the course of boundary scan interconnection test, according to the procedure of test, the text used the test algorithms of the whole " 0 " array (or "1") +并行 " 01 " array and "10 " array to diagnose the circuit board. The result was totally identical with the setting in advance and verified the exactness and validity of this algorithm. The ones that need proving are the method of the complementary vector test is feasible to test the most circuit boards, but have potential completeness for some multi-layer high-speed circuit board that need to lay the electric wire interlacely.

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