# Power On Behavior of Xilinx CPLDs

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## Introduction

### Why Programmable Logic is Different during Power On

Applying power to a standard logic chip, SRAM, or EPROM, usually results in output pins tracking the applied voltage as it rises. Programmable logic attempts to emulate that behavior, but physics forbids perfect emulation, due to the device programmability. It requires care to specify the pin behavior, because programmable parts encounter unknown variables – your design and your power environment.

Microprocessors require additional time during power up, to initialize registers, execute the boot EPROM, and so on. FPGAs exploit this time frame to configure in parallel with microprocessors, masking that operation. Only CPLDs are expected to mimic standard logic chips while still being programmable. This task is very difficult.

CPLDs must reset to a known state and load an internal configuration pattern (EPROM) into volatile logic cells (SRAM), extremely quickly, to appear "instantaneously on." In the case of CoolRunner$^{TM}$ CPLDs, to save power, internal EPROM cells are powered down after configuration. Configuration is also performed in XC9500$^{TM}$, XC9500XL$^{TM}$, and XC9500XV$^{TM}$ CPLD families as the power supply voltage rises, though due to architecture differences the mechanics are significantly different. Loading the EPROM into volatile memory saves power, but comes with the price of extended configuration time. To speed up configuration, a fast state machine starts early – when the $V_{CC}$ is about two-thirds of the way to $V_{CCMIN}$. This presents a gap in output pin tracking, as the pins remain unconfigured until the configuration point. They become configured when their SRAM cells are loaded.

As transistors shrink, voltages must drop, affecting configuration circuitry. These behaviors are noted in the Xilinx CPLD suite of data sheets, which include the 5 volt XC9500 family, the 3.3V XC9500XL and XPLA3 families, the 2.5V XC9500XV family and, of course, the 1.8V CoolRunner-II. Due to variations in $V_{CC}$ ramp rates, supply noise considerations, and reliable performance, the two-thirds $V_{CCMIN}$ rule of thumb is just an approximation.

As the supply voltage rises, internal level sensors trigger circuity to clear out volatile cells and reset internal logic to known states, then configuration proceeds to systematically load EPROM contents into them. CoolRunner-II$^{TM}$ performs checks during configuration to confirm that bits are being correctly held, and will restart configuration if an error is detected. This might occur if a noisy $V_{CC}$ ramp is applied, which might either cause incorrect voltage to start (false compare) or stored bits to get corrupted. The result is that configuration time can increase, as the controller assures a correct pattern gets configured.

The user pattern is a variable in the power up sequence. Depending on the pattern, differing current amounts are needed to charge the bits being configured. It is difficult to know how much current is needed during configuration, without measuring it. Another variable is the regulator's ability to successfully power the chip, during power up. The regulator itself must arrive at a solid regulation condition with an unknown loading. Even the timing for regulation becomes a factor.

Assigning a marginal power regulator to the CPLD configuration task risks creating designs that only behave with a pristine, noise free environment. Xilinx CPLDs are designed to support a wide range of power environments, but many difficulties can be avoided by advance planning to assure most favorable conditions.

This application note details the I/O behavior of Xilinx CPLDs during the power up operation. This knowledge helps users achieve greater success with these powerful parts.

# Sequencing Supplies Can Make a Difference

Today's system applications are comprised of devices that do not utilize identical voltages. Often, these devices must be able to interface to each other, and Xilinx CPLDs frequently find themselves used as the "glue" between these devices. To accommodate this new design trend, Xilinx CPLDs have evolved from having a separate $V_{CCIO}$ (I/O Supply) rail to having multiple I/O banks each having their own $V_{CCIO}$ rails. While these features have been introduced to allow Xilinx CPLDs to interface in more mixed signal environments, designers should be aware that they now have the burden of managing multiple power supplies. Gone are the days of a single supply voltage. Today a designer must recognize that each and every supply voltage will not simultaneously be applied. This section provides a designer with an understanding of how to best power sequence Xilinx CPLDs according to his system needs

## Sequencing Supplies: XC9500/XL/XV and CoolRunner CPLDs

Most Xilinx CPLDs are provided with two separate types of power supply pins. $V_{CCINT}$ supplies power for the internal logic, memory, and charge pumps. $V_{CCIO}$ supplies power for the output drivers and, in some cases, the input receivers. The I/O supply allows the CPLD to be used in various logic level systems (i.e. 5V, 3.3V, 2.5V, 1.8V, etc.) by appropriate attachment. This approach raises the issue of biasing internal structures in nonstandard configurations. Experimentation and analysis of the structures has shown that the devices are safe under all anticipated power sequences. Figure 1 shows the typical structure of a Xilinx CPLD. Impedances Z1 and Z2 provide superior ESD protection to the pins. Their behavior is key to understanding power sequencing operation.
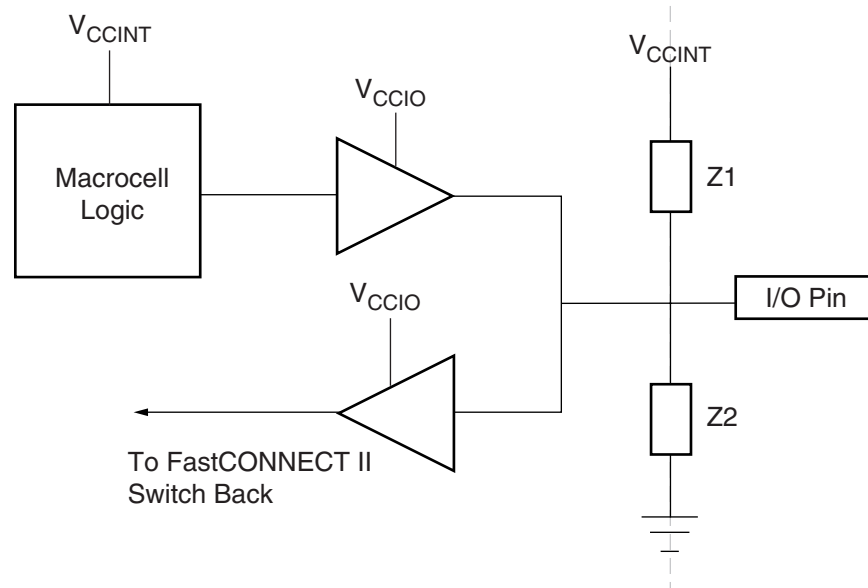


*Figure 1:* **Simplified I/O Cell Structure of Xilinx CPLDs**

Specific concerns arise if one of the power supplies is off while the other is on. There are two ways this could happen. Either $V_{CCINT}$ is on, and $V_{CCIO}$ is off; or, $V_{CCINT}$ is off and $V_{CCIO}$ is on. These cases are described below.
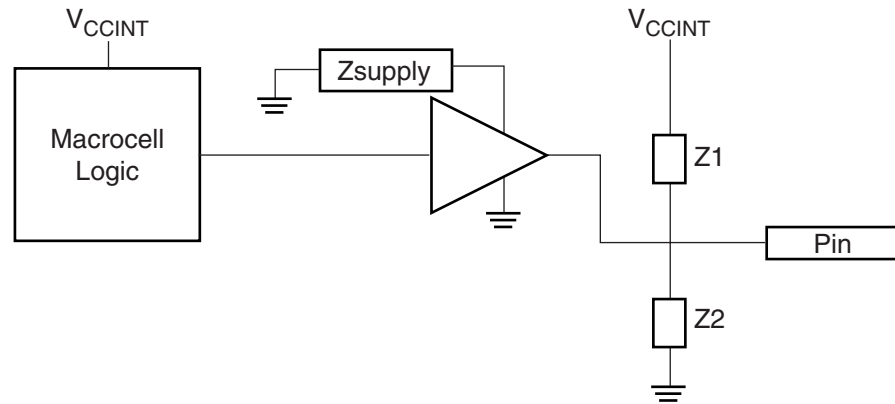
**Case 1: V$_{CCINT}$ ON, V$_{CCIO}$ OFF**

*Figure 2:* **CPLD Output Driver with V$_{CCIO}$ Turned Off (input receiver not shown)**

Figure 2 shows the general case for most Xilinx CPLDs, when V$_{CCINT}$ is on and V$_{CCIO}$ is off. When V$_{CCINT}$ is powered up, and V$_{CCIO}$ is not powered, everything except the output buffers are enabled. Let us take a closer look at the various Xilinx CPLD output buffers (Figure 3 and Figure 4).
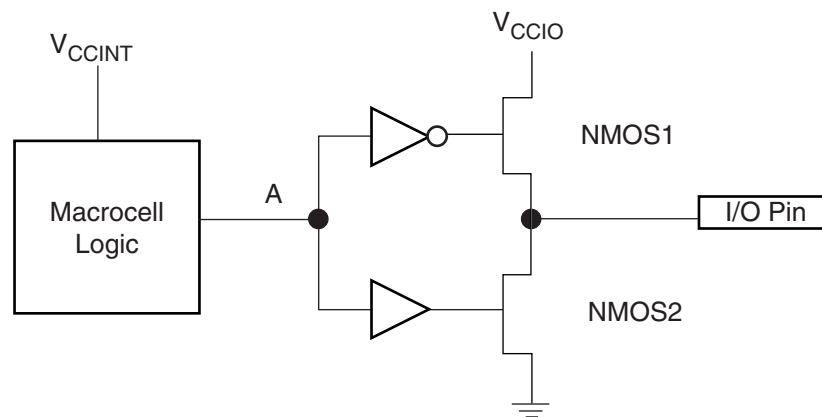
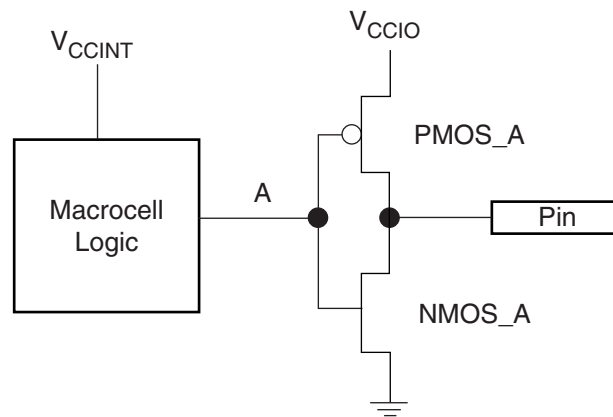*Figure 3:* **Detailed picture of XC9500 Output Buffer (ESD not shown)**

*Figure 4:* **Detailed picture of XC9500XL, XC9500XV, and CoolRunner-II Output Buffer (ESD not shown)**

As shown in Figure 3, the XC9500 CPLD utilizes stacked N-Channel output drivers. XC9500XL, XC9500XV, and CoolRunner-II CPLDs utilize full CMOS output structures as shown in Figure 4. However, for the sake of this discussion, both output structures can be viewed as behaving identically if we make reference to node 'A' in both diagrams. For the sake of simplicity, we shall from now on refer only to the CMOS output structure in the XC9500XL/XV and CoolRunner CPLDs. The reader should be aware that any reference to PMOS_A can be freely replaced with NMOS1 (Figure 3), and that any reference to NMOS_A can be freely replaced with NMOS2.

Since the macrocell logic is alive by virtue of $V_{CCINT}$ being powered, pins which should be configured as outputs will have the appropriate logic signals placed on node 'A', such that either the NMOS1/PMOS_A transistor or the NMOS2/NMOS_A transistor in the output buffer is turned on.

# I/O Pin Consequences

Upon power up, the CPLD must load the user's configuration pattern and make it active. Using the CoolRunner design technique of transferring EPROM content into volatile memory and powering down the EPROM saves a significant amount of power, but it comes at the price of extended configuration time. Most users expect a CPLD to be "instantaneously on", and therefore, all Xilinx CPLDs have been designed to make this memory transfer procedure extremely fast. In order to accomplish this goal, a state machine starts early – when the $V_{CC}$ supply reaches roughly two-thirds of $V_{CCmin}$. Figure 5 shows the sequence of events that occur for all Xilinx CPLDs as $V_{CC}$ rises.
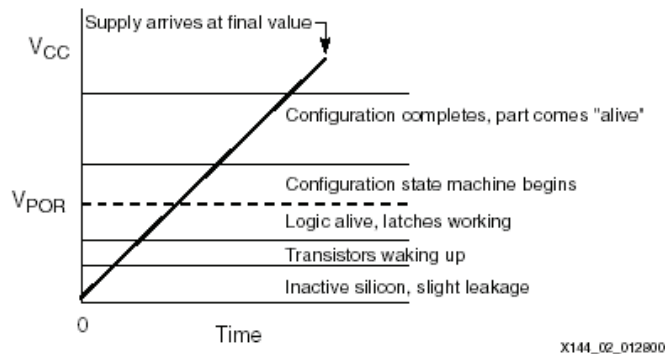


*Figure 5:* **Timing Diagram ($V_{CC}$ vs. Time)**

As $V_{CC}$ rises, transistors begin to wake up. The time frame from 0V to $V_{POR}$ is when transistors begin to come alive. As $V_{CC}$ reaches the $V_{POR}$ (Power On Reset) threshold, internal logic states are reset and the configuration state machine is allowed to begin. When all configuration is complete, the configuration state machine has finished its task and the CPLD assumes the user's configuration.

During the time frame between 0V and $V_{POR}$, it is difficult to determine the exact behavior of all transistors and internal nodes. Along the same lines, it is equally difficult to determine the state of the SRAM cells before $V_{POR}$ is reached. Since the user has no method of determining what is occurring inside the device during this early time frame, the most apparent aspect of configuration is the CPLD's I/O behavior.

All Xilinx CPLDs have been designed, as best as possible, to have the output pins track the applied voltage as it rises. However, CPLDs are programmable, which means that the behavior of the output pins is controlled by the user's configuration. Depending on the state of the SRAM cells and other nodes during power up, an I/O can drive low or high before the configuration

state machine has commenced operation. This can present a gap in an output pin's ability to track the applied voltage. Such a gap is shown in Figure 6.
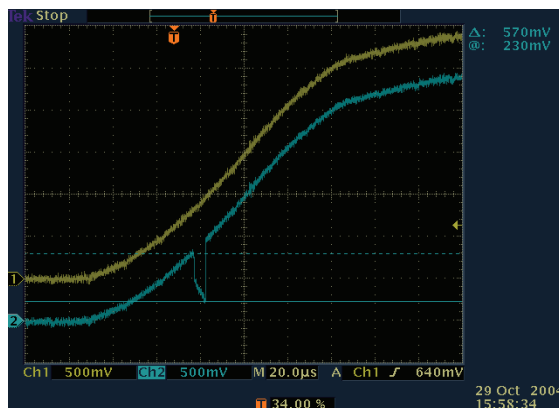


*Figure 6:* **XC9500XL Power-up with I/O Not Tracking V$_{CC}$**

The top trace represents V$_{CCINT}$ and V$_{CCIO}$ (both rails tied together) and the bottom represents a possible I/O behavior. The time frame from 0V to V$_{POR}$ is where the I/O pin might not track V$_{CC}$, and a slight gap may occur. This time frame is of particular concern because the SRAM transistors and output drivers are alive, but the Power On Reset signal has not yet forced the SRAM cells to known states and disabled the output drivers.

The I/O tracking gap described above occurs if configuration SRAM bits pass their values (zeros or ones) to device I/O cells before an internal Power-On Reset (POR) is able to clear them. It can also occur if internal nodes (such as Node A from the earlier supply sequencing discussion) cause the output drivers to become active before they have been formally disabled.

This tracking gap is not likely to cause problems in most systems as it occurs when V$_{CCINT}$ is between 0V and V$_{POR}$. Refer to Table 1 for typical values. During this time frame, other devices should not yet be alive. If the possibility exists for any downstream device to be alive, this tracking gap can be erroneously detected as a false edge to trigger an erroneous reset, start condition, or false clock edge. Care should be taken to avoid these issues if a downstream device may be alive.

*Table 1:* **Typical values for V$_{POR}$, V$_{DONE}$, and V$_{CC}$**

|  | V$_{POR}$ | V$_{DONE}$ | V$_{CC}$ |
|---|---|---|---|
| XC9500 | 1.2V | 3.5V | 5.0V |
| XC9500XL | 0.8V | 2.1V | 3.3V |
| XC9500XV | 0.75V | 1.4V | 2.5V |
| CoolRunner XPLA3 | 0.8V | 2.1V | 3.3V |
| CoolRunner-II | 1.0V | 1.4V | 1.8V |

As stated, the I/O tracking gap is unlikely to cause concern in most systems. However, if it is absolutely critical that the tracking gap be eliminated, a solution is to ramp V$_{CCIO}$ after V$_{CCINT}$ has reached V$_{DONE}$. Doing so will ensure that the output buffers remain unpowered during the configuration process.

## Conclusion

Xilinx CPLDs are designed to operate in multiple voltage systems, and can tolerate any power supply sequencing applied to them without damaging the CPLD, the supply, or the external circuits. Mixed voltage design has never been easier.

## Additional Information

[CoolRunner-II Data Sheets, Application Notes, and White Papers](#)

[Access to all Xilinx Data Sheets, Application Notes, and White Papers](#)

[Device Packages](#)

## Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 05/25/06 | 1.0 | Initial Xilinx release. |