Platform Independent Test Access Port Architecture

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Abstract

In this work, we present and analyze a generic Test Access Port (TAP) architecture capable of being re-used without any modifications in various system-on-chip (SoC) ICs as well as a "Modular Jtag" multi-TAP architecture that allows embedded IPs to control their boundary-scan segments and be IEEE 1149.1 compliant.

1. Introduction

Efficient test methodologies play one of the major roles in modern SoC designs. The majority of test and debug functions of a modern IC can be accessed through the TAP. Therefore, a reusable and modular TAP architecture is especially desirable for SoC ICs that include several cores, each potentially including its own TAP.

2. Debug port architecture

A number of different methods to interconnect multiple TAPs in an IC were proposed in the literature. Among those are Daisy-Chain architecture, TAP Selection-Pads architecture and Configurable Daisy-Chain architecture to name a few [1]. The main idea behind the latter is connecting multiple TAPs in a daisy-chain while allowing any TAP to be excluded from it or externally bypassed.

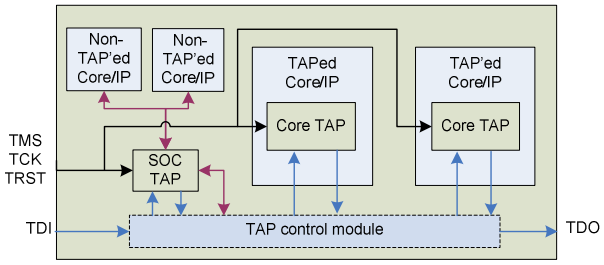

Figure 1 Multi-TAP configurable daisy chain connection.

Fig. 1 shows a Configurable Daisy-Chain TAP connectivity scheme with on-chip CPUs that include a debug controller as an integral part of their design. Many architectures can be attributed to this family, among those TAP Linking Module (TLM), Hierarchical TAP (HTAP) [2], Bypass Control Logic (BCL) as well as many others [3]. The difference between the various approaches is in the way the selection and muxing of the daisy-chain configuration is performed and controlled. In some cases the excluded TAPs are just removed from the chain. The proposed alternative is replacing the excluded TAPs with bypass logic inside the TCM, emulating their presence. This approach allows keeping the length of the instruction register (IR) as well as the bypassed data register (DR) paths constant, even when some of the TAPs are excluded bringing to simplification of the test and debug vectors. The daisy-chain configuration is controlled by a Shared DR (SDR) that can be mapped to the address space of any of the TAPs in the IC without actually modifying their design. TCM is tracking the instructions loaded into the IR address space of every TAP in the IC and will re-configure the TAPs chain based on the contents of the SDR. The alternative "Modular-Jtag" architecture (Fig. 2) allows cores/IPs to have Boundary-Scan (BS) logic controlled entirely by their own TAPs and still be IEEE compliant. This is achieved by special "snooping" logic. After reset only main-TAP is connected between TDI and TDO. All the other TAPs are connected to TDI in parallel to the main-TAP and are "snooping". In this mode only BS instructions will be executed by the IP TAPs, all other instructions are ignored. When a BS instruction is detected, the main-TAP reconnects other TAPs into the daisy-chain only for the duration of this instruction.

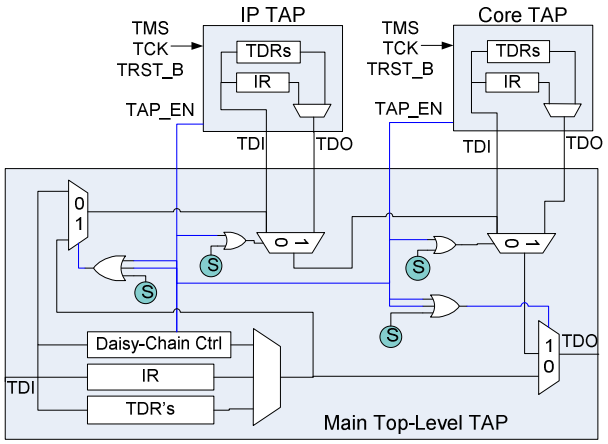

Figure 2 "Modular-Jtag" multi-TAP architecture.

3. References

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