

# A Test Architecture for System-on-a-Chip

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## Abstract

*This paper proposes a configurable TAM-Bus, a P1500 compliant Test Access Mechanism (TAM), and the TAM-Bus controller (TAM-controller) that is interfaced with JTAG at chip level of chip. All IP (Intellectual Property) cores' test can be controlled through the TAP under the control of the TAM-controller. The test architecture we presented has been implemented in an industry SoC. The test coverage remains 99.40%. The overhead increases only 0.17% due to TAM. The experiment results demonstrate that the test architecture can offer the solution for testing SoC.*

## 1. Introduction

SoCs introduce new challenges to the test [1, 2]. Three types of features are needed to test a SoC: test sources and sinks, a Test Access Mechanism and IP core test wrappers. SoC test standards are currently under development, such as core wrappers and core test language [2,3]. The TAM is not standardized unlike the core test wrapper and core test language. Development of TAM is then left to the SoC integrator.

A P1500 compliant configurable TAM named TAM-Bus and its controller, which also provides the P1500 wrapper test control signals, will be proposed in this paper. The SoC test scheme will also be presented based on the P1500 wrapper and the TAM-Bus architecture.

## 2. SoC Test Architecture

The SoC test architecture we proposed consists of following components as shown in Figure 1 (Omitted): (I) The TAM control module that consists of a TAM controller and a Configuration Register (CR) provides control capability of the overall test operation of the chip. (II) Chip-level JTAG module performs IEEE 1149.1 boundary scan operation to support circuit-board test strategies based on the IEEE 1149.1 standards [4]. It also provides SoC TAM control signals interface. (III) TAM-Bus provides access to embedded IP cores. The TAM-Bus architecture is composed of two elements: TAM-Bus Interface (TBI) and test bus pairs (WPI\_bus and

WPO\_bus). According the CR content, TAM-Bus can be configured to three modes: Local bus mode, Concatenation bus mode and Bypass mode. (IV) IEEE P1500 compliant Wrappers around IP cores provide test access mechanism between core and environments outside.

At power-up, only chip-level JTAG Test Access Port (TAP) controller will be visible and active that can perform original IEEE 1149.1 boundary scan test operations. At the same time, TAM is inactive. A user can enable the low level TAM controller that will in turn disable the chip-level TAP controller. The TAM controller can be enabled in either of two ways: Shift the Enable\_TAM instruction into the chip-level JTAG TAP controller's instruction registers or assert ET for two JTAG test clock cycles. Under control of the TAM controller, load data into the Configuration Register (CR) to establish the TAM-Bus configuration: Bypass bus mode, Local bus mode or Concatenation bus mode. Then, load instructions into WIR of each wrapper to establish the operation mode of wrapper. After that, test transport and apply test pattern, complete corresponding test.

## 3. Experimental Results and Conclusion

The proposed test scheme has provided the complete test for LILAC, an industry SoC chip. The SoC chip can keep high test coverage (99.40%). Moreover, the hardware overhead of the test architecture is quite low. The overhead increases only 0.17% due to TAM.

## References

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