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Use of JTAG Boundary-Scan for Testing Electronic Circuit Boards and Systems

Be Van Ngo
Lockheed Martin
Address Here
bevan.ngo@lmco.com

Peter Law
Lockheed Martin
Address Here
peter.h.law@lmco.com

Anthony Sparks
JTAG Technologies
620 State St. Suite 318
San Diego, CA. 92101
anthony@jtag.com

Abstract – Today's complex printed circuit boards and high-density ball-grid array and other chip-size package ICs have led to the standardization and wide-spread use of JTAG (Joint Test Action Group) boundary-scan technology for test and debug. Topics include the evolution of JTAG standards, basic fundamentals of boundary-scan architecture, board testability using boundary-scan and system-level testing. Additionally, this paper will address the advantages and disadvantages of JTAG testing and propose advanced JTAG test methodologies including remote testing and diagnostics.

INTRODUCTION

The complexity and density of circuit cards commonly encountered today presents significant challenges in the test and inspection arena. Circuit cards with thousands of devices, in excess of 10,000 electrical nodes and 20 or more PCB layers are not unusual in modern design practices. Unfortunately, with the increase in complexity comes an increase in defect opportunities.

Conversely, with the increase in densities the ability to provide the adequate number of test points to enable traditional test strategies, such as In-Circuit Test (ICT), to verify the structural integrity of complex circuit cards has diminished. This is further exacerbated by the widespread use of Ball-Grid-Array (BGA) packaging with concealed contacts, complicating the access problem.

This lack of physical access has lead to extensive adoption of the IEEE 1149.1 boundary-scan standard. Also known as JTAG for the Joint Test Action Group that initiated work on the subsequent standard, this test methodology provides extremely high test coverage of complex digital circuit cards via a simple 4-wire (5-wire if the optional asynchronous reset TRST signal is included) interface called the Test Access Port (TAP), alleviating the physical access problem.

This test strategy has been primarily used for manufacturing test and in-system programming and configuration at the board level. However, with the extensive selection of scan path management devices from various silicon vendors, the capabilities of boundary-scan can be extended to the system environment.

Furthermore, the system-level boundary-scan architecture also enables embedded boundary-scan test in the field as well as remote test, diagnosis and configuration.

THE PROBLEM

Traditionally, the method of testing electronic assemblies for structural faults has been In-Circuit Test. This practice applies electrical stimuli to the Device-Under-Test (DUT) and measures the response using physical probes that make contact with the DUT via test-pads on each electrical node. The physical nails are arranged within a test fixture, commonly referred to as a "bed-of-nails", which is unique for each DUT.

Despite the vast capabilities of ICT, board designers are finding it increasingly difficult to provide sufficient nodal access for this test technique, leading board manufacturers to rely on other test methods to ensure structural integrity before advancing to the next process step – usually functional test.

Several factors contribute to the decrease in placement of test pads including:

1. Blind or hidden traces not accessible on either side of the board.
2. Direct access to package pins is not possible in the case of new SMT package types such as Array-Style and Chip-Scale Packaging.

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3. Densely packed circuit cards do not have the physical space for adequate test pads to be placed during layout.
4. High performance systems prohibit the use of test pads to avoid introducing EMI noise.

As test coverage deteriorates, the number of faulty boards passed to the next process step, usually functional or system test increases. Diagnosis of structural faults at this stage is often difficult and time consuming due to ambiguous diagnostic messages. This can result in a "bone pile" of boards that contain structural faults that are extremely difficult to diagnose, or may require engineering to be involved to identify the root cause of the failure, ultimately leading to greater cost and possibly delayed deliveries.

Motivated by the increased cost associated with undetected faults at the structural test phase, and the diminishing physical access limiting the effectiveness of ICT, board manufacturers are relying on alternative, complimentary test strategies in addition to – or in place of – ICT, such as Automated X-ray Inspection (AXI), Automated Optical Inspection (AOI), Flying Probe Testers (FPT) and most common for digital design, boundary-scan.

BOUNDARY-SCAN PRINCIPLES

A boundary-scan, or IEEE 1149.1 compliant device, consists of several key elements including a TAP, an instruction register, and a minimum of two data registers among other mandatory and optional structures.

The boundary register, a series of boundary-scan cells running the periphery of the device, is accessed from each end by the Test Data Input (TDI) and Test Data Output (TDO) pins of the TAP. It is this register that provides serial access to each device pin for the purpose of driving stimuli, capturing responses or both in the case of bi-directional pins. These boundary registers are concatenated when multiple boundary-scan devices are placed in a "scan chain" by connecting the TDO pin of one device to the TDI pin of the next.

The Test Mode Select (TMS) and Test Clock (TCK) pins of the TAP are used to control the finite state machine, which is part of the TAP Controller responsible for control of the boundary-scan test logic *Figure 1*.

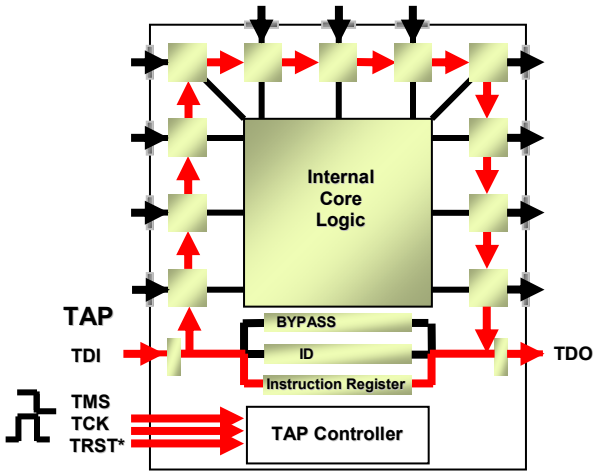

Fig. 1

The instruction register is used to load defined opcodes that place the boundary-scan logic in specific modes and insert the desired data register between the TDI and TDO pins. For example, loading the mandatory instruction EXTEST places the boundary-register in the serial path and gains control of the pins of the device for use as "silicon nails". Utilizing this instruction, a large number of board tests and In-System Programming (ISP) operations can be executed.

BOARD-LEVEL BOUNDARY-SCAN

Circuit cards with even a single boundary-scan device can realize the benefits of numerous test and ISP applications, all via the simple 4 or 5 wire TAP. These applications include:

Infrastructure – verifies the serial data path from the first TDI signal through the last TDO signal is intact and the parallel control signals; TMS, TCK and TRST function correctly. Also, if the optional IDCODE instruction and associated identification register is implemented, the IC manufacturers code, the part number and its revision will be checked. It is required that this infrastructure be operational before any other test will yield useful results.

Interconnect – utilizing the EXTEST instruction, the interconnect test will check the integrity of the connections between boundary-scan devices. This test is extremely thorough as it includes the scan cell, driver and/or sensor, bondwire, leg or ball and the solder joint of each interconnected device as well as the PCB trace. In highly complex digital designs, this test

can provide an extremely high percentage of structural fault coverage alone.

Memory test – accesses non-boundary-scan memory devices such as SRAM, DRAM, DDR, etc. with adjacent boundary-scan devices, which emulate read and write bus cycles to ensure there are no stuck-at or bridging faults on the address, data or control signals.

Cluster test – can be performed on any non-boundary-scan logic provided that access to the Primary Inputs and Primary Outputs is possible via a boundary-scan resource and there are not stringent clocking requirements.

Flash ISP – is accomplished in a similar fashion as memory test. However, in the case of Flash programming, every cell of the flash device can be targeted and thus can be a lengthy operation. To speed flash programming, it is recommended to utilize the Flash AutoWrite signal driven by the boundary-scan controller[3].

In-System Configuration – of cPLD's and FPGA's is performed via the boundary-scan chain. The device loads are provided in the form of SVF, JEDEC, JAM or STAPL files. Or, if the device is IEEE 1532 compliant, the standard for boundary-scan-based in system configuration of programmable devices, an ISC file in conjunction with a IEEE 1532 BSDL file will provide the data and programming algorithms for the device. Furthermore, 1532 allows for multiple devices, from multiple vendors, to be configured concurrently.

EXTENSIONS TO IEEE 1149.1

In addition to the aforementioned IEEE 1149.1 based tests and programming applications, the definition of the IEEE 1149.4 and 1149.6 standards has added additional test capabilities and overcome some of the limitations of traditional boundary-scan.

IEEE 1149.4, also known as Analog Boundary-Scan, was approved by the IEEE in July of 1999. This standard defined an Analog TAP (ATAP) consisting of two pins for sourcing an analog stimulus and making an analog measurement, Analog Boundary Modules (ABM) for each analog pin, A Test Bus Interface Circuit (TBIC) for control of the ATAP and internal analog test bus and a PROBE instruction for monitoring the device pins while in normal operation. The primary goal of this standard was to provide the capability to measure passive components without the need of physical access to the targeted devices.

This standard has been extremely slow to gain acceptance in the industry. The reason for this could be due to many factors, including; lack of commercially available supporting silicon, the need for additional instrumentation for the analog stimulus and measurement, or lack of fault models for diagnosis of complex networks just to name a few.

There are several reasons mixed-signal device vendors may be reluctant to include 1149.4 in their devices. The inclusion of the ABMs in the device can have a significant impact on device performance. Furthermore, mixed-signal devices are commonly low-pin-count devices that do not include 1149.1. For a device to comply with 1149.4, it must also comply with 1149.1. Therefore, it would be necessary to dedicate a minimum of 6 pins for the TAP and the ATAP, which is an expensive proposition in the push for miniaturization.

The IEEE 1149.6 standard for testing advanced digital networks on the other hand has quickly gained momentum and already has a substantial number of adopters and supporting devices since its acceptance by the IEEE in March of 2003. The primary goal of this standard is to provide comprehensive fault detection to advanced digital networks, such as differential signaling, and the ability to test AC-Coupled signals.

To accomplish this, several additions to 1149.1 were defined by this standard. An AC Test Signal Generator was added for purpose of creating a test signal that can propagate through AC-Coupling. This test signal is in turn captured by a Test Receiver with edge-detect capability and memory, the output of which is captured by a basic boundary-scan cell. Also, two additional instructions were defined; EXTEST_PULSE and EXTEST_TRAIN. Further detail about the additional structures and instructions are beyond the scope of this paper.

The addition of 1149.6 in silicon does not require any additional package pins, nor does it require any additional instrumentation beyond a boundary-scan controller. Furthermore, access to the test structures is via an 1149.1 compliant TAP and utilization is very similar to that of traditional boundary-scan, enabling boundary-scan tool vendors to quickly provide support.

SYSTEM TESTING

With the support of system-level scan path management devices from a variety of silicon vendors, the boundary-scan test capability implemented for

board-level manufacturing test can be extended to the system level.

Designing in this boundary-scan "backbone" in the system provides many capabilities in addition to those realized at board-level test as detailed below.

- Reuse of board-level test vectors leading to reduced test development times.
- Verification of board-to-board interconnections supporting diagnosis of backplane interconnection failures at the connector pin level.
- Eliminate redundant functional tests with ambiguous diagnostics.
- Facilitate system checkout prior to shipment.
- Provides access for firmware verification and upgrade without disassembly.
- Supports pin-level diagnostics during environmental stress testing.
- Provides infrastructure to exercise embedded test structures embedded in ASICs and FPGAs.
- Data collection, or data mining, throughout the system via single point of access.

In order to realize these benefits, it is imperative to plan the system-level test strategy in the system's conceptual phase. This will require early collaboration by designers and system architects to define the system-level boundary-scan architecture.

SYSTEM-LEVEL BOUNDARY-SCAN ARCHITECTURE

The primary concern in planning a system-level boundary-scan strategy is routing of the TAP to gain access to each board and the boundary-scan chains therein. There are several topologies used in the industry; RING, STAR and MULTI-DROP to name the most common, but with MULTI-DROP being the most popular *Figure 2*.

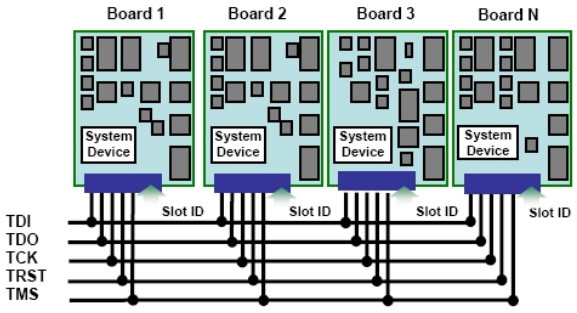

Fig. 2

This scheme utilizes a single JTAG bus comprised of the five TAP signals TDI, TDO, TCK, TMS and TRST. This JTAG bus is then routed in parallel to each backplane slot within the system. Since the TAP of each slot is connected in parallel, a unique address must be assigned to each slot, which can be hard-wired within the backplane.

This architecture requires an addressable system-level scan path management device, also know by other names specific to the device manufacturer such as; gateway, scan bridge, addressable scan port, among others. Although these devices and their protocols are not defined by a standard, they are readily supported by boundary-scan tool vendors.

Each of the boards within the system can be accessed individually by broadcasting its unique backplane address via the JTAG bus. Upon receipt of a valid address, the corresponding device will grant access to Local Scan Ports (LSP) of the targeted board. In order to support board-to-board testing, the system-level devices also support what is commonly referred to as a multi-cast address. When this address is issued, all system-level devices will be active allowing all boards to Update and Capture in concert.

For system checkout, environmental stress testing and update/repair by a field technician, this architecture provides a single point of access to the entire system where an external boundary-scan controller can be connected. However, it may also be desirable to embed certain test capabilities into the system.

EMBEDDED VECTOR DELIVERY

Implementing system-level boundary-scan architectures opens the door to many valuable possibilities for supporting systems in the field. For example, embedded boundary-scan tests can be initiated as part of a Power-On Self Test (POST) or initiated remotely for diagnostic purposes when a system failure occurs. If the root cause of a failure can be determined remotely, a field technician can visit the remote site with the appropriate replacements in hand.

The key element in an embedded vector delivery strategy is the inclusion of an embedded boundary-scan controller, or JTAG test bus master. This embedded controller can be implemented in many ways.

A processor located on any of the cards can assume the role of JTAG test bus master. In this case, the test

vectors will reside in local flash memory which is then accessed by the processor and applied to the JTAG bus, typically via the general purpose I/O. It must be considered that this strategy requires that the processor not be boundary-scan test mode, and thus can not be included in the test. Furthermore, the processor must be able to boot in order to take the role of JTAG test bus master. A fault in the processor subsystem will preclude any embedded boundary-scan tests.

As with system-level scan path management devices, there are also a variety of embedded boundary-scan controllers from several silicon vendors, each with their own suite of capabilities. Some rely on a host processor while others are completely autonomous. The selection of an embedded controller must be made by weighing the trade-offs of each solution.

REMOTE TEST AND DIAGNOSIS

An alternative to embedding the boundary-scan test vectors in the target system and implementing an embedded boundary-scan controller is to execute tests and perform diagnosis remotely. Traditionally, this has not been a possibility due to the short cable lengths required for accessing the JTAG bus. However, new technology has made it possible to access the internal boundary-scan architecture of a system via any inherent communication channel.

This technology, called TapCommunicator[10], provided by JTAG Technologies, is comprised of a transceiver pair; an Uplink and a Downlink *Figure 3*.

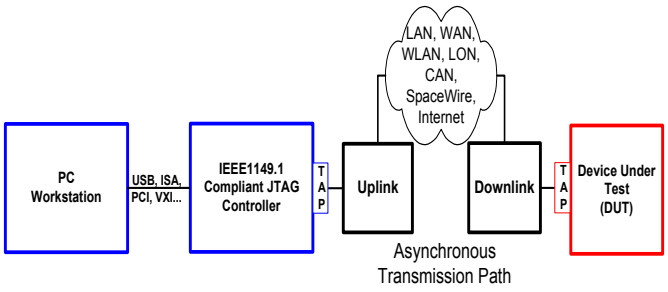

Fig. 3

The Uplink will be located in a centralized location in close proximity to the boundary-scan controller and the workstation that contains the boundary-scan applications and test execution software. The boundary-scan controller is connected directly to the Uplink module. The function of the Uplink is to take the serial bit-stream from the boundary-scan controller, packetize the data and then broadcast the data to the target via any wired or wireless communication protocol. The Uplink is also responsible for receiving result packets from the target, serializing the data back into a JTAG bit-stream, synchronizing the bit-stream with the boundary-scan controller and returning the TDO data back to the boundary-scan controller for analysis.

The Downlink will be located near, or embedded within, the target system. Consisting of very minimal logic, the Downlink can be embedded in an ASIC, FPGA or even a small PLD. Its primary purpose is to receive test data packets from the Uplink, serialize them into a JTAG bit-stream and apply the vectors to the target. Upon receipt of valid TDO data, this information is packetized and sent back to the Uplink.

Ultimately, TapCommunicator provides a transparent solution for remote wired or wireless communication to board and system level boundary-scan architectures utilizing the inherent serial communication protocol of the target design.

CONCLUSION

Increasing densities and array-style component packaging have led to diminished physical access for traditional ICT strategies. It has become evident that a combination of complementary test methods is required to achieve sufficient fault detection at structural test before advancing to the next stage in test, typically functional test, where diagnosis can be much more costly.

Boundary-scan has proven itself as an invaluable tool in testing today's complex digital circuit card assemblies. Moreover, the board-level boundary-scan infrastructures can also be used in a system-level test strategy.

System-level boundary-scan enables a fast and inexpensive method to perform test during environment stress screening with pin-level diagnosis upon failure, firmware updates without disassembly required, system checkout before shipment, field test and updates, among many other possibilities.

The same boundary-scan infrastructure can also be accessed by an embedded boundary-scan controller in order to perform embedded boundary-scan test as part of POST, remotely initiated Built-In Test (BIT) or even accessed via the target's inherent serial communication channel for remote test and diagnostics.

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