# rtfBitmapController

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## Clocks:

The controller uses three independent clocks. These are the video pixel clock, the WISHBONE bus master clock, and the WISHBONE bus slave clock. It is assumed that the slave port will be connected to some sort of processor, and the master port will be connected as a DMA port.

## Display Format:

This controller relies on an external sync generator. The display generated is relative to the positive edge of the horizontal and vertical synchronization signals.

## Registers:

The controller responds to the word address range: $FFDC5xxx.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Regno | Width | R/W | Moniker | Description |  |  |
| 0 | 32 | R/W | REG\_CTRL | Master Control Register |  |  |
| 1 | 32 | R/W | REG\_CTRL2 | Secondary control register / Status register |  |  |
| 2 | 12 | R/W | REG\_HDISPLAYED | Horizontal displayed |  |  |
| 3 | 12 | R/W | REG\_VDISPLAYED | Vertical displayed |  |  |
| 5 | 32 | R/W | REG\_PAGE1ADDR | Page one memory address |  |  |
| 6 | 32 | R/W | REG\_PAGE2ADDR | Page two memory address |  |  |
| 7 | 32 | R/W | REG\_REFDELAY | sync reference delay register |  |  |
| $800 to $9FF | 32 | R/W | REG\_PALETTE | Color palette used when the color depth is 00 (eight bits per pixel). |  |  |

### Master Control Register (REG #0)

This register contains bits that control the bitmap controller.

|  |  |  |  |
| --- | --- | --- | --- |
| BitNo |  | Description |  |
| 0 | On/off | Turns the display controller on=1 or off=0, default is 1 |  |
| 10,9 | Color Depth | This register identifies the number of bits used per pixel |  |
|  |  | |  |  |  | | --- | --- | --- | | 10,9 | Color Depth |  | | 00 | 8 bits per pixel (default) |  | | 01 | 16 bits per pixel |  | | 10 | Not supported |  | | 11 | 32 bits per pixel |  | |  |
| 17,16 | hres | Horizontal resolution control   |  |  |  | | --- | --- | --- | | 17,16 |  |  | | 11 | Not Supported |  | | 10 | 4 video clocks per pixel |  | | 01 | 2 video clocks per pixel |  | | 00 | 1 video clock per pixel |  | |  |
| 19,18 | vres | Vertical resolution control   |  |  |  | | --- | --- | --- | | 19,18 |  |  | | 00 | 1 scanlines per pixel |  | | 01 | 2 scanlines per pixel |  | | 10 | 4 scanline per pixel |  | | 11 | Not Supported |  | |  |
|  |  |  |  |

### Control Register 2 / Status Register (REG #1)

|  |  |  |
| --- | --- | --- |
| Bitno |  |  |
| 16 | Page | This bit controls which memory page address is used. Default is 0. |

### HDisplayed (REG #2)

|  |  |  |
| --- | --- | --- |
| Bits |  |  |
| 11 to 0 | HDISP | The number of pixel displayed horizontally on screen |

The number of pixels displayed depends on both the horizontal resolution setting and the video mode used. For example, if a 1366x768 display mode is used and the horizontal resolution is set to divide by four, then this register should be set to 340. (1366 / 4 rounded).

### VDisplayed (REG #3)

|  |  |  |
| --- | --- | --- |
| Bits |  |  |
| 11 to 0 | VDISP | The number of pixel displayed vertically on screen |

The number of pixels displayed depends on both the vertical resolution setting and the video mode used. For example, if a 1366x768 display mode is used and the vertical resolution is set to divide by four, then this register should be set to 192. (768 / 4 rounded).

### Page One Address (REG #5)

|  |  |  |
| --- | --- | --- |
| Bits |  |  |
| 31 to 0 | PAGE1ADDR | The word memory location of the first bitmap page |

### Page Two Address (REG #6)

|  |  |  |
| --- | --- | --- |
| Bits |  |  |
| 31 to 0 | PAGE2ADDR | The word memory location of the second bitmap page |

### Reference Delay Register (REG #7)

|  |  |  |
| --- | --- | --- |
| Bits | Name | Description |
| 11 to 0 | HRefDelay | Horizontal reference delay (default 218) |
| 27 to 16 | VRefDelay | Vertical reference delay (default 27) |

The reference delay register may be used to control the position of the bitmap on the screen. The horizontal reference delay is relative to the rising edge of the horizontal sync pulse. The vertical reference delay is relative to the rising edge of the vertical sync pulse.

### Palette Registers (REG $800 to $9FF)

The palette registers map an eight bit color code from memory into a 24 bit RGB (8,8,8) value.

Only the first 256 palette registers are currently used. The last 256 registers may be used as scratchpad storage. For example a second set of palette values.

## Port Signals

|  |  |  |  |
| --- | --- | --- | --- |
| Name | Width | I/O |  |
| rst\_i | 1 | i | This active high signal resets the core and WISHBONE bus interfaces |
| s\_clk\_i | 1 | i | Clock signal for slave peripheral interface |
| s\_cyc\_i | 1 | i | cycle is valid |
| s\_stb\_i | 1 | i | data transfer in progress |
| s\_ack\_o | 1 | o | data transfer acknowledge |
| s\_we\_i | 1 | i | write enable to register set |
| s\_adr\_i | 34 | i | addresses the registers of the core |
| s\_dat\_i | 32 | i | data input for registers |
| s\_dat\_o | 32 | o | data output of registers |
| clk\_i | 1 | i | clock signal for bus master interface |
| bte\_o | 2 | o | Burst type (always 00 for linear burst) |
| cti\_o | 3 | o | Cycle type indicator |
| bl\_o | 6 | o | Burst length (burst length is 8 words) |
| cyc\_o | 1 | o | cycle is valid |
| stb\_o | 1 | o | data transfer is taking place |
| ack\_i | 1 | i | data transfer acknowledge |
| we\_o | 1 | o | This signal is always inactive (low) |
| adr\_o | 34 | o | Memory address for bitmap data read |
| dat\_i | 32 | i | data input from bitmap memory |
| dat\_o | 32 | o | this signal is always zero (not used) |
| vclk | 1 | i | This is the video clock input |
| hSync | 1 | i | This is an externally supplied horizontal sync signal |
| vSync | 1 | i | This is an externally supplied vertical sync signal |
| blank | 1 | i | video blanking indicator |
| rgbo | 24 | o | color output video data in RGB (8,8,8) format |
| xonoff | 1 | i | externally supplied on/off signal for core |
|  |  |  |  |

All bus transfers are 32 bits. The low order two address bits should be fixed at zero.

## WISHBONE Compatibility Datasheet

The rtfBitmapController core may be directly interfaced to a WISHBONE compatible bus.

|  |  |  |
| --- | --- | --- |
| WISHBONE Datasheet  WISHBONE SoC Architecture Specification, Revision B.3 | | |
|  |  | |
| Description: | Specifications: | |
| General Description: | Bitmap controller | |
| Supported Cycles: | SLAVE, READ / WRITE  SLAVE, BLOCK READ / WRITE  SLAVE, RMW | |
| Data port, size:  Data port, granularity:  Data port, maximum operand size:  Data transfer ordering:  Data transfer sequencing | 32 bit  32 bit  32 bit  Little Endian  any (undefined) | |
| Clock frequency constraints: |  | |
| Supported signal list and cross reference to equivalent WISHBONE signals | Signal Name:  rst\_i  S\_ack\_o  S\_adr\_i(33:0)  S\_clk\_i  S\_dat\_i(31:0)  S\_dat\_o(31:0)  S\_cyc\_i  S\_stb\_i  S\_we\_i  ack\_i  adr\_o(33:0)  clk\_i  dat\_i(31:0)  dat\_o(31:0)  cyc\_o  stb\_o  we\_o  bte\_o  cti\_o | WISHBONE Equiv.  RST\_I  ACK\_O  ADR\_I()  CLK\_I  DAT\_I()  DAT\_O()  CYC\_I  STB\_I  WE\_I   ACK\_I  ADR\_O  CLK\_I  DAT\_I  DAT\_O  CYC\_O  STB\_O  WE\_O  BTE\_O  CTI\_O |
| Special Requirements: |  | |