rtfBitmapController1364x768

Summary:

This controller can display an image from memory in 1364x768x8bpp resolution. High-speed memory such as DDR2 dram is required.

Clocks:

The controller was designed to work in a system with a system clock of 33MHz, a graphics pixel clock of 85.7MHz, and a DDR2 dram clock of 571MHz. The controller is flexible and it is possible to use a higher system clock frequency.

Interface:

The controller uses a WISHBONE burst interface. One additional signal (bl\_o) is defined to set the burst length.

Line Buffer:

The memory for the line buffer is generated using a core generator. It is a dual ported memory with a 32 bit write side, and 8 bit read side.

Operation:

The controller operates in a periodic fashion. During the active display area, burst fetches occur at periodic intervals during the horizontal scan. 1364 bytes of memory are fetched for each scan line using 22 burst access cycles. 21 of the cycles fetch 64 bytes, the last cycle fetches 20 bytes for a total of 1364 bytes.