SPI Master / Slave Core Specification

SPI_MASTER_SLAVE

SPI Master and Slave Interfaces

VHDL

RTL Architecture

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Revision History

Rev.	Date	Author	Description
0.1	11/05/18	JD	First Draft Described the SPI_MASTER and SPI_SLAVE cores.

Contents

1

Introduction

The SPI_MASTER_SLAVE core implements two related but independent design blocks: the SPI_MASTER and the SPI_SLAVE blocks.

Each core is a small RTL description for the widely used Serial Peripheral Interface, written in VHDL.

The SPI bus signals follow the de-facto standard for the SPI interface, and are named after the Motorola original naming convention, with the 4 SPI signals (SSEL, SCK, MOSI, MISO). The SPI mode and serial word size can be controlled at instantiation by VHDL generics.

There are two interfaces to each core, the SPI bus interface, with the SPI signals, and the parallel read/write interface. The cores work on 2 asynchronous clock domains, the SPI bus clock, SCK, and the user internal logic clock, to which the parallel interfaces are synchronous.

All operation is fully static, and the parallel interface is simple to use, similar to a synchronous RAM block.

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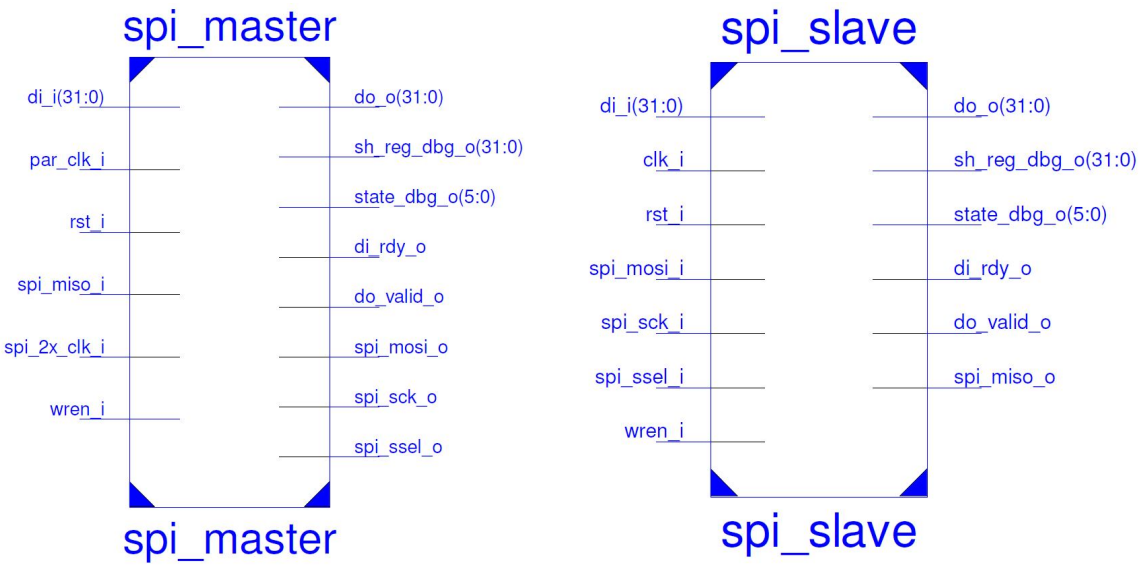
Architecture

Each core is implemented as a single design entity. The block diagram for each core is detailed below:



Each core has 2 interfaces, the SPI bus and the parallel data I/O ports. Separate clock domains inside the cores synchronize the operations of the core RTL registers and the parallel I/O ports.

The spi_master core generates the **`spi_sck_o`** clock by dividing input clock **`spi_2x_clk_i`**.

Small but significant differences exist in the state machines of the master and slave functions to have specialized cores for each function. Instead of making a universal master/slave core with runtime selection of operation mode, the function and mode are selected during instantiation, using generics, to achieve efficient silicon usage.

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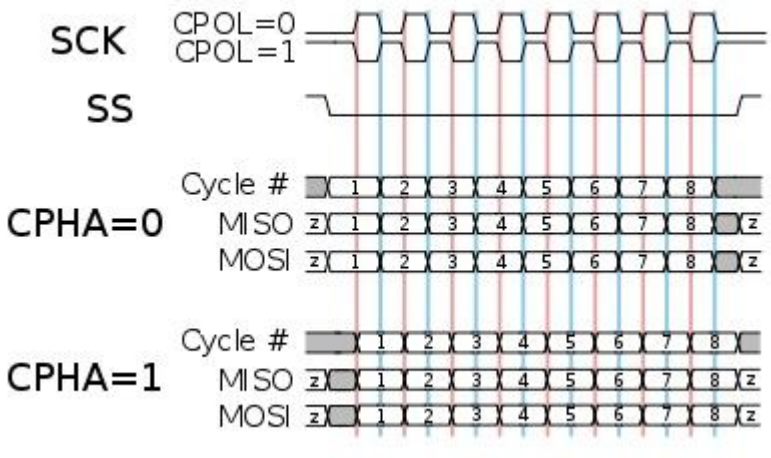
Operation

The internal logic of each core is a sequencer implemented as a single RTL state machine. The state machine is clocked by the SPI SCK clock. The spi_master block generates the spi clock from a 2x input clock, using 2 FFDs to derive two in-phase clocks, one continuous clock to control the sequencer, and an output spi clock, that is controlled with the CE input of a second FFD. Both clocks have high phase correlation, so serial data change is synchronous to the output SCK generated.

The SPI bus has 4 modes of operation, controlled by 2 parameters: Clock Polarity (CPOL) and Clock Phase (CPHA). The master and slave in a SPI connection must have the same SPI mode to interoperate. The modes are depicted in the following waveform diagram.



Serial data output signal changes at the clock edge selected by CPOL and CPHA.

The serial data input is sampled at the opposite clock edge. Data setup time to the data sampling edge is the limiting factor for maximum SPI operating frequency. If transmit-only operation is intended, the master can achieve a much higher clock frequency.

The model has generics to control generation of SPI mode, word width and data prefetch timing.

The operation of the spi_master block starts with a write to the parallel data in port.

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Clocks

[This section specifies all the clocks. All clocks, clock domain passes and the clock relations should be described.]

Name	Source	Rates (MHz)			Remarks	Description
		Max	Min	Resolution		
clk_pad_i	Input Pad	10	4	0.1	Duty cycle 70/30.	For external interface.
wb_clk_I	PLL	200	-	-	Must be synchronized to sm_clk_i	System clock.
sm_clk_i	Input port	55	40	1	There are multi-clocks paths.	Clock 55MHz for State machine.

Table 1: List of clocks

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IO Ports

[This section specifies the core IO ports.]

Port	Width	Direction	Description
wb_clk_i	1	Input	Block's WISHBONE Clock Input
wb_rst_i	1	Input	Block's WISHBONE Reset Input
wb_sel_i	4	Input	Block's WISHBONE Select Inputs
foo_pad_o	1	Output	Block's foo output to output pad
…			

Table 2: List of IO ports

Appendix A

Name

[This section may be added to outline different specifications.]

Appendix B

Name

[This section may be added to outline different specifications.]

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