STORM SoC – System on Chip
by Stephan Nolting

Altera / Terasic DE-2 Board

Important notes:

- **the I²C controller is not fully tested yet**
- **the SDRAM controller is not operating yet**

Proprietary Notice

Contact: stnolting@googlemail.com, zero_gravity@opencores.org

The most recent versions of them can be found at
STORM Core: http://www.opencores.com/project,storm_core
STORM SoC: http://www.opencores.com/project,storm_soc

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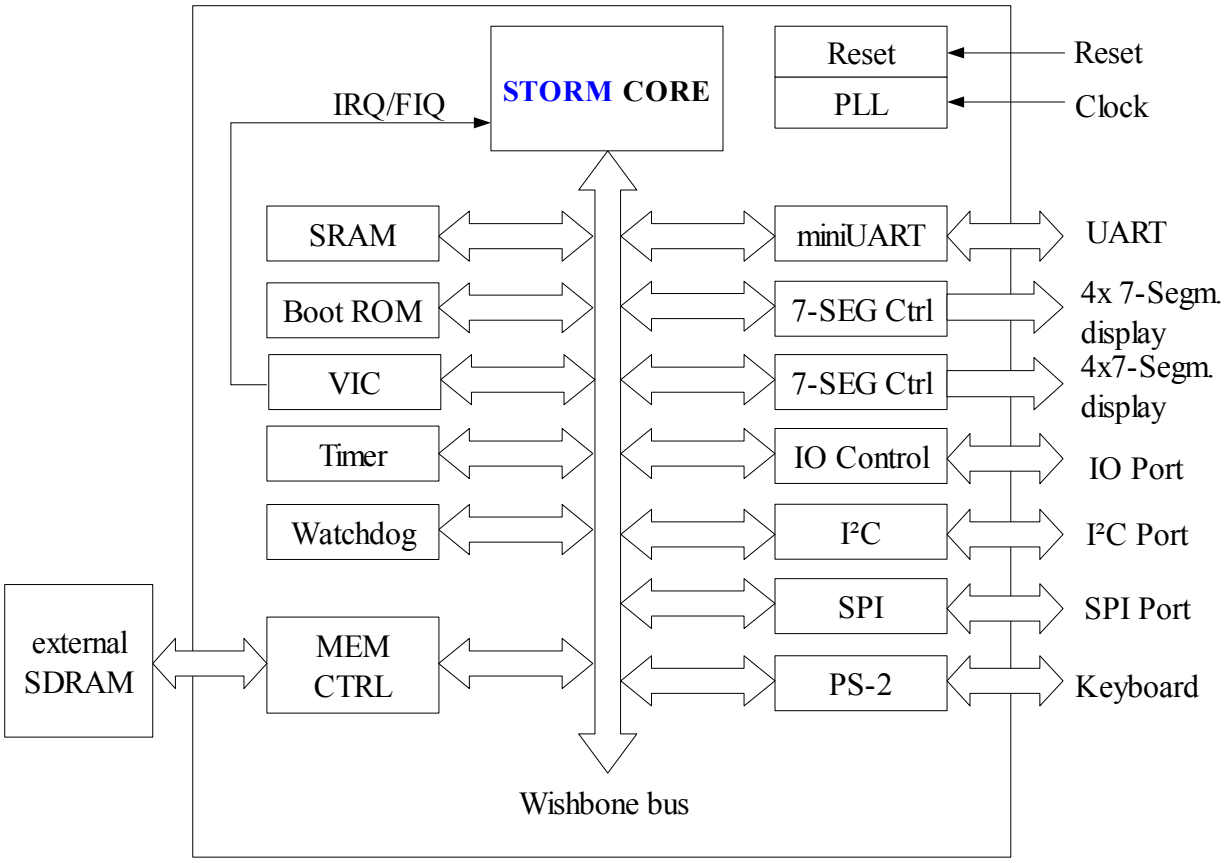

STORM Soc for ALTERA DE2-Board

2. Features

- ✔ Based on the STORM Core Processor System (ARM compatible)
- ✔ 32-bit Wishbone bus system
- ✔ 50 MHz system clock
- ✔ Internal 8 kbRAM memory for code/data
- ✔ Internal 2 kb ROM memory for bootcode
- ✔ 32-bit timer
- ✔ Vectorized interrupt controller, LPC compatible
- ✔ Seven segment controller
- ✔ IO port controller
- ✔ Simple mini UART
- ✔ SPI controller with 8 directly controlled slave select lines
- ✔ I²C controller
- ✔ PS2 keyboard interface
- ✔ Reset protection system

3. System Setup

Start Altera Quartus 2, create a new project and select the device setup corresponding to the DE2 board. Add all HDL source files of the needed components – or simply add the HDL files of all components – to the project. The **STORM_SoC_DE2.vhd** is the top entity of the implementation. Compile the project and download it into the FPGA.

Alternatively you can use the **storm_soc_de2.sof** file from the implementation's syn folder for configuring the FPGA. The **storm_soc_de2.pof** file can be used to program the EEPROM configuration device, so the FPGA will automatically be configured after applying power.

Connect the RS-232 port via an compatible adapter to you computer and start the program Terminal.exe from the tools folder. Configure the interface: 9600-8-N-1 (baud rate is 9600, 8 data bits, no parity bit, 1 stop bit). Click connect. Now power up the FPGA board and/or push the reset button (KEY0) for at least 3 seconds to generate a valid system reset.

The 4 right seven segment display will show “boot” and a basic menu is displayed in the Termial.exe console. A timer (left 4 seven segment displays) display a countdown. If this reaches 0, the application software within the core's memory is automatically started. Alternatively the application software can be directly started by pushing KEY1.

Go to the UART terminal and press '1' (and send). Now the bootloader waits for the program data. Click on send file and select the corresponding **storm_program.dat** file (for example form the blink_demo folder). These ***.dat** files are automatically created by the makefiles from the software folder.

After the download has completed, you can wait for a timeout, so the core starts the application. Alternatively you can reset the core (press KEY0 for minimum 3 seconds) and then start the application manually by pressing KEY1 or sending an 'x' within the terminal program.

4. Pin Table

Signal name suffix: **I = Input, O = output, IO = bidirectional port**

Signal name	FPGA pin	Function
CLK_I	PIN_N2	Global clock input, 50Mhz
GP_IO_PORT_I[0]	PIN_N25	General purpose input port bit 0 → SW0
GP_IO_PORT_I[1]	PIN_N26	General purpose input port bit 1 → SW1
GP_IO_PORT_I[2]	PIN_P25	General purpose input port bit 2 → SW2
GP_IO_PORT_I[3]	PIN_AE14	General purpose input port bit 3 → SW3
GP_IO_PORT_I[4]	PIN_AF14	General purpose input port bit 4 → SW4
GP_IO_PORT_I[5]	PIN_AD13	General purpose input port bit 5 → SW5
GP_IO_PORT_I[6]	PIN_AC13	General purpose input port bit 6 → SW6
GP_IO_PORT_I[7]	PIN_C13	General purpose input port bit 7 → SW7
GP_IO_PORT_I[8]	PIN_B13	General purpose input port bit 8 → SW8
GP_IO_PORT_I[9]	PIN_A13	General purpose input port bit 9 → SW9
GP_IO_PORT_I[10]	PIN_N1	General purpose input port bit 10 → SW10
GP_IO_PORT_I[11]	PIN_P1	General purpose input port bit 11 → SW11
GP_IO_PORT_I[12]	PIN_P2	General purpose input port bit 12 → SW12
GP_IO_PORT_I[13]	PIN_T7	General purpose input port bit 13 → SW13
GP_IO_PORT_I[14]	PIN_U3	General purpose input port bit 14 → SW14
GP_IO_PORT_I[15]	PIN_U4	General purpose input port bit 15 → SW15
GP_IO_PORT_I[16]	PIN_N23	General purpose input port bit 16 → KEY1
GP_IO_PORT_I[17]	PIN_P23	General purpose input port bit 16 → KEY2
GP_IO_PORT_I[18]	PIN_W26	General purpose input port bit 16 → KEY3
GP_IO_PORT_O[0]	PIN_AE23	General purpose output port bit 0 → LED_G0
GP_IO_PORT_O[1]	PIN_AF23	General purpose output port bit 1 → LED_G1
GP_IO_PORT_O[2]	PIN_AB21	General purpose output port bit 2 → LED_G2
GP_IO_PORT_O[3]	PIN_AC22	General purpose output port bit 3 → LED_G3
GP_IO_PORT_O[4]	PIN_AD22	General purpose output port bit 4 → LED_G4
GP_IO_PORT_O[5]	PIN_AD23	General purpose output port bit 5 → LED_G5
GP_IO_PORT_O[6]	PIN_AD21	General purpose output port bit 6 → LED_G6
GP_IO_PORT_O[7]	PIN_AC21	General purpose output port bit 7 → LED_G7
GP_IO_PORT_O[8]	PIN_AA14	General purpose output port bit 8 → LED_G8
GP_IO_PORT_O[9]	PIN_Y13	General purpose output port bit 9 → LED_G9
GP_IO_PORT_O[10]	PIN_AA13	General purpose output port bit 10 → LED_G10
GP_IO_PORT_O[11]	PIN_AC14	General purpose output port bit 11 → LED_G11
GP_IO_PORT_O[12]	PIN_AD15	General purpose output port bit 12 → LED_G12
GP_IO_PORT_O[13]	PIN_AE15	General purpose output port bit 13 → LED_G13
GP_IO_PORT_O[14]	PIN_AF13	General purpose output port bit 14 → LED_G14
GP_IO_PORT_O[15]	PIN_AE13	General purpose output port bit 15 → LED_G15
LED_DT_O	PIN_AE22	Data transfer status light → LED_R0
LED_IO_O	PIN_AF22	IO access status light → LED_R1
LED_IT_O	PIN_W19	Instruction transfer status light → LED_R1
RST_I	PIN_G26	Global reset → KEY0
UART0_RXD_I	PIN_C25	UART Receiver
UART0_TXD_O	PIN_B25	UART Transceiver
HEX_O[0]	PIN_AF10	Seven segment display 0, A-segment
HEX_O[1]	PIN_AB12	Seven segment display 0, B-segment

Signal name	FPGA pin	Function
HEX_O[2]	PIN_AC12	Seven segment display 0, C-segment
HEX_O[3]	PIN_AD11	Seven segment display 0, D-segment
HEX_O[4]	PIN_AE11	Seven segment display 0, E-segment
HEX_O[5]	PIN_V14	Seven segment display 0, F-segment
HEX_O[6]	PIN_V13	Seven segment display 0, G-segment
HEX_O[7]	PIN_V20	Seven segment display 1, A-segment
HEX_O[8]	PIN_V21	Seven segment display 1, B-segment
HEX_O[9]	PIN_W21	Seven segment display 1, C-segment
HEX_O[10]	PIN_Y22	Seven segment display 1, D-segment
HEX_O[11]	PIN_AA24	Seven segment display 1, E-segment
HEX_O[12]	PIN_AA23	Seven segment display 1, F-segment
HEX_O[13]	PIN_AB24	Seven segment display 1, G-segment
HEX_O[14]	PIN_AB23	Seven segment display 2, A-segment
HEX_O[15]	PIN_V22	Seven segment display 2, B-segment
HEX_O[16]	PIN_AC25	Seven segment display 2, C-segment
HEX_O[17]	PIN_AC26	Seven segment display 2, D-segment
HEX_O[18]	PIN_AB26	Seven segment display 2, E-segment
HEX_O[19]	PIN_AB25	Seven segment display 2, F-segment
HEX_O[20]	PIN_Y24	Seven segment display 2, G-segment
HEX_O[21]	PIN_Y23	Seven segment display 3, A-segment
HEX_O[22]	PIN_AA25	Seven segment display 3, B-segment
HEX_O[23]	PIN_AA26	Seven segment display 3, C-segment
HEX_O[24]	PIN_Y26	Seven segment display 3, D-segment
HEX_O[25]	PIN_Y25	Seven segment display 3, E-segment
HEX_O[26]	PIN_U22	Seven segment display 3, F-segment
HEX_O[27]	PIN_W24	Seven segment display 3, G-segment
HEX_O[28]	PIN_U9	Seven segment display 4, A-segment
HEX_O[29]	PIN_U1	Seven segment display 4, B-segment
HEX_O[30]	PIN_U2	Seven segment display 4, C-segment
HEX_O[31]	PIN_T4	Seven segment display 4, D-segment
HEX_O[32]	PIN_R7	Seven segment display 4, E-segment
HEX_O[33]	PIN_R6	Seven segment display 4, F-segment
HEX_O[34]	PIN_T3	Seven segment display 4, G-segment
HEX_O[35]	PIN_T2	Seven segment display 5, A-segment
HEX_O[36]	PIN_P6	Seven segment display 5, B-segment
HEX_O[37]	PIN_P7	Seven segment display 5, C-segment
HEX_O[38]	PIN_T9	Seven segment display 5, D-segment
HEX_O[39]	PIN_R5	Seven segment display 5, E-segment
HEX_O[40]	PIN_R4	Seven segment display 5, F-segment
HEX_O[41]	PIN_R3	Seven segment display 5, G-segment
HEX_O[42]	PIN_R2	Seven segment display 6, A-segment
HEX_O[43]	PIN_P4	Seven segment display 6, B-segment
HEX_O[44]	PIN_P3	Seven segment display 6, C-segment
HEX_O[45]	PIN_M2	Seven segment display 6, D-segment
HEX_O[46]	PIN_M3	Seven segment display 6, E-segment
HEX_O[47]	PIN_M5	Seven segment display 6, F-segment
HEX_O[48]	PIN_M4	Seven segment display 6, G-segment
HEX_O[49]	PIN_L3	Seven segment display 7, A-segment

Signal name	FPGA pin	Function
HEX_O[50]	PIN_L2	Seven segment display 7, B-segment
HEX_O[51]	PIN_L9	Seven segment display 7, C-segment
HEX_O[52]	PIN_L6	Seven segment display 7, D-segment
HEX_O[53]	PIN_L7	Seven segment display 7, E-segment
HEX_O[54]	PIN_P9	Seven segment display 7, F-segment
HEX_O[55]	PIN_N9	Seven segment display 7, G-segment
SDRAM_ADR_O[0]	PIN_T6	On-board SDRAM address bit 0
SDRAM_ADR_O[1]	PIN_V4	On-board SDRAM address bit 1
SDRAM_ADR_O[2]	PIN_V3	On-board SDRAM address bit 2
SDRAM_ADR_O[3]	PIN_W2	On-board SDRAM address bit 3
SDRAM_ADR_O[4]	PIN_W1	On-board SDRAM address bit 4
SDRAM_ADR_O[5]	PIN_U6	On-board SDRAM address bit 5
SDRAM_ADR_O[6]	PIN_U7	On-board SDRAM address bit 6
SDRAM_ADR_O[7]	PIN_U5	On-board SDRAM address bit 7
SDRAM_ADR_O[8]	PIN_W4	On-board SDRAM address bit 8
SDRAM_ADR_O[9]	PIN_W3	On-board SDRAM address bit 9
SDRAM_ADR_O[10]	PIN_Y1	On-board SDRAM address bit 10
SDRAM_ADR_O[11]	PIN_V5	On-board SDRAM address bit 11
SDRAM_DAT_IO[0]	PIN_V6	On-board SDRAM data bit 0
SDRAM_DAT_IO[1]	PIN_AA2	On-board SDRAM data bit 1
SDRAM_DAT_IO[2]	PIN_AA1	On-board SDRAM data bit 2
SDRAM_DAT_IO[3]	PIN_Y3	On-board SDRAM data bit 3
SDRAM_DAT_IO[4]	PIN_Y4	On-board SDRAM data bit 4
SDRAM_DAT_IO[5]	PIN_R8	On-board SDRAM data bit 5
SDRAM_DAT_IO[6]	PIN_T8	On-board SDRAM data bit 6
SDRAM_DAT_IO[7]	PIN_V7	On-board SDRAM data bit 7
SDRAM_DAT_IO[8]	PIN_W6	On-board SDRAM data bit 8
SDRAM_DAT_IO[9]	PIN_AB2	On-board SDRAM data bit 9
SDRAM_DAT_IO[10]	PIN_AB1	On-board SDRAM data bit 10
SDRAM_DAT_IO[11]	PIN_AA4	On-board SDRAM data bit 11
SDRAM_DAT_IO[12]	PIN_AA3	On-board SDRAM data bit 12
SDRAM_DAT_IO[13]	PIN_AC2	On-board SDRAM data bit 13
SDRAM_DAT_IO[14]	PIN_AC1	On-board SDRAM data bit 14
SDRAM_DAT_IO[15]	PIN_AA5	On-board SDRAM data bit 15
SDRAM_BA_O[0]	PIN_AE2	On-board SDRAM bank address bit 0
SDRAM_BA_O[1]	PIN_AE3	On-board SDRAM bank address bit 0
SDRAM_DQM_O[0]	PIN_AD2	On-board SDRAM data mask bit 0
SDRAM_DQM_O[1]	PIN_Y5	On-board SDRAM data mask bit 1
SDRAM_CASN_O	PIN_AB3	On-board SDRAM column address strobe
SDRAM_CKE_O	PIN_AA6	On-board SDRAM clock enable
SDRAM_CLK_O	PIN_AA7	On-board SDRAM clock signal
SDRAM_CSN_O	PIN_AC3	On-board SDRAM chip select
SDRAM_RASN_O	PIN_AB4	On-board SDRAM row address strobe
SDRAM_WEN_O	PIN_AD3	On-board SDRAM write enable
SPI_CLK_O	PIN_K25	SPI, serial clock
SPI_MISO_I	PIN_K26	SPI, serial data out
SPI_MOSI_O	PIN_M22	SPI, serial data in
SPI_SS_O[0]	PIN_M23	SPI, chip select 0

Signal name	FPGA pin	Function
SPI_SS_O[1]	PIN_M19	SPI, chip select 1
SPI_SS_O[2]	PIN_M20	SPI, chip select 2
SPI_SS_O[3]	PIN_N20	SPI, chip select 3
SPI_SS_O[4]	PIN_M21	SPI, chip select 4
SPI_SS_O[5]	PIN_M24	SPI, chip select 5
SPI_SS_O[6]	PIN_M25	SPI, chip select 6
SPI_SS_O[7]	PIN_N24	SPI, chip select 7
I2C_SCL_IO	PIN_D25	I²C, serial clock
I2C_SDA_IO	PIN_J22	I²C, serial data
PS2_CLK_IO	PIN_D26	PS2-keyboard clock
PS2_DAT_IO	PIN_C24	PS2-keyboard data

5. System Address Map

Memory Address Map

Address (hex)	Name	R/W	Module	Sub module
0x00000000 ... 0x00001000	IRAM_BASE + offset	R/W	Internal SRAM	32-bit memory cell
0xFFF00000 ... 0xFFF00800	ROM_BASE + offset	R	Internal boot ROM	32-bit memory cell

IO Address Map

Address (hex)	Name	R/W	Module	Sub module
0xFFFF0000	GPIO0_OUT	R	IO controller 0	Output port
0xFFFF0004	GPIO0_IN	R/W		Input port
0xFFFF0008	SSEG0_DATA	R/W	7-Seg controller 0	Hex DATA register
0xFFFF000C	SSEG0_CTRL	R/W		Segment CTRL register
0xFFFF0010	SSEG1_DATA	R/W	7-Seg controller 1	Hex DATA register
0xFFFF0014	SSEG1_CTRL	R/W		Segment CTRL register
0xFFFF0018	UART0_DATA	R/W	miniUART 0	RX/TX data register
0xFFFF001C	UART0_SREG	R/W		Status register
0xFFFF0020	STME0_CNT	R/W	System timer 0	Counter register
0xFFFF0024	STME0_VAL	R/W		Threshold value
0xFFFF0028	STME0_CONF	R/W		Configuration register
0xFFFF002C	STME0_SCRT	R/W		Scratch register
0xFFFF0030	SPI0_CONF	R/W	SPI controller 0	Configuration register
0xFFFF0034	SPI0_PRSC	R/W		Prescaler value
0xFFFF0038	SPI0_SCSR	R/W		Slave select register
0xFFFF0040	SPI0_DAT0	R/W		FIFO data register 0
0xFFFF0044	SPI0_DAT1	R/W		FIFO data register 0
0xFFFF0048	SPI0_DAT2	R/W		FIFO data register 0
0xFFFF004C	SPI0_DAT3	R/W		FIFO data register 0
0xFFFF0050	I2C0_CMD	R/W	I²C controller 0	Command register
0xFFFF0050	I2C0_STAT	R/W		Status register
0xFFFF0060	I2C0_PRLO	R/W		Prescaler, low byte

Address (hex)	Name	R/W	Module	Sub module
0xFFFF0064	I2C0_PFHI	R/W	I²C controller 0	Prescaler, high byte
0xFFFF0068	I2C0_CTRL	R/W		Control register
0xFFFF006C	I2C0_DATA	R/W		RX/TX data register
0xFFFF0070	PS2_DATA	R/W	PS2 keyboard controller 0	Data register
0xFFFF0074	PS2_STAT	R/W		Status / control register
0xFFFFEF00	XMC_CSR	R/W	External memory controller	Status / control register
0xFFFFEF04	XMC_POC	R		Power-on configuration register
0xFFFFEF08	XMC_BA_MASK	R/W		Base address mask register
0xFFFFEF10	XMC_CSC0	R/W		Chip select config, module 0
0xFFFFEF14	XMC_TMS0	R/W		Timing config, module 0
0xFFFFEF18	XMC_CSC1	R/W		Chip select config, module 1
0xFFFFEF1C	XMC_TMS1	R/W		Timing config, module 1
0xFFFFEF20	XMC_CSC2	R/W		Chip select config, module 2
0xFFFFEF24	XMC_TMS2	R/W		Timing config, module 2
0xFFFFEF28	XMC_CSC3	R/W		Chip select config, module 3
0xFFFFEF2C	XMC_TMS3	R/W		Timing config, module 3
0xFFFFEF30	XMC_CSC4	R/W		Chip select config, module 4
0xFFFFEF34	XMC_TMS4	R/W		Timing config, module 4
0xFFFFEF38	XMC_CSC5	R/W		Chip select config, module 5
0xFFFFEF3C	XMC_TMS5	R/W		Timing config, module 5
0xFFFFEF40	XMC_CSC6	R/W		Chip select config, module 6
0xFFFFEF44	XMC_TMS6	R/W		Timing config, module 6
0xFFFFEF48	XMC_CSC7	R/W		Chip select config, module 7
0xFFFFEF4C	XMC_TMS7	R/W		Timing config, module 7
0xFFFFF000	VICIRQStatus	R	Vector interrupt controller	IRQ status (masked)
0xFFFFF004	VICFIQStatus	R		FIQ status (masked)
0xFFFFF008	VICRawIntr	R		Unmasked interrupt req. status
0xFFFFF00C	VICIntSelect	R/W		Interrupt type, '1' FIQ, '0' IRQ
0xFFFFF010	VICIntEnable	R/W		INT request lines enable
0xFFFFF014	VICIntEnClear	W		Clear INT request line enable bit
0xFFFFF018	VICSoftInt	W		Trigger INT line by software
0xFFFFF01C	VICSoftintClear	W		Clear SW INT request enable bit

Address (hex)	Name	R/W	Module	Sub module
0xFFFFF020	VICProtection	R/W	Vector interrupt controller	Protected mode (only priv. acc.)
0xFFFFF030	VICVectAddr	R/W		ISR address / INT acknowledge
0xFFFFF034	VICDefVectAddr	R/W		ISR addr for unvectorized INT
0xFFFFF038	VICTrigLevel	R/W		Hi/Lo / rising/falling edge detect
0xFFFFF03C	VICTrigMode	R/W		Level/edge INT detector
0xFFFFF040	VICVectAddr0	R/W		ISR address for VEC_INT 0
0xFFFFF044	VICVectAddr1	R/W		ISR address for VEC_INT 1
0xFFFFF048	VICVectAddr2	R/W		ISR address for VEC_INT 2
0xFFFFF04C	VICVectAddr3	R/W		ISR address for VEC_INT 3
0xFFFFF050	VICVectAddr4	R/W		ISR address for VEC_INT 4
0xFFFFF054	VICVectAddr5	R/W		ISR address for VEC_INT 5
0xFFFFF058	VICVectAddr6	R/W		ISR address for VEC_INT 6
0xFFFFF05C	VICVectAddr7	R/W		ISR address for VEC_INT 7
0xFFFFF060	VICVectAddr8	R/W		ISR address for VEC_INT 8
0xFFFFF064	VICVectAddr9	R/W		ISR address for VEC_INT 9
0xFFFFF068	VICVectAddr10	R/W		ISR address for VEC_INT 10
0xFFFFF06C	VICVectAddr11	R/W		ISR address for VEC_INT 11
0xFFFFF070	VICVectAddr12	R/W		ISR address for VEC_INT 12
0xFFFFF074	VICVectAddr13	R/W		ISR address for VEC_INT 13
0xFFFFF078	VICVectAddr14	R/W		ISR address for VEC_INT 14
0xFFFFF07C	VICVectAddr15	R/W		ISR address for VEC_INT 15
0xFFFFF080	VICVectCntl0	R/W		Source select / EN VEC_INT 0
0xFFFFF084	VICVectCntl1	R/W		Source select / EN VEC_INT 1
0xFFFFF088	VICVectCntl2	R/W		Source select / EN VEC_INT 2
0xFFFFF08C	VICVectCntl3	R/W		Source select / EN VEC_INT 3
0xFFFFF090	VICVectCntl4	R/W		Source select / EN VEC_INT 4
0xFFFFF094	VICVectCntl5	R/W		Source select / EN VEC_INT 5
0xFFFFF098	VICVectCntl6	R/W		Source select / EN VEC_INT 6
0xFFFFF09C	VICVectCntl7	R/W		Source select / EN VEC_INT 7
0xFFFFF0A0	VICVectCntl8	R/W		Source select / EN VEC_INT 8
0xFFFFF0A4	VICVectCntl9	R/W		Source select / EN VEC_INT 9
0xFFFFF0A8	VICVectCntl10	R/W		Source select / EN VEC_INT 10
0xFFFFF0AC	VICVectCntl11	R/W		Source select / EN VEC_INT 11

Address (hex)	Name	R/W	Module	Sub module
0xFFFFF0B0	VICVectCntl12	R/W	Vector interrupt controller	Source select / EN VEC_INT 12
0xFFFFF0B4	VICVectCntl13	R/W		Source select / EN VEC_INT 13
0xFFFFF0B8	VICVectCntl14	R/W		Source select / EN VEC_INT 14
0xFFFFF0BC	VICVectCntl15	R/W		Source select / EN VEC_INT 15