六、各个子模块仿真

**1. ALU**控制器模块

1) 仿真模块

|  |
| --- |
| module aluctrsim;  // Inputs  reg [1:0] ALUOp;  reg [5:0] funct;  // Outputs  wire [3:0] ALUctr;  // Instantiate the Unit Under Test (UUT)  aluctr uut (  .ALUOp(ALUOp),  .funct(funct),  .ALUCtr(ALUctr)  );  initial begin  // Initialize Inputs  ALUOp = 0;  funct = 0;  // Wait 100 ns for global reset to finish  #100;  // Add stimulus here  ALUOp = 2'b01;  funct = 0;  #100;  ALUOp = 2'b10;  funct = 6'b100000;  #100;  ALUOp = 2'b10;  funct = 6'b101010;  end  endmodule |

**2.** 寄存器模块

1) 仿真代码

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| --- |
| module regsim;  // Inputs  reg clk;  reg reset;  reg [31:0] regWriteData;  reg [4:0] regWriteAddr;  reg regWriteEn;  reg [4:0] RsAddr;  reg [4:0] RtAddr;  wire [31:0] RsData;  wire [31:0] RtData;  // Instantiate the Unit Under Test (UUT)  regFile uut (  .clk(clk),  .reset(reset),  .regWriteData(regWriteData),  .regWriteAddr(regWriteAddr),  .regWriteEn(regWriteEn),  .RsData(RsData),  .RtData(RtData),  .RsAddr(RsAddr),  .RtAddr(RtAddr)  );  initial begin  // Initialize Inputs  clk = 0;  reset = 0;  regWriteData = 0;  regWriteAddr = 0;  regWriteEn = 0;  RsAddr = 0;  RtAddr = 0;  // Wait 100 ns for global reset to finish  #100;  regWriteData = 32'h55aaaa55;  regWriteEn = 1; |
| reset = 1;  #100  reset = 0;  // Add stimulus here  end  parameter PERIOD = 20;  always begin  clk = 1'b0;  #(PERIOD / 2) clk = 1'b1;  #(PERIOD / 2) ;  end  integer i;  always begin  for(i = 30; i >= 1; i = i - 1) begin  regWriteAddr = i;  RsAddr = i;  #PERIOD;  end  end  endmodule |

**4. ALU**模块

1) 仿真代码

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| --- |
| module alusim;  // Inputs  reg [31:0] input1;  reg [31:0] input2;  reg [3:0] aluCtr;  // Outputs  wire [31:0] aluRes;  wire zero;  // Instantiate the Unit Under Test (UUT)  alu uut (  .input1(input1),  .input2(input2),  .aluCtr(aluCtr),  .aluRes(aluRes),  .zero(zero)  );  initial begin  // Initialize Inputs  input1 = 1;  input2 = 1;  aluCtr = 4'b0110;  #100;  input1 = 2;  input2 = 1;  aluCtr = 4'b0110;  #100  input1 = 1;  input2 = 1;  aluCtr = 4'b0010;  #100  input1 = 1;  input2 = 0;  aluCtr = 4'b0000;  #100  input1 = 1;  input2 = 0;  aluCtr = 4'b0001;  #100  input1 = 1;  input2 = 0;  aluCtr = 4'b0111;  #100  input1 = 0;  input2 = 1;  aluCtr = 4'b0111;  end  endmodule |

**5.** 顶层仿真

1) 仿真代码

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| --- |
| module topsim;  // Inputs  reg clkin;  reg reset;  // Instantiate the Unit Under Test (UUT)  top uut (  .clkin(clkin),  .reset(reset)  );  initial begin  // Initialize Inputs  clkin = 0;  reset = 1;  // Wait 100 ns for global reset to finish  #100;  reset = 0;  end  parameter PERIOD = 20;  always begin  clkin = 1'b0;  #(PERIOD / 2) clkin = 1'b1;  #(PERIOD / 2) ;  end  endmodule |