Allegro Introduction





内容提要

• PCB Editor 设计环境和设置

- ➤ Allegro SPB工作界面
 - ✓ 产品说明及选项面板
- ➤ Allegro SPB参数设置
- ➤ Allegro SPB环境设置

· PCB设计前处理

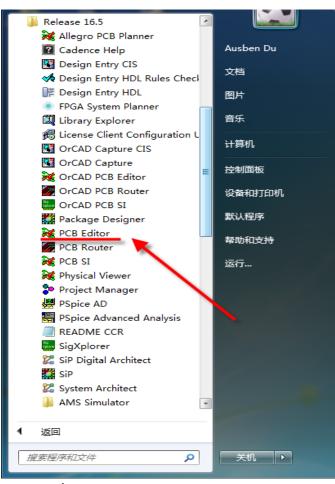
- ▶ 导网表
 - ✓ 库路径设定
 - ✓ Capture网表调入
 - ✔ 第三方网表
- > 建立板框
 - ✓ 手动绘制
 - ✔ DXF导入/导出
- ▶ 禁布区设置





· Allegro SPB 工作界面与产品说明

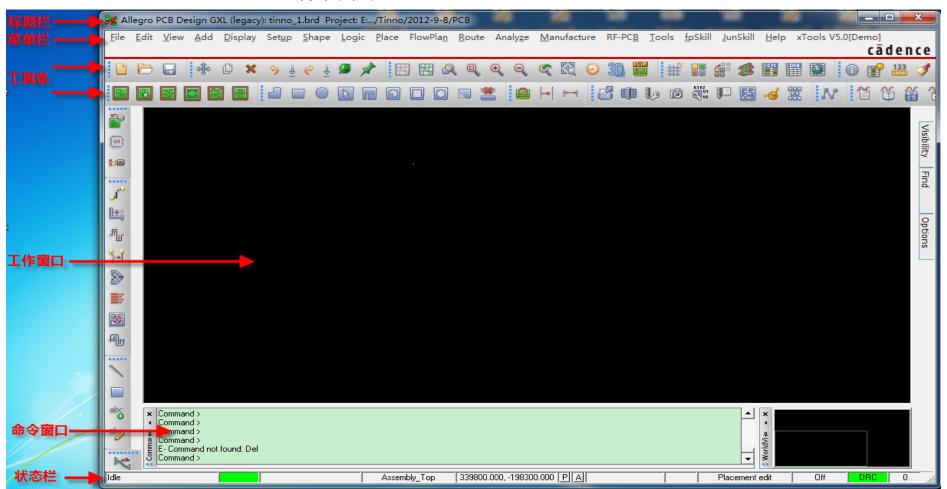
- 打开PCB Editor







- PCB Editor工作界面







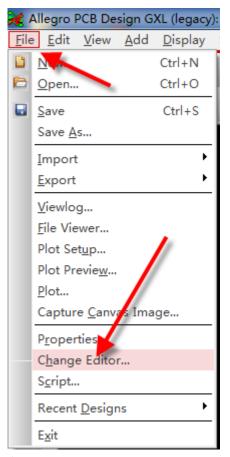
- · Allegro SPB 工作界面与产品说明
 - 其他主要工具

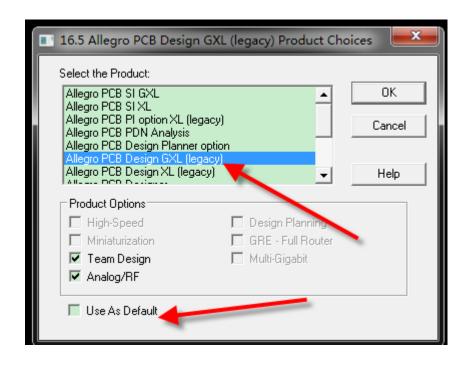






- Allegro SPB 工作界面与产品说明
 - Cadence Allegro 产品选择

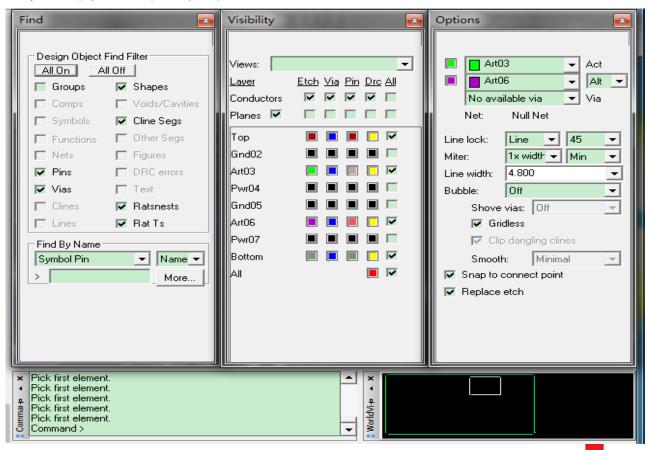








- Allegro SPB 选项面板
 - 5个可折叠式选项卡

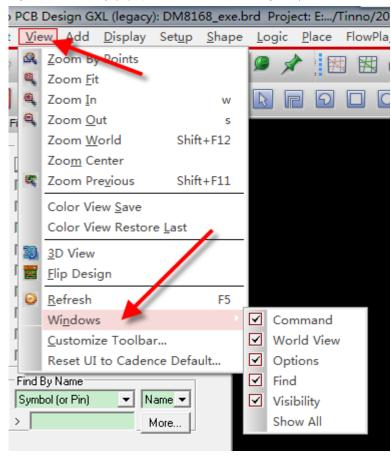


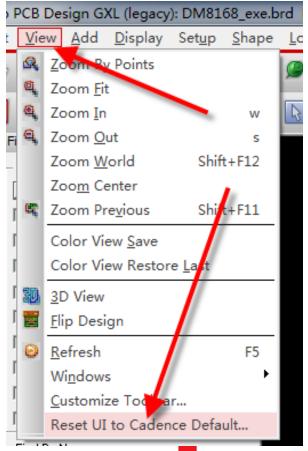


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- Allegro SPB 选项面板
 - 关闭、打开、重置选项卡



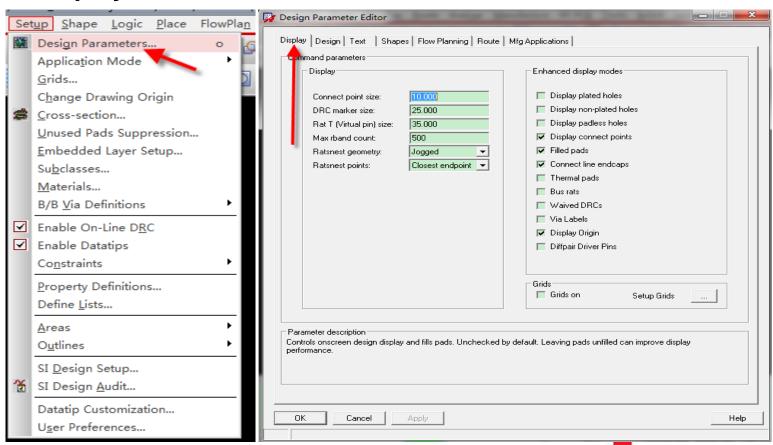






Design Parameter

- Display选项卡

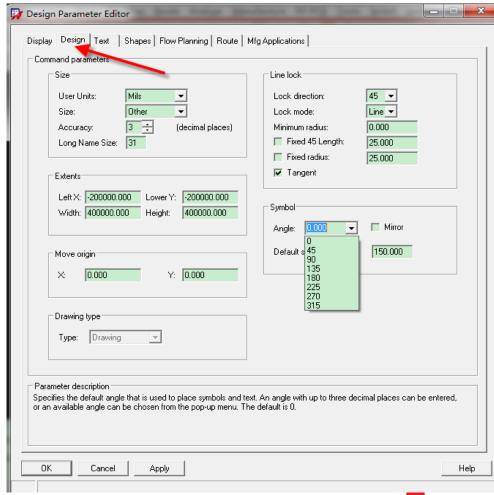






Design Parameter

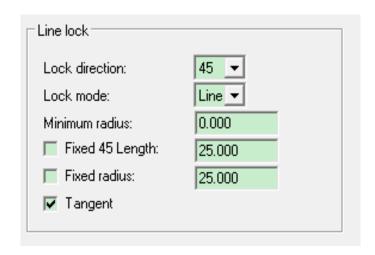
- Design选项卡

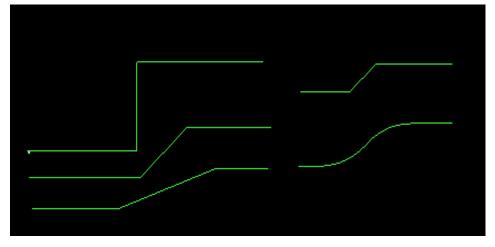






- Design Parameter
 - Design下面的布线选项

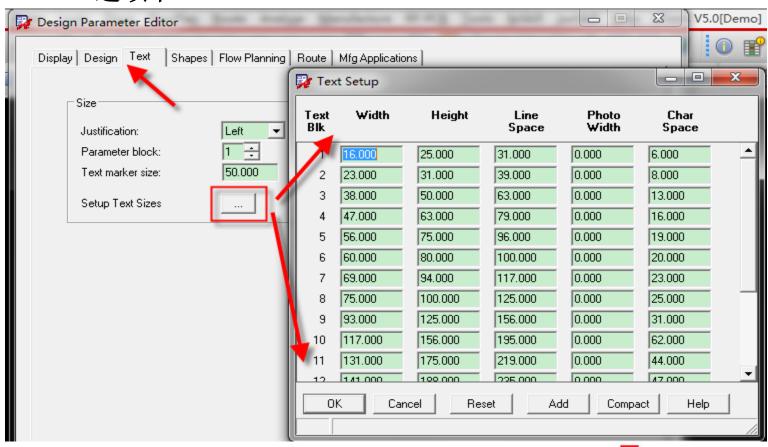








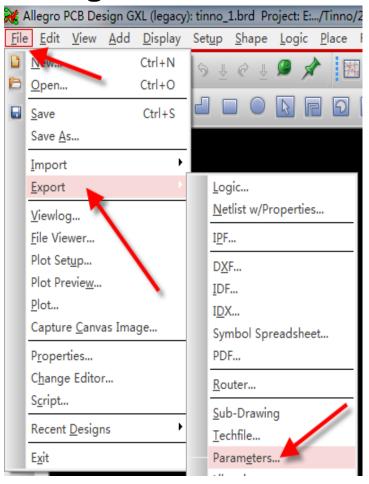
- Design Parameter
 - Text选项卡

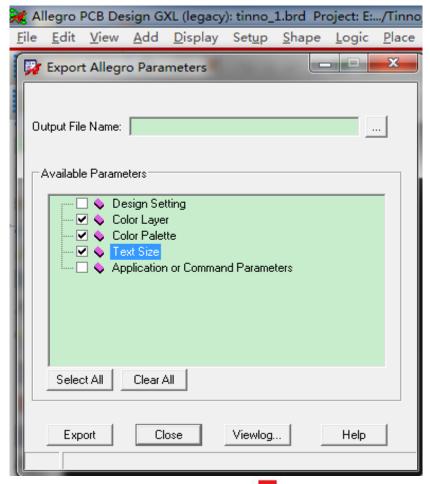






Design Parameter参数的导入与导出

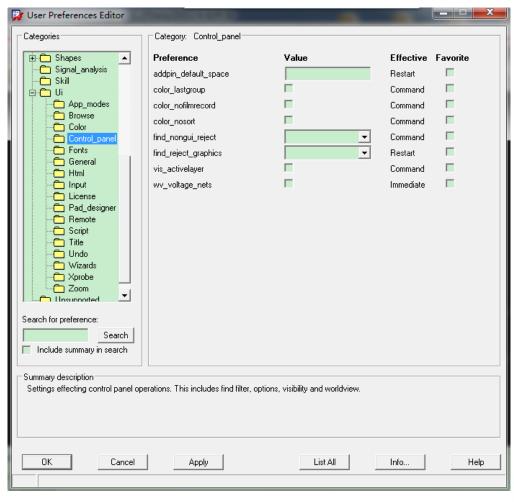








• 用户环境设置界面







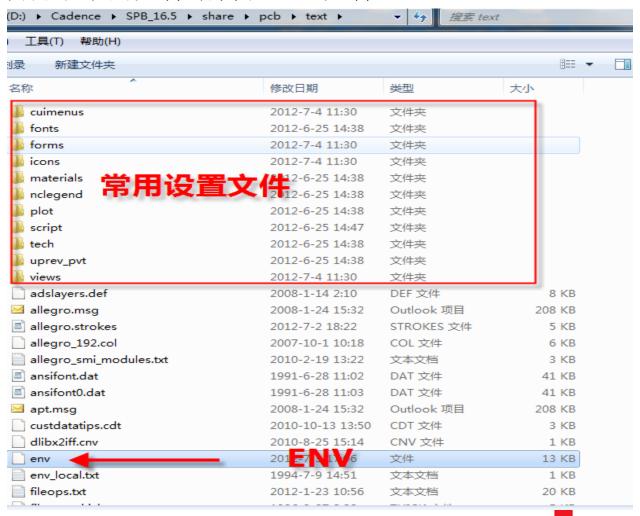
· 环境变量和Home路径







- 安装目录下的文件结构和ENV文件







· ENV内容及快捷键定义

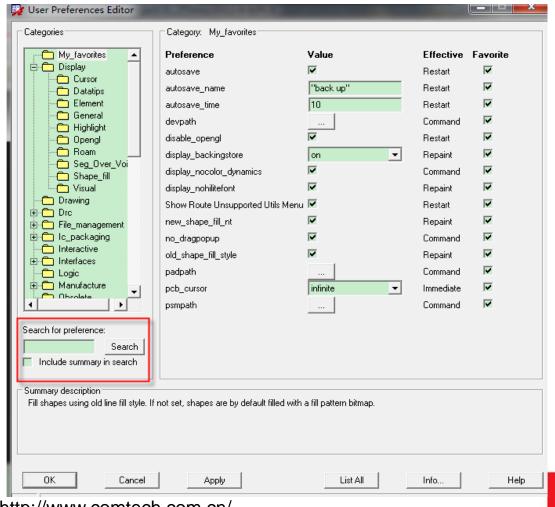
```
# SigNoise model variables.
set SI_MODEL_PATH = . $ALLEGRO_SITE/signal_$signal_install_dir
set SI_MODEL_FILE_EXT = Generic_IBIS(ibs) IBIS_Buffer(buf) IBIS_EBD(ebd)
IBIS_ICM (icm) IBIS_Pin_List (pin) IBIS_Package (pkg) Quad (mod) Generic_SPICE
(spc) HSpice_Input(sp) HSpice_Output(lis) Spectre(spc) Touchstone(S?p, s??, snp)
DML(ndx, dml) Interconnect(iml) ABIML(abiml)
# Non-HDL Supported Design Search Path Variables
set MISCPATH = . $ALLEGRO_SITE/misc
set ARTPATH = . . . $ALLEGRO_SITE
set APTPATH = . . . $ALLEGRO_SITE
set CLIPPATH = .
set DCLPATH = . .. $ALIBPATH $COMPLIBPATH
set DEVPATH = . devices .. ../devices $ALLEGRO_SITE/devices $ALIBPATH/devices
$COMPLIBPATH/devices
set DFAAUDITPATH = . $ALLEGRO_SITE/assembly $ALLEGRO_INSTALL DIR/assembly
set DFACNSPATH = . dfa .. ../dfa $ALLEGRO_SITE/dfa
set NCDPATH = . .. $ALLEGRO_SITE/nclegend $GLOBAL/nclegend
set SCRIPTPATH = . $ALLEGRO_SITE/scripts $GLOBAL/script
set TEXTPATH = . $ALLEGRO_SITE/extracta $GLOBAL/views
set VIEWPATH = . $ALLEGRO_SITE/views
set XTALK_TABLE_PATH = . xtalk_tables . . . ./xtalk_tables $ALLEGRO_SITE/xtalk
$ALIBPATH/xtalk_tables
set WIZARD_TEMPLATE_PATH = . $ALLEGRO_SITE/new_templates
$ALLEGRO INSTALL DIR/pcb lib/symbols/template
set LDFPATH = ...
# System Configuration .scf file search path
set SCFPATH = . scfs .. ../scfs
```

```
alias F2 toggle
alias F3 grid toggle
alias F4 show element
alias F5 redraw
alias F6 done
alias F7 next
alias F8 oops
alias F9 cancel
alias F10
alias F11 zoom in
alias F12 zoom out
alias SF2 property edit
alias SF3 slide
alias SF4 show measure
alias SF5 copv
alias SF6 move
alias SF7 dehilight all
alias SF8 hilight pick
alias SF9 vertex
alias SF10 save as temp
alias SF11 zoom previous
alias SF12 zoom world
alias CF2 next
alias CF5 color192
alias CF6 layer priority
alias CSF5 status
```

```
funckev a slide
funckev A
funckey b custom smooth
funckev B dbdoctor
funckey c copy
funckey C shape void copy
funckey d done
funckey D diff pairs
funckey e move
funckey E cmgr
funckey f shape add
funckey F create fanout
funckey g shape edit boundary
funckev G
funckey h assign color
funckev H x ea cline
funckey I island delete
funckey j dehilight all
funckey J x_cmd_align_text
funckev k color192
funckey K
funckey 1
funckev L
funckey m show measure
```



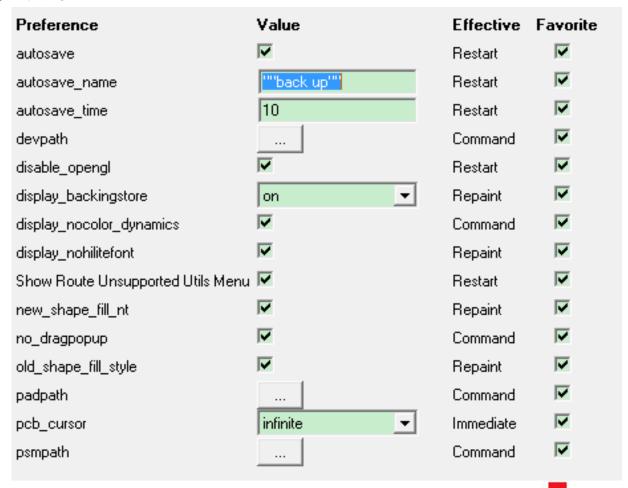
搜索及My_favorites的使用







• 常用项目设置

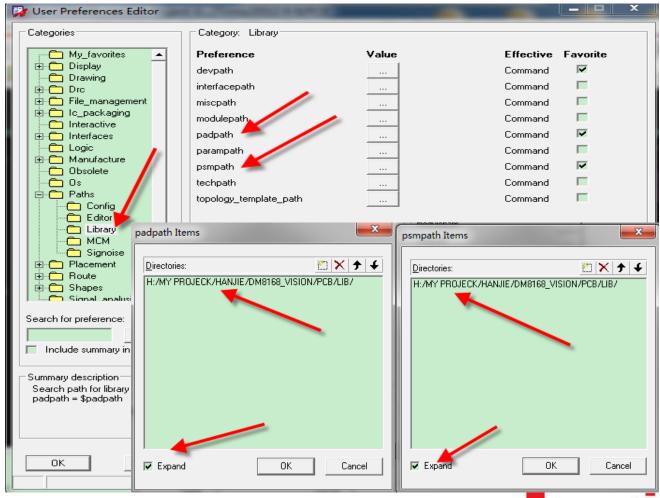




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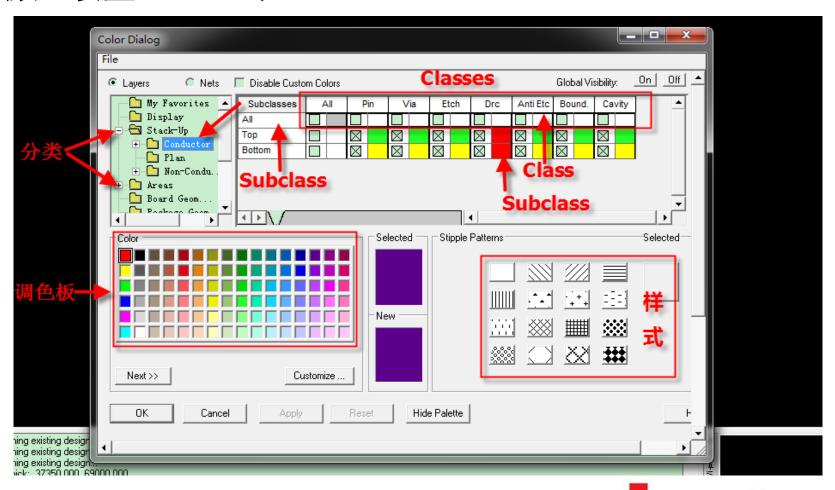


• 库路径设置





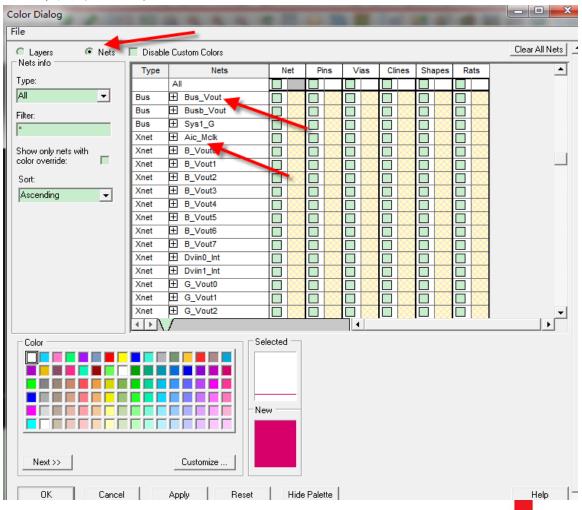
・ 颜色设置(Class和Subclass)







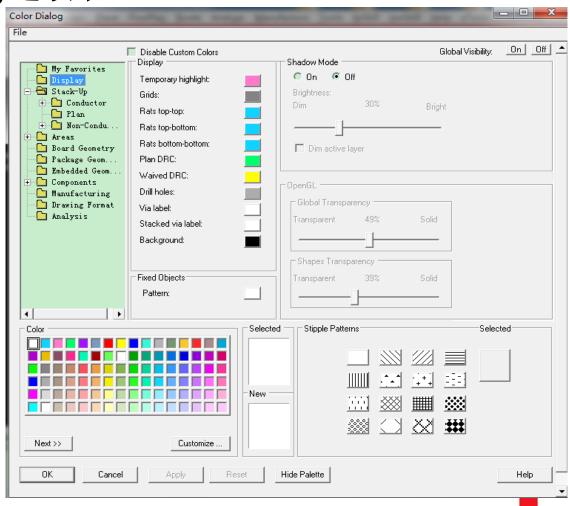
· 按照Net进行颜色设置







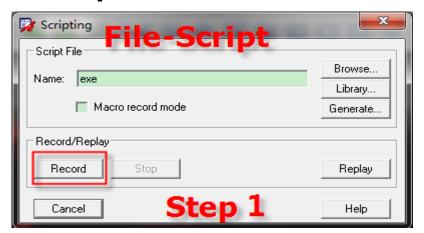
· Display选项卡



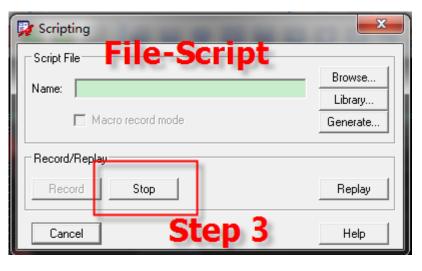


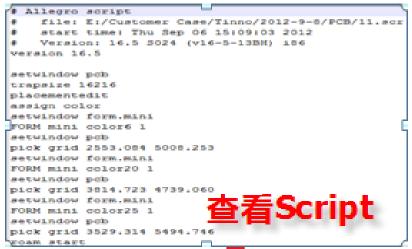


· Script功能应用







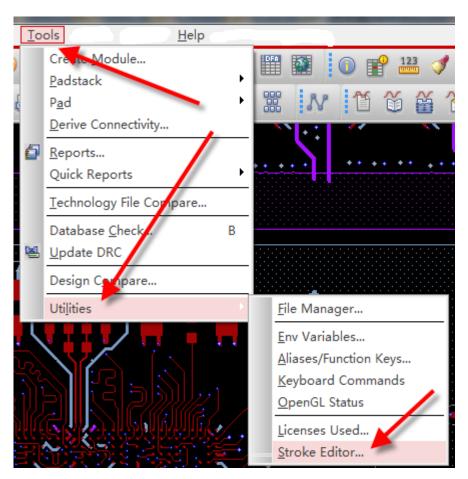






· Stroke功能应用

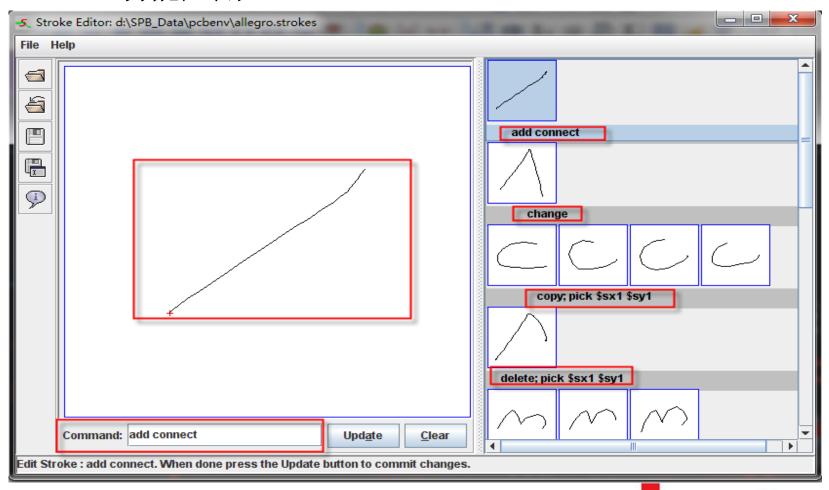








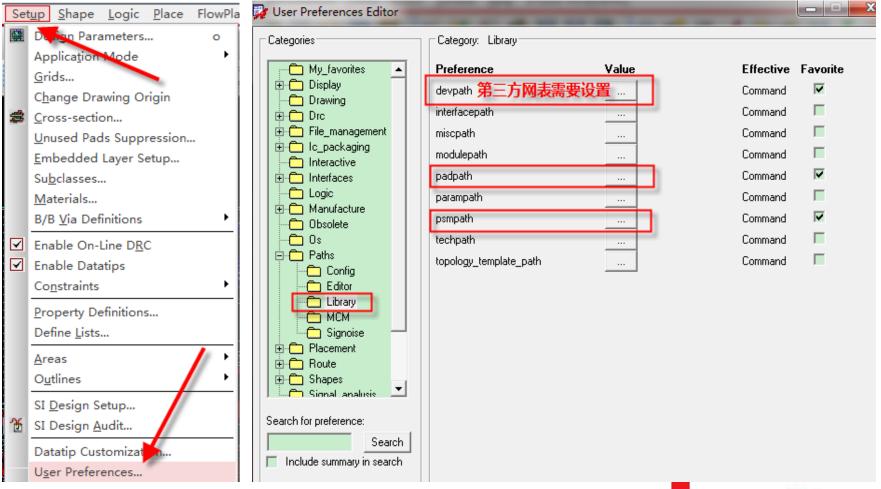
· Stroke功能应用







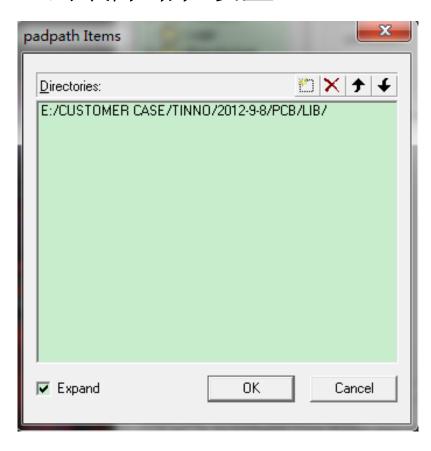
• 封装库路径设置

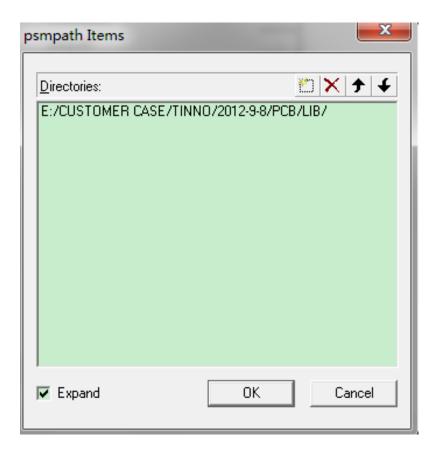






• 封装库路径设置

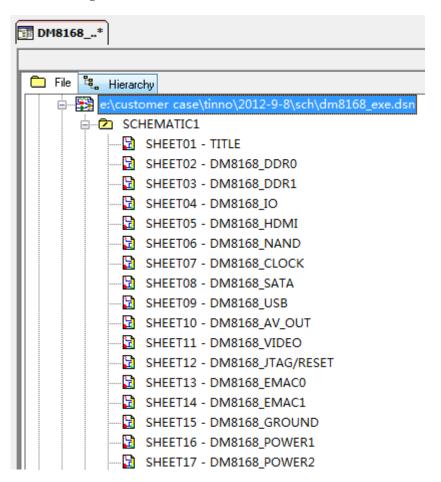


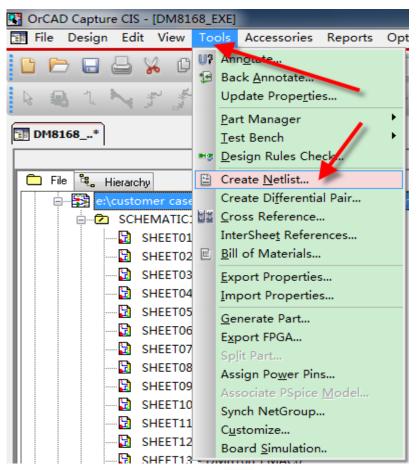






· Capture CIS第一方网表导出/导入

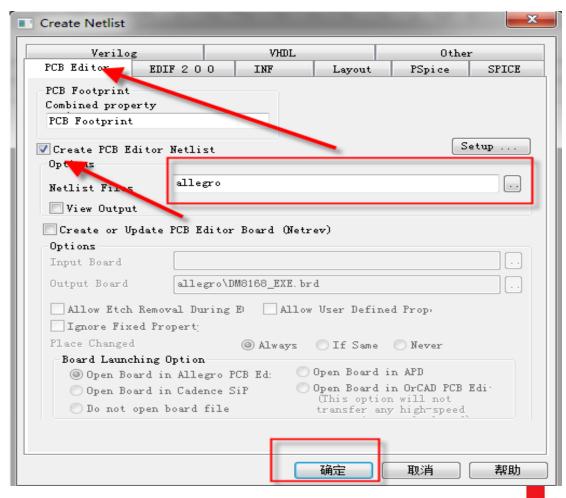








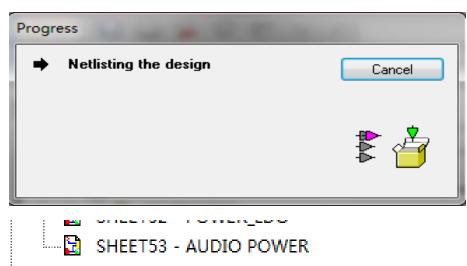
Capture CIS第一方网表导出/导入

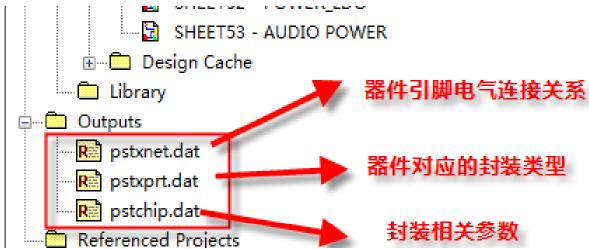






· Capture CIS第一方网表导出/导入

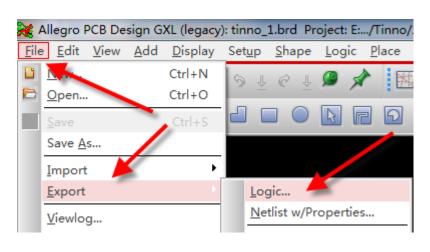


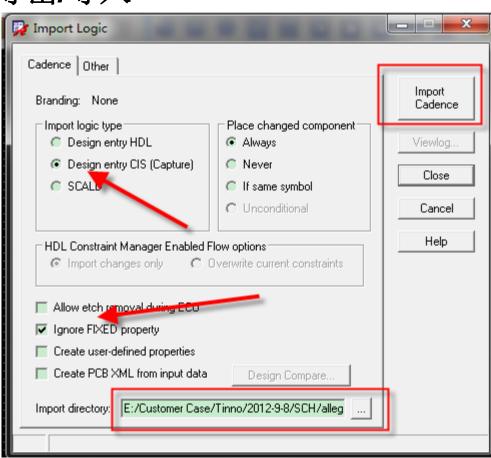






· Capture CIS第一方网表导出/导入

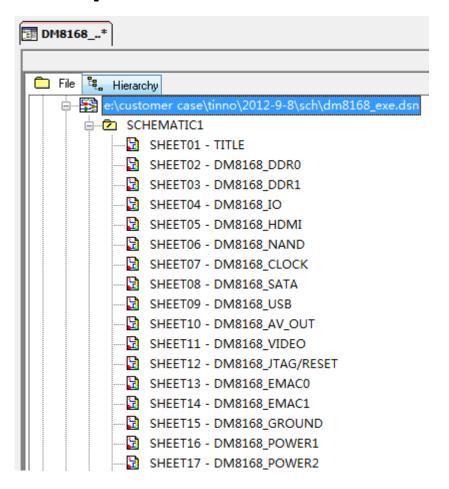


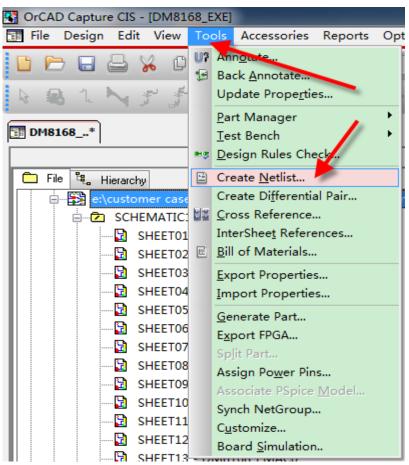






Capture CIS第三方网表导出/导入

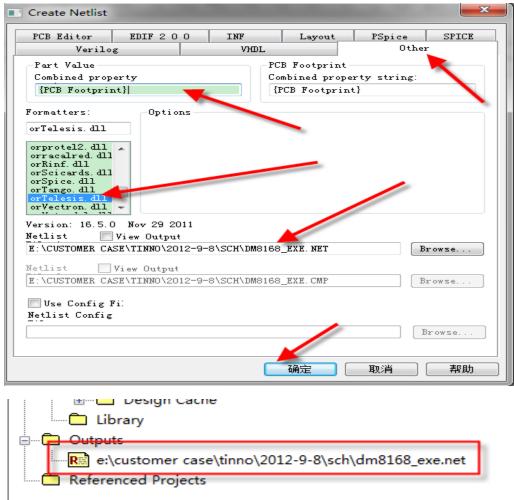








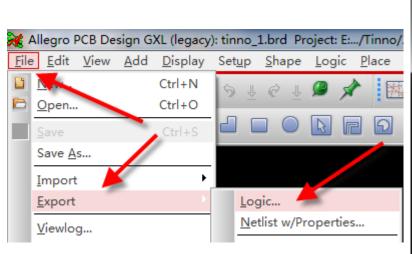
Capture CIS第三方网表导出/导入

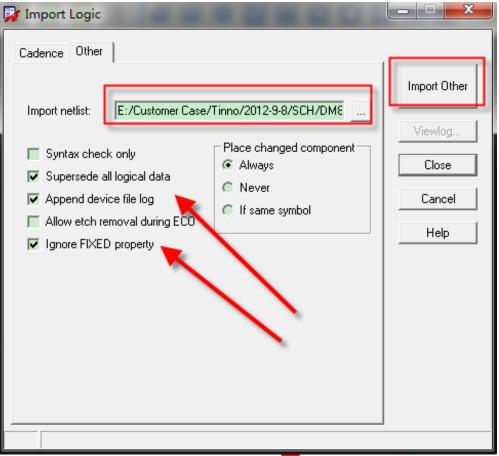






Capture CIS第三方网表导出/导入



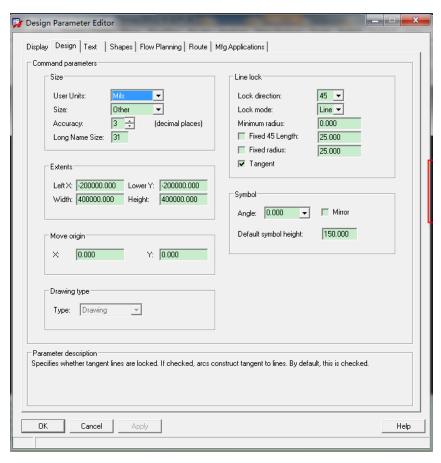






PCB 设计前处理——建立板框

- 手动绘制
 - Setup Design Parameter Editor







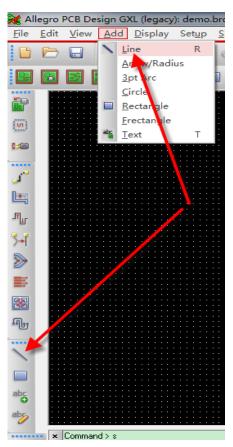
- 手动绘制
 - 设置格点

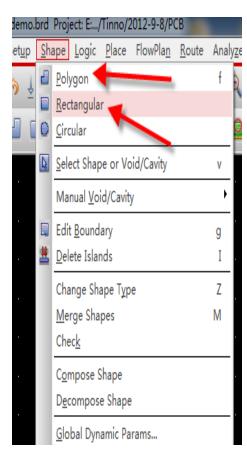


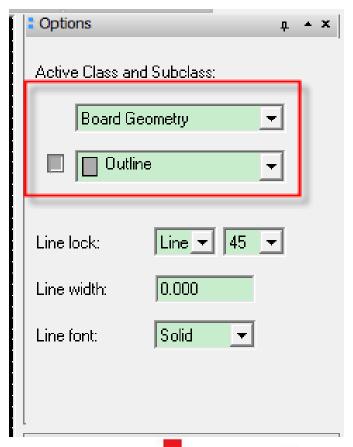




- 手动绘制
 - 创建板框



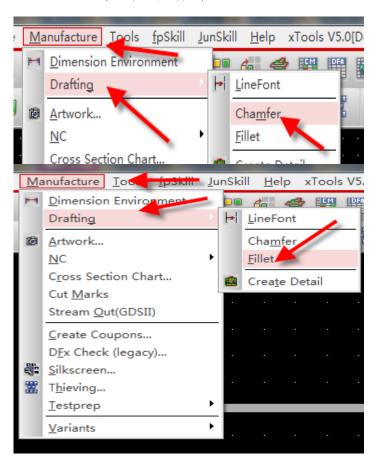


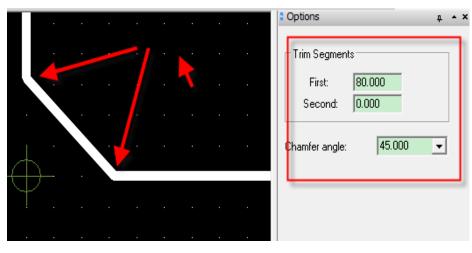






- 手动绘制
 - 板框倒角



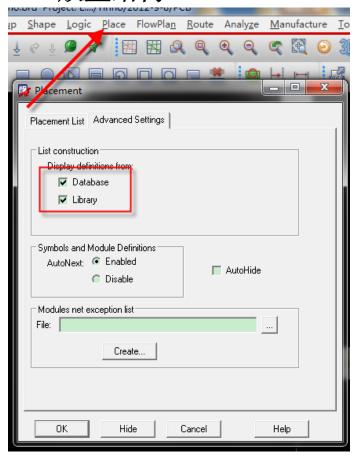


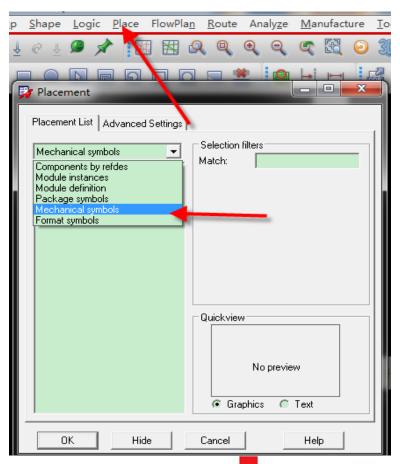






- 手动绘制
 - 放置结构

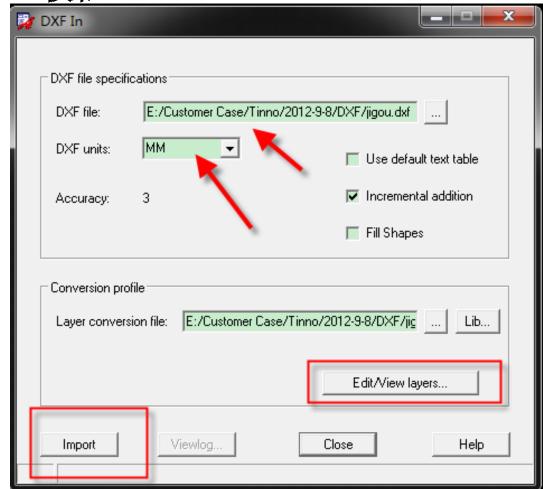








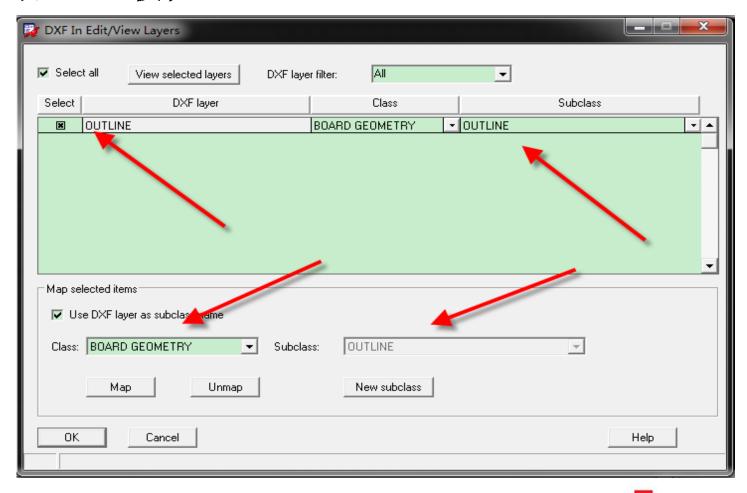
· 导入DXF板框







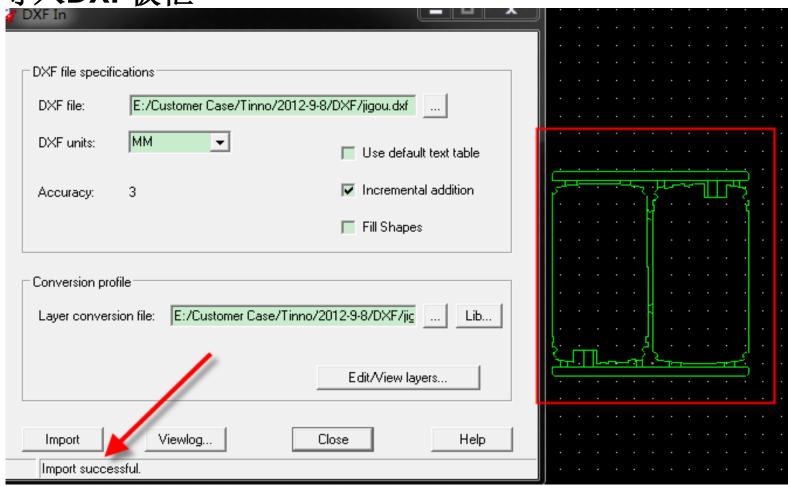
· 导入DXF板框







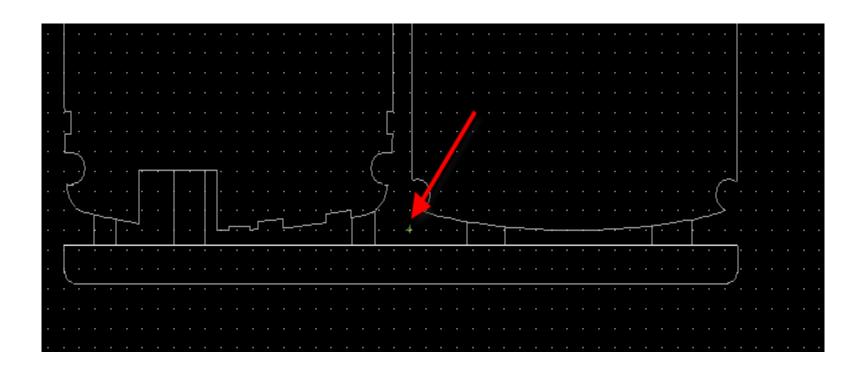
·导入DXF板框







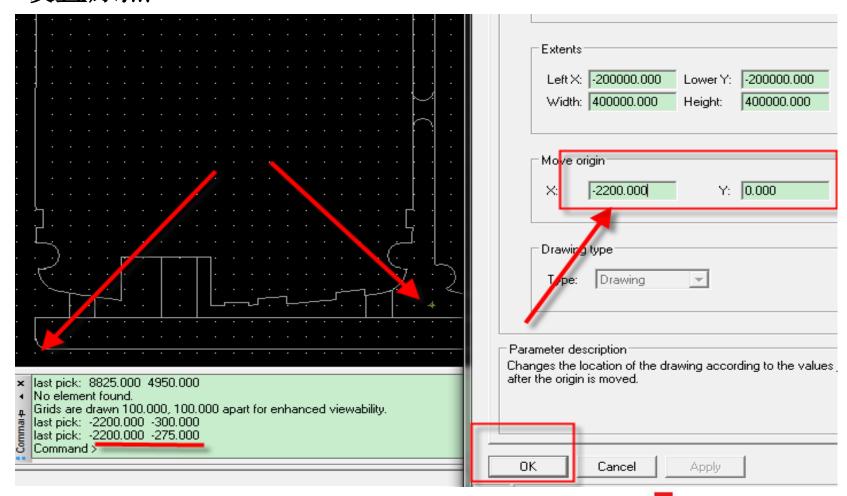
• 设置原点







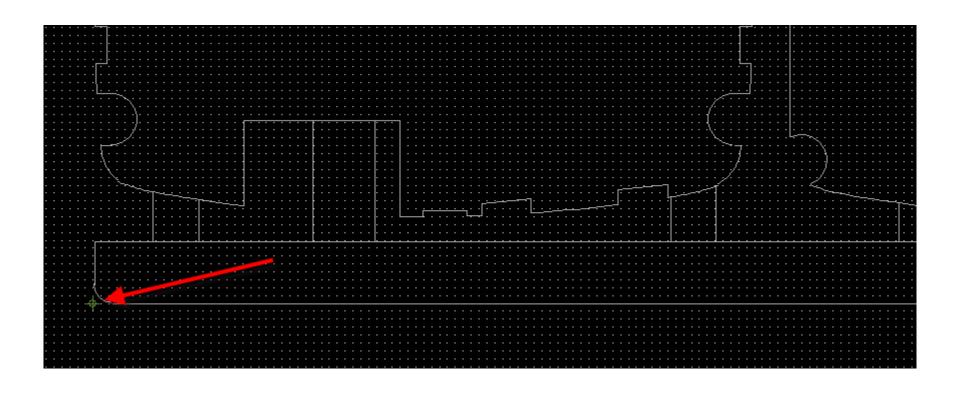
• 设置原点







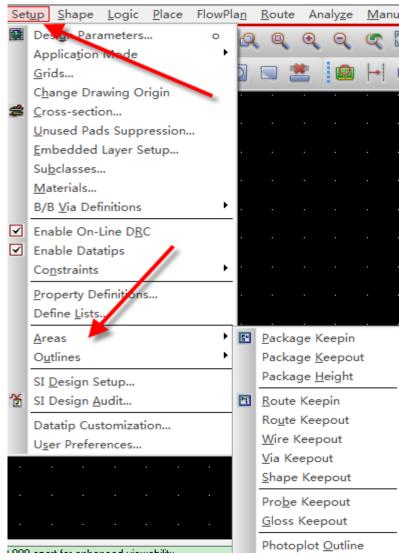
• 设置原点







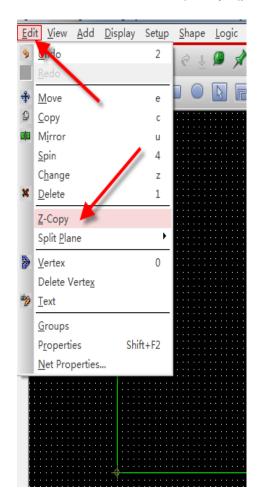
• 添加禁布区

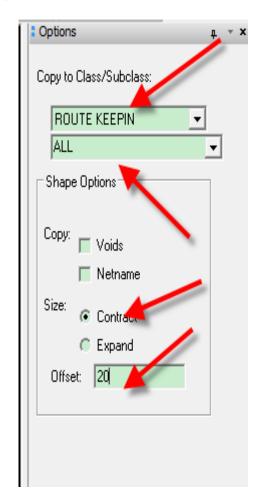


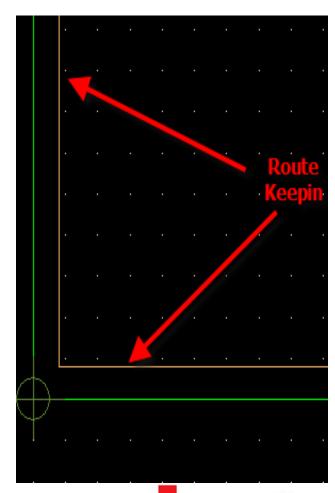




· Z-COPY命令使用



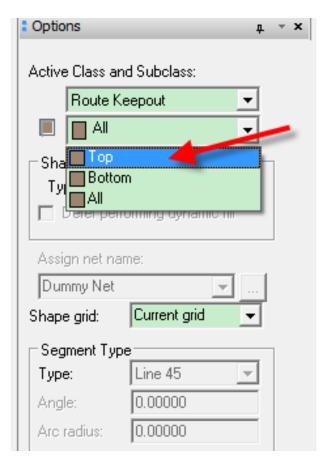


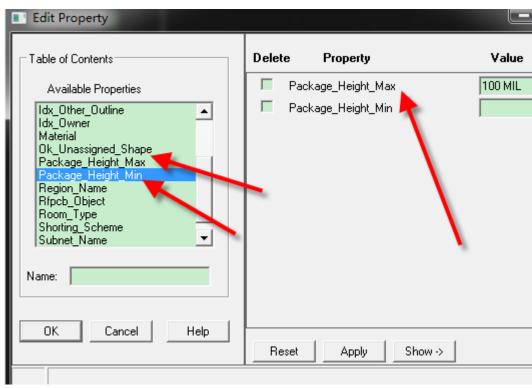






• 禁布区分层添加、限高区域添加

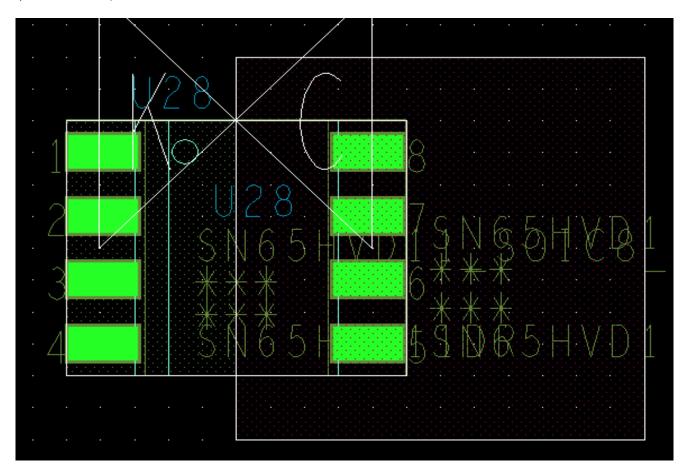








· 禁布DRC检查





Q&A



- Q&A
- Summary





Thank you!

SEP 8, 2012
By: Ausben Du
ausbendu@comtech.com.cn

