cadence

INVENTIVE

Allegro Constraint Manager

------Channel Partner COMTECH 科通

内容提要

- 约束管理器（**Constraint Manager**）介绍
- 物理约束 与间距约束
  - **Physical Constraint & Spacing Constraint —**介绍
  - 物理约束（**Physical Constraint**）
  - 间距约束（**Spacing Constraint**）
  - **Same Net Spacing Constraint**
  - 区域约束（**Region Constraint**）
  - **Net**属性
  - **Component**属性和**Pin**属性
  - **DRC**工作表
- 电气约束（**Electrical Constraint**）
  - **Relative Propagation Delay**工作表
  - **Differential Pair** 工作表
  - **Differential Pair**示例

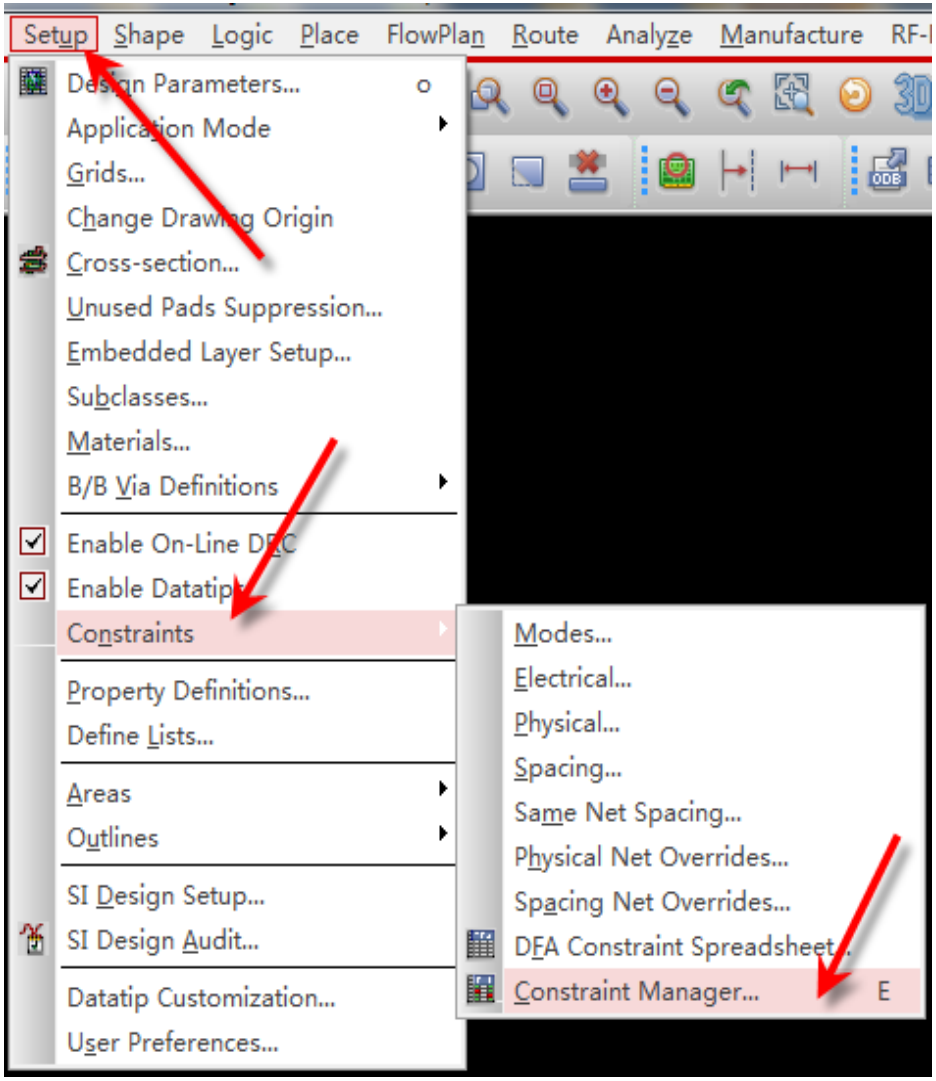
约束管理器（Constraint Manager）介绍

- 约束管理器(CM)是一个交叉的平台，以工作薄和工作表的形式管理Cadence PCB和IC Package设计流程中的所有工具的约束。

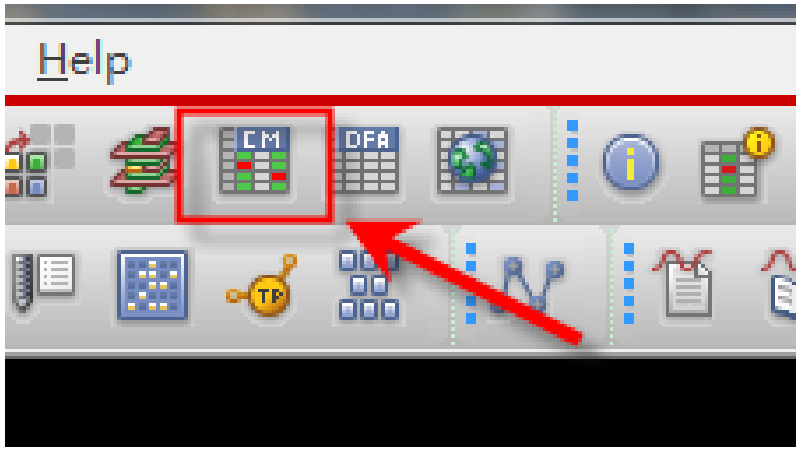
- 用户可以通过约束管理器在设计流程中的任意一个环节进行约束定义、查看和验证。

- 当约束设置完成后，PCB工具会自动根据定义 的约束对设计进行检查，不合符约束的地方会用DRC Markers 标记出来。

约束管理器（Constraint Manager）介绍



进入CM



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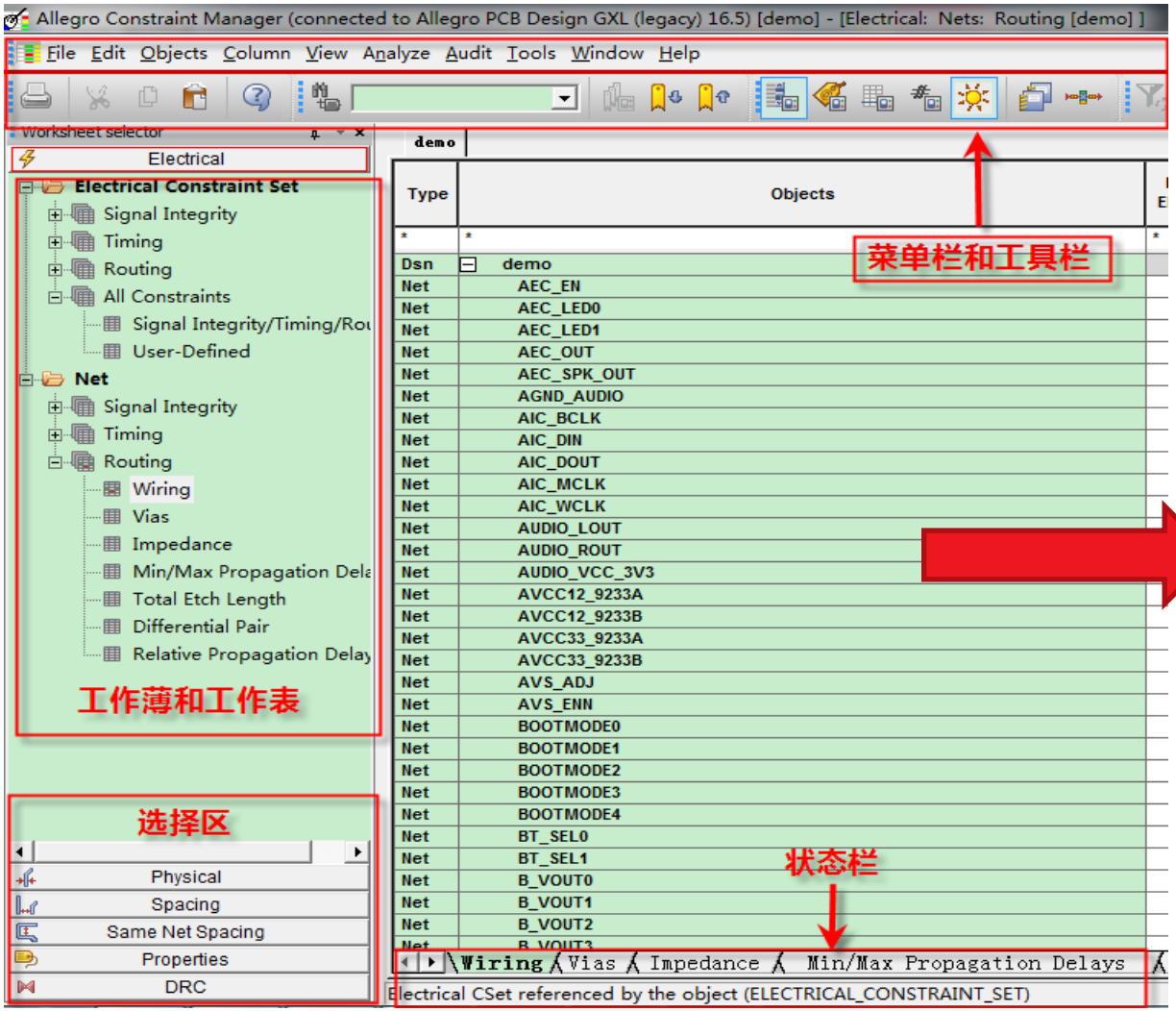

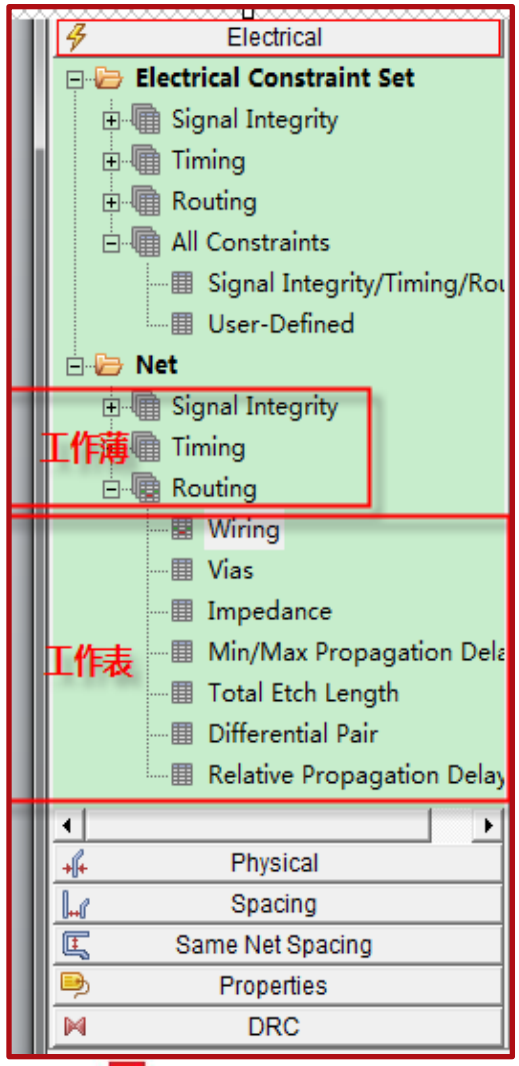

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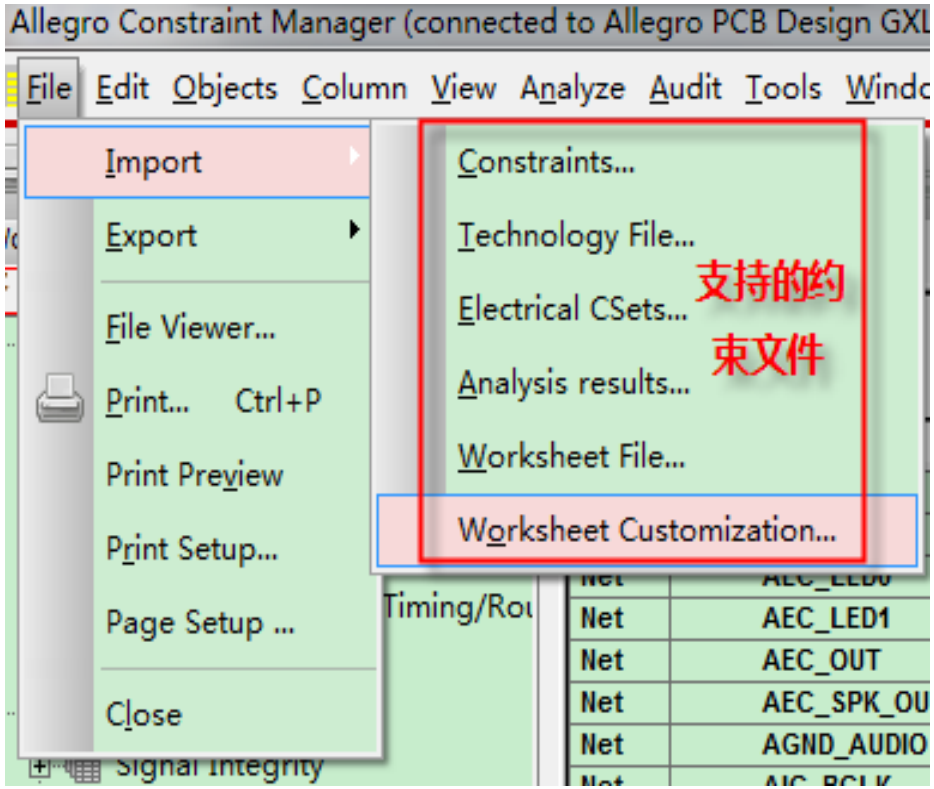
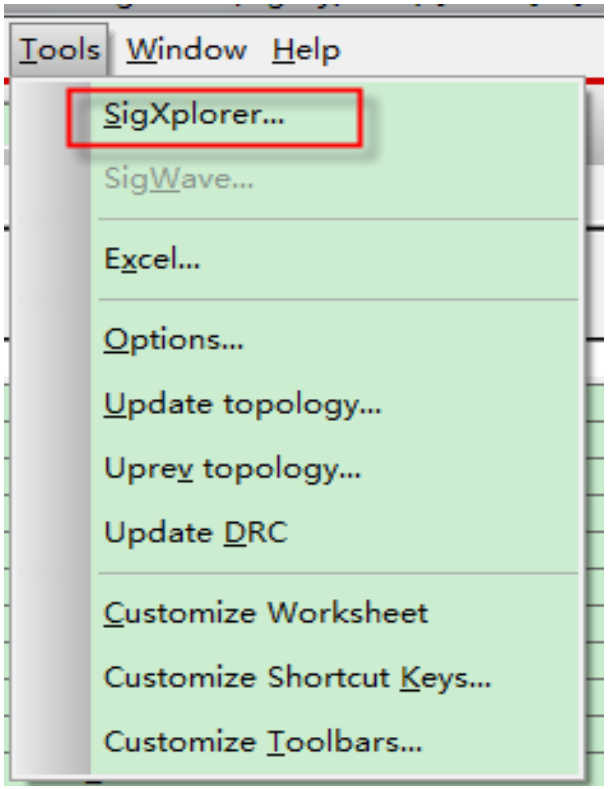
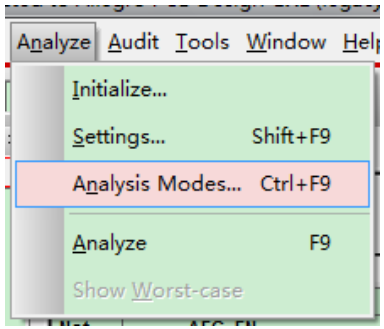
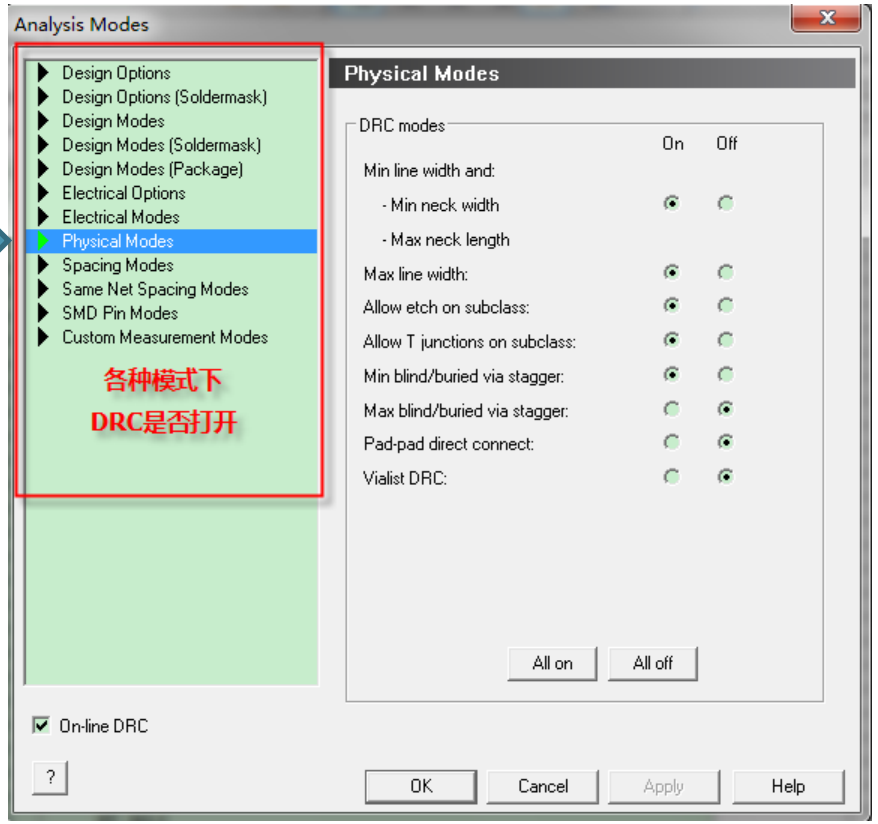
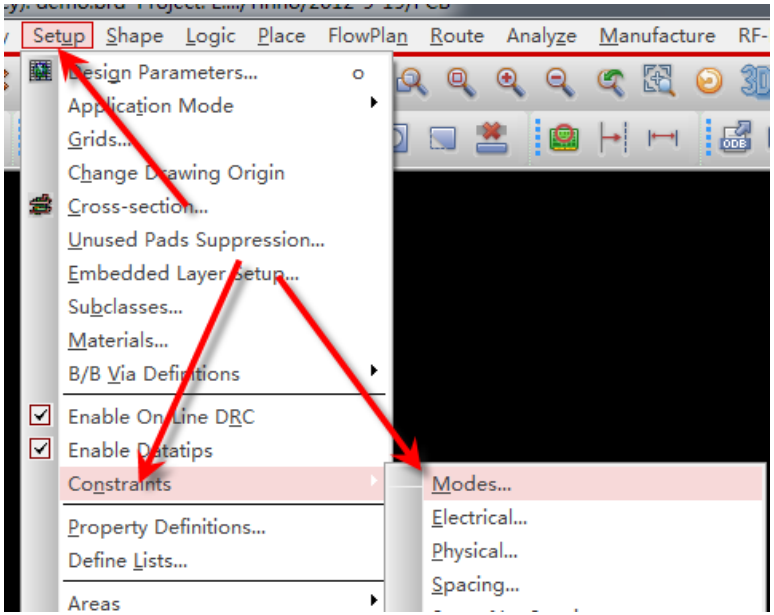




约束管理器（Constraint Manager）介绍







物理约束与间距约束——介绍

- 有四类关于Net的设计约束与规则:
  - 物理约束（*Physical Constraint*）
    - Line（布线）线宽和Layer（层）约束
  - 间距约束（*Spacing Constraint*）
    - 不同Net（网络）的Lines、Pads、Vias、Shapes之间的间距
  - 相同网络间距约束（*Same Net Spacing Constraint*）
    - 相同Net的Lines、Pads、Vias、Shapes之间的间距
  - 电气约束（*Electrical Constraint*）
    - 管理电路信号特性（Cross Talk、Delay…）
- 对于物理和间距规则主要分两类:
  - 默认规则（*Default*规则）
  - 扩展规则

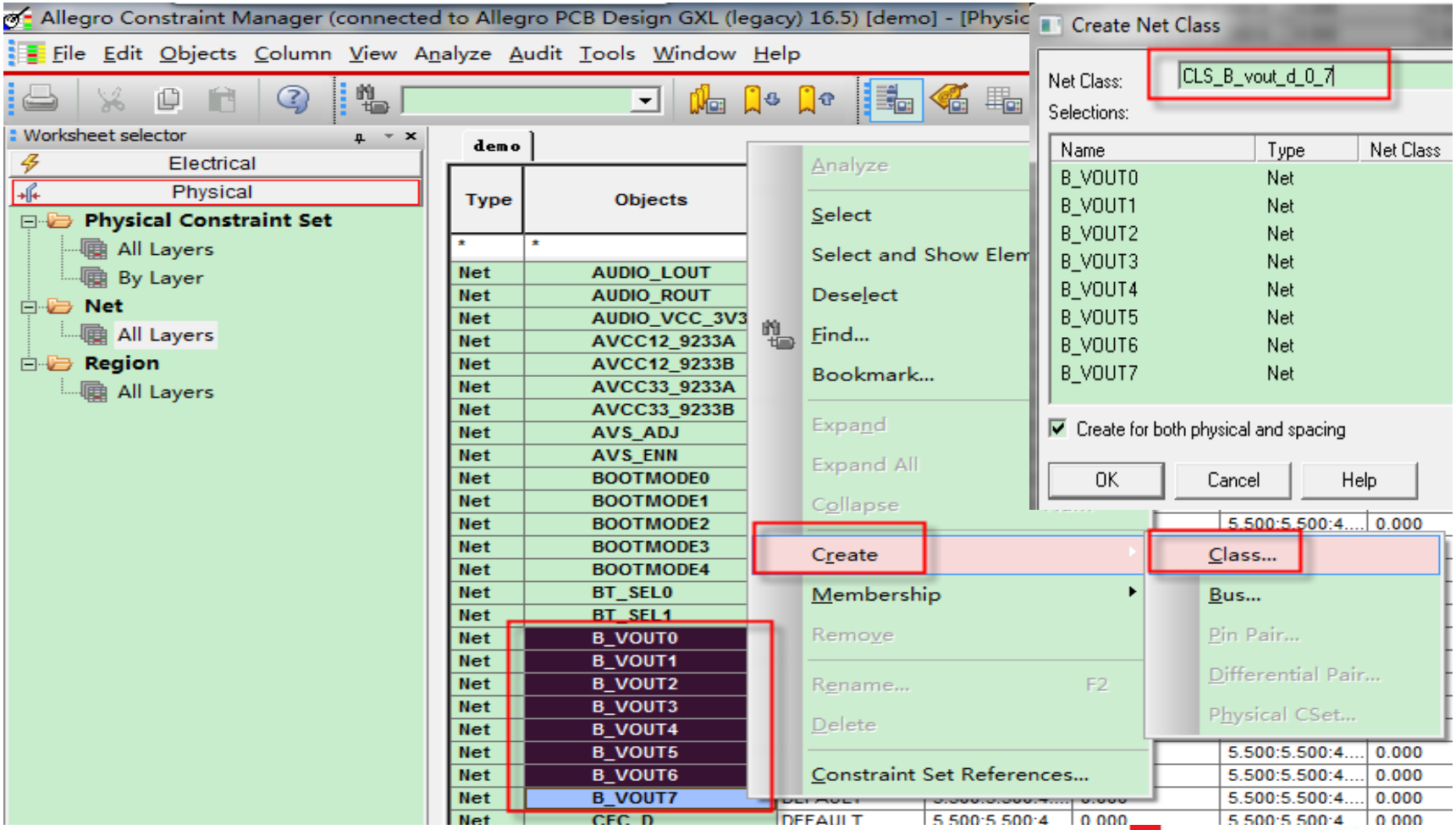
物理约束与间距约束——介绍

- 在设计的初期，**Allegro PCB Editor将Physical、Spacing、Same Net Spacing的Default规则赋予了设计中的所有网络。**

- 若设计中有些**Net**的设计规则要不同于**Default**规则，用户需要先创建包含这些网络的**Net Class**，再建立扩展的**Physical、Spacing、Same Net Spacing**约束，最后将这些扩展的约束赋予**Net Class**。

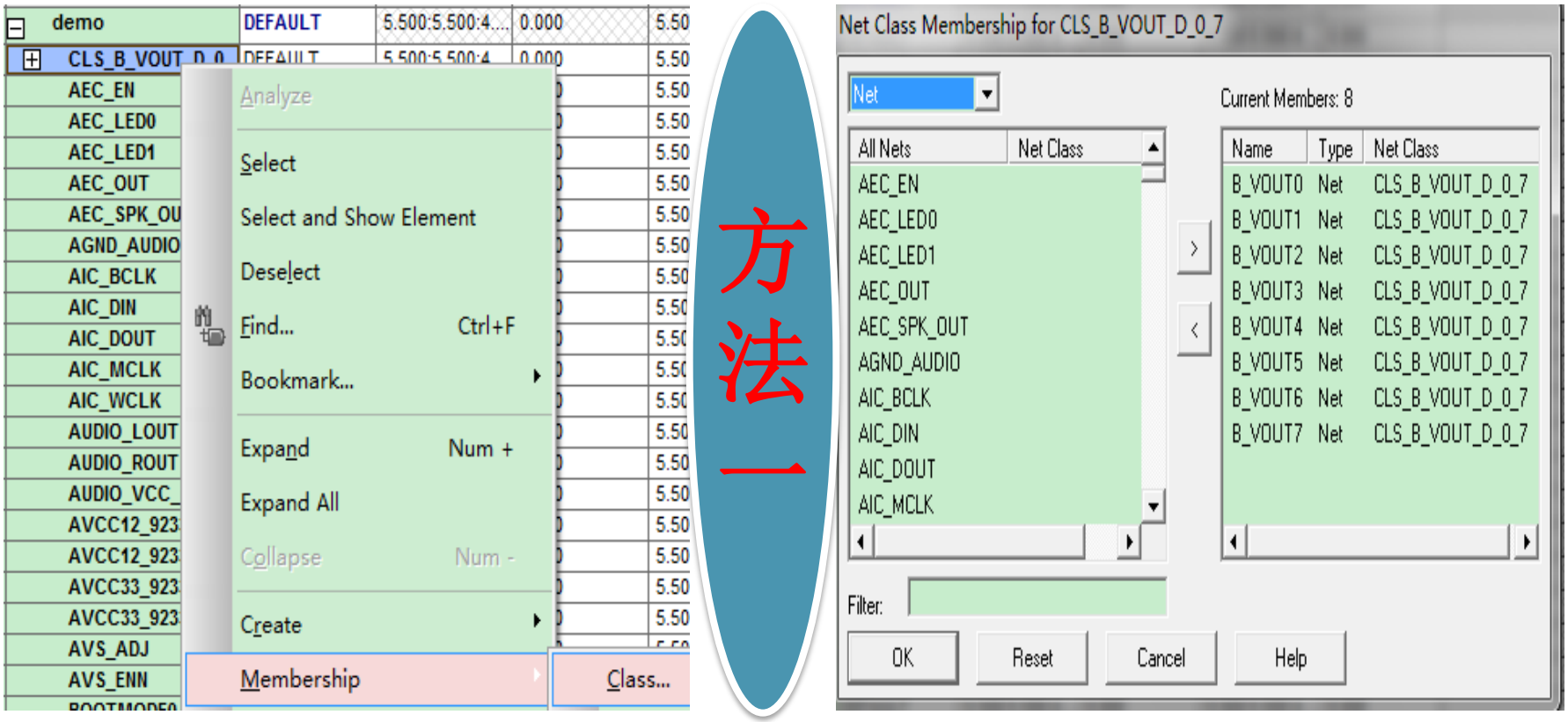
物理约束（Physical Constraint）

- 建立Net Class



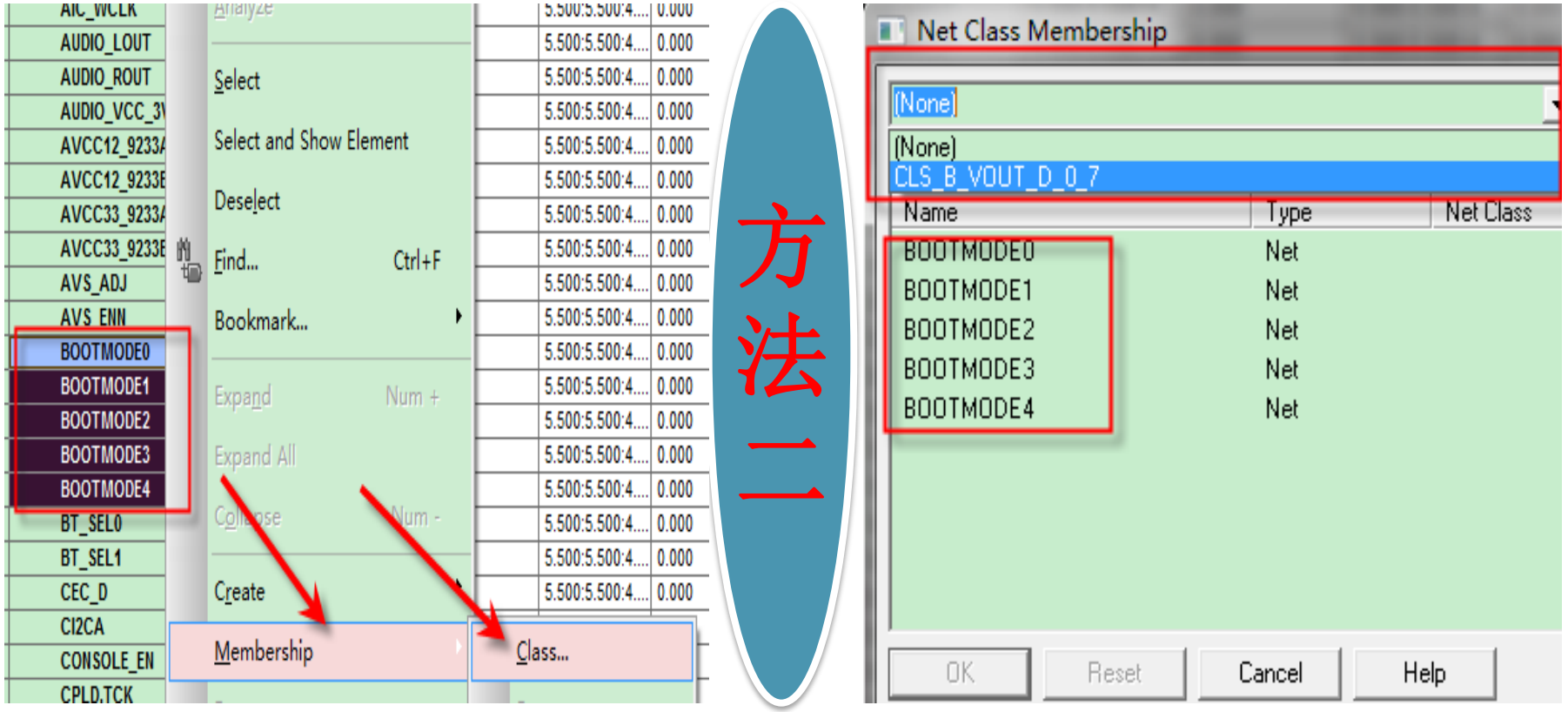
物理约束（Physical Constraint）

- 为Class添加对象（Assigning Objects to Classes）



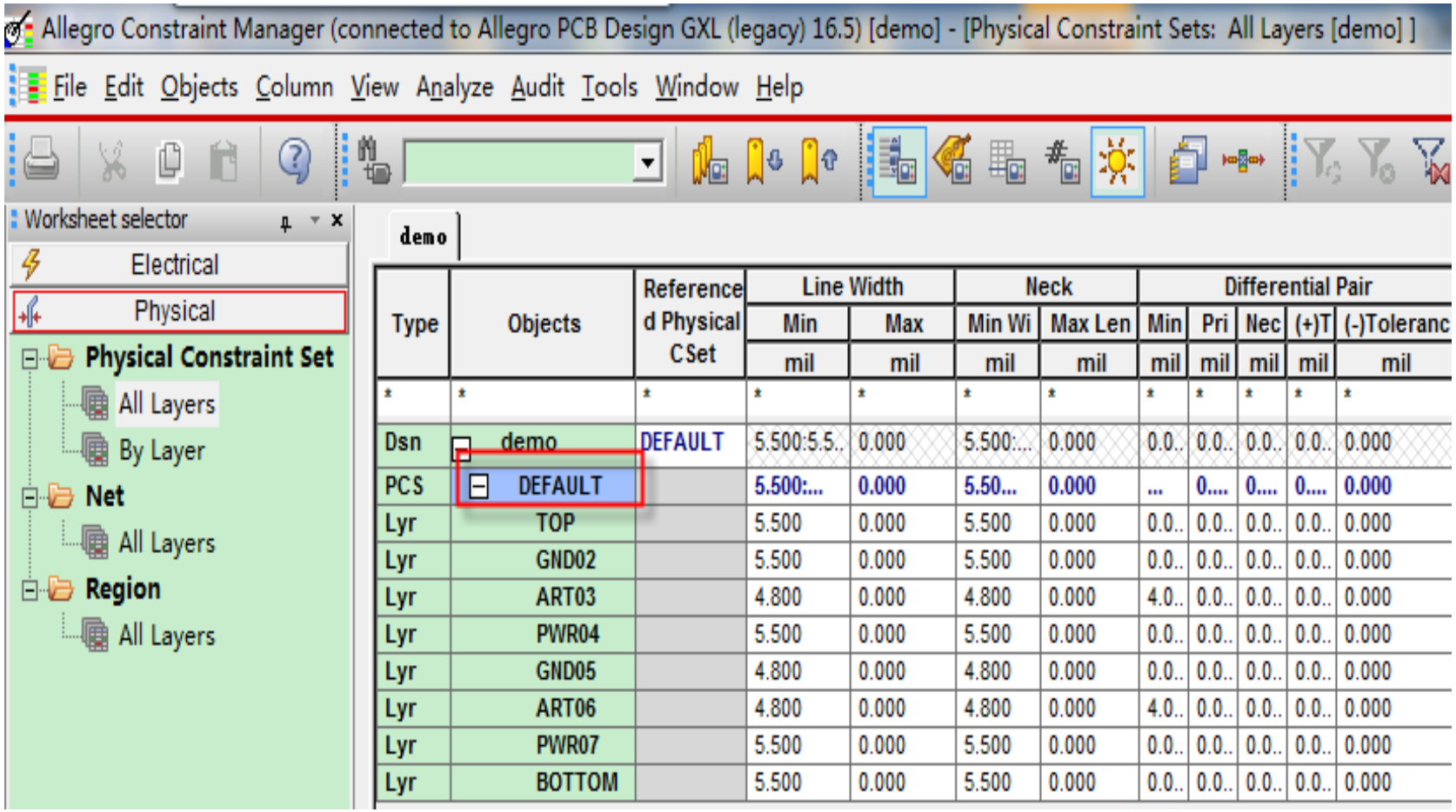
物理约束（Physical Constraint）

- 为Class添加对象（Assigning Objects to Classes）



物理约束（Physical Constraint）

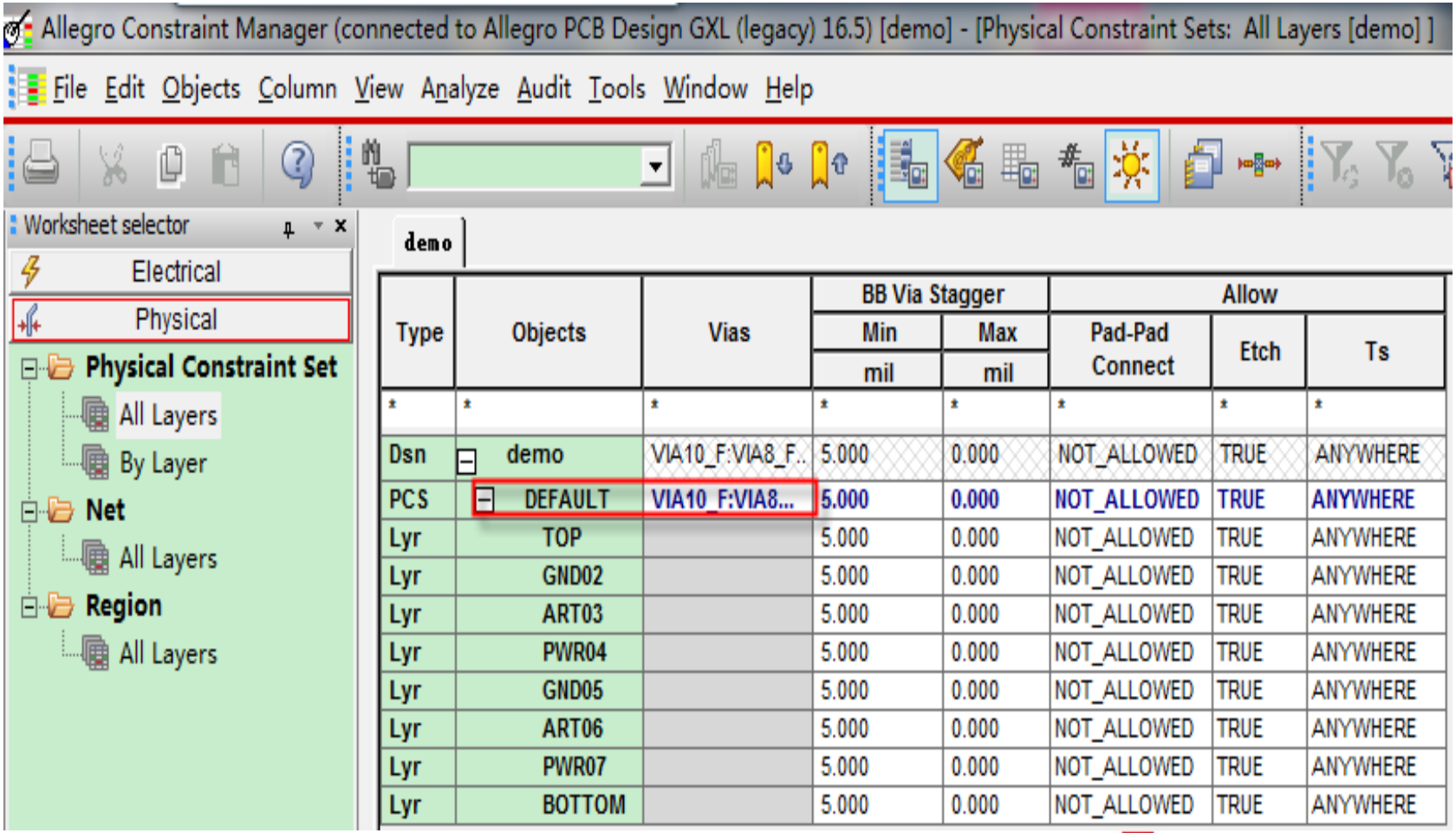
- 设置Default约束



Type	Objects	Referenced Physical CSet	Line Width Min	Line Width Max	Neck Min Wi	Neck Max Len	Differential Pair Min	Differential Pair Pri	Differential Pair Nec	Differential Pair (+)T	Differential Pair (-)Toleranc
			mil	mil	mil	mil	mil	mil	mil	mil	mil
*	*	*	*	*	*	*	*	*	*	*	*
Dsn	demo	DEFAULT	5.500:5.5..	0.000	5.500:...	0.000	0.0..	0.0..	0.0..	0.0..	0.000
PCS	DEFAULT		5.500:...	0.000	5.50...	0.000	...	0....	0....	0....	0.000
Lyr	TOP		5.500	0.000	5.500	0.000	0.0..	0.0..	0.0..	0.0..	0.000
Lyr	GND02		5.500	0.000	5.500	0.000	0.0..	0.0..	0.0..	0.0..	0.000
Lyr	ART03		4.800	0.000	4.800	0.000	4.0..	0.0..	0.0..	0.0..	0.000
Lyr	PWR04		5.500	0.000	5.500	0.000	0.0..	0.0..	0.0..	0.0..	0.000
Lyr	GND05		4.800	0.000	4.800	0.000	0.0..	0.0..	0.0..	0.0..	0.000
Lyr	ART06		4.800	0.000	4.800	0.000	4.0..	0.0..	0.0..	0.0..	0.000
Lyr	PWR07		5.500	0.000	5.500	0.000	0.0..	0.0..	0.0..	0.0..	0.000
Lyr	BOTTOM		5.500	0.000	5.500	0.000	0.0..	0.0..	0.0..	0.0..	0.000

物理约束（Physical Constraint）

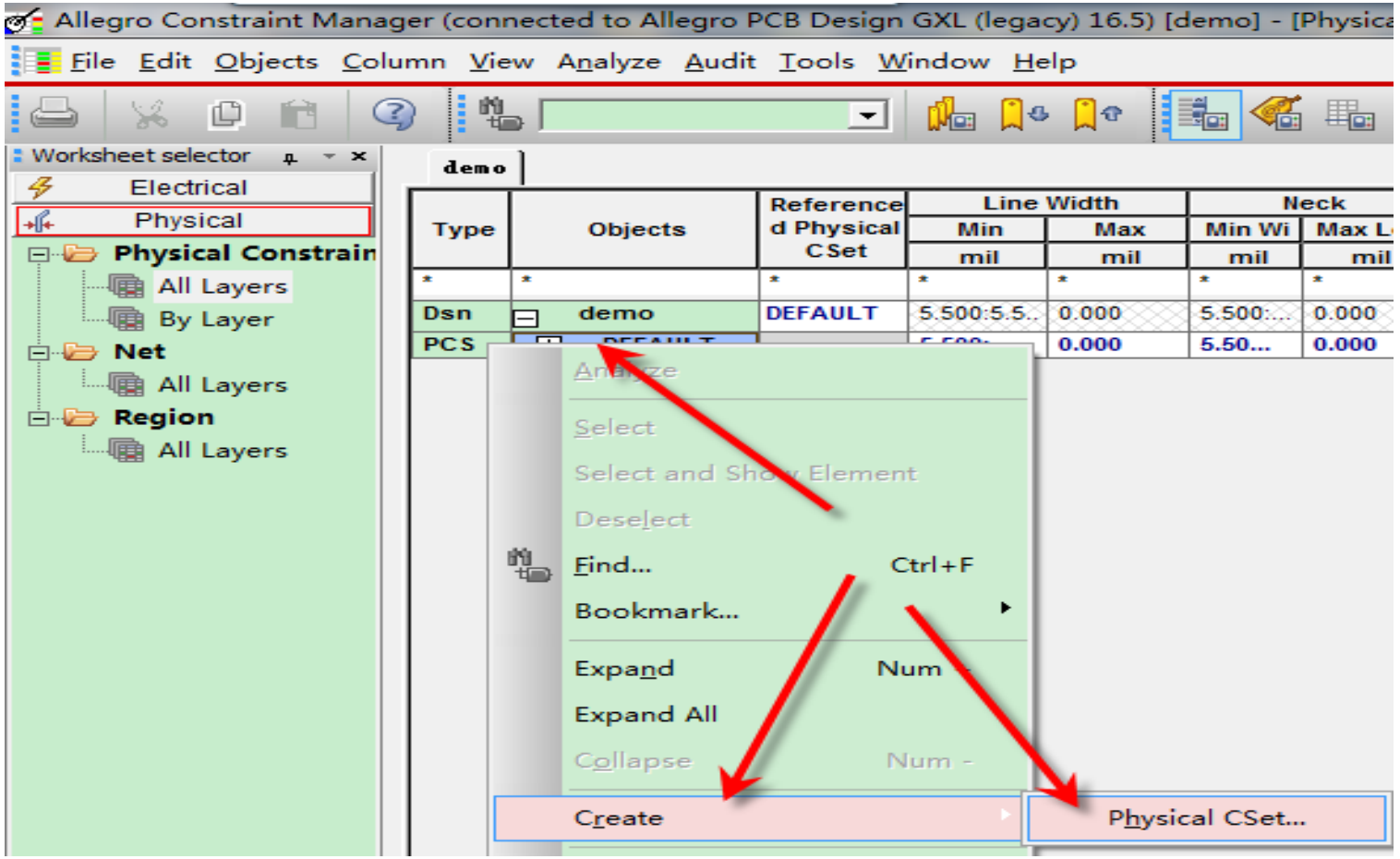
- 设置Default约束



Type	Objects	Vias	BB Via Stagger		Allow		
			Min	Max	Pad-Pad Connect	Etch	Ts
			mil	mil			
*	*	*	*	*	*	*	*
Dsn	demo	VIA10_F:VIA8_F..	5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE
PCS	DEFAULT	VIA10_F:VIA8...	5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE
Lyr	TOP		5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE
Lyr	GND02		5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE
Lyr	ART03		5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE
Lyr	PWR04		5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE
Lyr	GND05		5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE
Lyr	ART06		5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE
Lyr	PWR07		5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE
Lyr	BOTTOM		5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE

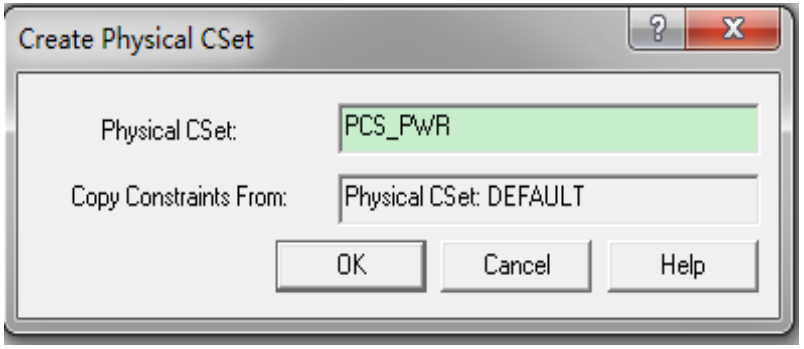
物理约束（Physical Constraint）

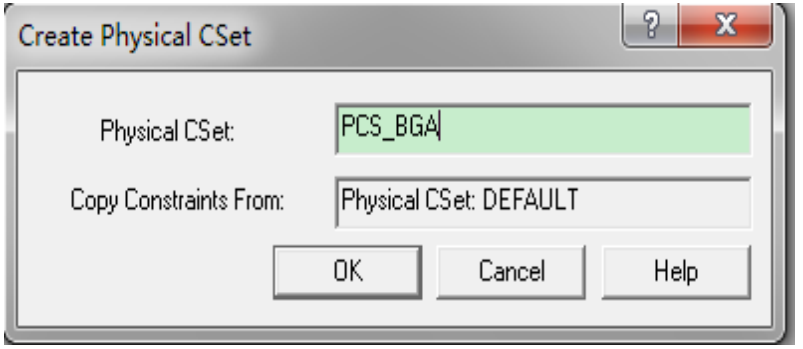
- 建立扩展Physical约束

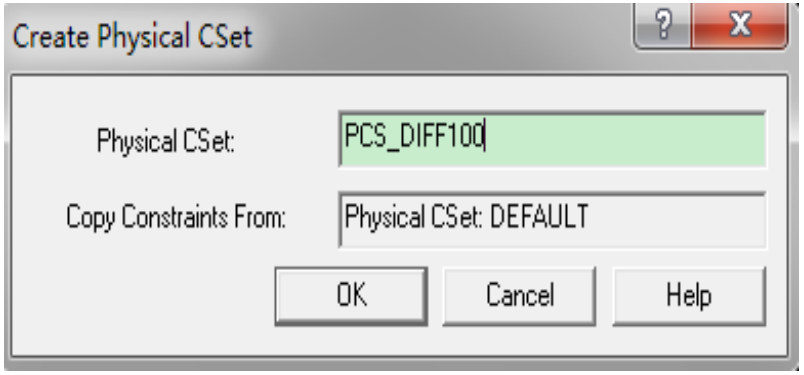


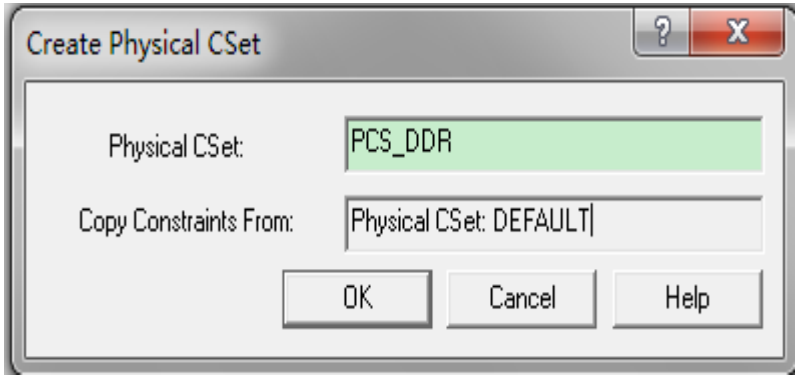
物理约束（Physical Constraint）

- 建立扩展Physical约束



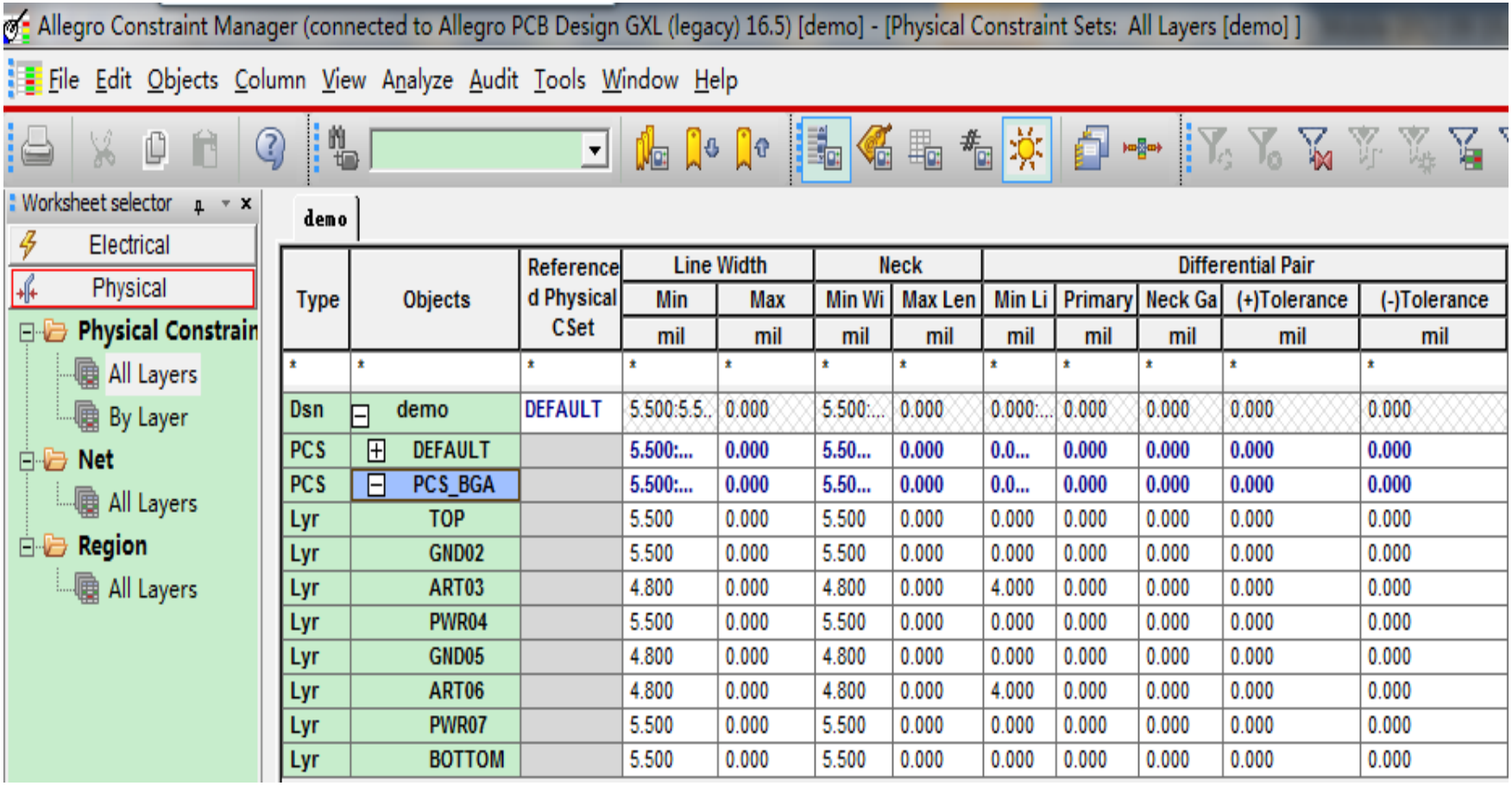






物理约束（Physical Constraint）

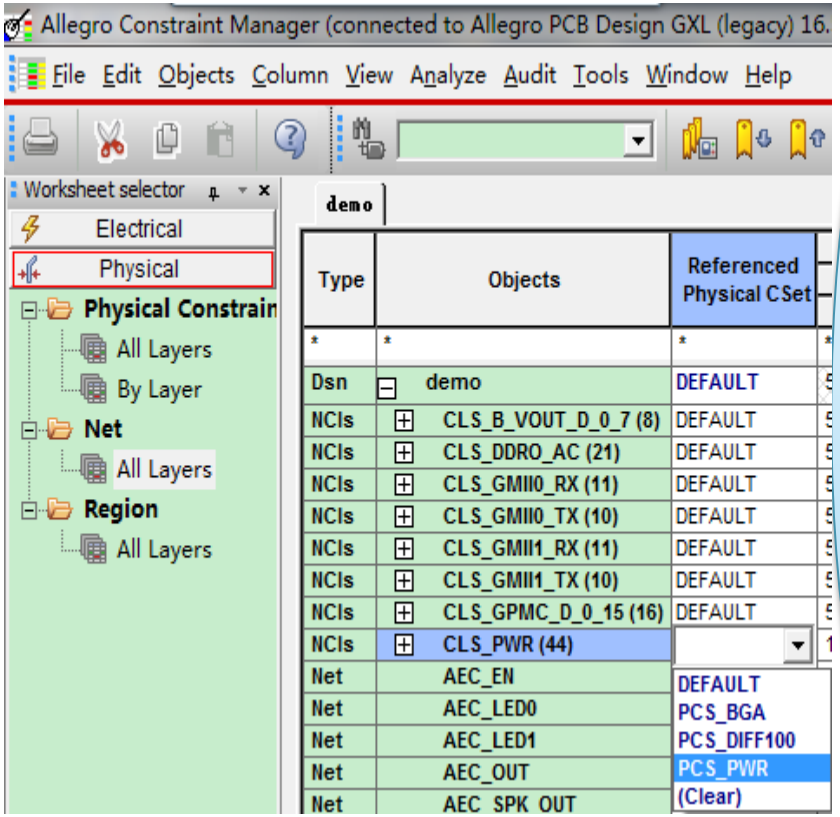
- 建立扩展Physical约束



Type	Objects	Referenced Physical CSet	Line Width		Neck		Differential Pair				
			Min	Max	Min Wi	Max Len	Min Li	Primary	Neck Ga	(+)Tolerance	(-)Tolerance
			mil	mil	mil	mil	mil	mil	mil	mil	mil
*	*	*	*	*	*	*	*	*	*	*	*
Dsn	demo	DEFAULT	5.500:5.5..	0.000	5.500:...	0.000	0.000:...	0.000	0.000	0.000	0.000
PCS	DEFAULT		5.500:...	0.000	5.50...	0.000	0.0...	0.000	0.000	0.000	0.000
PCS	PCS_BGA		5.500:...	0.000	5.50...	0.000	0.0...	0.000	0.000	0.000	0.000
Lyr	TOP		5.500	0.000	5.500	0.000	0.000	0.000	0.000	0.000	0.000
Lyr	GND02		5.500	0.000	5.500	0.000	0.000	0.000	0.000	0.000	0.000
Lyr	ART03		4.800	0.000	4.800	0.000	4.000	0.000	0.000	0.000	0.000
Lyr	PWR04		5.500	0.000	5.500	0.000	0.000	0.000	0.000	0.000	0.000
Lyr	GND05		4.800	0.000	4.800	0.000	0.000	0.000	0.000	0.000	0.000
Lyr	ART06		4.800	0.000	4.800	0.000	4.000	0.000	0.000	0.000	0.000
Lyr	PWR07		5.500	0.000	5.500	0.000	0.000	0.000	0.000	0.000	0.000
Lyr	BOTTOM		5.500	0.000	5.500	0.000	0.000	0.000	0.000	0.000	0.000

物理约束（Physical Constraint）

- 为Net Class添加 Physical约束

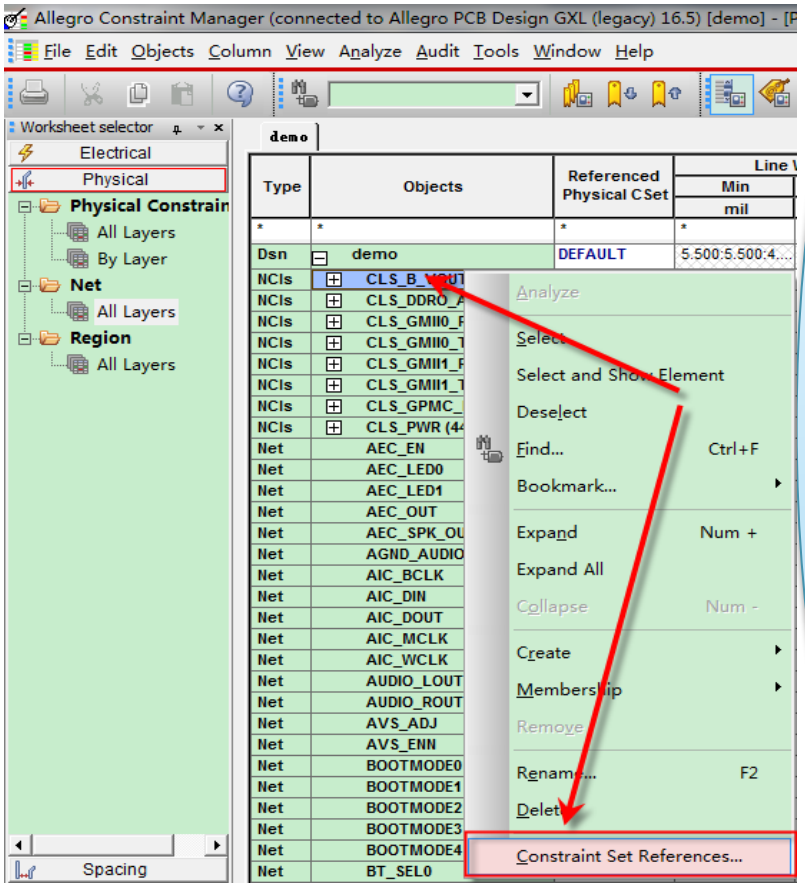


方法一

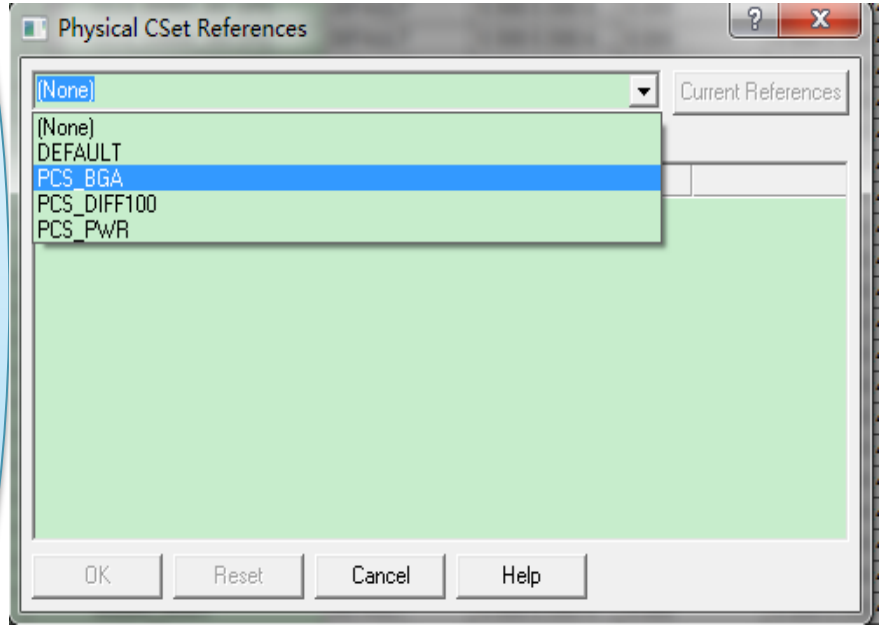
Type	Objects	Referenced Physical CSet	Line Width Min mil	Line Width Max mil
*	*	*	*	*
Dsn	demo	DEFAULT	5.500:5.500:4....	0.000
NCIs	CLS_B_VOUT_D_0_7 (8)	DEFAULT	5.500:5.500:4....	0.000
NCIs	CLS_DDRO_AC (21)	DEFAULT	5.500:5.500:4....	0.000
NCIs	CLS_GMII0_RX (11)	DEFAULT	5.500:5.500:4....	0.000
NCIs	CLS_GMII0_TX (10)	DEFAULT	5.500:5.500:4....	0.000
NCIs	CLS_GMII1_RX (11)	DEFAULT	5.500:5.500:4....	0.000
NCIs	CLS_GMII1_TX (10)	DEFAULT	5.500:5.500:4....	0.000
NCIs	CLS_GPMC_D_0_15 (16)	DEFAULT	5.500:5.500:4....	0.000
NCIs	CLS_PWR (44)	PCS_PWR	10.000	0.000

物理约束（Physical Constraint）

- 为Net Class添加 Physical约束

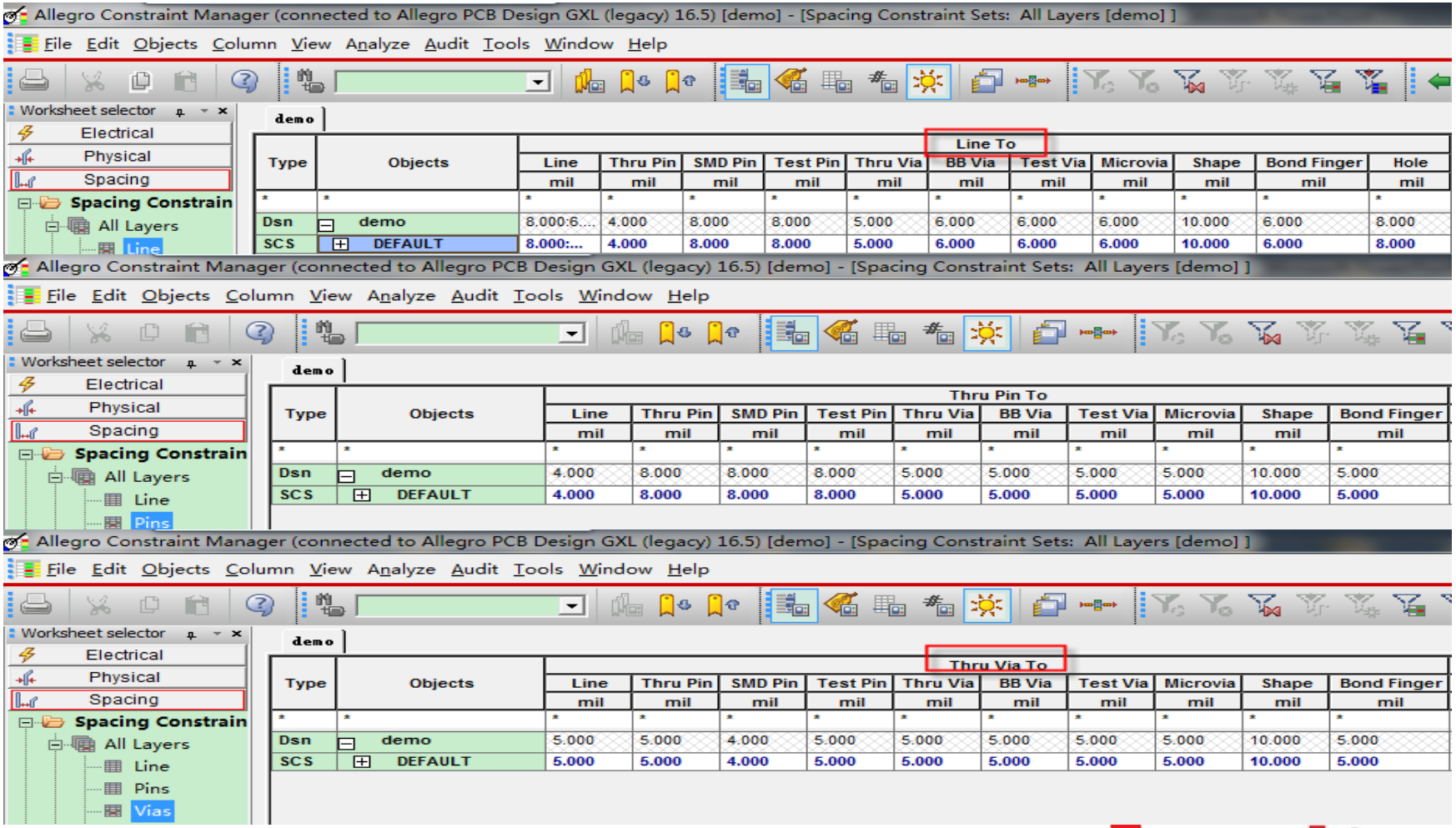


方法二



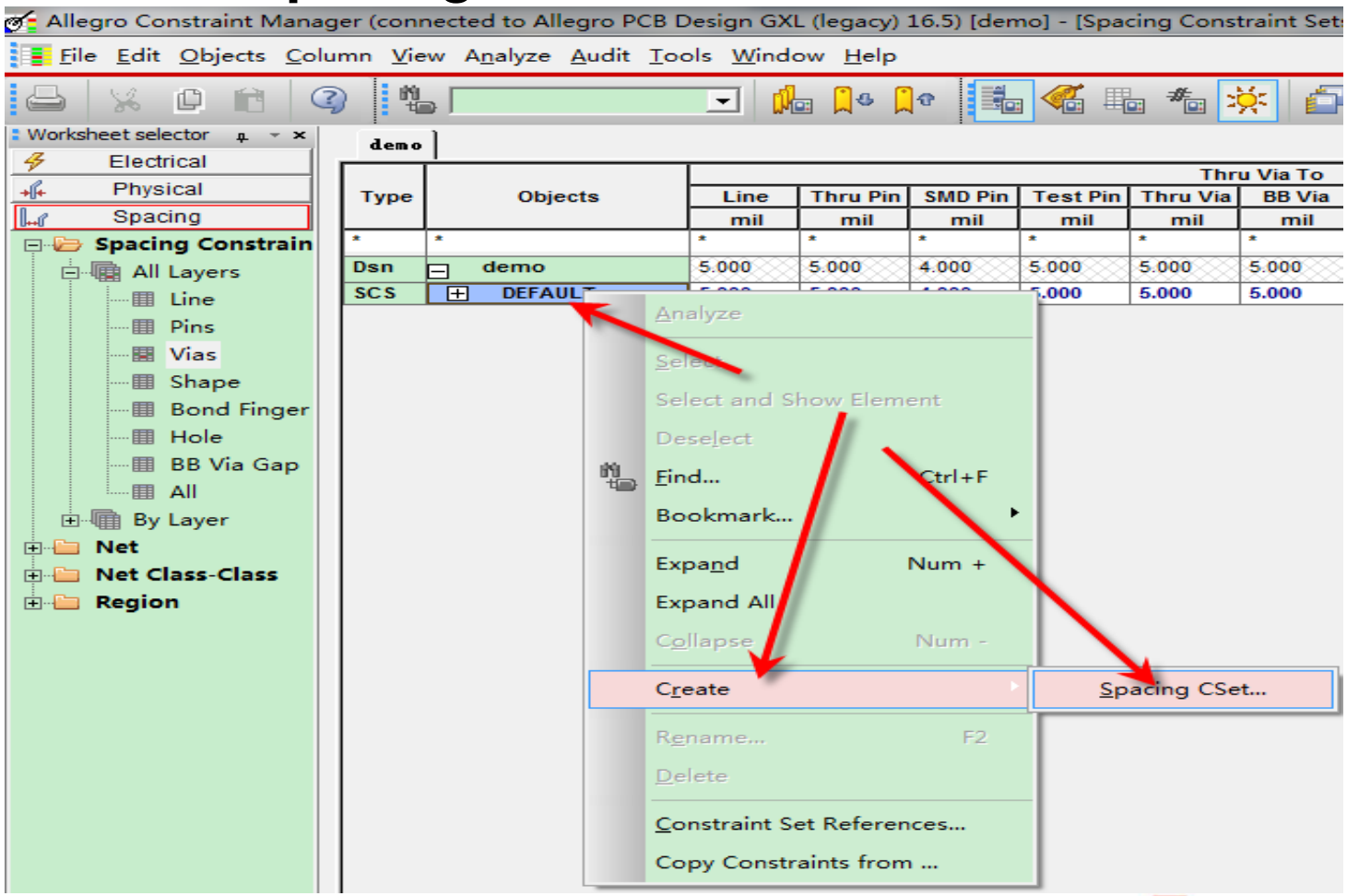
间距约束（Spacing Constraint）

- 设置Default约束



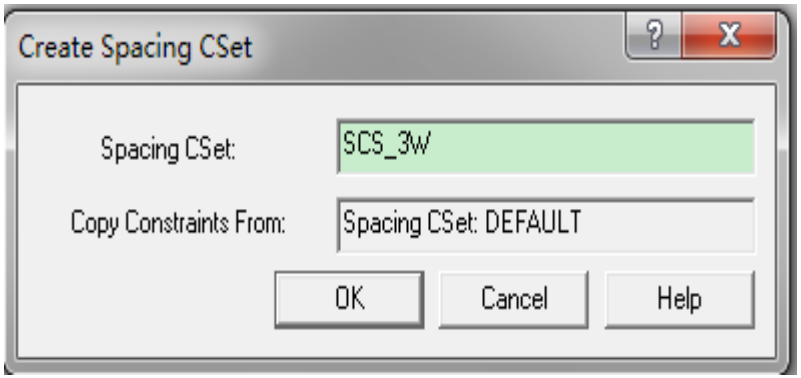
间距约束（Spacing Constraint）

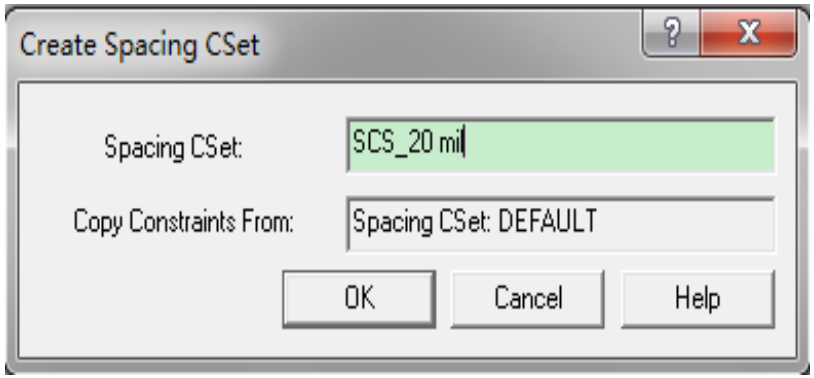
- 建立扩展Spacing约束

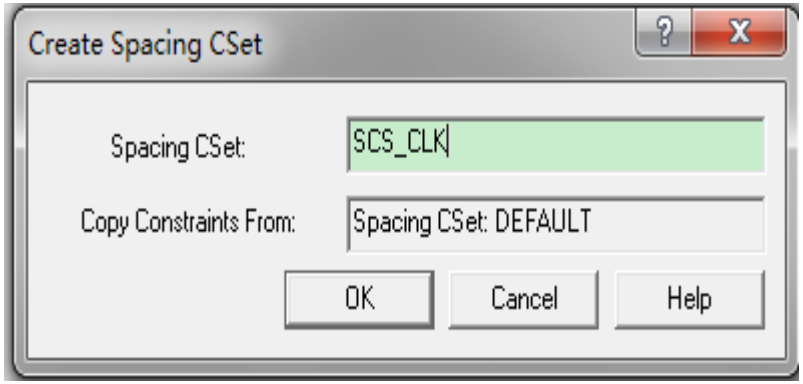


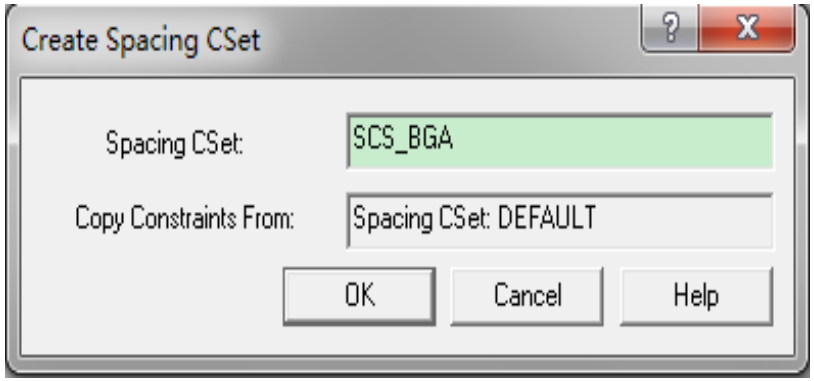
间距约束（Spacing Constraint）

- 建立扩展Spacing约束



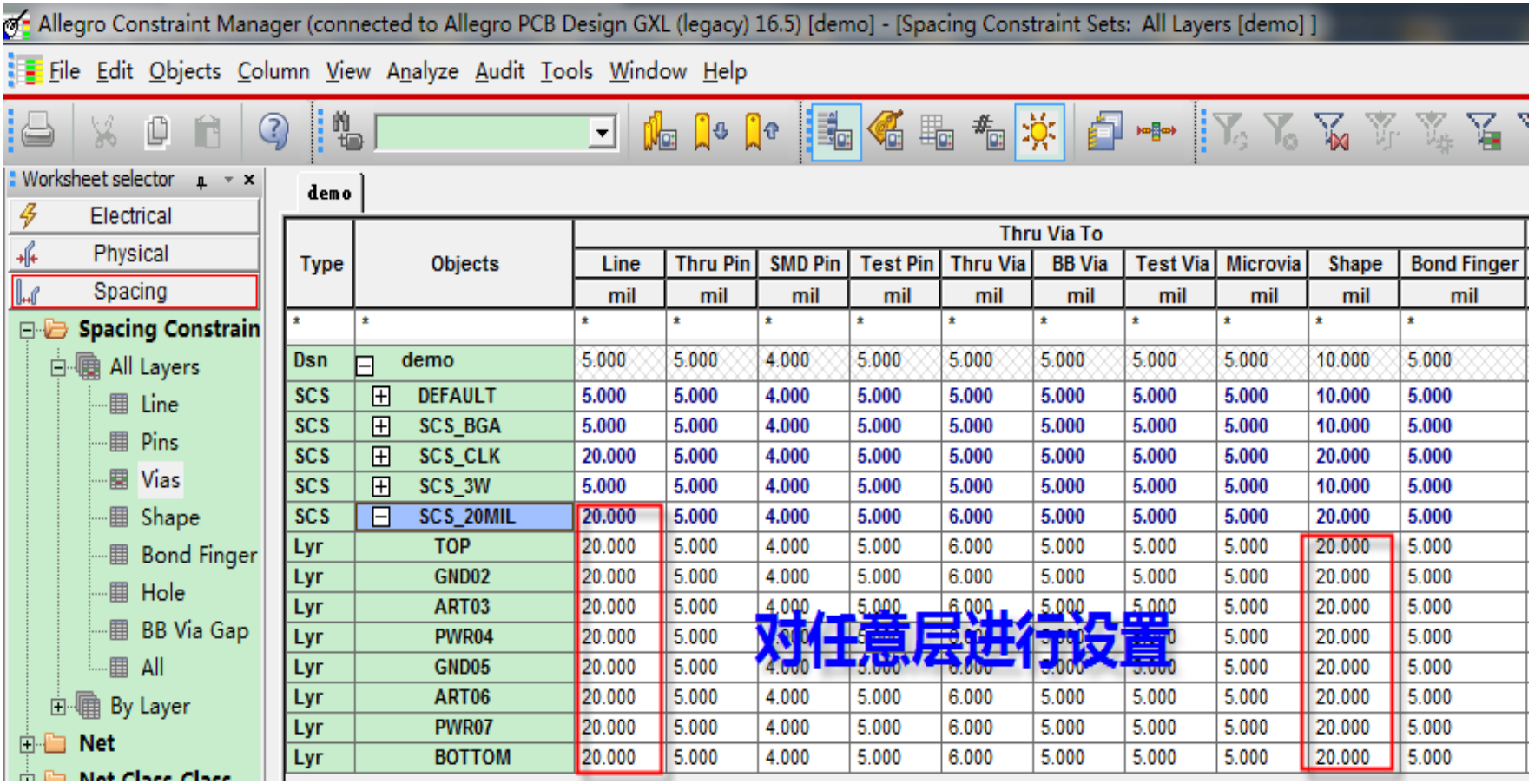






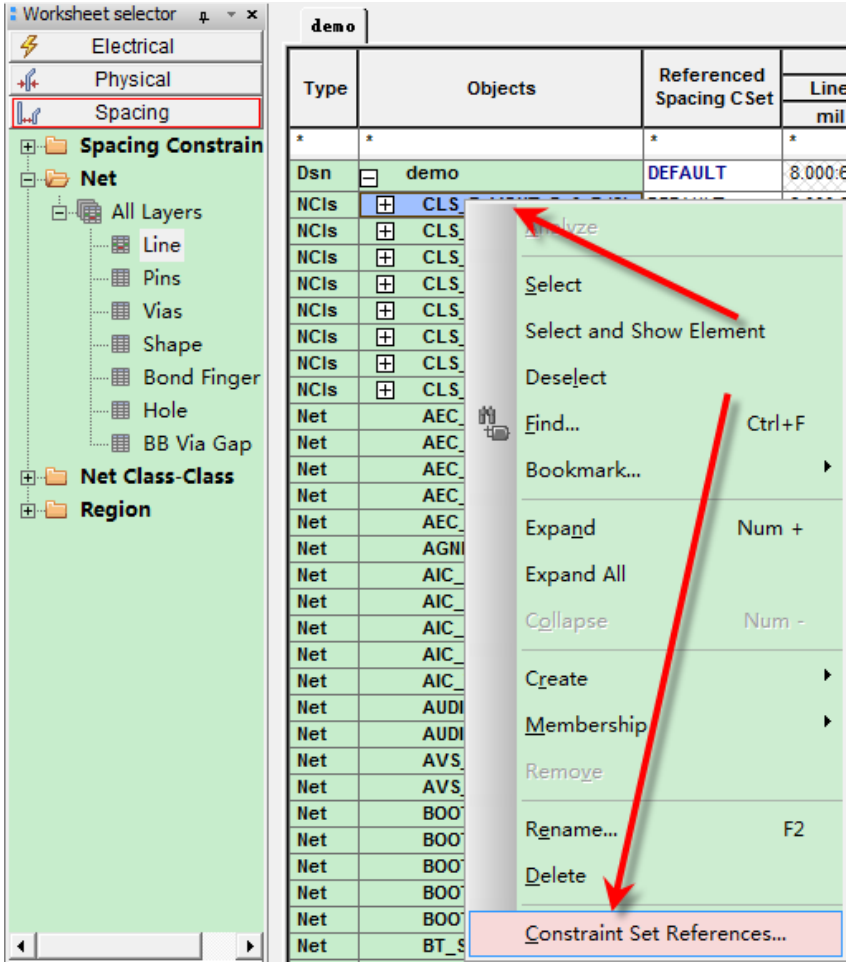
间距约束（Spacing Constraint）

- 建立扩展Spacing约束

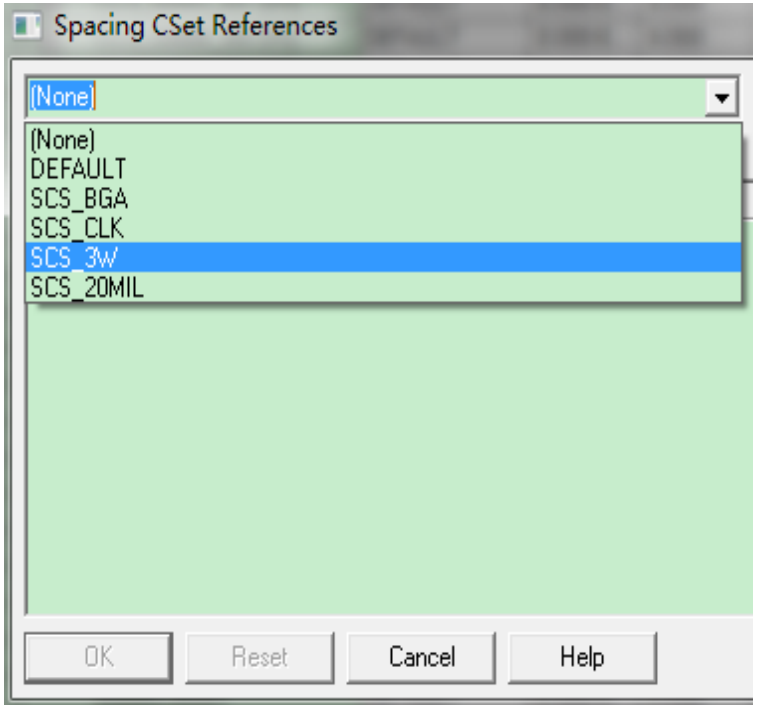


间距约束（Spacing Constraint）

- 为Net Class 添加 Spacing约束

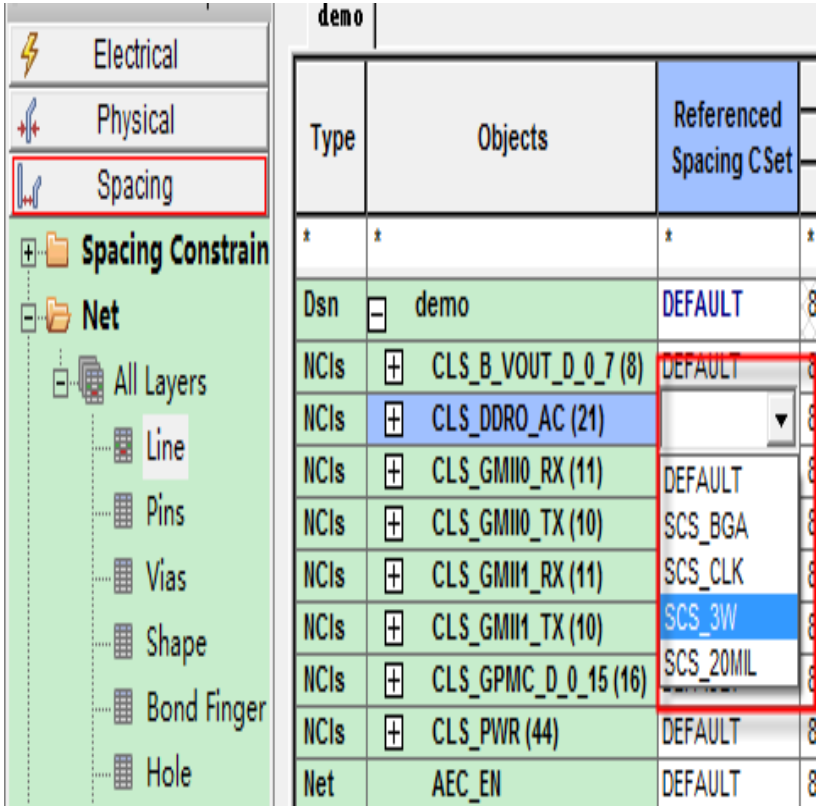


方法一



间距约束（Spacing Constraint）

- 为Net Class 添加 Spacing约束

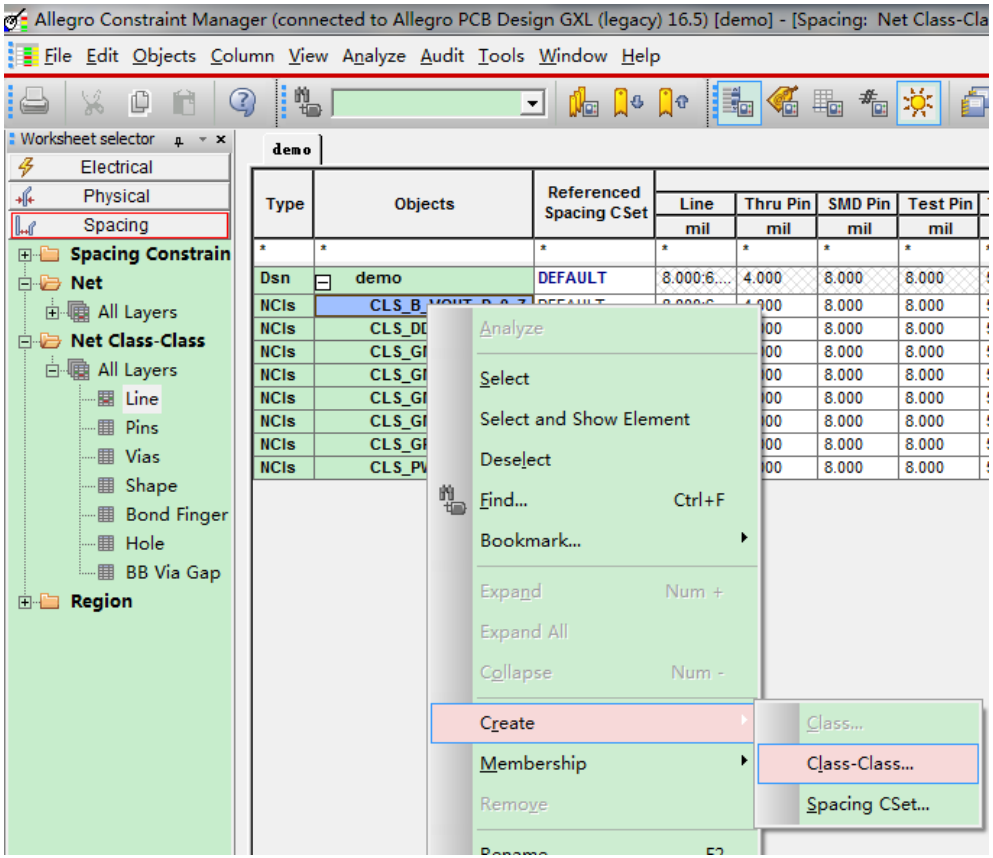


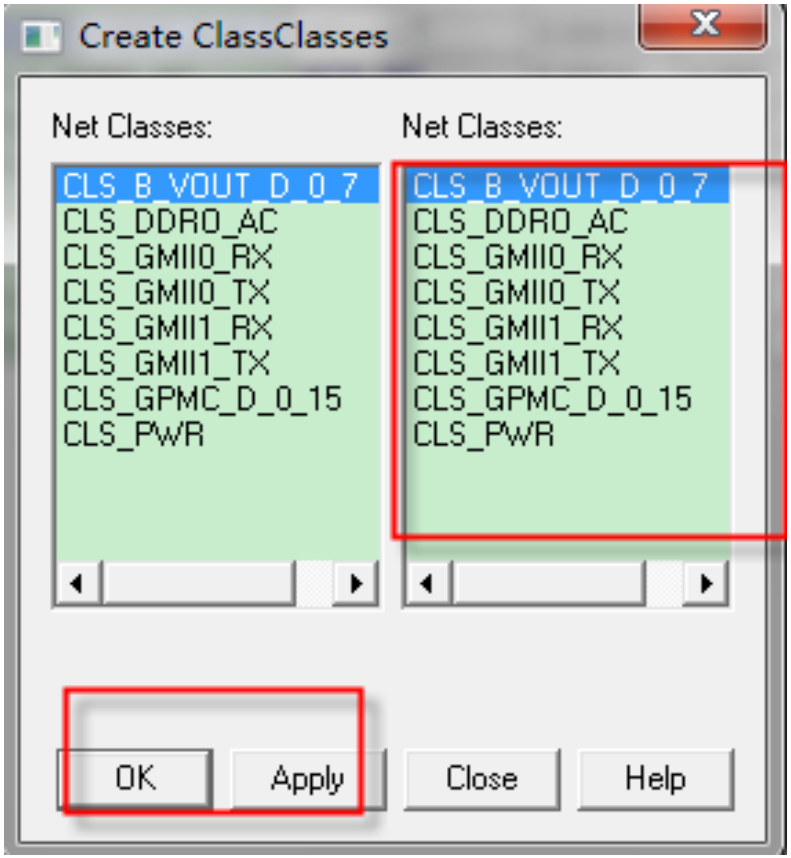
方法二

NCIs	CLS_DDR0_AC (21)	SCS_3W	8.000:6....	4.000
Net	DDR0_A0	SCS_3W	8.000:6....	4.000
Net	DDR0_A1	SCS_3W	8.000:6....	4.000
Net	DDR0_A2	SCS_3W	8.000:6....	4.000
Net	DDR0_A3	SCS_3W	8.000:6....	4.000
Net	DDR0_A4	SCS_3W	8.000:6....	4.000
Net	DDR0_A5	SCS_3W	8.000:6....	4.000
Net	DDR0_A6	SCS_3W	8.000:6....	4.000
Net	DDR0_A7	SCS_3W	8.000:6....	4.000
Net	DDR0_A8	SCS_3W	8.000:6....	4.000
Net	DDR0_A9	SCS_3W	8.000:6....	4.000
Net	DDR0_A10	SCS_3W	8.000:6....	4.000
Net	DDR0_A11	SCS_3W	8.000:6....	4.000
Net	DDR0_A12	SCS_3W	8.000:6....	4.000
Net	DDR0_A13	SCS_3W	8.000:6....	4.000
Net	DDR0_A14	SCS_3W	8.000:6....	4.000
Net	DDR0_BA0	SCS_3W	8.000:6....	4.000
Net	DDR0_BA1	SCS_3W	8.000:6....	4.000
Net	DDR0_BA2	SCS_3W	8.000:6....	4.000
Net	DDR0_CASN	SCS_3W	8.000:6....	4.000
Net	DDR0_CKE	SCS_3W	8.000:6....	4.000
Net	DDR0_CSN	SCS_3W	8.000:6....	4.000

间距约束（Spacing Constraint）

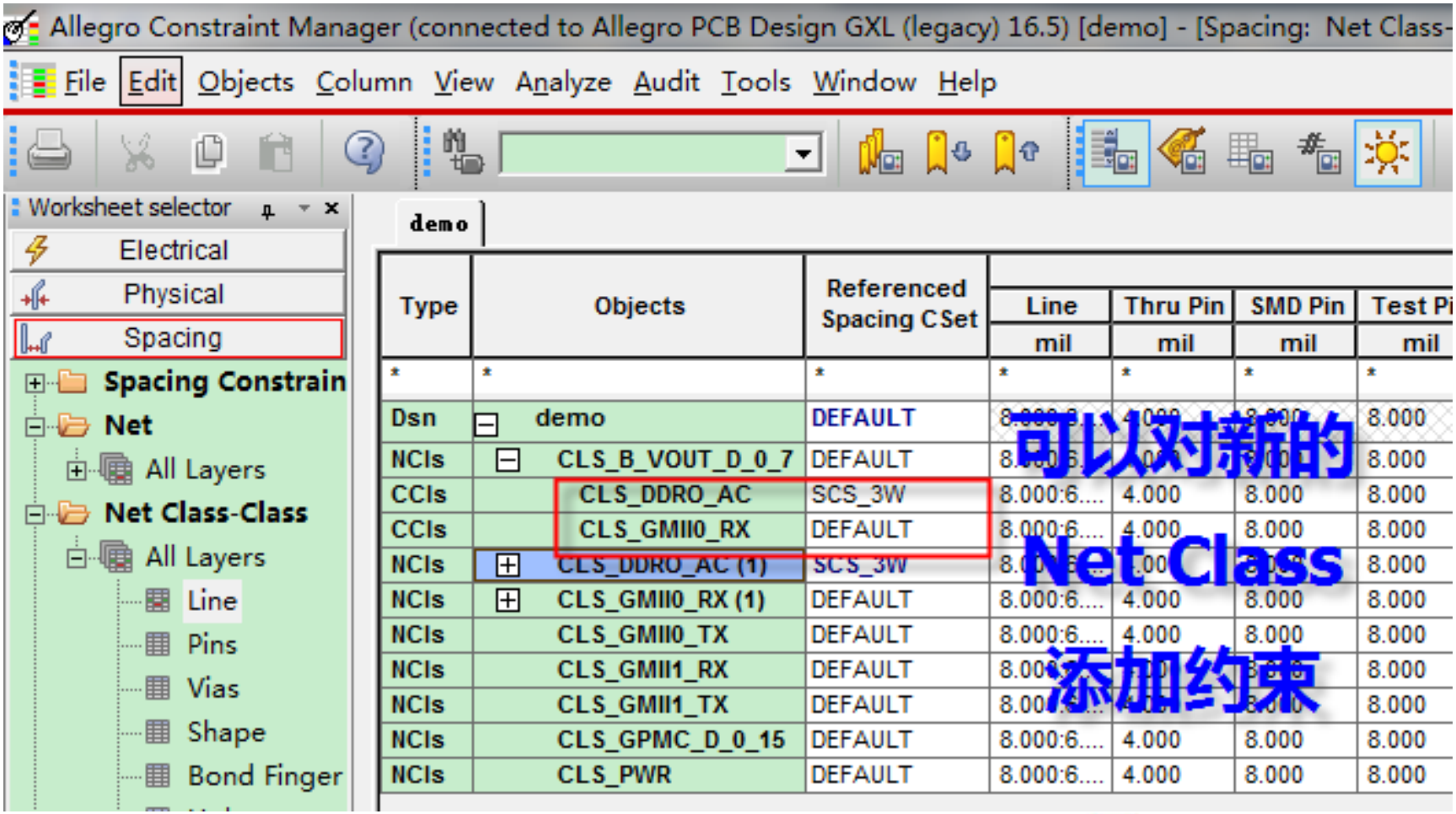
- 建立Net Class-Class 间距约束





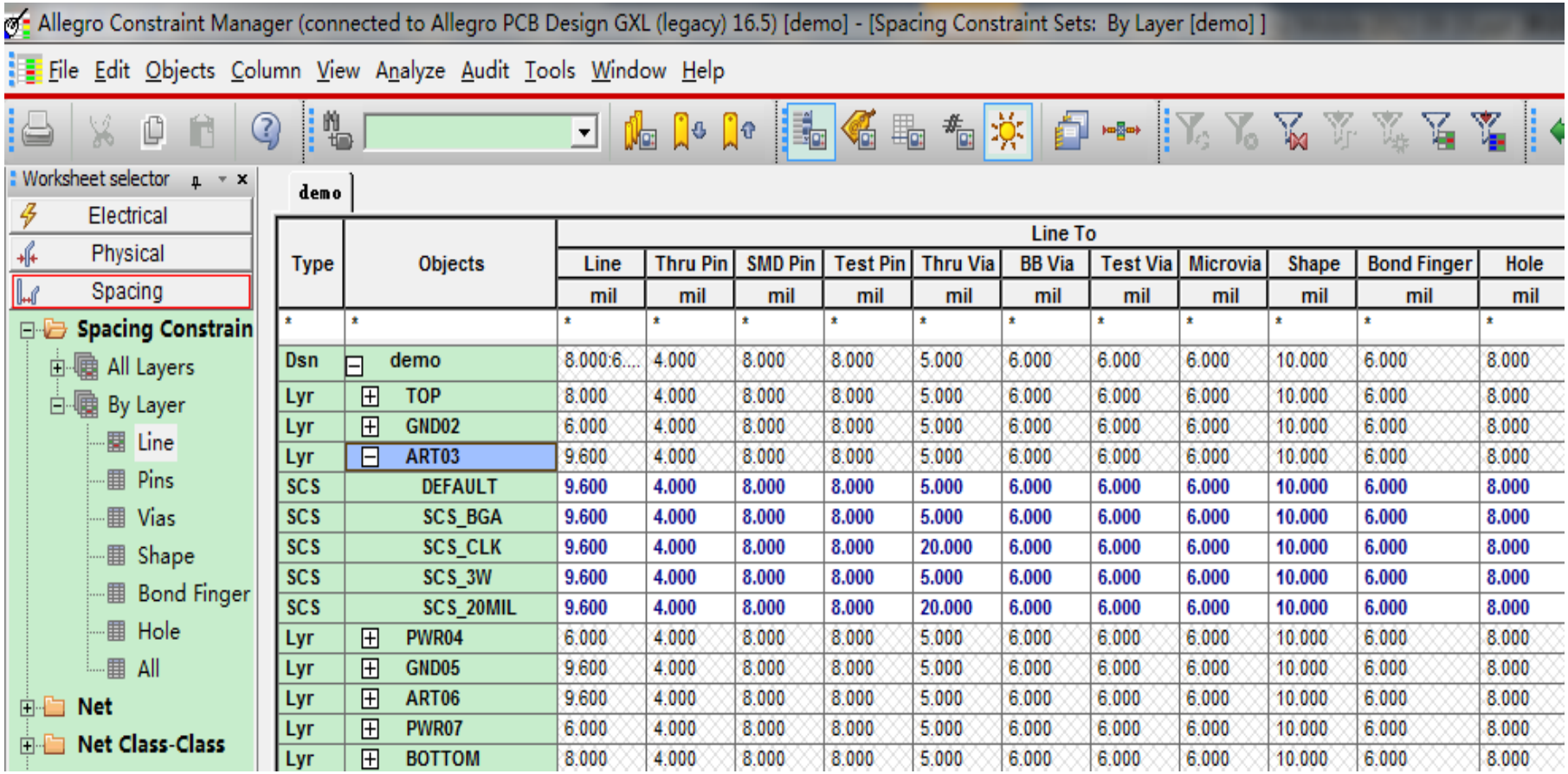
间距约束（Spacing Constraint）

- 建立Net Class-Class 间距约束



间距约束（Spacing Constraint）

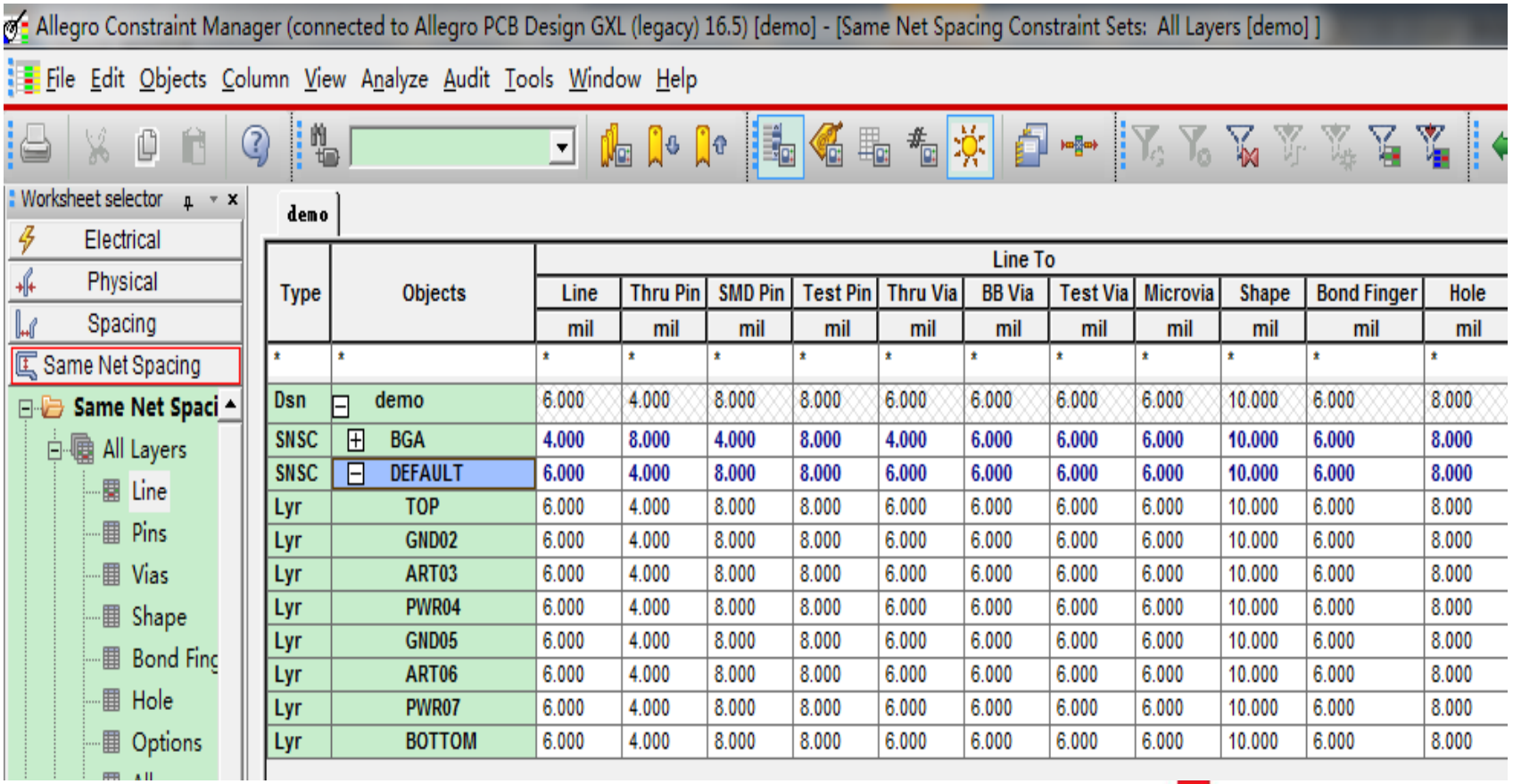
- 层间约束（Constraint By Layer）



Type	Objects	Line To										
		Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Microvia	Shape	Bond Finger	Hole
		mil	mil	mil	mil	mil	mil	mil	mil	mil	mil	mil
*	*	*	*	*	*	*	*	*	*	*	*	*
Dsn	demo	8.000:6....	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	TOP	8.000	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	GND02	6.000	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	ART03	9.600	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
SCS	DEFAULT	9.600	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
SCS	SCS_BGA	9.600	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
SCS	SCS_CLK	9.600	4.000	8.000	8.000	20.000	6.000	6.000	6.000	10.000	6.000	8.000
SCS	SCS_3W	9.600	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
SCS	SCS_20MIL	9.600	4.000	8.000	8.000	20.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	PWR04	6.000	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	GND05	9.600	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	ART06	9.600	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	PWR07	6.000	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	BOTTOM	8.000	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000

Same Net Spacing Constraint

- 设置和**Spacing**约束操作一样，注意是相同网络的对象之间的间距。

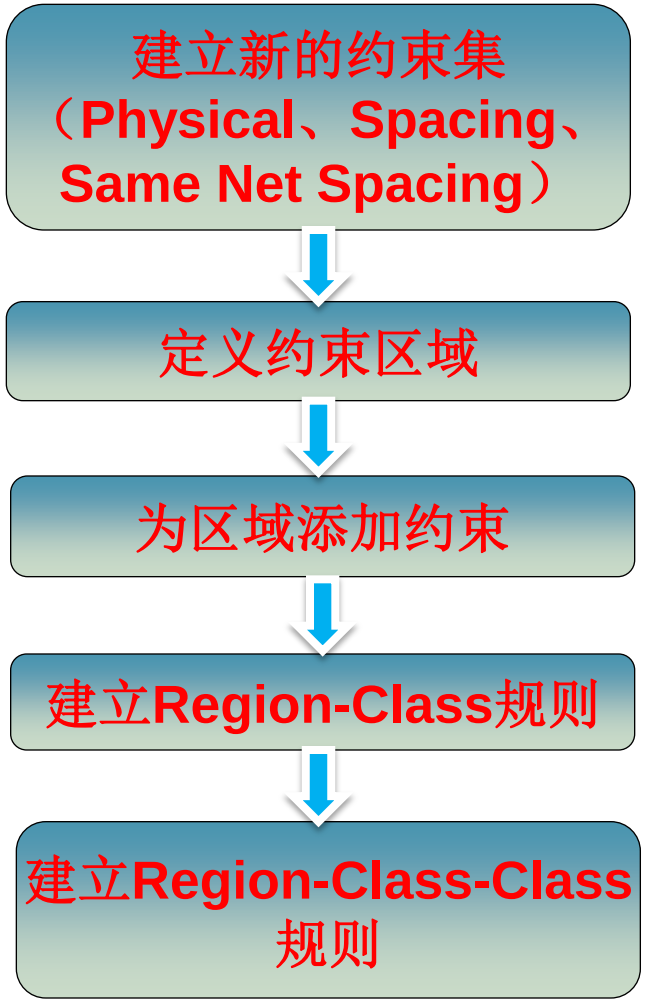


Type	Objects	Line To										
		Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Microvia	Shape	Bond Finger	Hole
		mil	mil	mil	mil	mil	mil	mil	mil	mil	mil	mil
*	*	*	*	*	*	*	*	*	*	*	*	*
Dsn	demo	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000
SNSC	BGA	4.000	8.000	4.000	8.000	4.000	6.000	6.000	6.000	10.000	6.000	8.000
SNSC	DEFAULT	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	TOP	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	GND02	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	ART03	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	PWR04	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	GND05	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	ART06	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	PWR07	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	BOTTOM	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000

区域约束（Region Constraint）

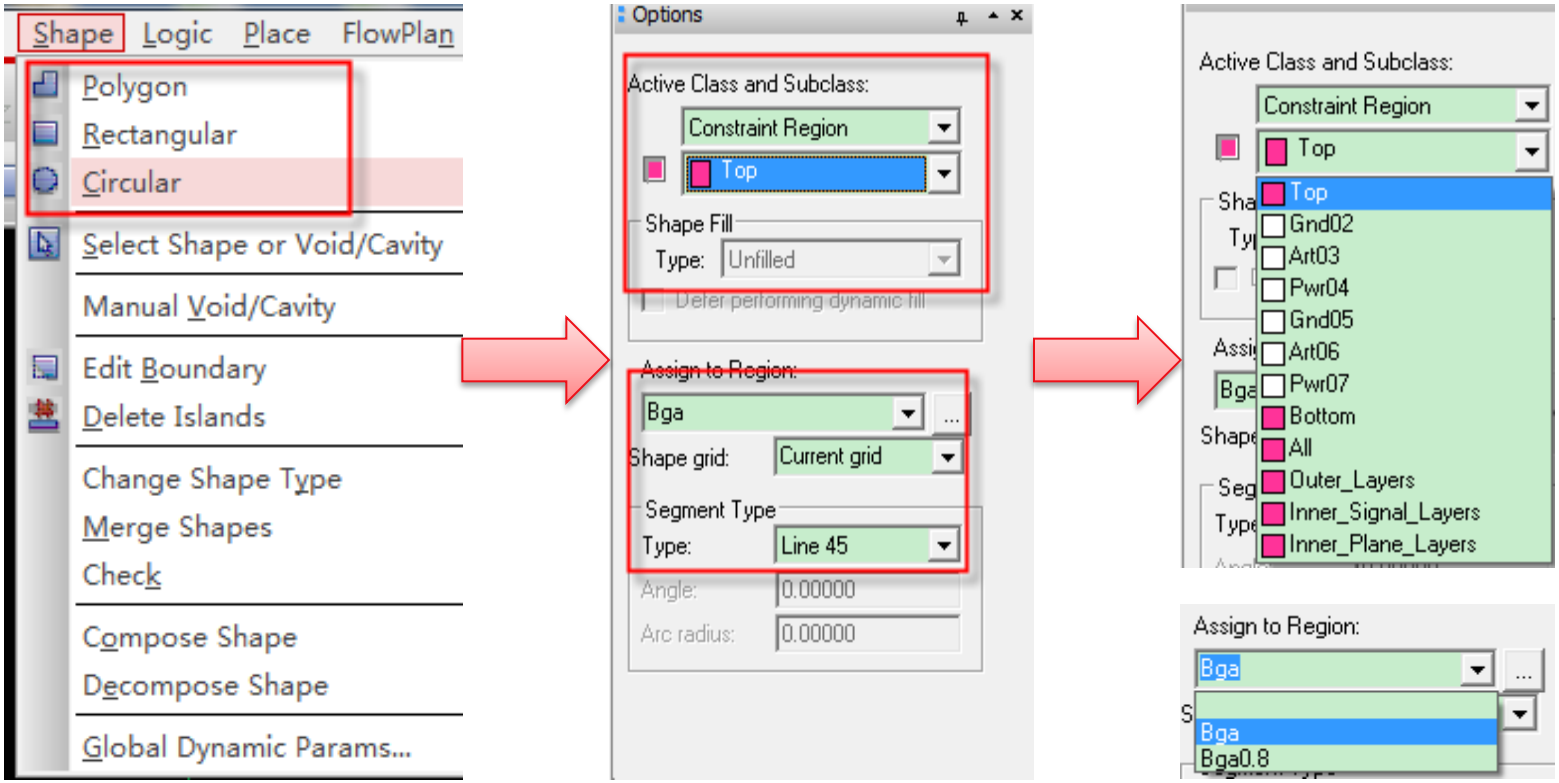
- 某些设计，用户会在部分区域使用特殊的设计规则，如BGA的附近区域需要用到更小的Line宽度和间距等。
- 首先，用户需要根据设计需求建立新的扩展（Physical、Spacing、Same Net Spacing）约束；
- 其次，用Shape命令来定义约束区域，绕后为区域添加新的约束；
- 最后，如果约束区域中不同的Net Class需要不同的设计规则或者不同Net Class的网络之间需要不同的设计规则，则需要建立Region-Class或者Region-Class-Class，并对其添加约束。

区域约束（Region Constraint）



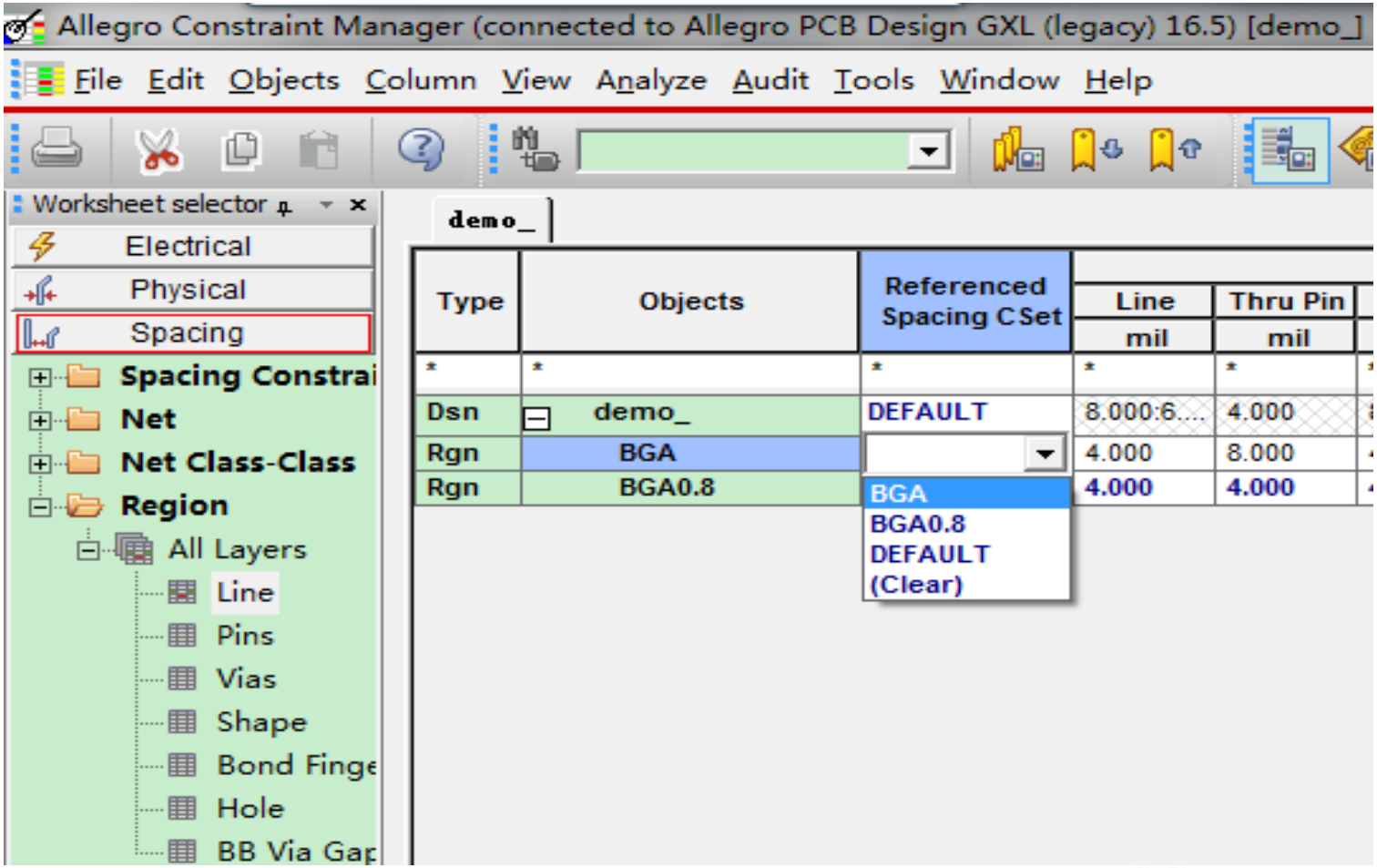
区域约束（Region Constraint）

- 定义约束区域



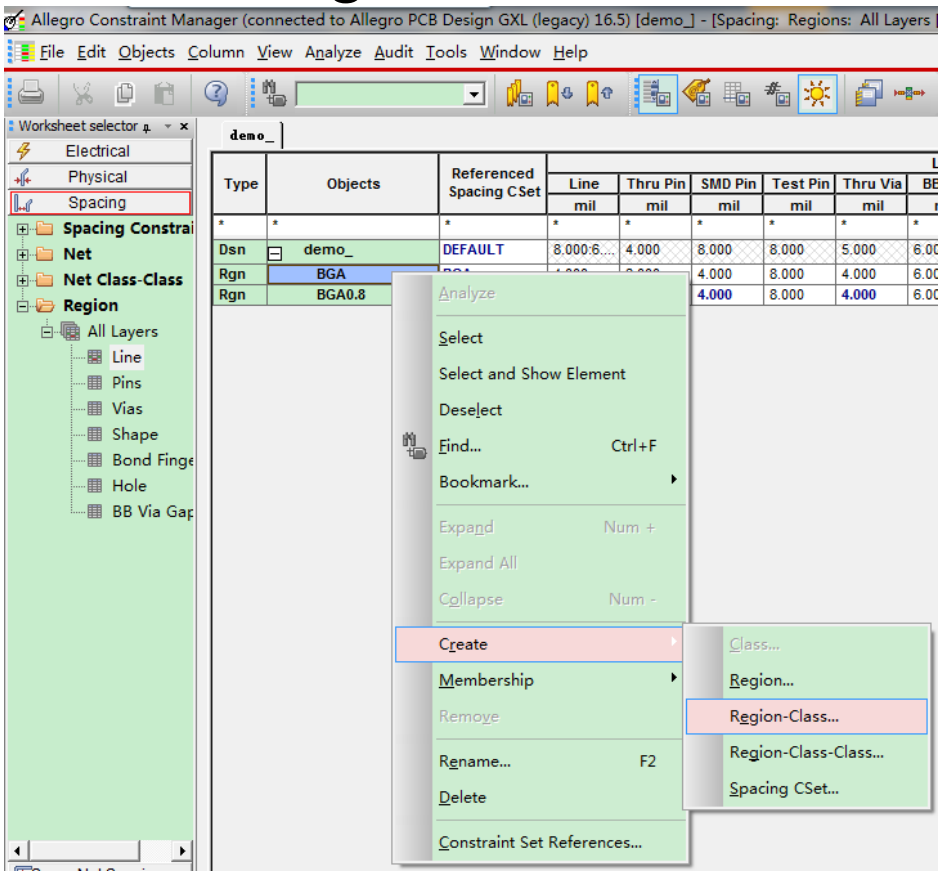
区域约束（Region Constraint）

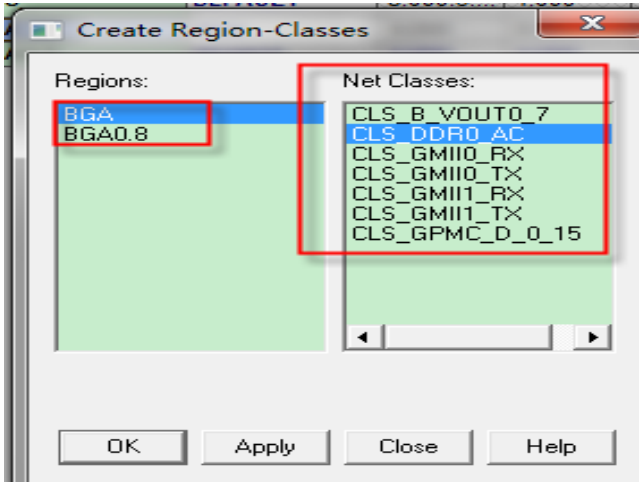
- 为区域添加约束

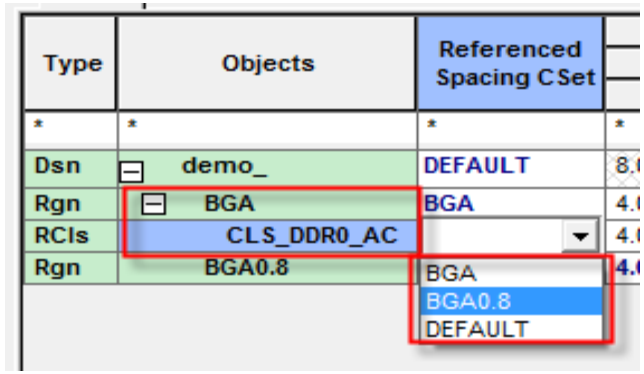


区域约束（Region Constraint）

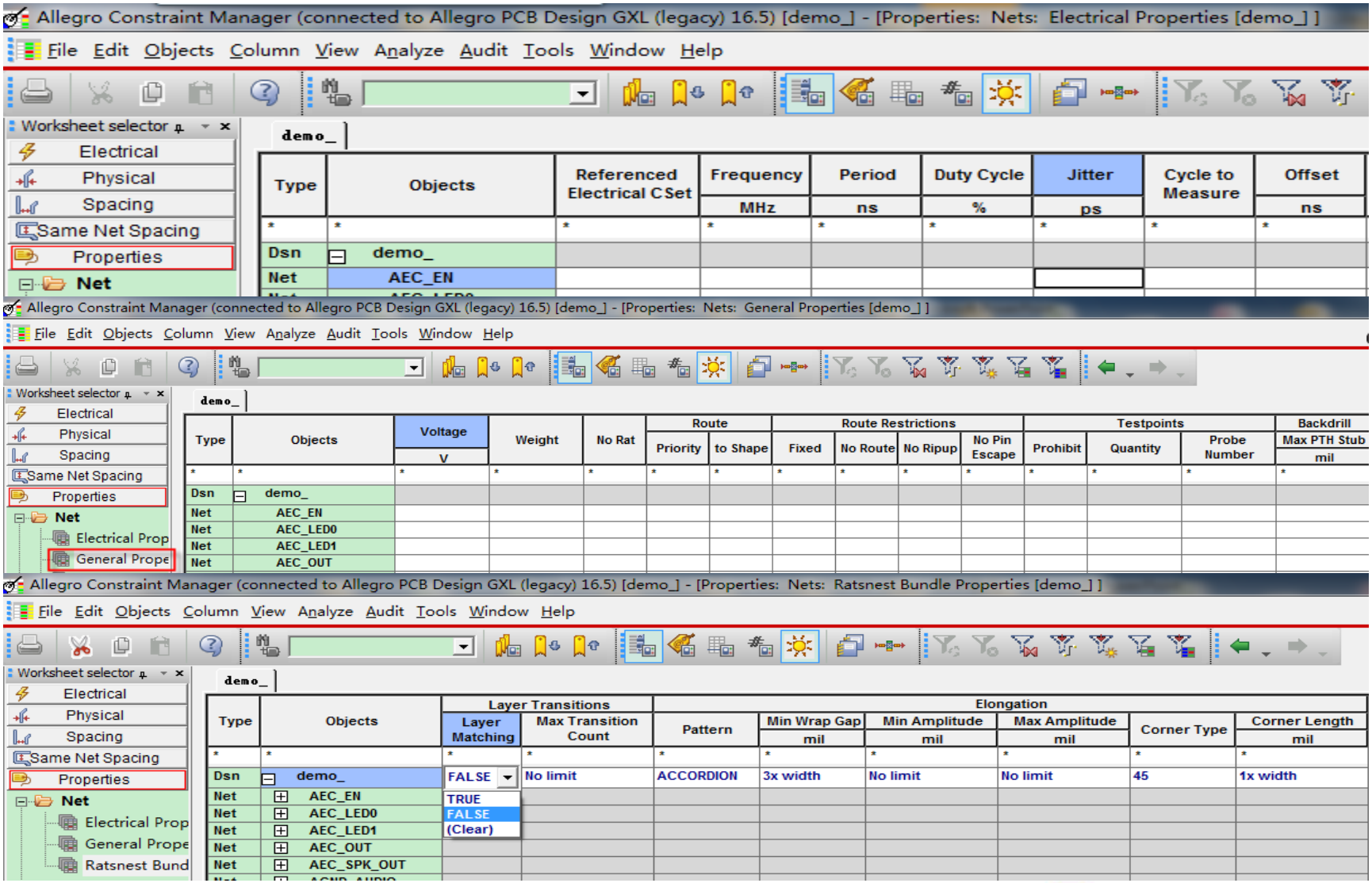
- 建立Region-Classes规则（Net & Net Class都采用区域规则）Region-Class-Class类似



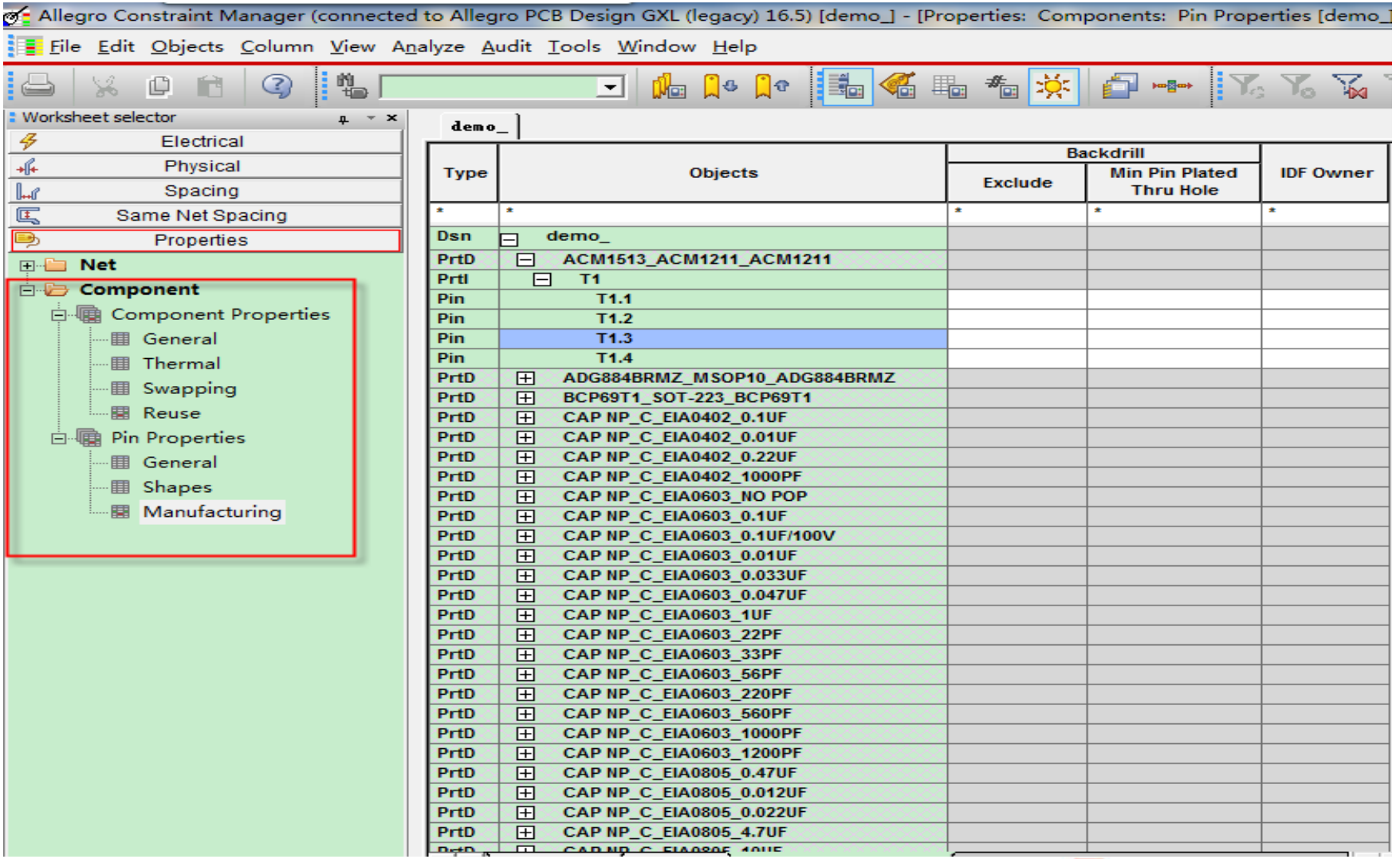




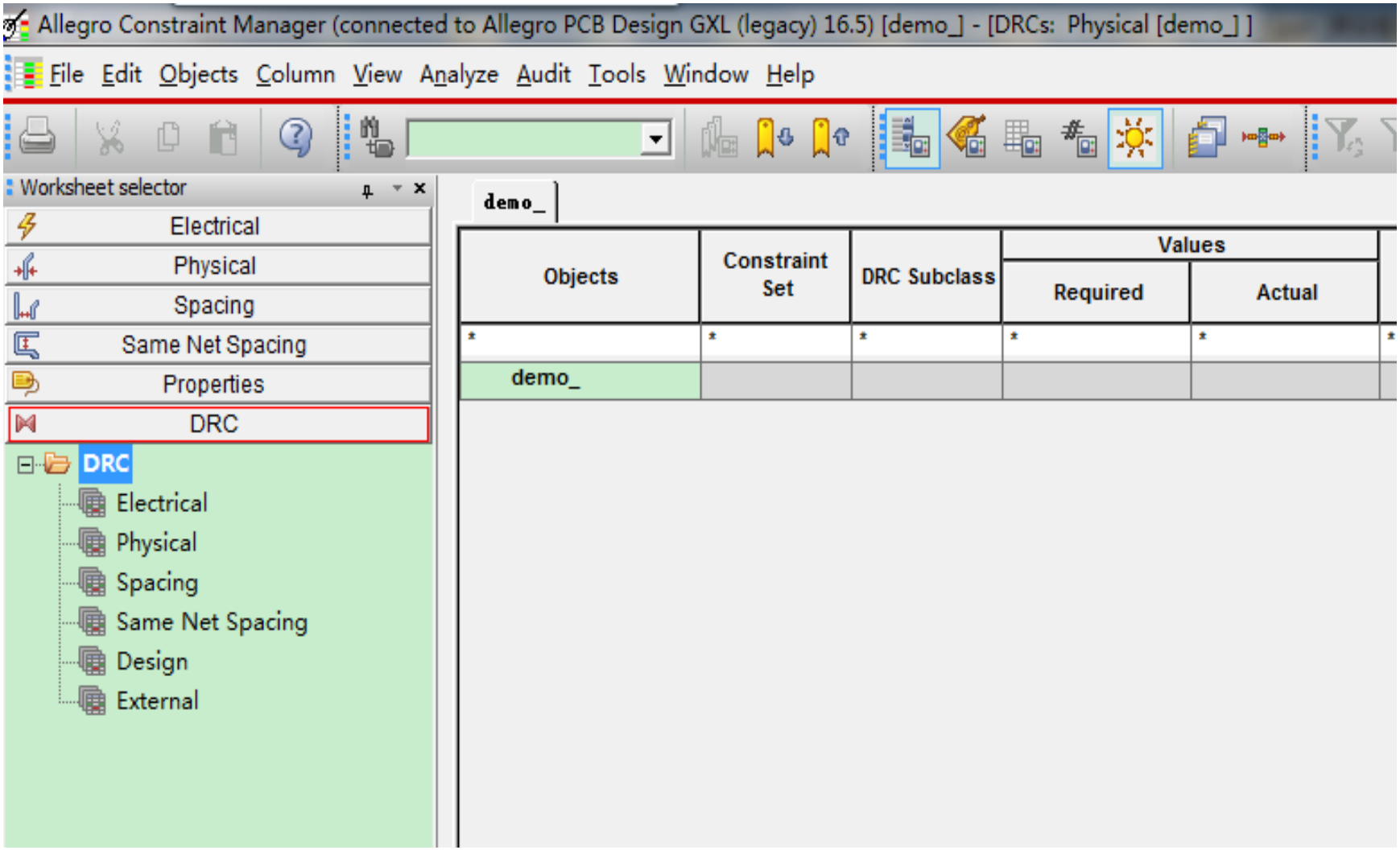
Net属性


Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo_] - [Properties: Nets: Electrical Properties [demo_]]
File Edit Objects Column View Analyze Audit Tools Window Help
Worksheet selector
Electrical
Physical
Spacing
Same Net Spacing
Properties
Net
demo_
Type | Objects | Referenced Electrical CSet | Frequency MHz | Period ns | Duty Cycle % | Jitter ps | Cycle to Measure | Offset ns
Dsn demo_
Net AEC_EN
Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo_] - [Properties: Nets: General Properties [demo_]]
Electrical Prop
General Prope
Type | Objects | Voltage V | Weight | No Rat | Route: Priority, to Shape | Route Restrictions: Fixed, No Route, No Ripup, No Pin Escape | Testpoints: Prohibit, Quantity, Probe Number | Backdrill: Max PTH Stub mil
Net AEC_LED0
Net AEC_LED1
Net AEC_OUT
Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo_] - [Properties: Nets: Ratsnest Bundle Properties [demo_]]
Ratsnest Bund
Type | Objects | Layer Transitions: Layer Matching, Max Transition Count | Elongation: Pattern, Min Wrap Gap mil, Min Amplitude mil, Max Amplitude mil, Corner Type, Corner Length mil
Dsn demo_ FALSE No limit ACCORDION 3x width No limit No limit 45 1x width
Net AEC_EN
Net AEC_LED0
Net AEC_LED1
Net AEC_OUT
Net AEC_SPK_OUT
TRUE
FALSE
(Clear)

Component属性和Pin属性

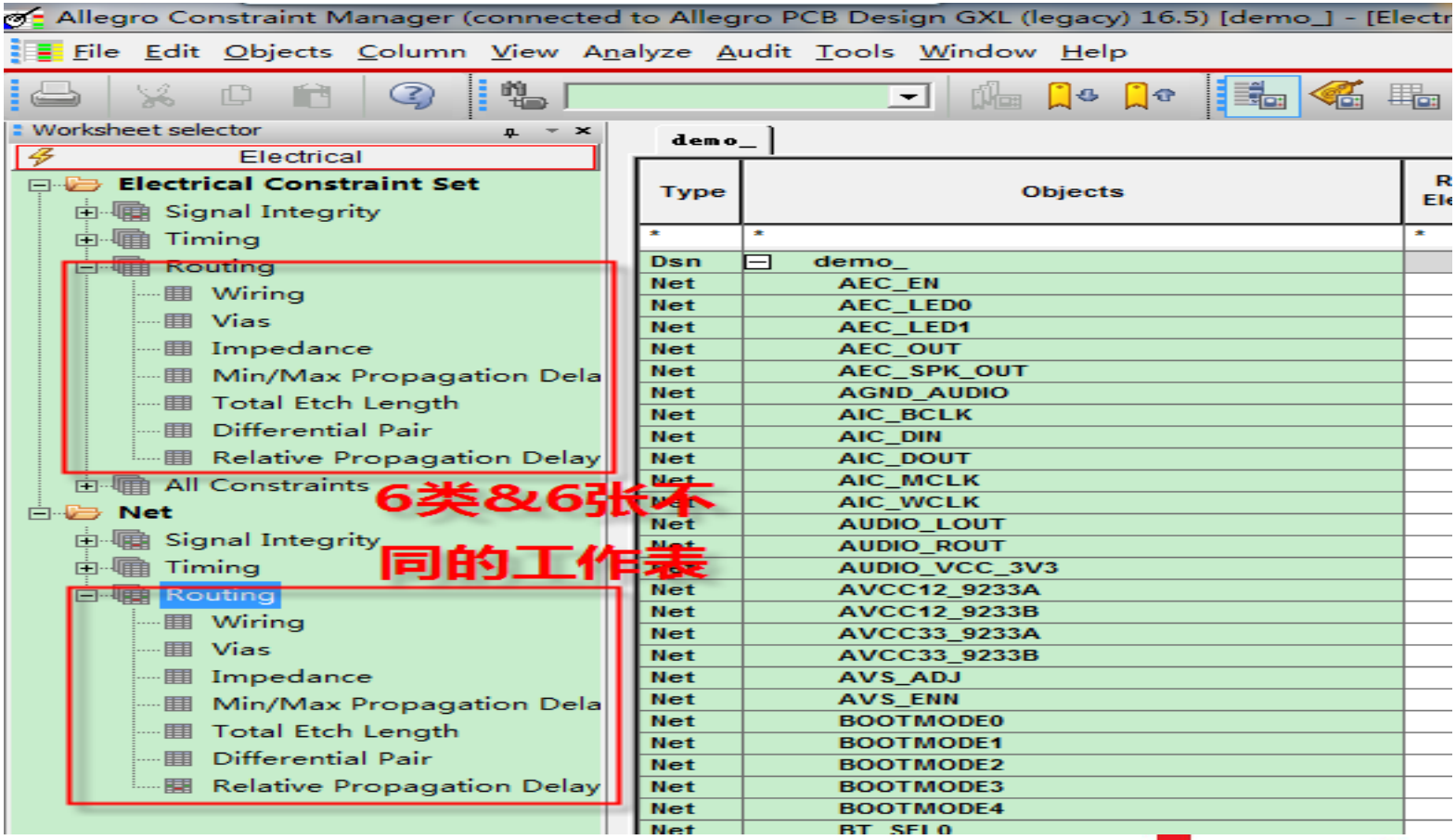


DRC工作表


Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo_] - [DRCs: Physical [demo_]]
File Edit Objects Column View Analyze Audit Tools Window Help
Worksheet selector
Electrical
Physical
Spacing
Same Net Spacing
Properties
DRC
DRC
Electrical
Physical
Spacing
Same Net Spacing
Design
External
demo_
Objects
Constraint Set
DRC Subclass
Values
Required
Actual
demo_

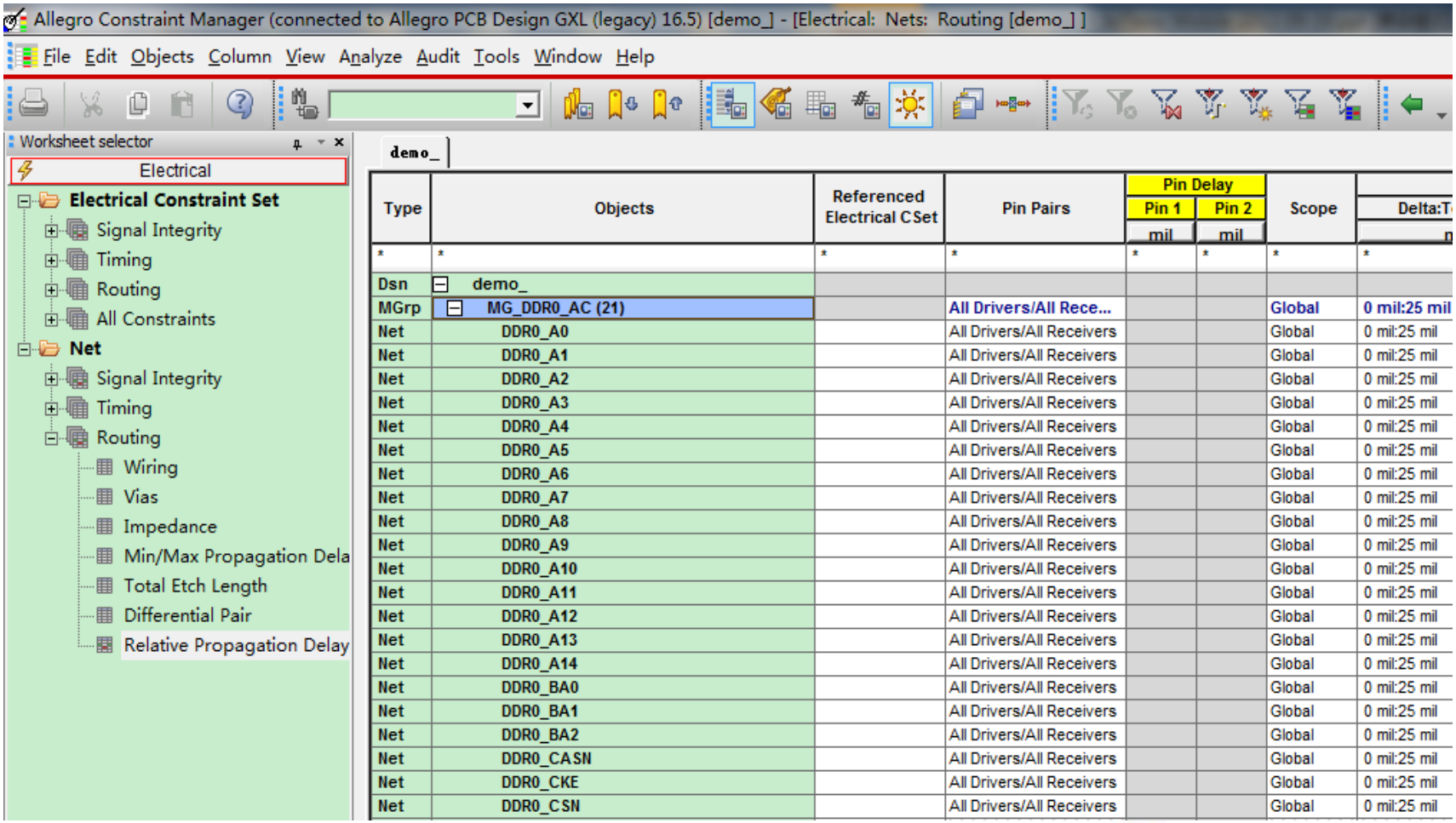
电气约束（Electrical Constraint）

- 用户可以通过Electrical约束对设计中的高速信号进行约束设计。



电气约束（Electrical Constraint）

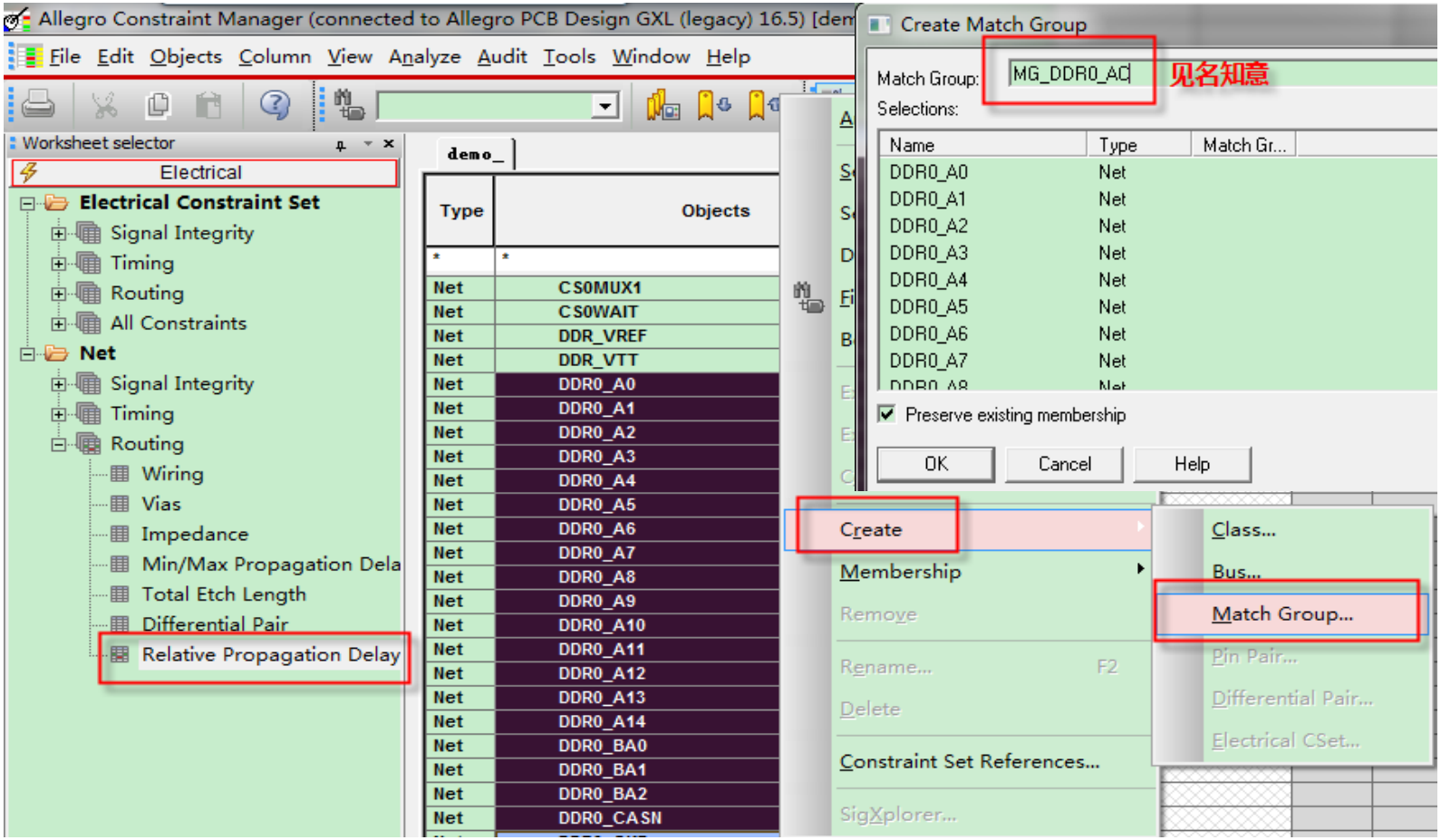
- **Relative Propagation Delay工作表**



Type	Objects	Referenced Electrical CSet	Pin Pairs	Pin Delay Pin 1 mil	Pin Delay Pin 2 mil	Scope	Delta:T
*	*	*	*	*	*	*	*
Dsn	demo_						
MGrp	MG_DDR0_AC (21)		All Drivers/All Rece...			Global	0 mil:25 mil
Net	DDR0_A0		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A1		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A2		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A3		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A4		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A5		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A6		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A7		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A8		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A9		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A10		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A11		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A12		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A13		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A14		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_BA0		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_BA1		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_BA2		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_CASN		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_CKE		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_CSN		All Drivers/All Receivers			Global	0 mil:25 mil

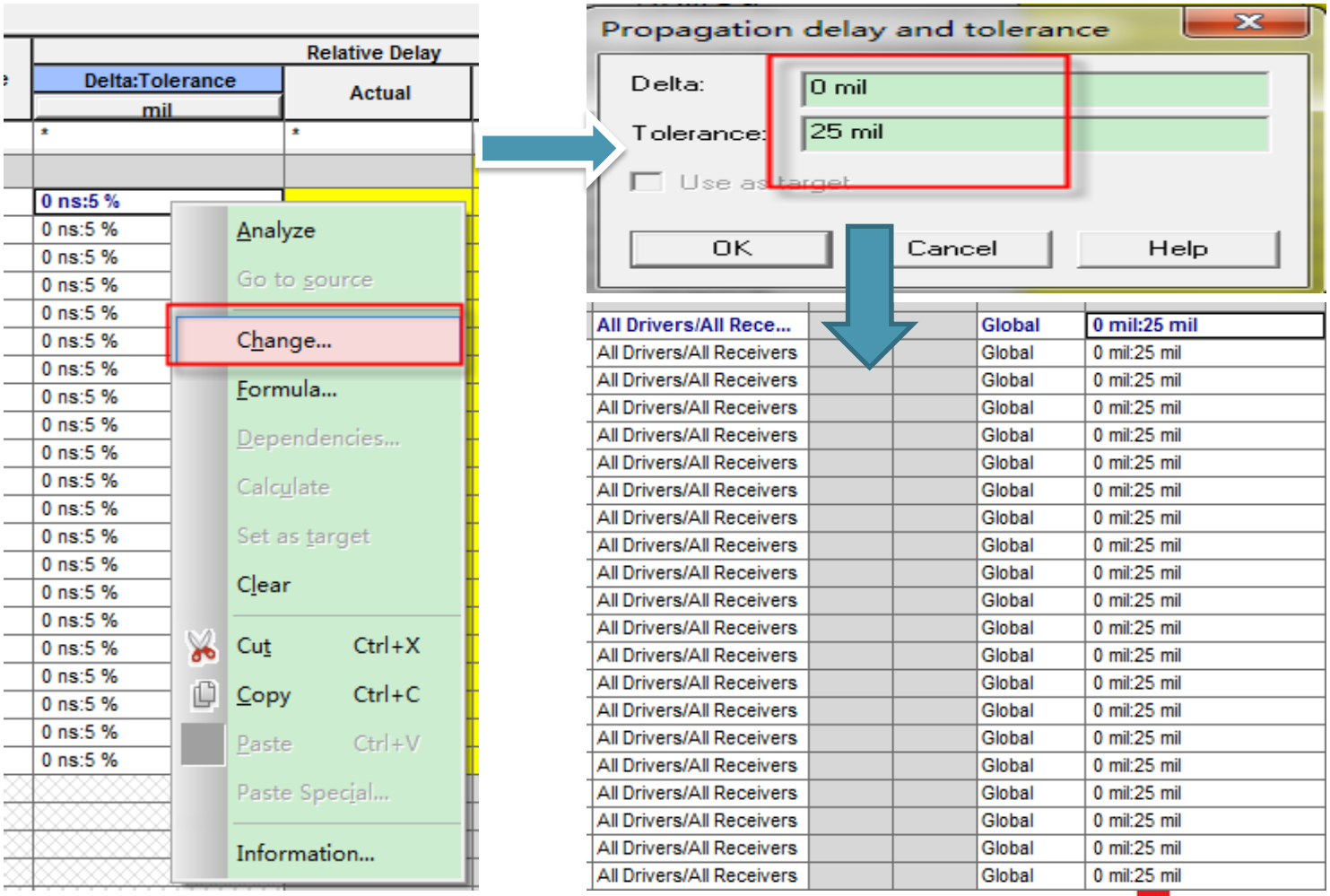
电气约束（Electrical Constraint）

- 创建Relative Propagation Delay约束（方式一）



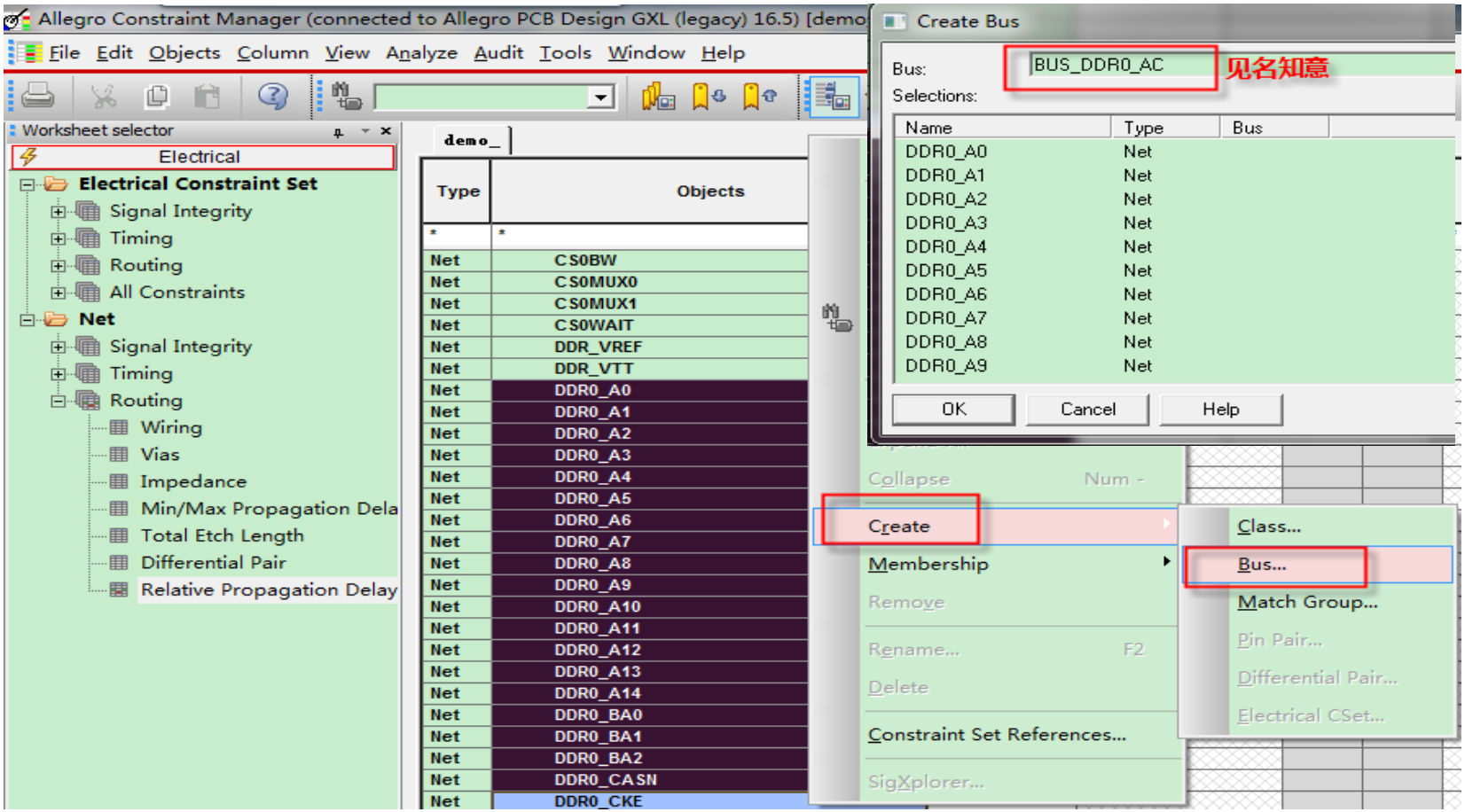
电气约束（Electrical Constraint）

- 创建Relative Propagation Delay约束（方式一）



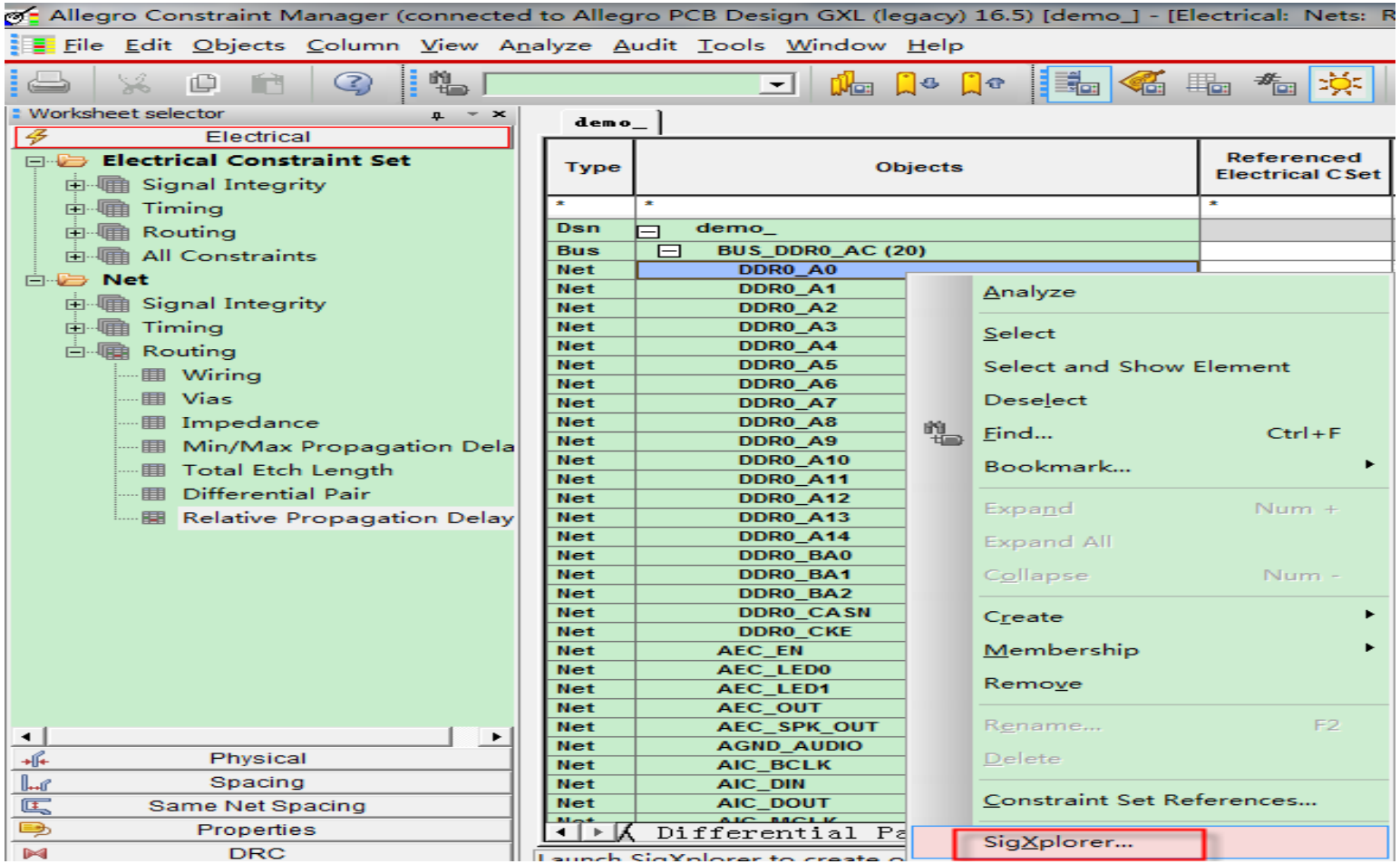
电气约束（Electrical Constraint）

- 创建Relative Propagation Delay约束（方式二）



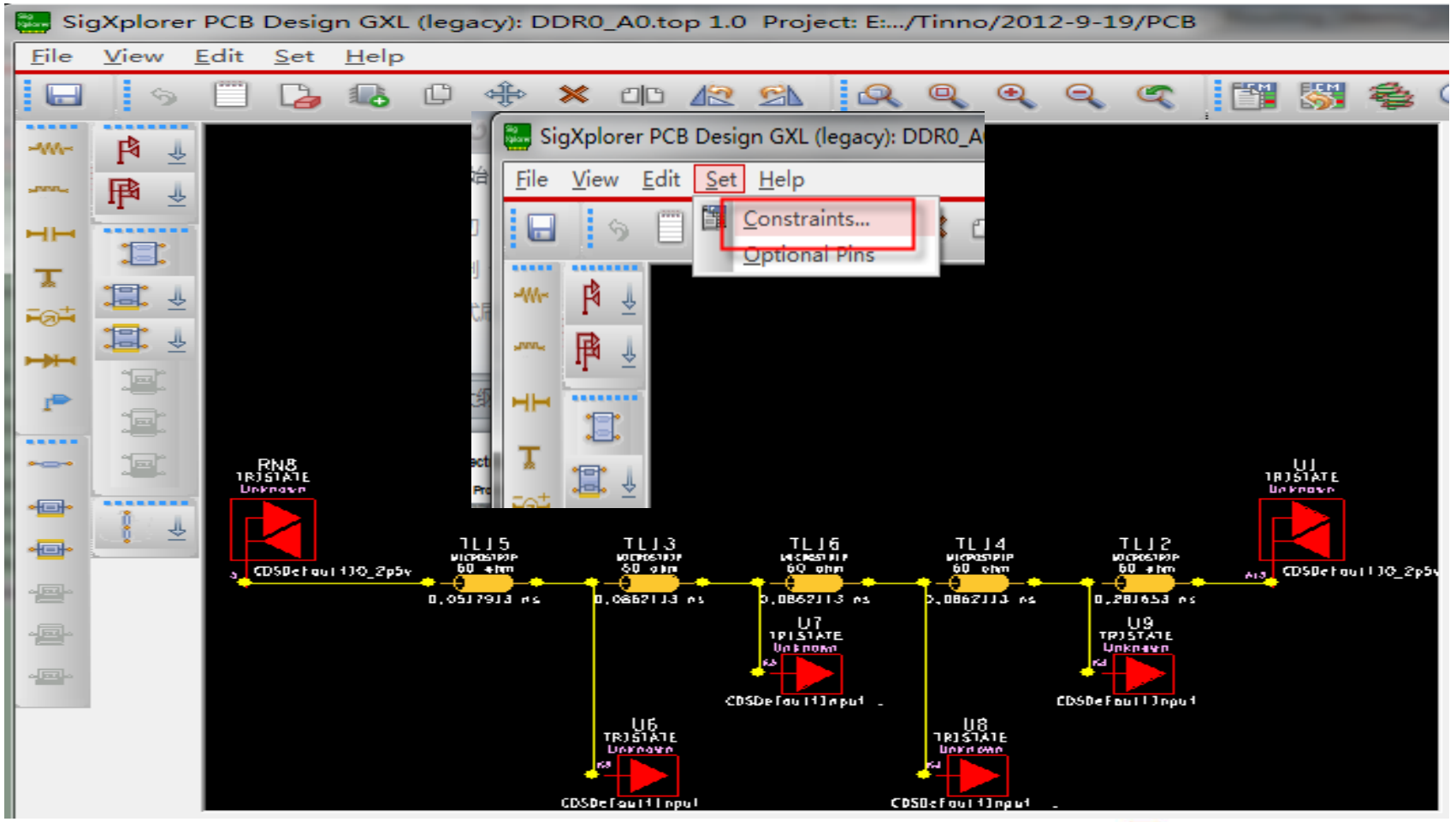
电气约束（Electrical Constraint）

- 创建Relative Propagation Delay约束（方式二）



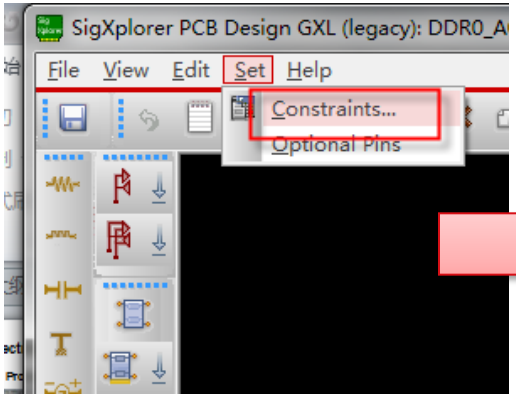
电气约束（Electrical Constraint）

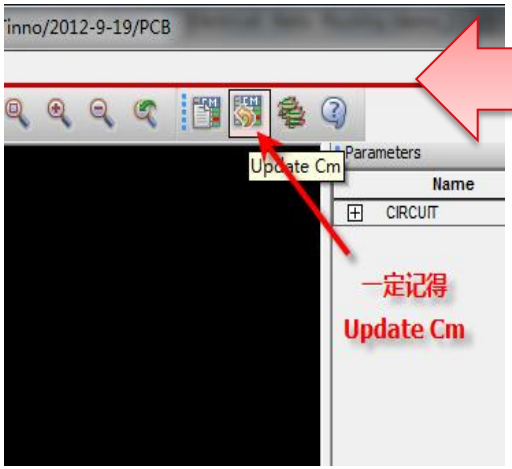
- 创建Relative Propagation Delay约束（方式二）

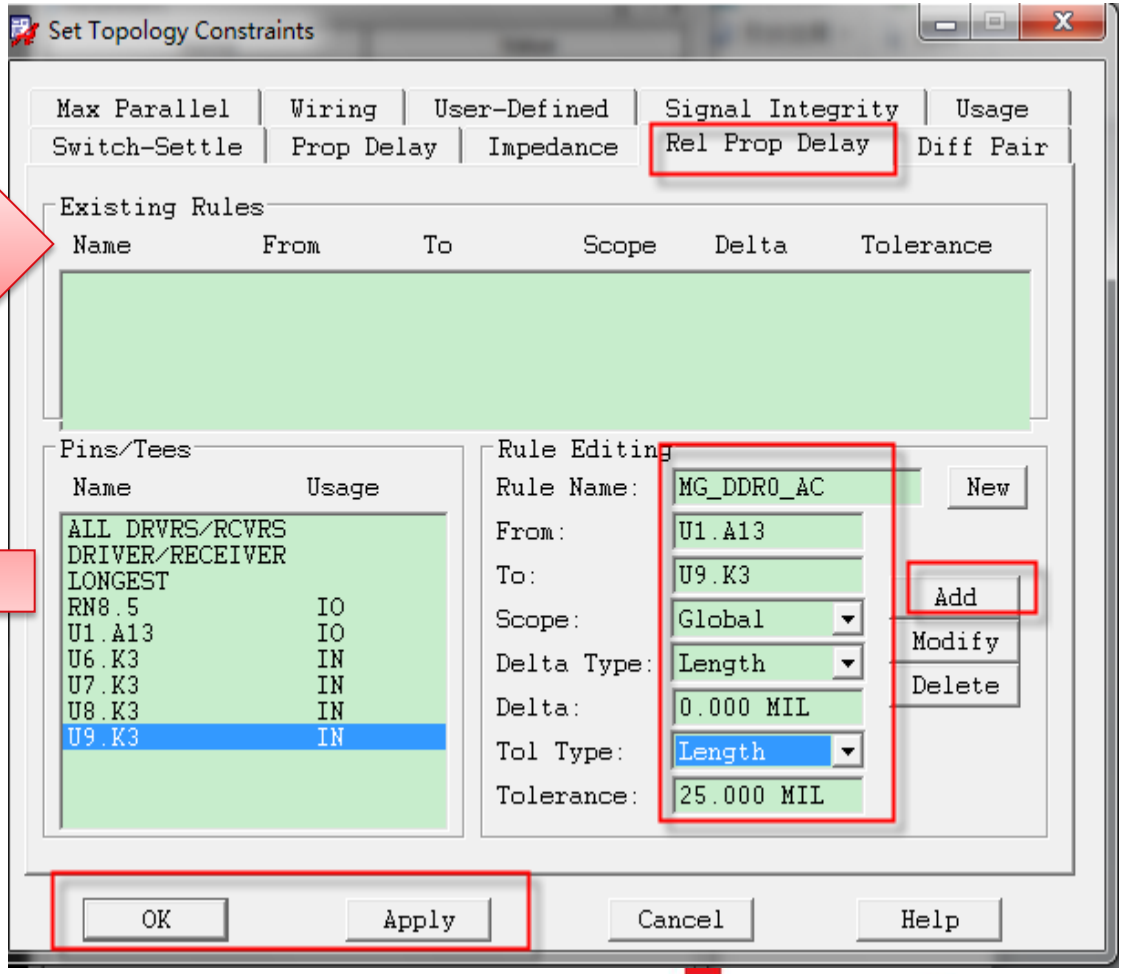


电气约束（Electrical Constraint）

- 创建Relative Propagation Delay约束（方式二）

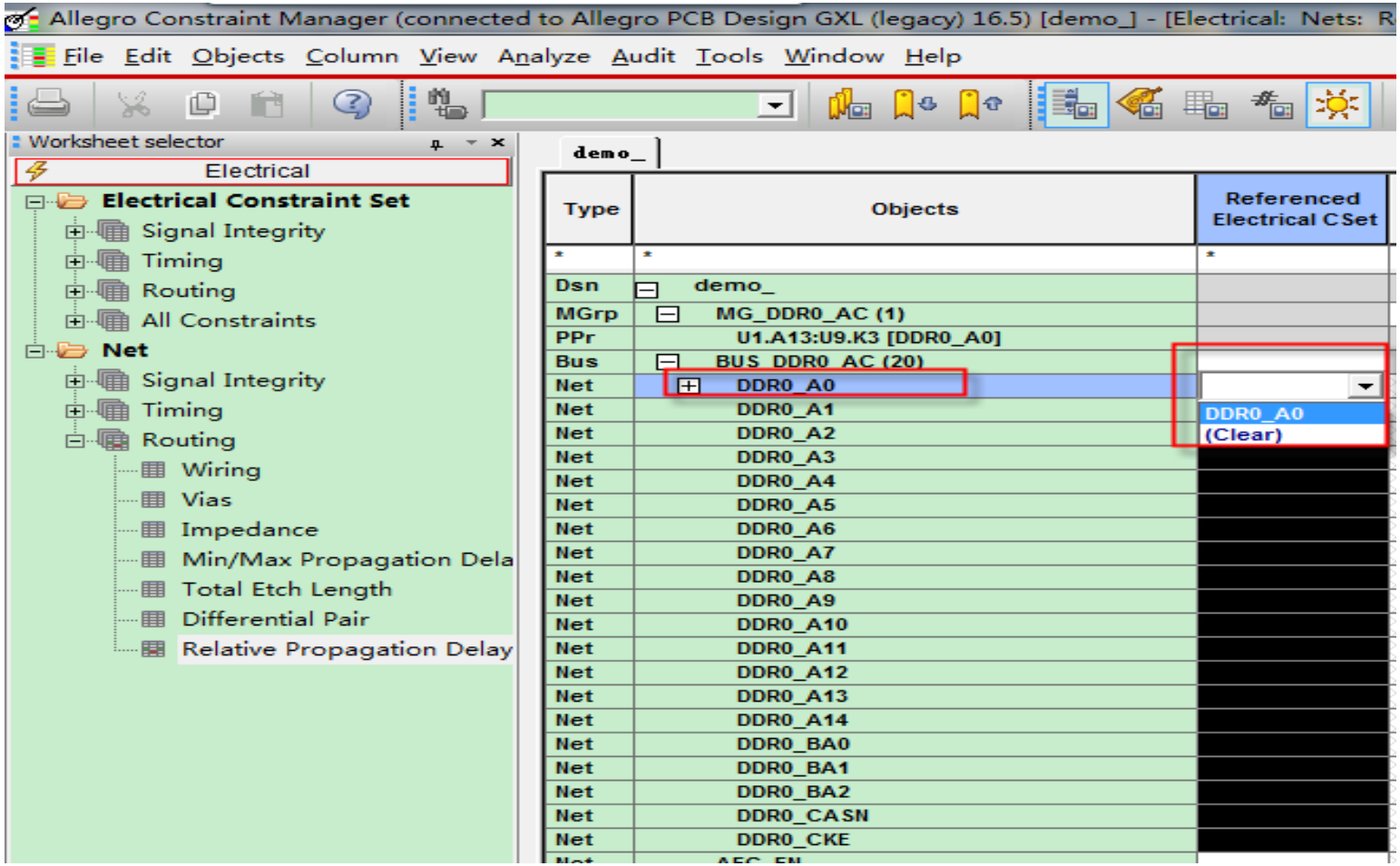






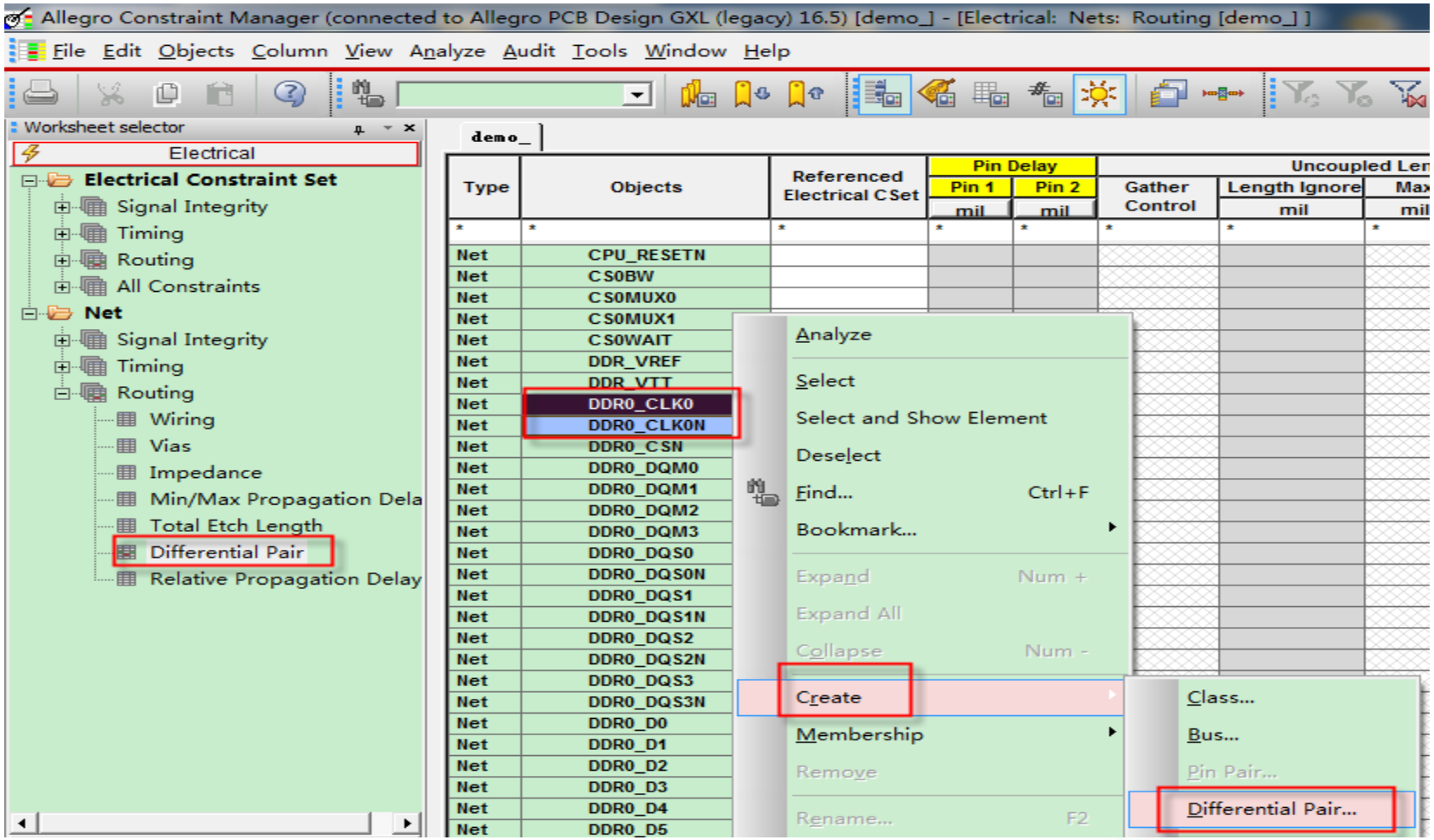
电气约束（Electrical Constraint）

- 创建Relative Propagation Delay约束（方式二）



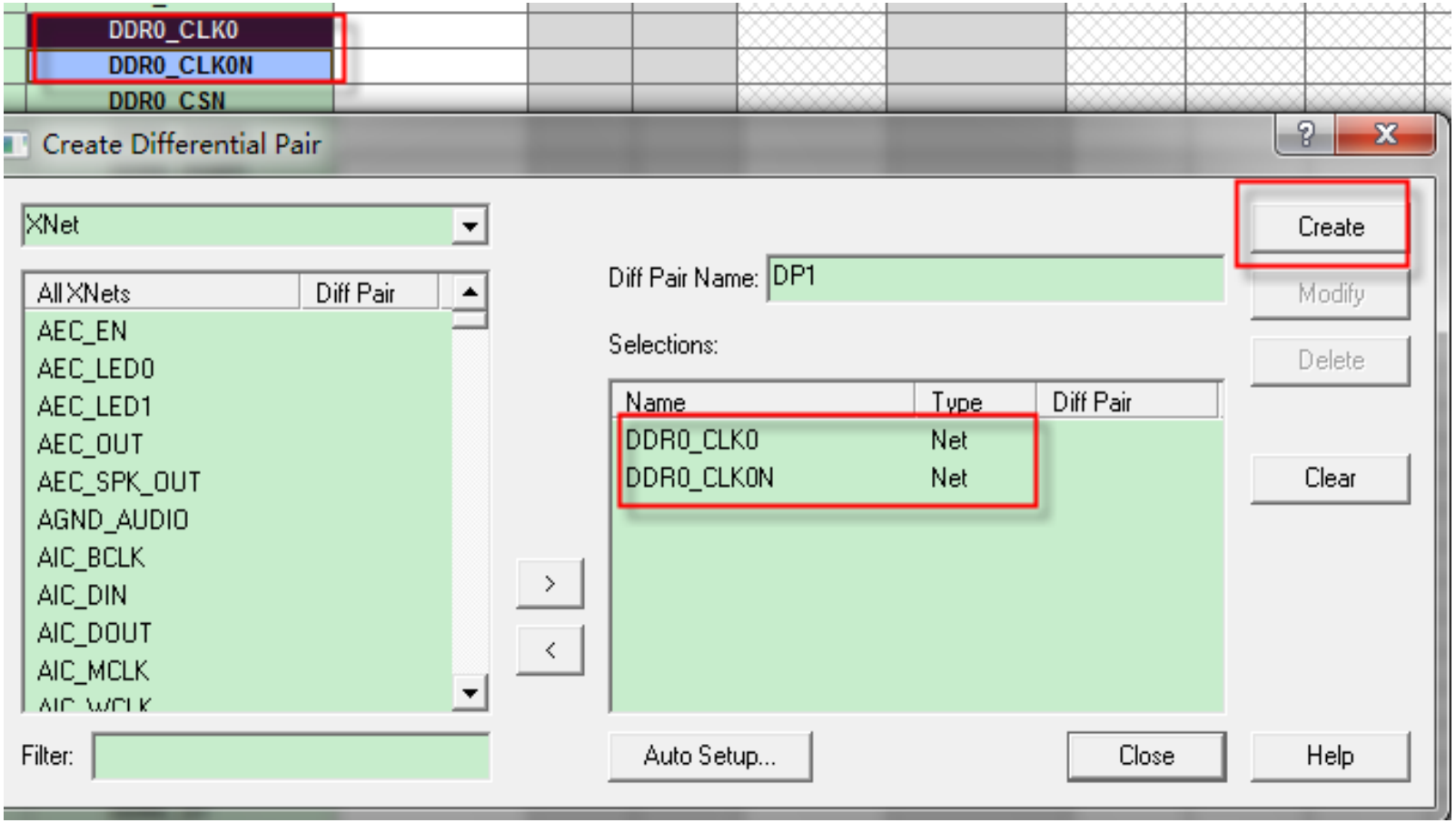
电气约束（Electrical Constraint）

- **Differential Pair 工作表**



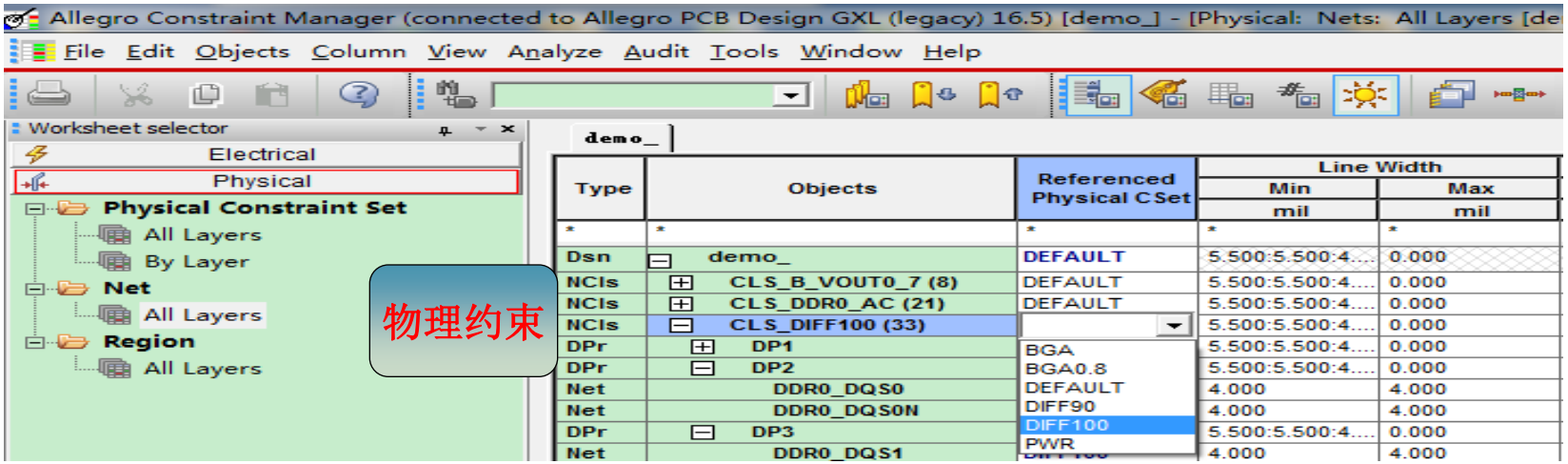
电气约束（Electrical Constraint）

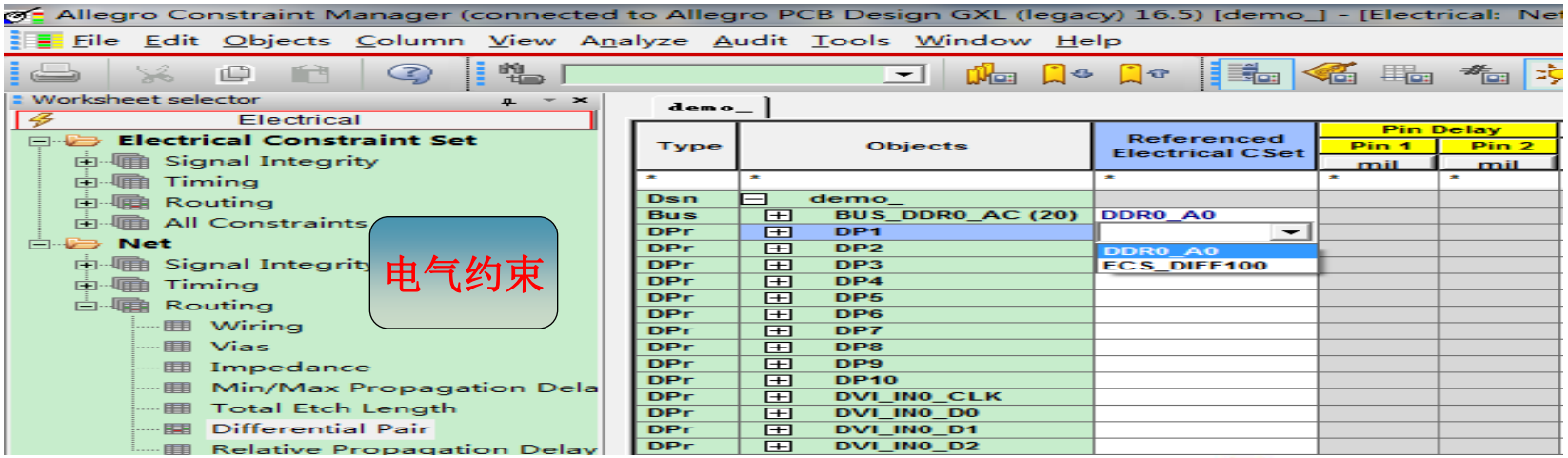
- 创建Differential Pair



电气约束（Electrical Constraint）

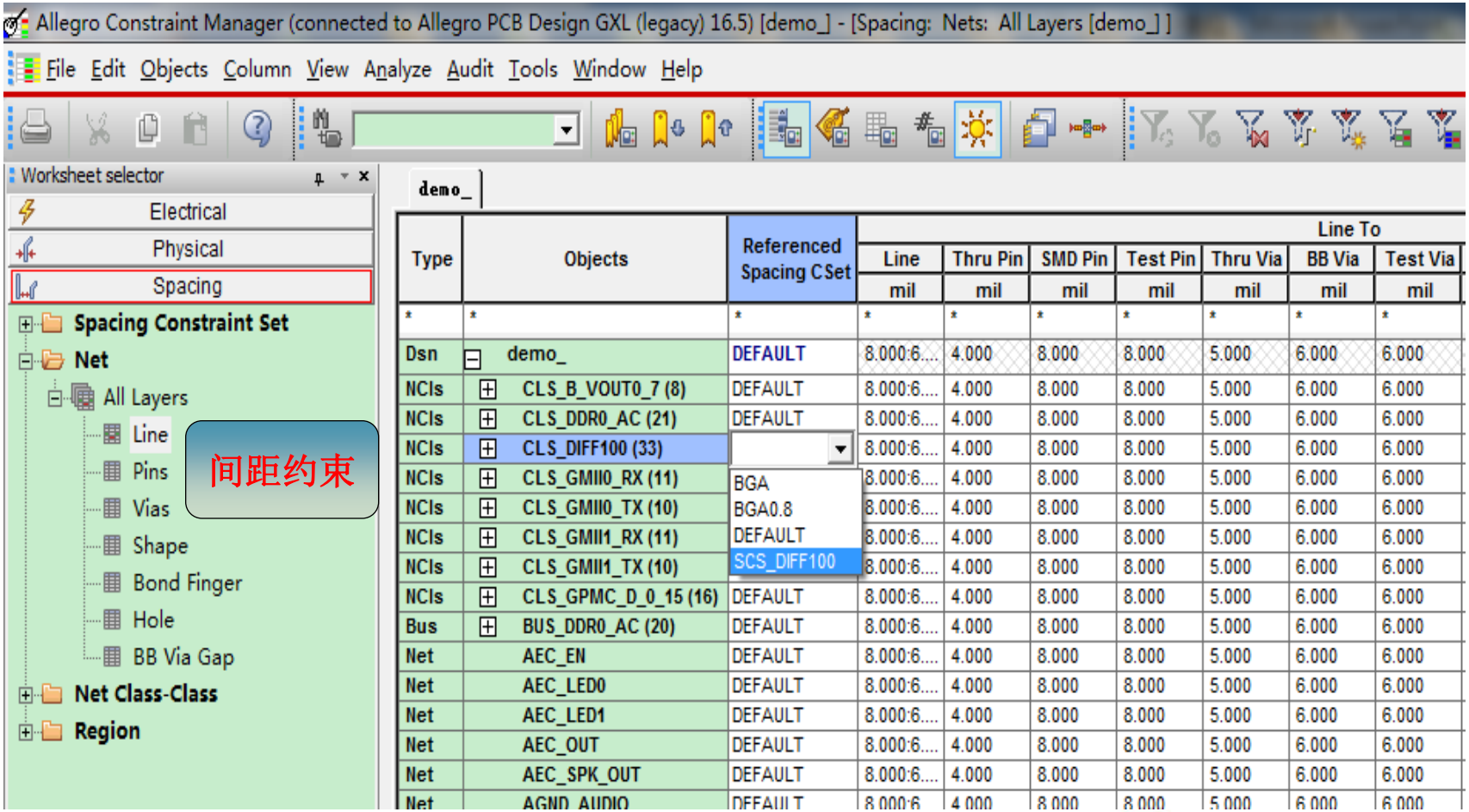
- 为Differential Pair添加约束





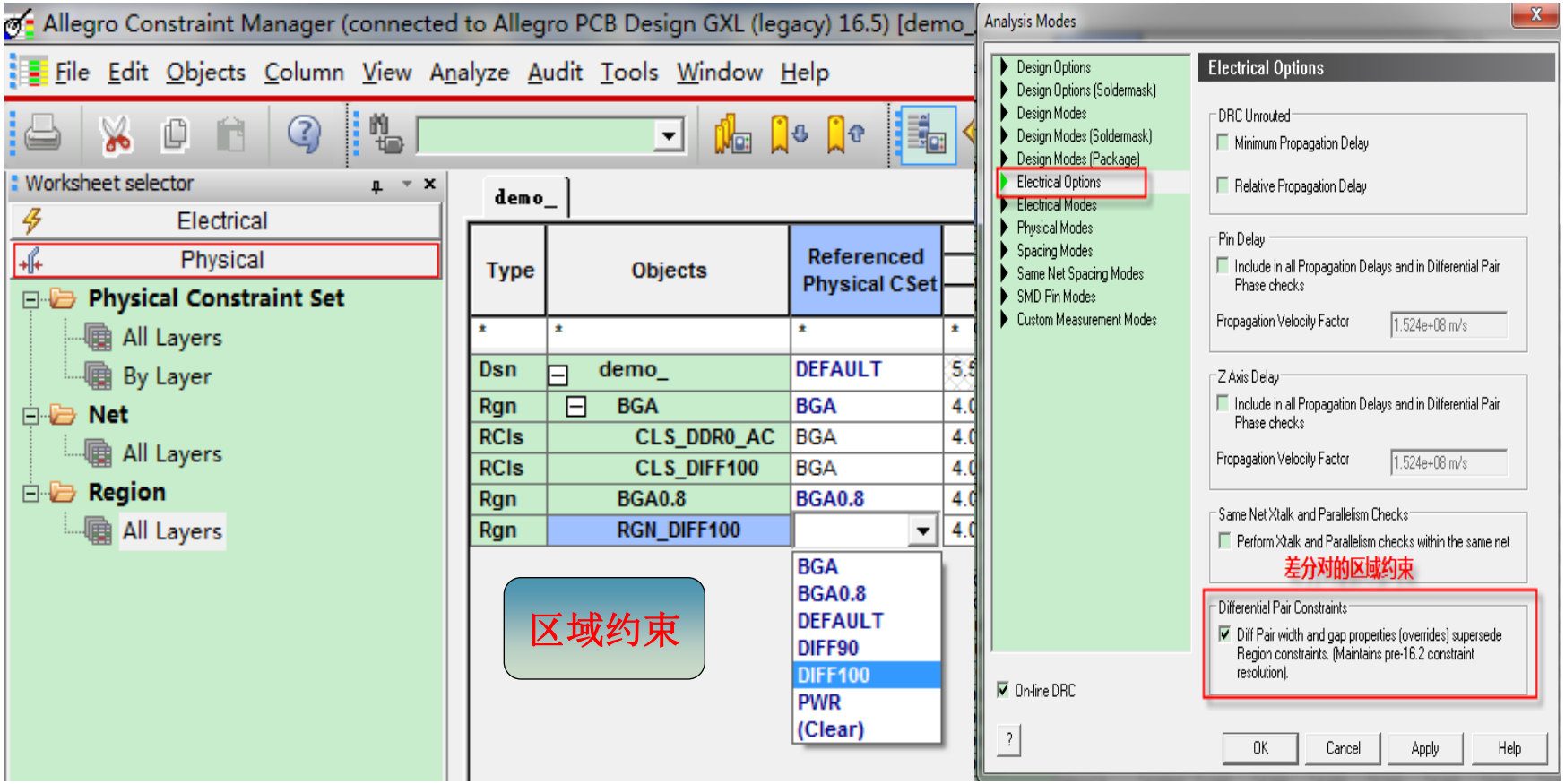
电气约束（Electrical Constraint）

- 为Differential Pair添加约束



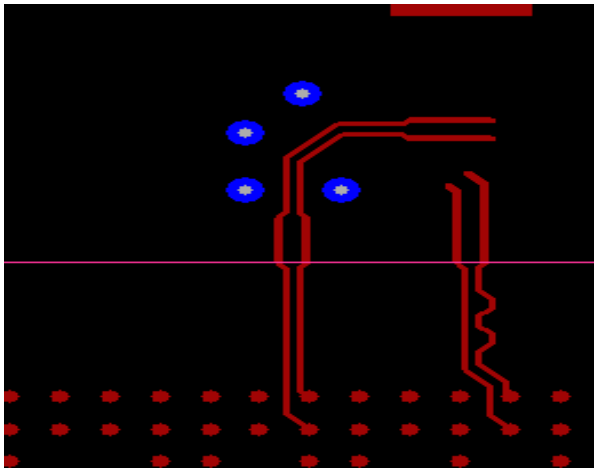
电气约束（Electrical Constraint）

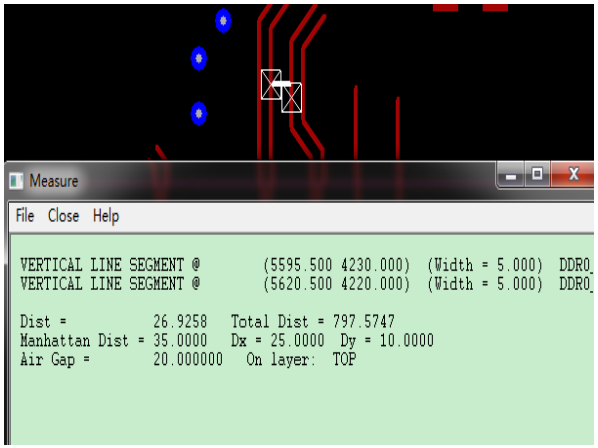
- 为Differential Pair添加约束

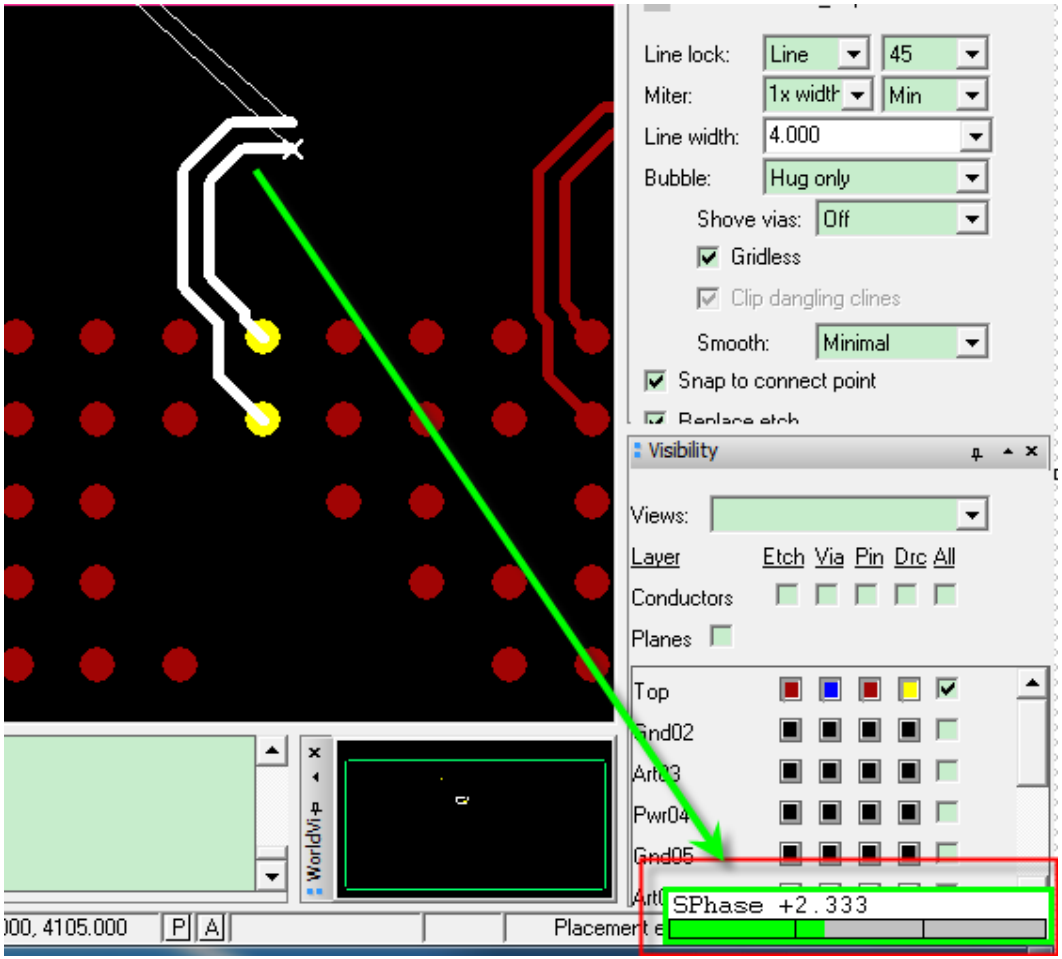


电气约束（Electrical Constraint）

- **Differential Pair约束示例**







Q&A

- Q&A
- Summary

Thank you!

SEP 19，2012
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