cadence

INVENTIVE

Design Skills & Case Analysis

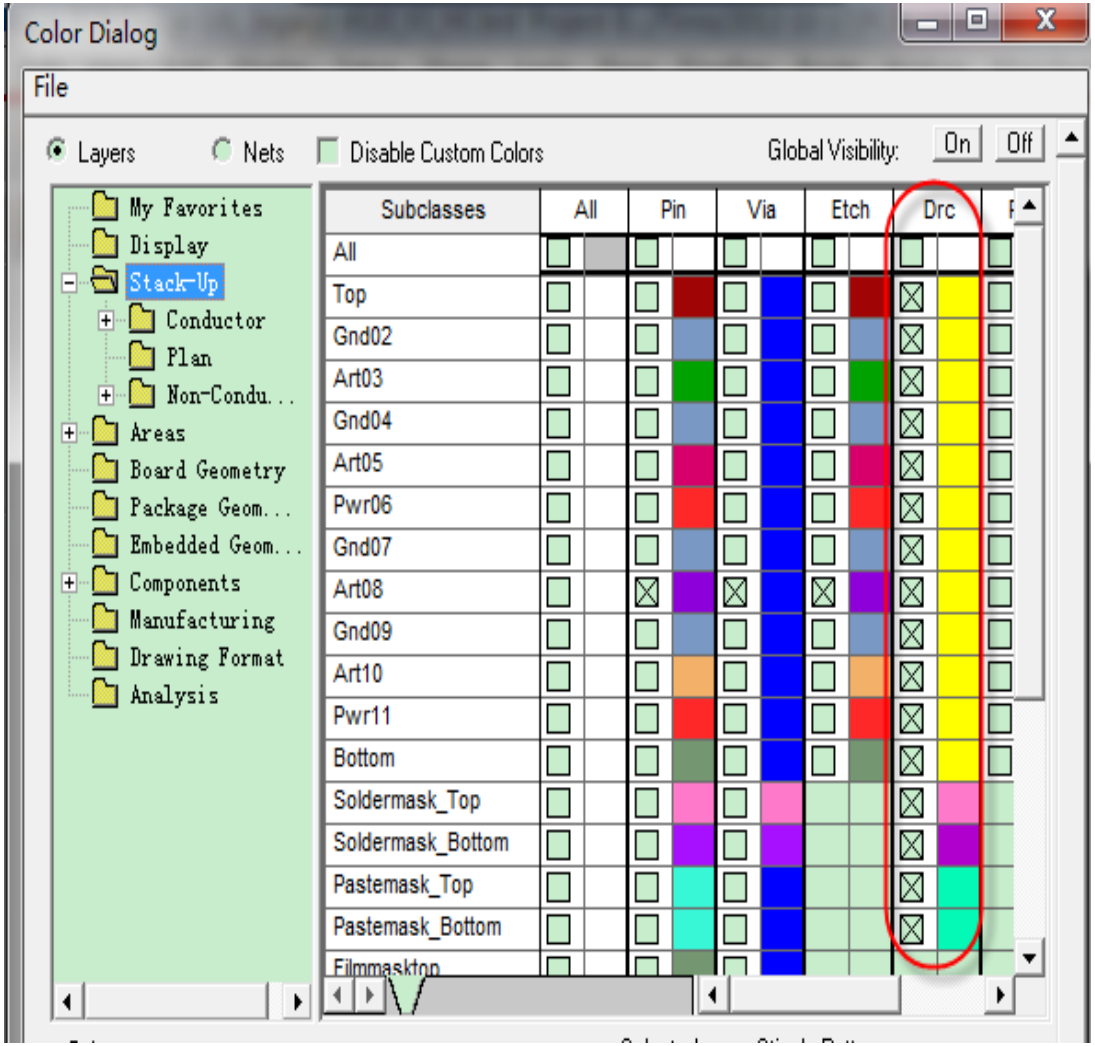
------Channel Partner COMTECH 科通

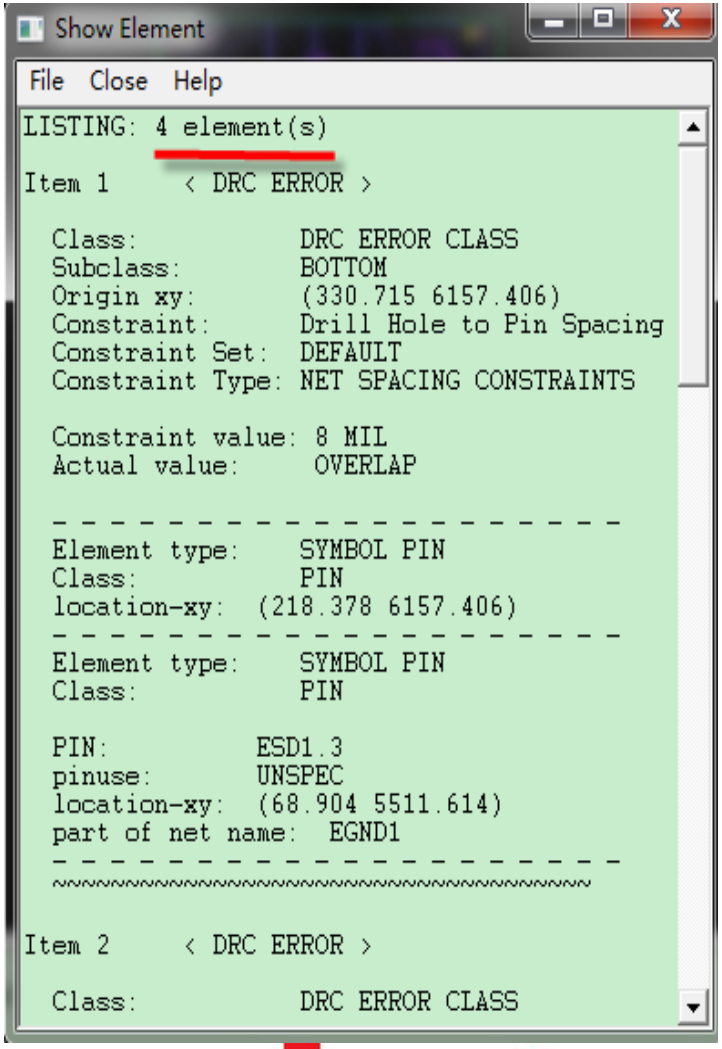
内容提要

- **Allegro DRC 代码错误释义**
- **Allegro PCB设计技巧**
  - 团队协同设计（**Physical Team Design**）
  - 设计数据的导入/导出
  - 无焊盘设计
  - 走线跨分割检查（ Segments Over Voids ）
  - 优化（**Gloss**）
  - **Data Tips**
  - **3D Viewer**
  - 任意角度走线
- 案例分析
  - **0.65 mm BGA 带DDR3案例**
  - **HDI-0.5 mm BGA 盲埋孔设计案例**

Allegro PCB设计技巧

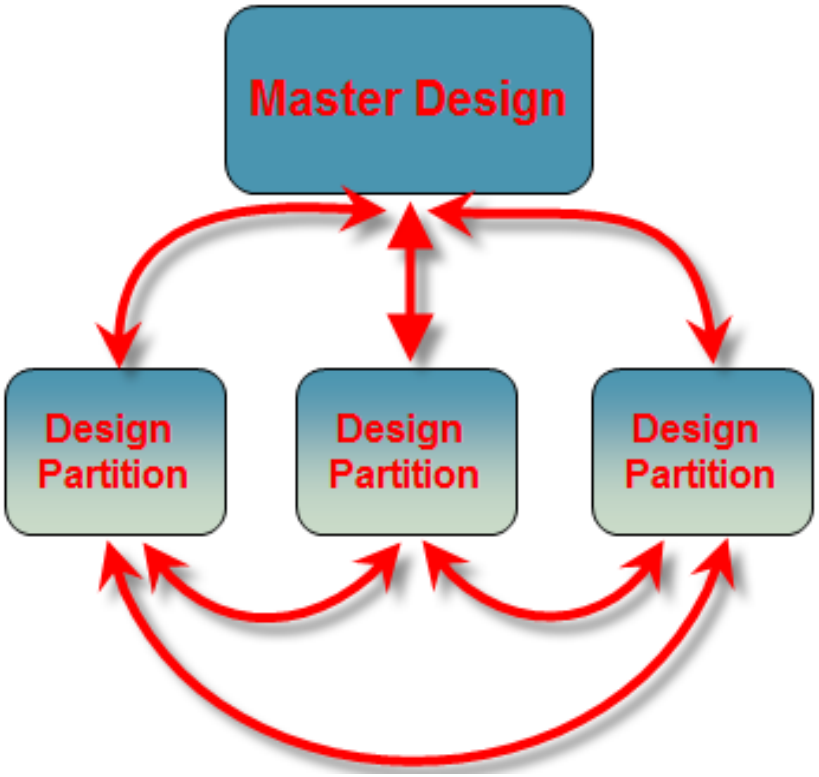
- **Allegro DRC 代码：** Allegro DRC 错误代码释义.pdf

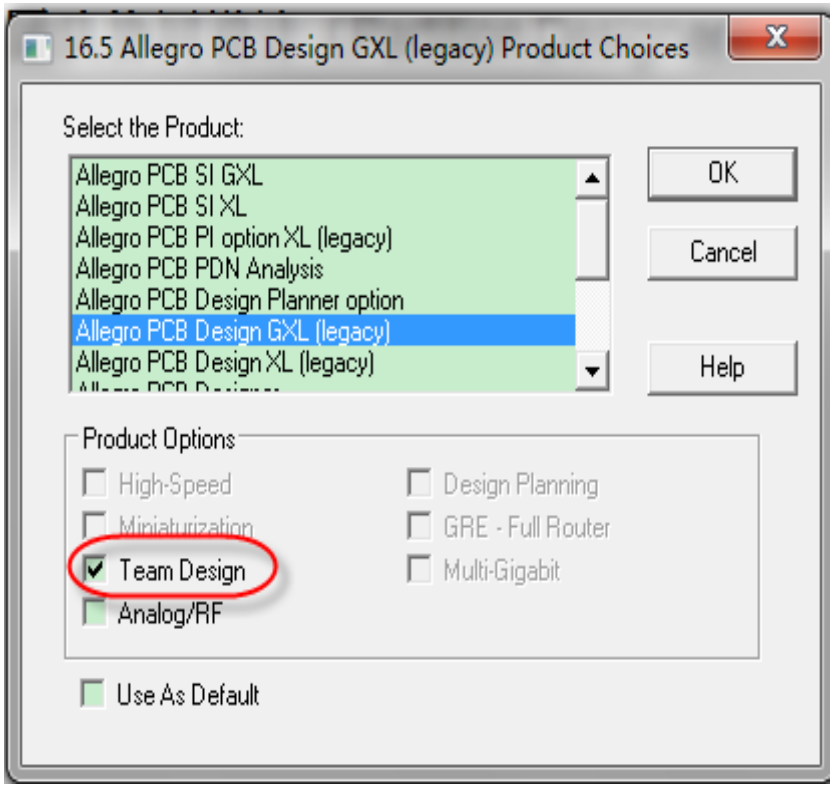




团队协同设计(Physical Team Design)

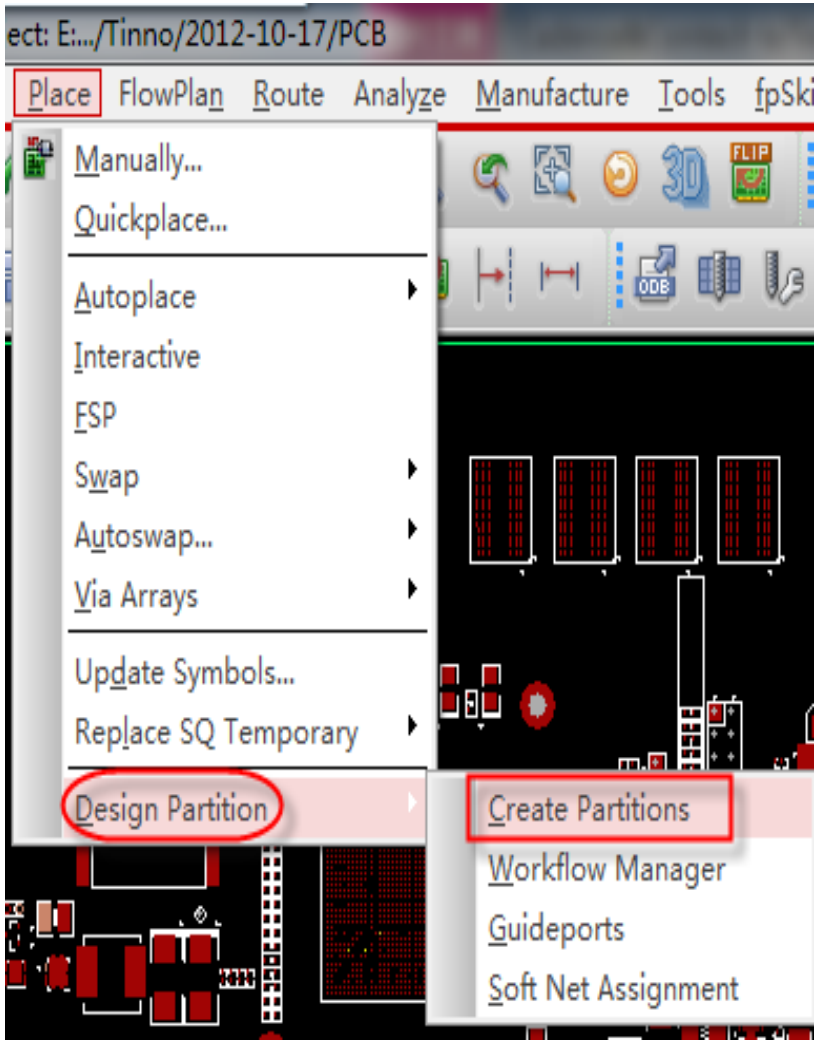
- **Design Partition**
  - 基于多人协作完成的**PCB**设计技术，可将一块复杂的**PCB**分成多个简单的**PCB**，通过团队合作设计，合并设计的方法，可以大大提升设计效率，缩短设计周期。

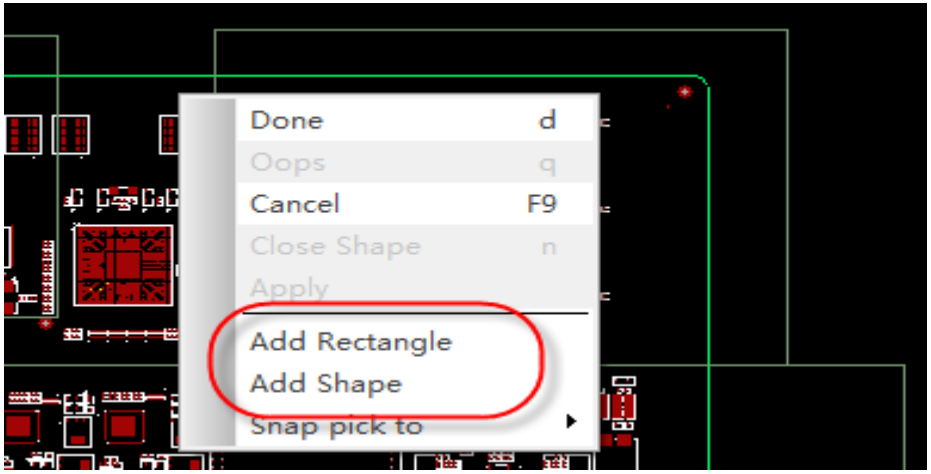


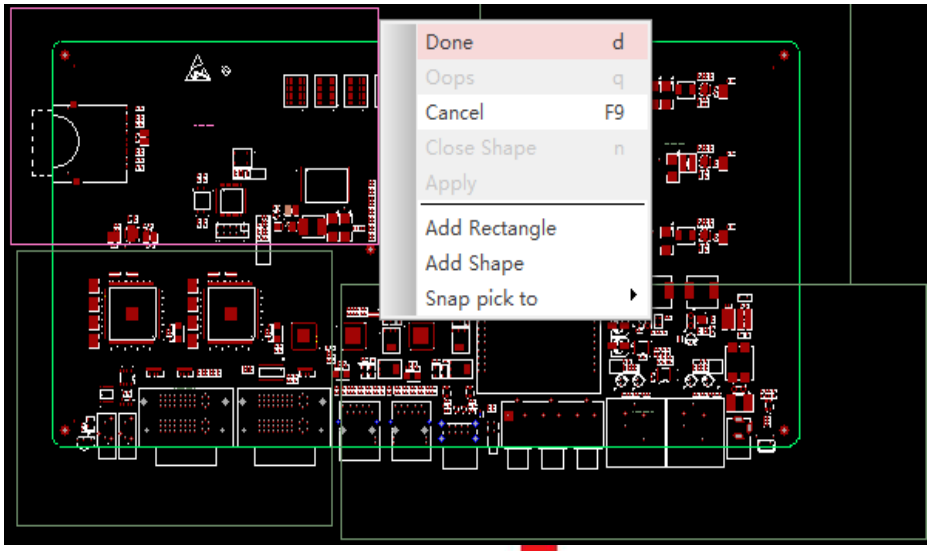


团队协同设计(Physical Team Design)

- **Design Partition-Create Partitions**

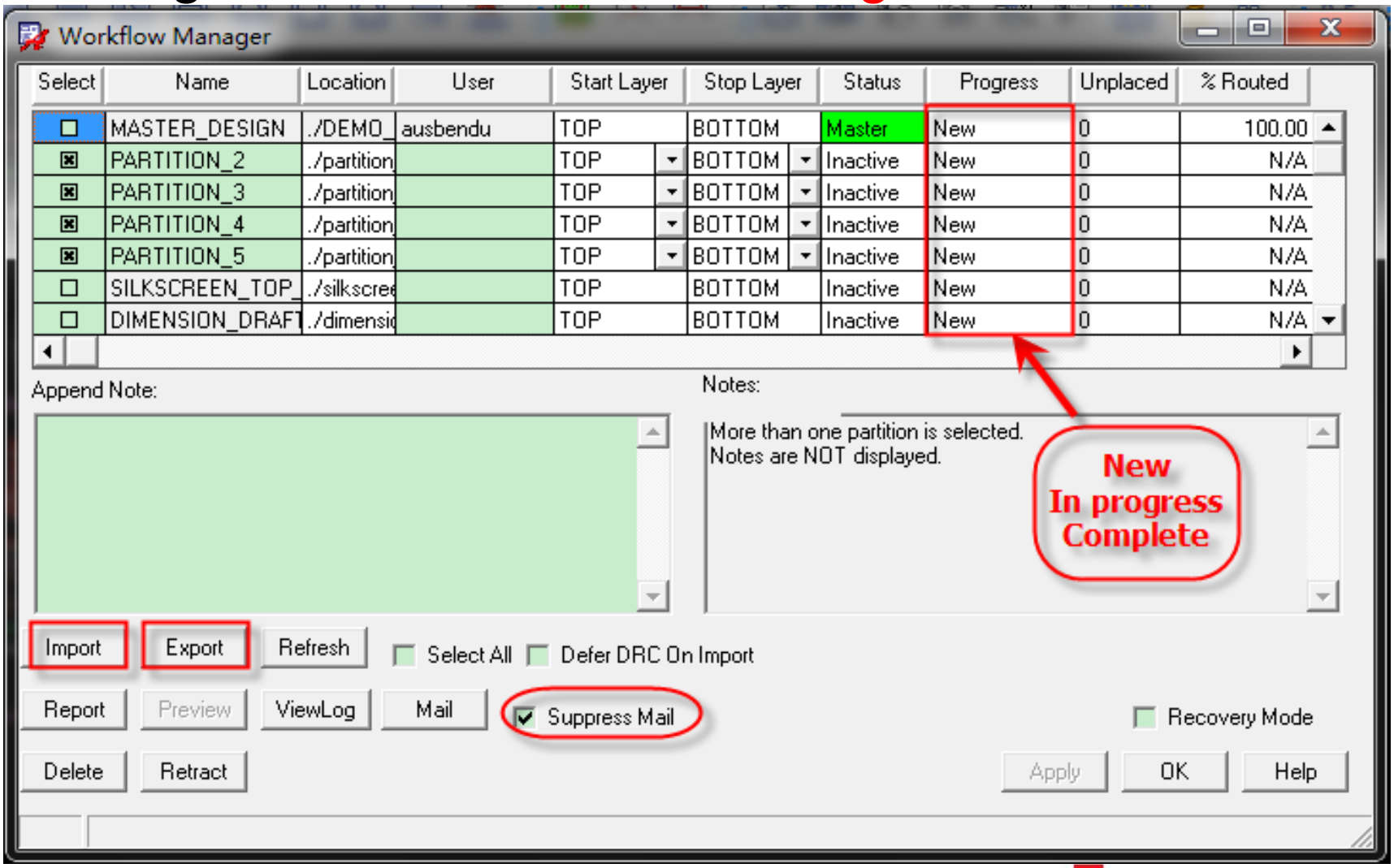






团队协同设计(Physical Team Design)

- **Design Partition-Workflow Manager**



团队协同设计(Physical Team Design)

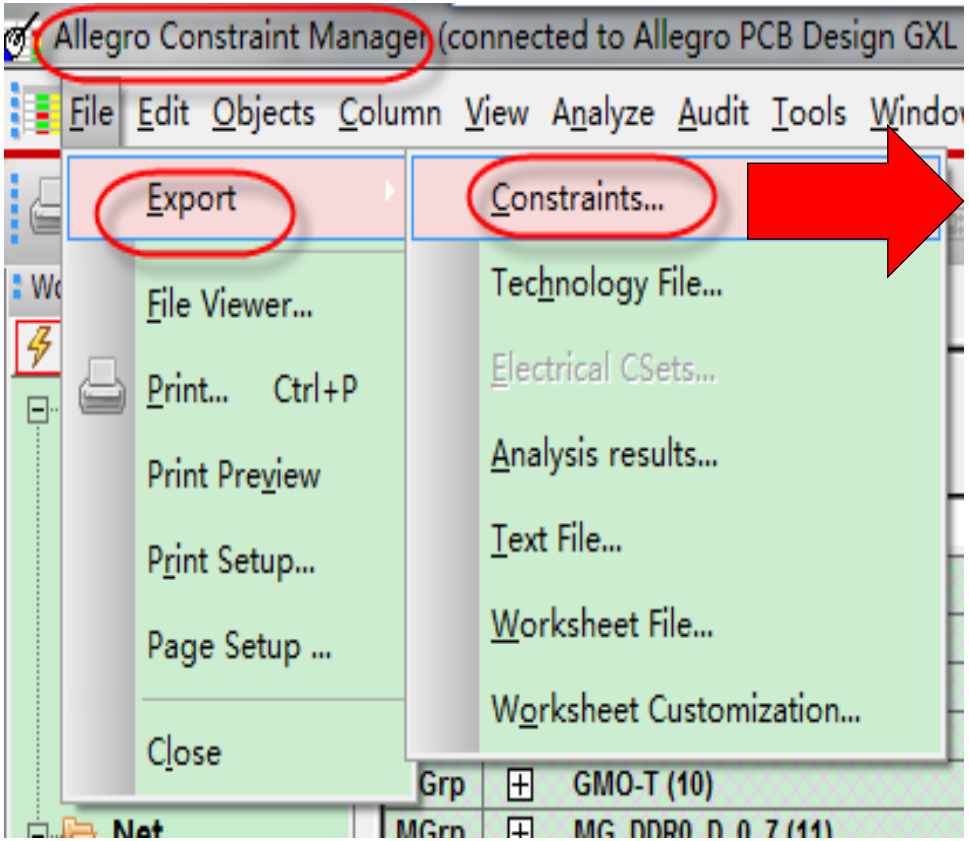
- **Design Partition-文件格式**

- 总结

  –**Allegro Partition设计过程中，子设计相互独立，只能通过Report、Refresh了解其他设计进展，工程师之间必须有较好的沟通。划分区域边界不要有小缝隙，对设计重新划分区域时需要导入所有的子设计，导入导出要有周期性，设计中注意备份。**

设计数据的导入/导出

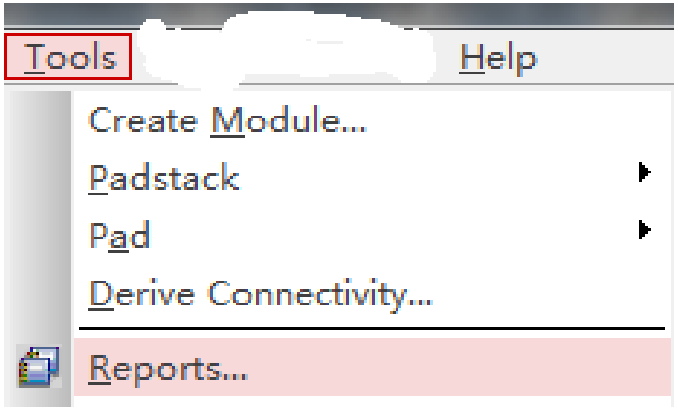
- 导出Constraint信息

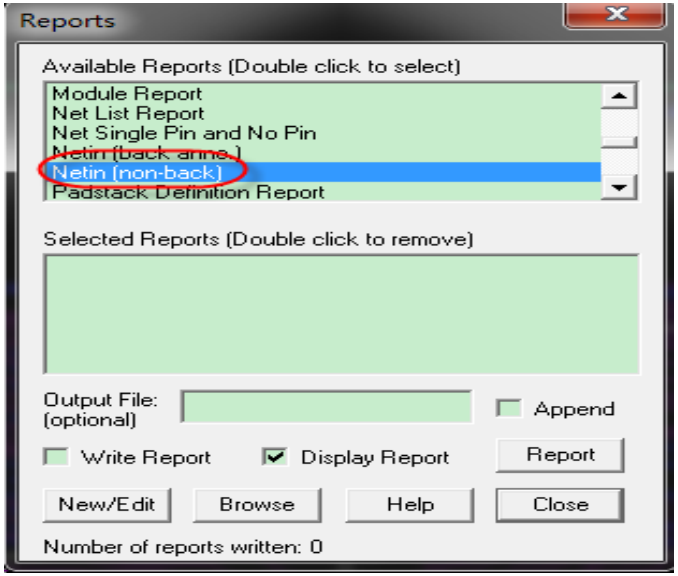


- Spacing Constraint Sets
- Physical Constraint Sets
- Extended Constraint Sets
- Electrical Constraint Sets
- Cross-Section Constraint Sets
- Net/Comp Properties

设计数据的导入/导出

- 网表导出（第三方网表，可被其他设计文件导入）

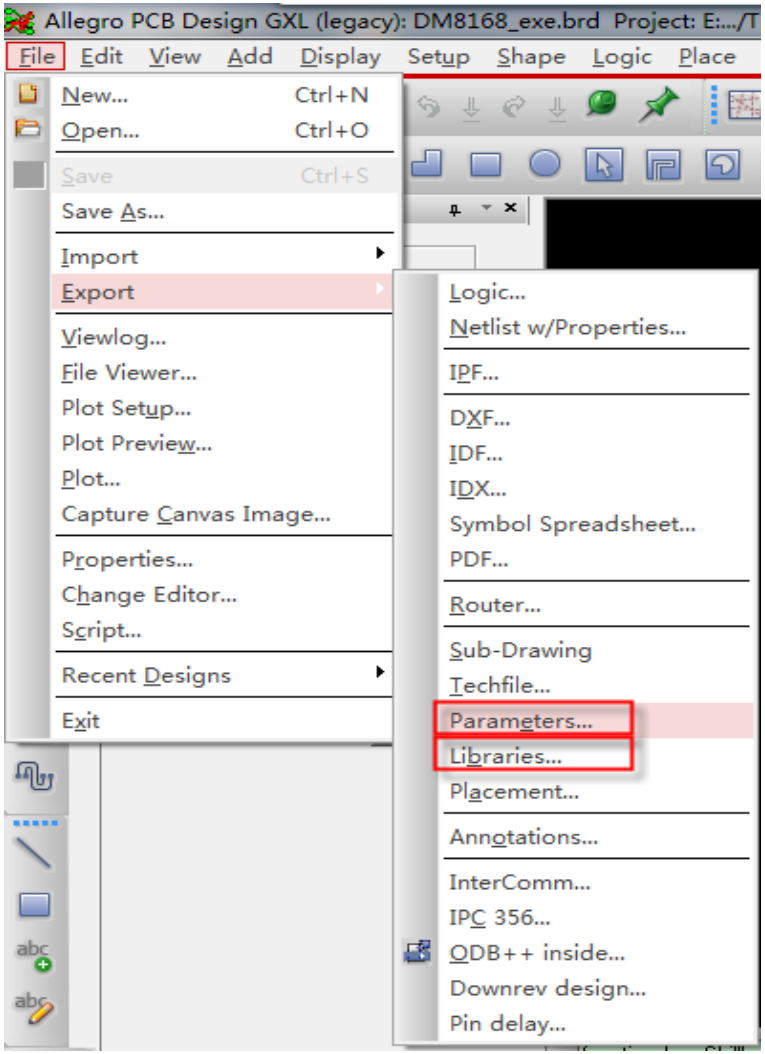


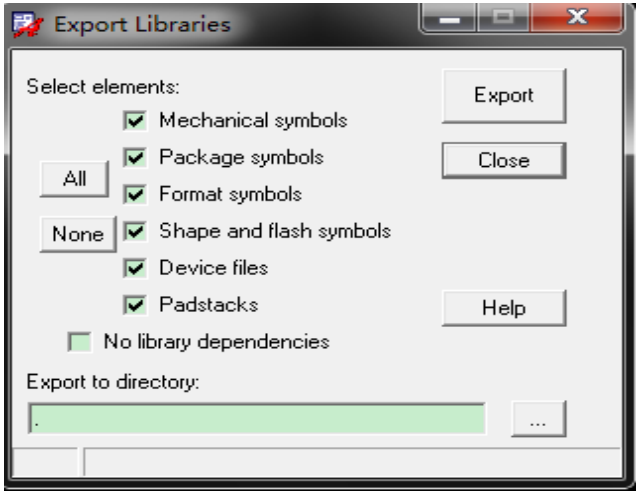


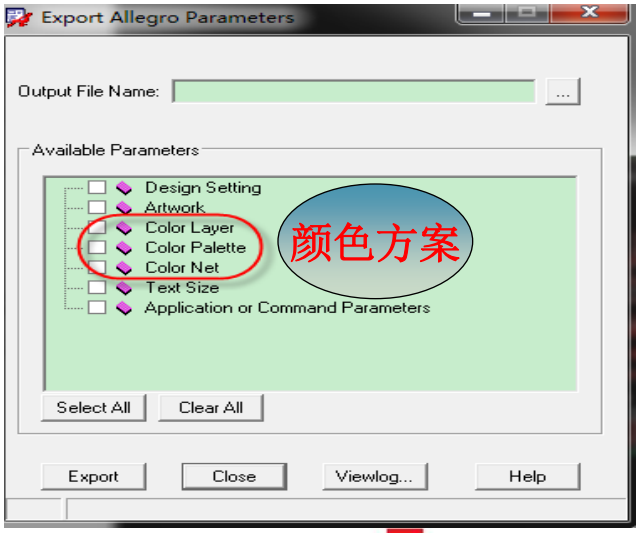

```
(NETLIST)
(FOR DRAWING: E:/Customer Case/Tinno/2012-10-17/PCB/DEMO_10_10.brd)
(Mon Oct 15 15:56:01 2012)
$PACKAGES
16TSSOP ! MAX3221CPWR_16TSSOP_MAX3221CPWR ! MAX3221CPWR ; D20
32VQFN ! TLV320AIC32_32VQFN_TLV320AIC32 ! TLV320AIC32 ; D21
'6605814-6' ! '6605814-6_6605814-6_6605814-6' ! '6605814-6' ; XXX6 XXX7
ACM1211 ! ACM1513_ACM1211_ACM1211 ! ACM1211 ; '#REFDE1'
AUDIO_JACK3 ! 'PHONEJACK STEREO_0_AUDIO_JACK3_' ! 'PHONEJACK STEREO' ; ,
        'X 1' 'X 2'
BUTTON1 ! 'SW SPST_BUTTON1_BUTTON' ! BUTTON ; S1
C_1206 ! CAP_C_1206_33UF ! 33uF ; C16 C17 C18 C19 C28 C72 C73 C77 C85 C86 ,
        C90 C91 C120 C121 C122 C123 C136 C387 C388 C389 C390 C405 C585 C597 ,
        C598 C639 C689 C694 C733 C735 C787 C789
C_7343 ! CAP_C_7343_180UF ! 180uF ; C7 C8 C26 C44 C45 C61 C66 C268 C398 ,
        C561 C592 C596
C_DIP ! CAP_C_DIP_10UF ! 10uF ; C105
C_DIP_2MM ! CAP_C_DIP_2MM_10UF ! 10uF ; C125 C126 C127 C128
C_EIA0402 ! 'CAP NP_C_EIA0402_0.01UF' ! '0.01uF' ; C25 C27 C32 C33 C34 C38 ,
        C401 C412 C501 C546 C547 C551 C570
C_EIA0402 ! 'CAP NP_C_EIA0402_0.1UF' ! '0.1uF' ; C46 C47 C48 C49 C68 C69 ,
        C70 C71 C92 C96 C112 C113 C141 C142 C143 C144 C145 C146 C147 C148 ,
        C149 C150 C151 C152 C153 C154 C155 C156 C157 C158 C159 C160 C161 ,
        C162 C163 C164 C165 C166 C167 C168 C169 C170 C171 C172 C173 C174 ,
        C175 C176 C177 C178 C179 C180 C181 C182 C183 C184 C185 C186 C187 ,
        C188 C189 C190 C192 C193 C194 C195 C196 C197 C199 C200 C201 C202 ,
        C203 C204 C205 C206 C207 C208 C209 C210 C211 C212 C213 C214 C215 ,
        C216 C217 C219 C220 C221 C222 C223 C224 C225 C226 C227 C228 C229 ,
        C230 C231 C232 C233 C234 C235 C236 C237 C238 C239 C240 C241 C242 ,
        C243 C244 C247 C248 C249 C250 C251 C252 C254 C255 C256 C257 C258 ,
        C259 C260 C261 C262 C263 C264 C265 C266 C267 C269 C270 C271 C272 ,
        C273 C274 C275 C276 C277 C278 C280 C281 C282 C283 C284 C285 C286 ,
```

设计数据的导入/导出

- 导出库/设计参数文件

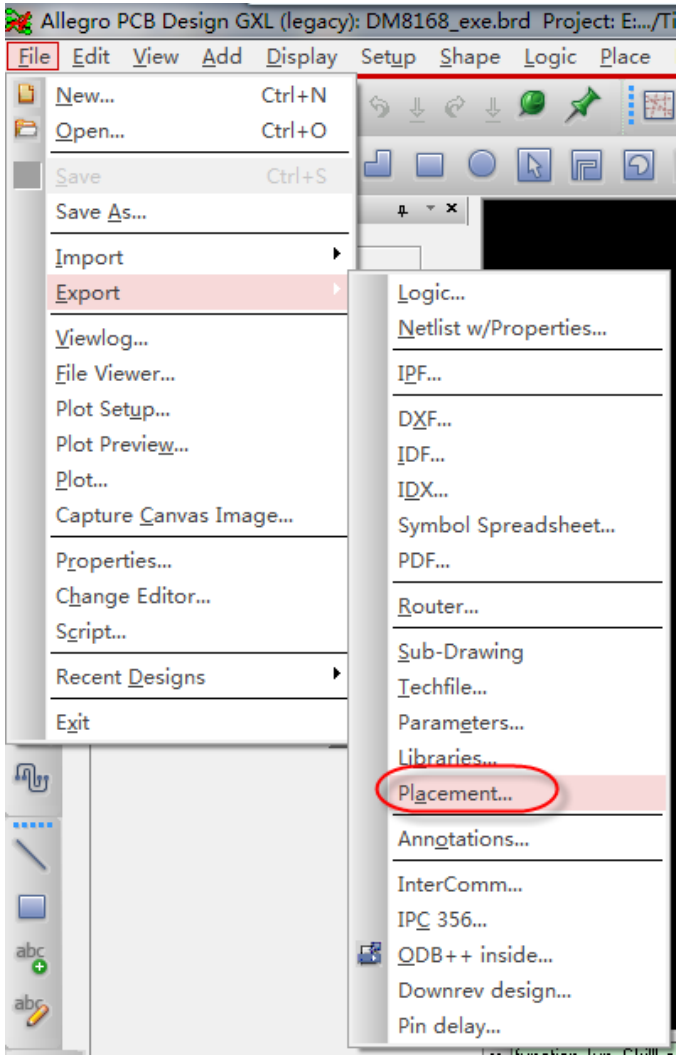


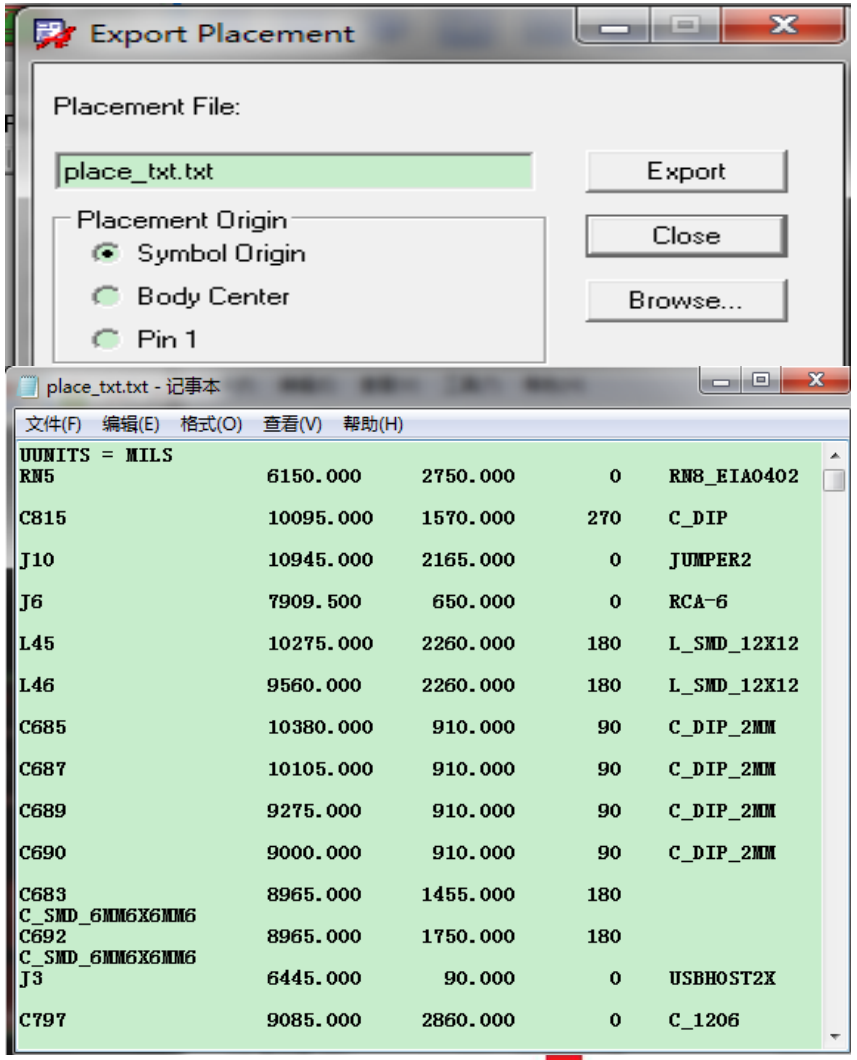




设计数据的导入/导出

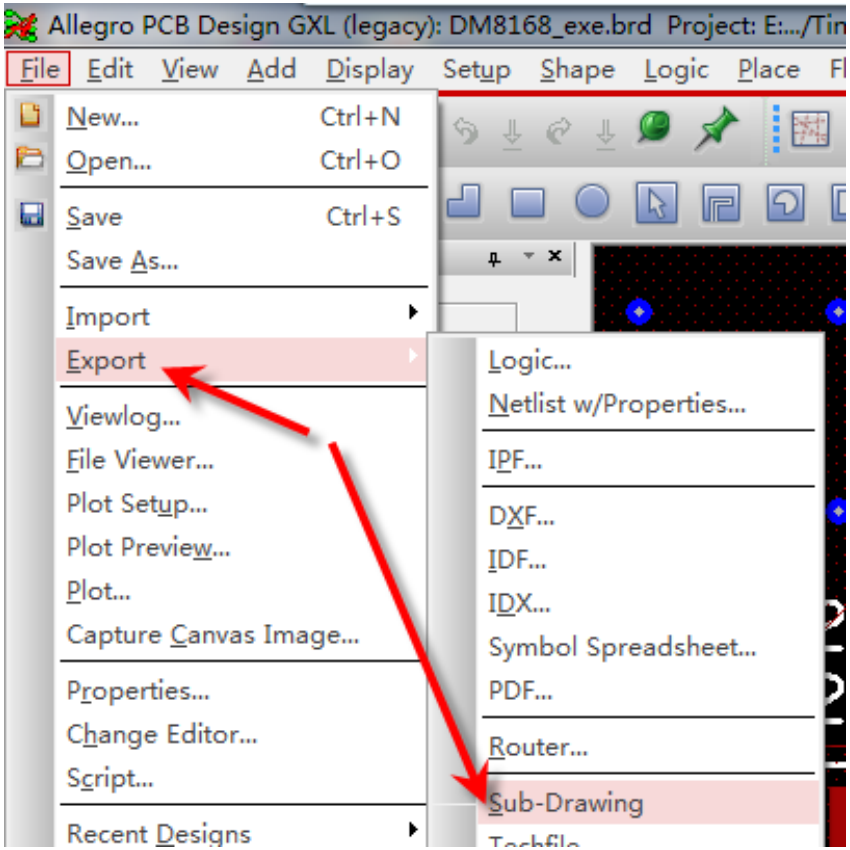
- 导出布局文件





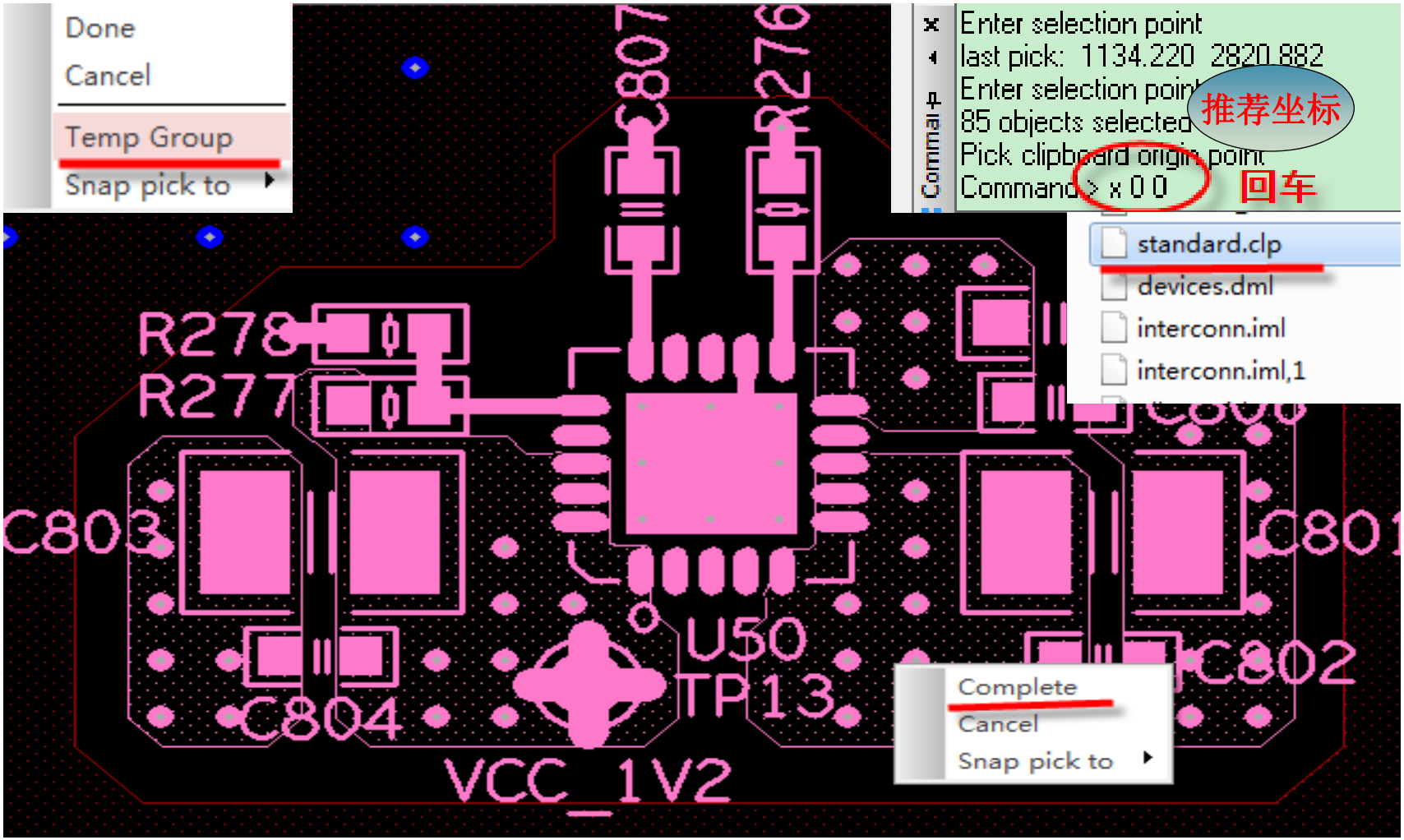
设计数据的导入/导出

- 导出**Sub Drawing**
  - 此功能非常强大，可以完成几乎所有的可见数据的传递和复用，包括布局、布线、标注等。



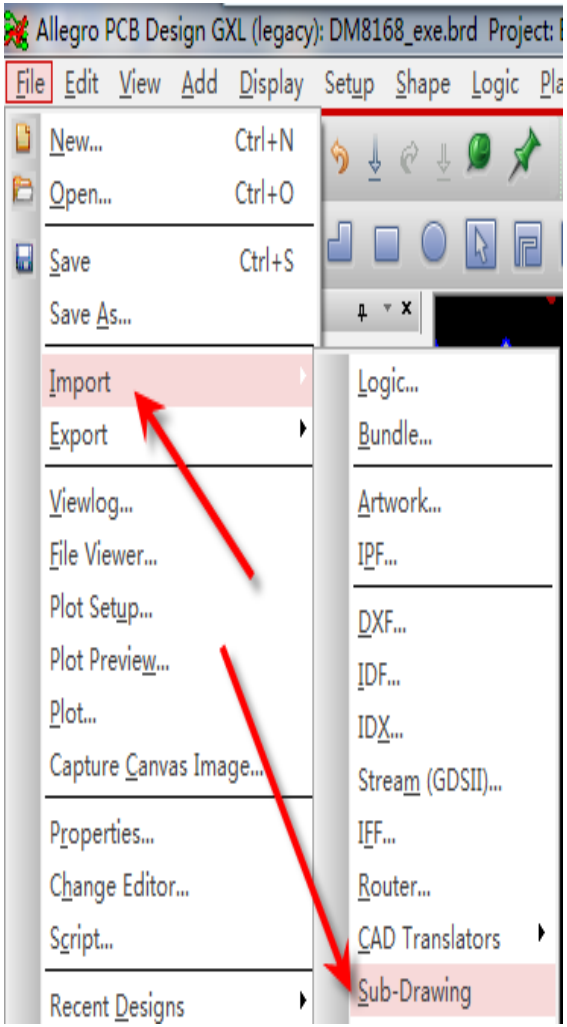
设计数据的导入/导出

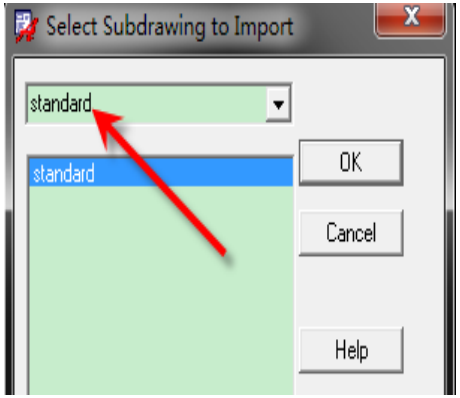
- 导出**Sub Drawing**

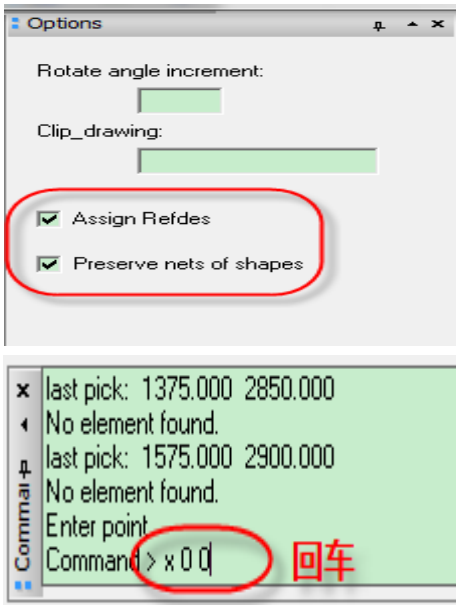


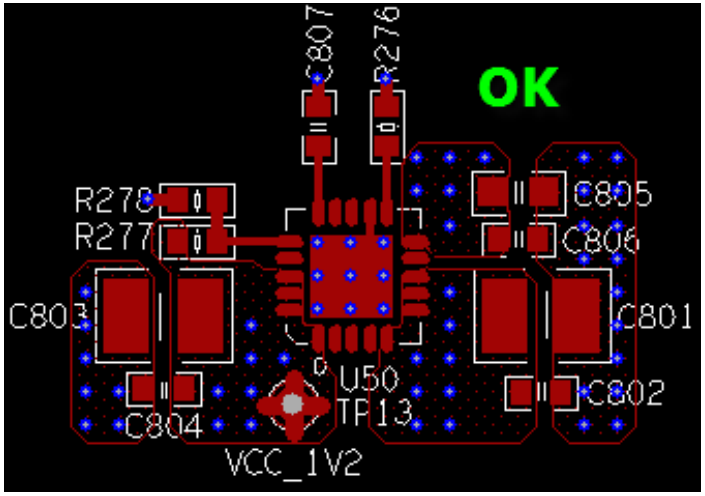
设计数据的导入/导出

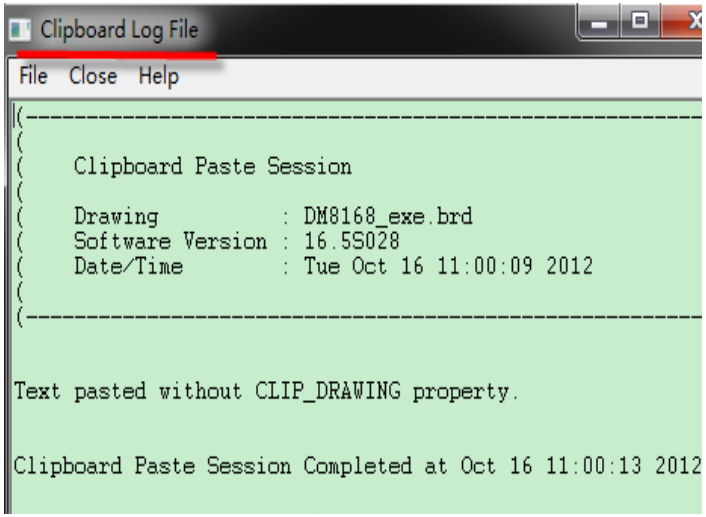
- 导入**Sub Drawing**





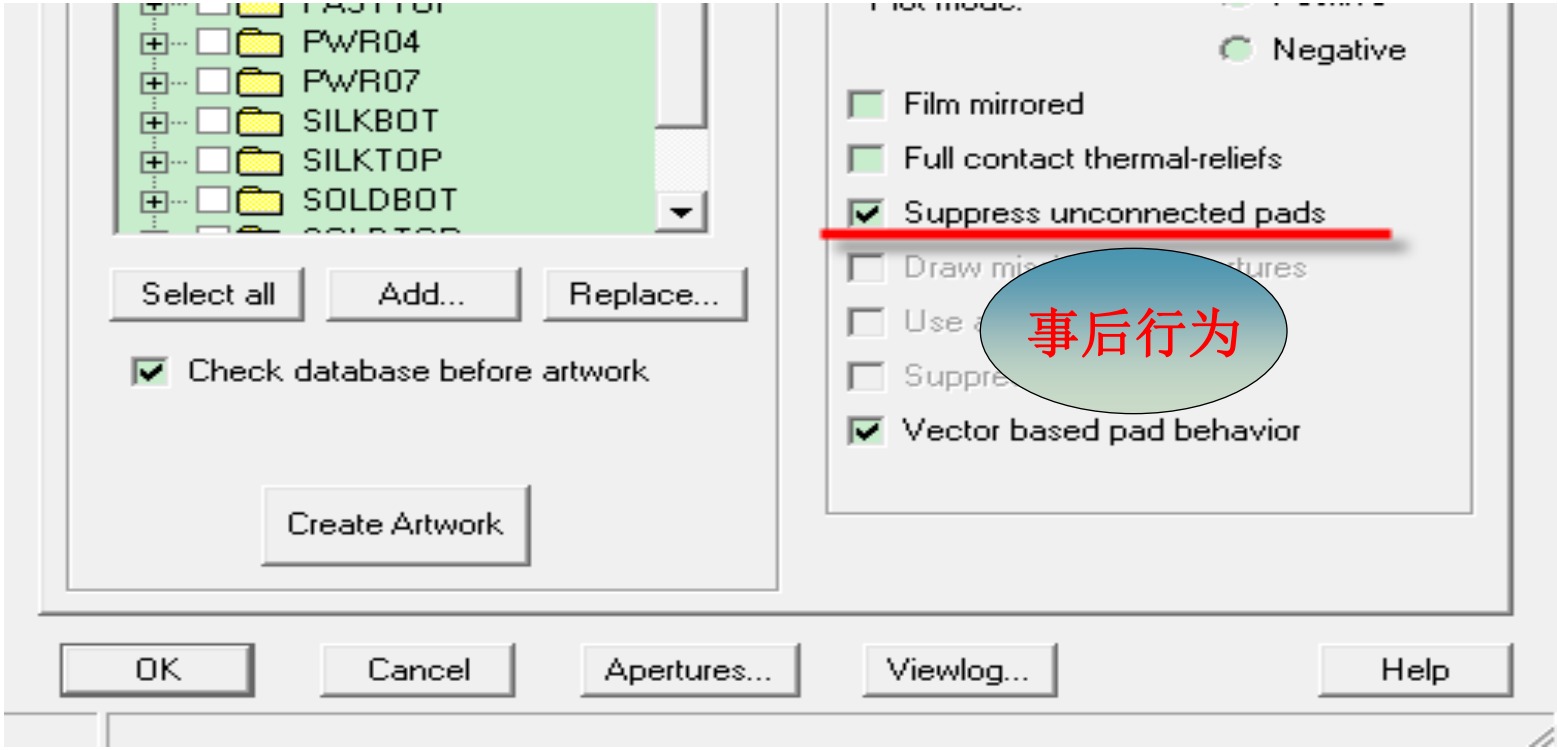






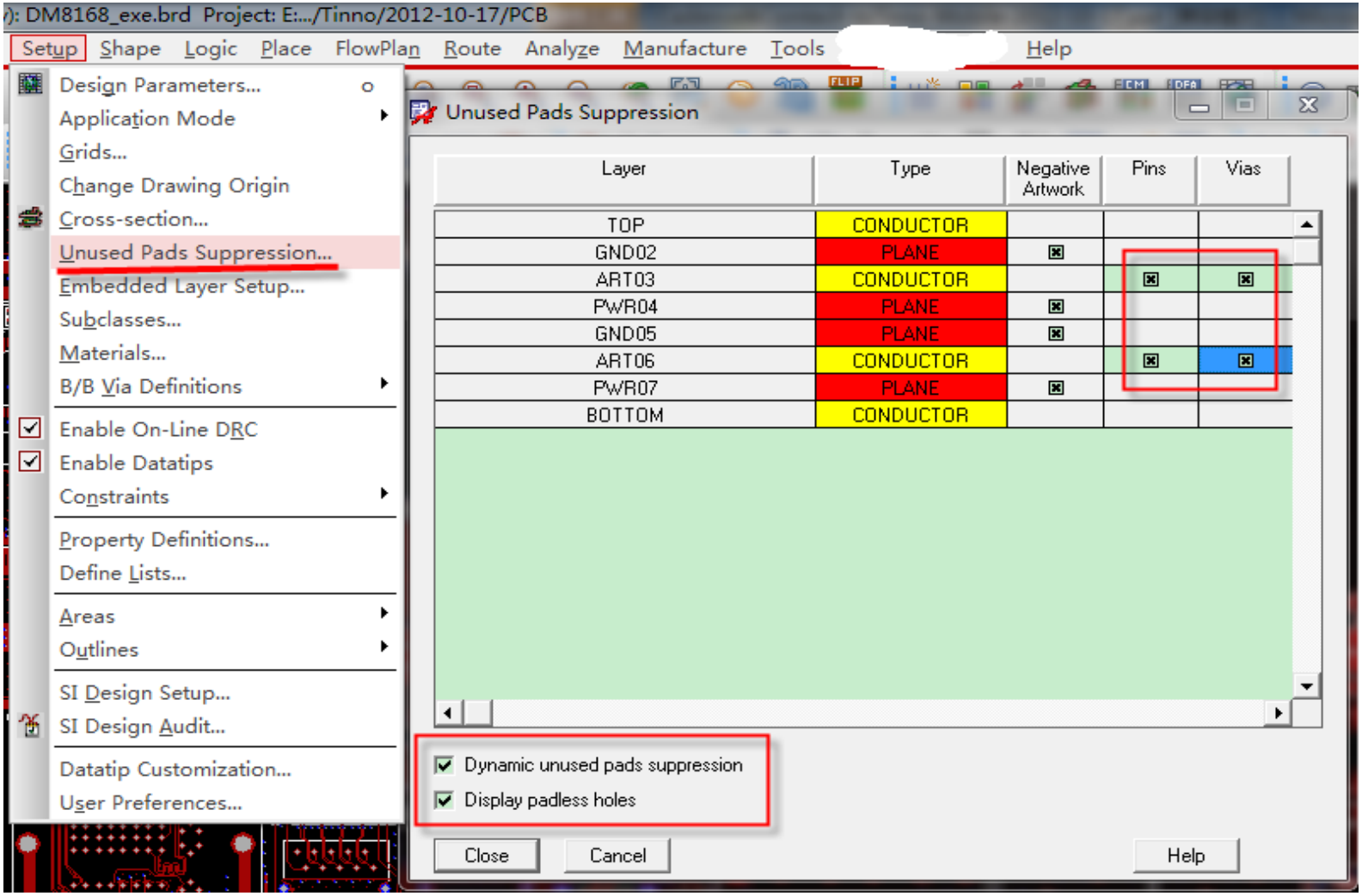
无焊盘设计

- 高密场合，如高密的BGA区域
- HDI小型化设计，如0.65的BGA，不想用盲埋孔来设计
- 高速设计要求，去除无用焊盘可以提升高速性能
  - Allegro有2个地方可以实现无盘设计



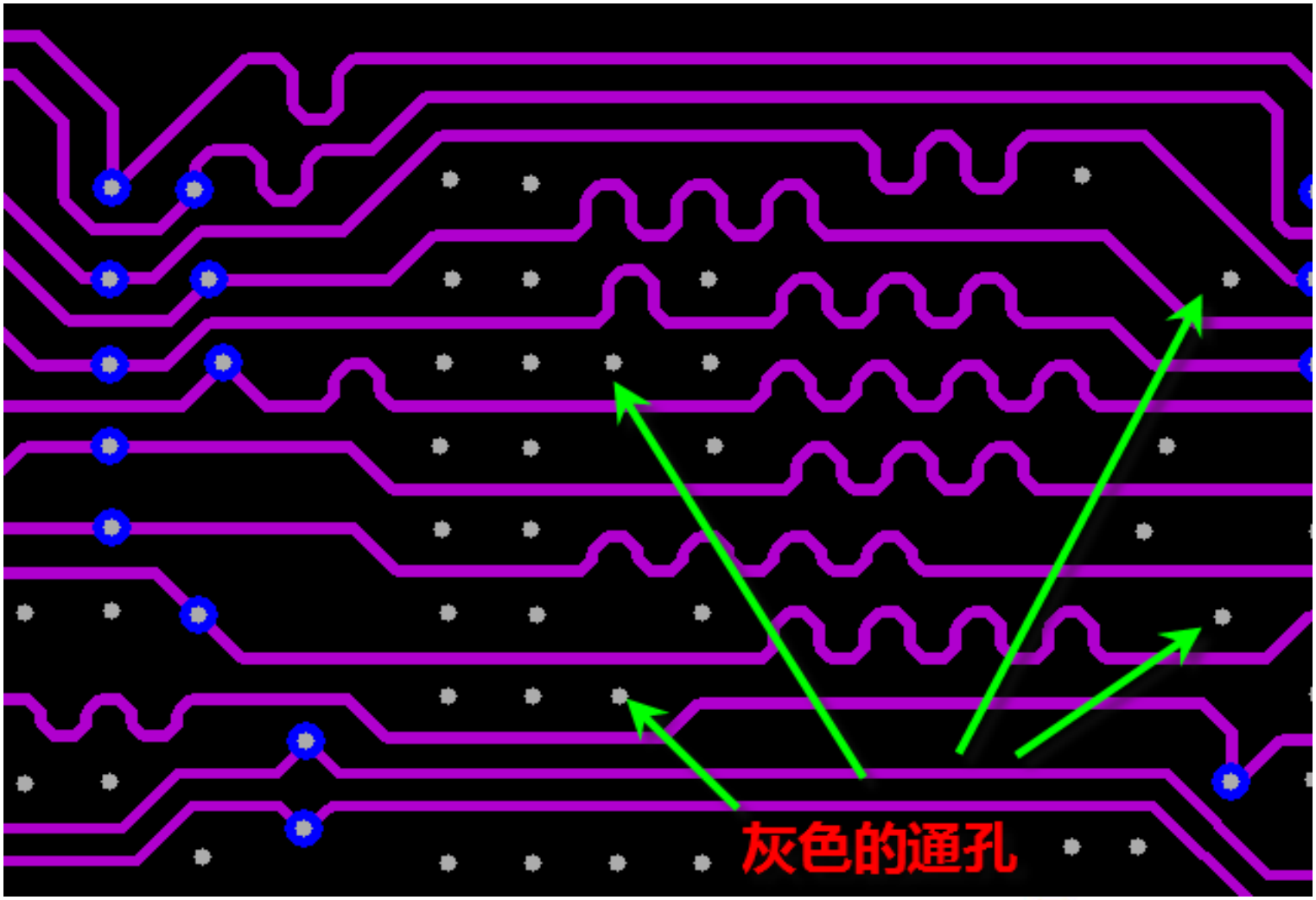
无焊盘设计

– 无盘设计的前处理模式



无焊盘设计

– 无盘设计优化后



无焊盘设计

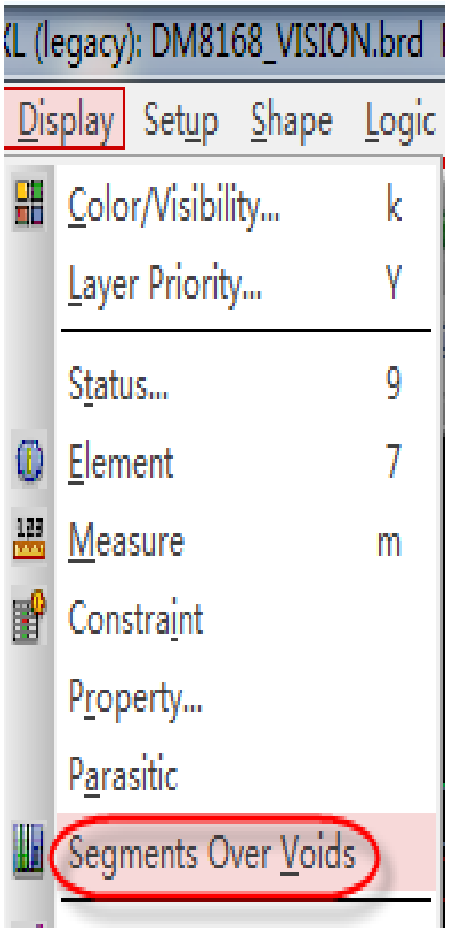
- 无盘设计相关技术问题
  - 单独显示孔的颜色和背景区分开
  - 设置孔（**Hole**）到其他元素的物理和间距规则

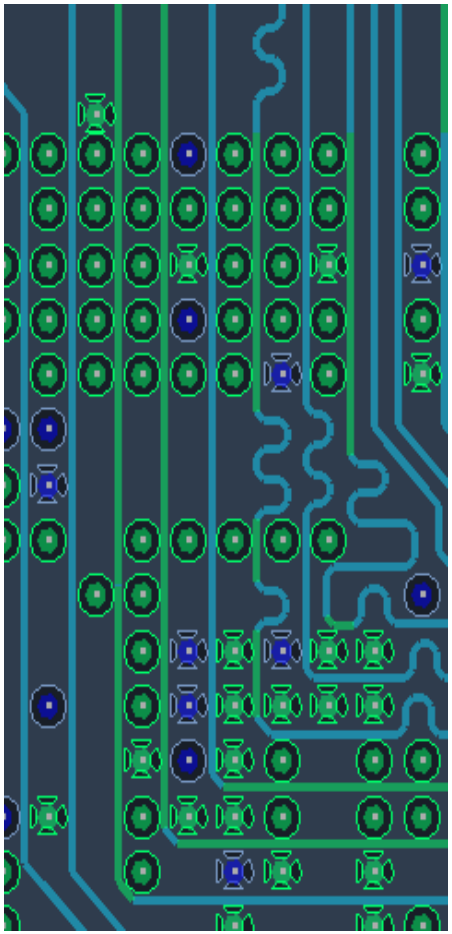
Type	Objects	Hole To				
		Line	Pin	Via	Shape	Hole
		mil	mil	mil	mil	mil
*	*	*	*	*	*	*
Dsn	⊟ DM8168_VISION	8.000	8.000	5.000	10.000	8.000
SCS	⊞ BGA	8.000	8.000	5.000	10.000	8.000
SCS	⊞ BGA0.8	8.000	8.000	5.000	10.000	8.000
SCS	⊞ DEFAULT	8.000	8.000	5.000	10.000	8.000
SCS	⊞ 1	8.000	8.000	5.000	10.000	8.000

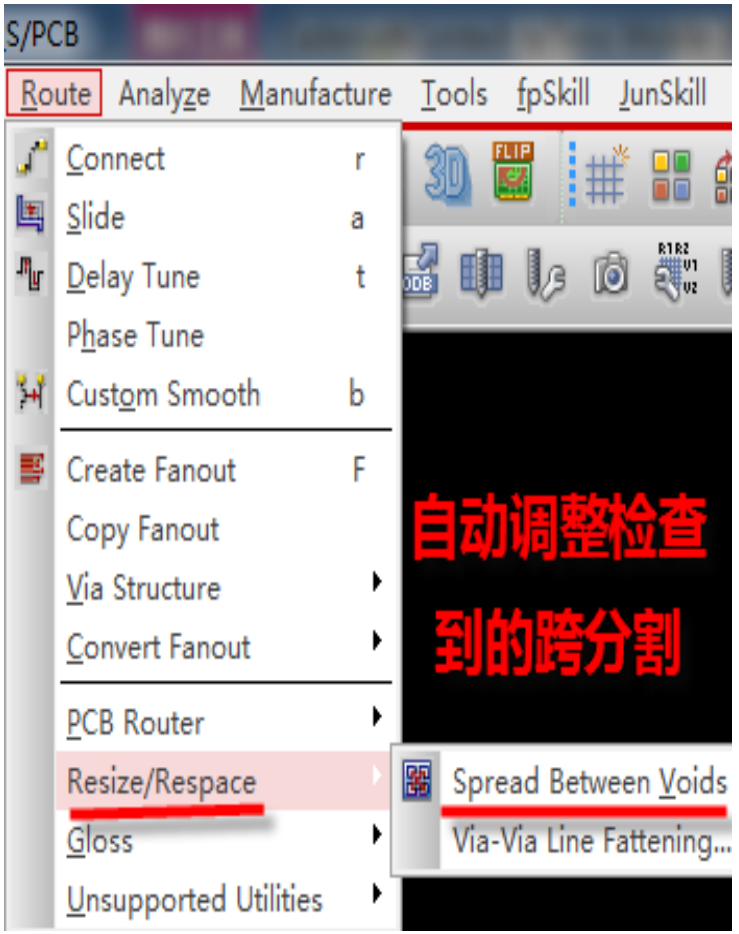
注：Hole到Cline或者shape的的距离，不能和有焊盘时一样，设置为4~5Mil，大部分板厂不具备这样的生产能力。

大于8mil才是比较保险的值

走线跨分割检查（Segments Over Voids）

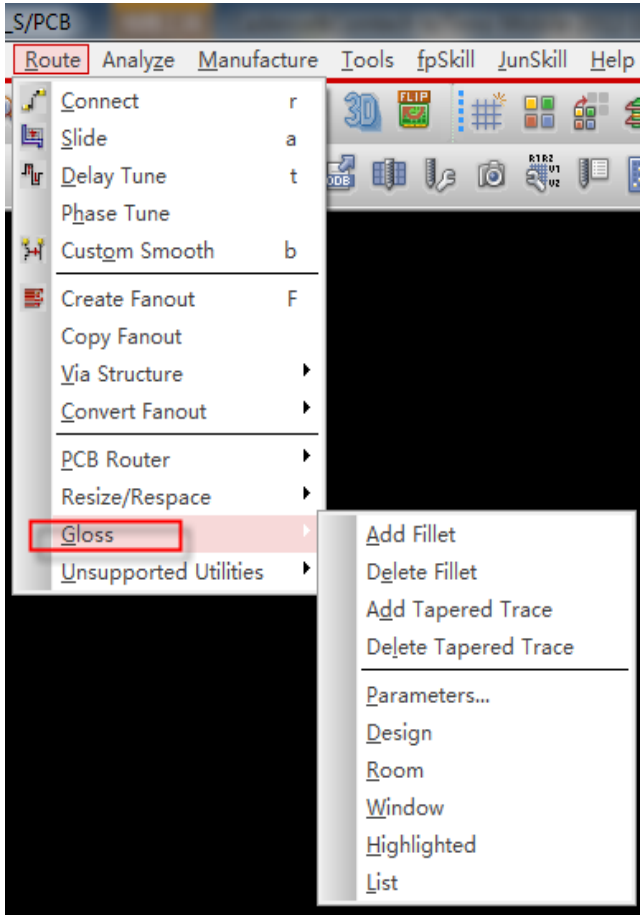


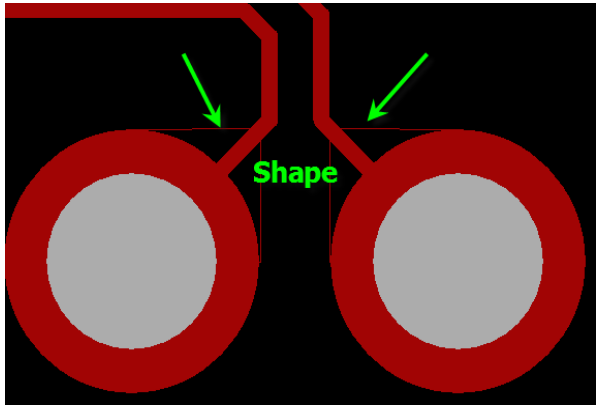


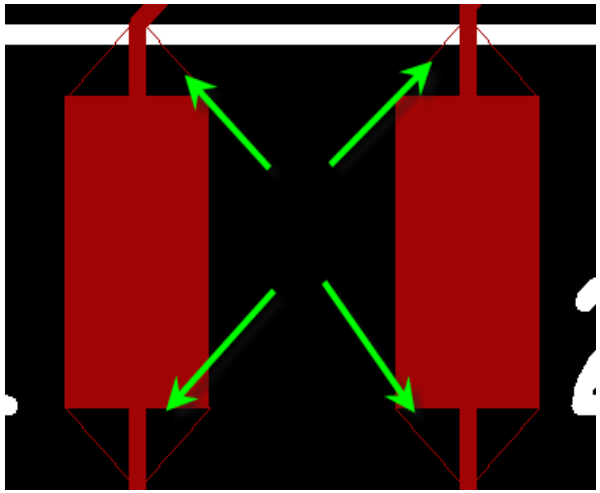


优化（Gloss）

- **Gloss是为了布线后消除一些多余的过孔及把曲线拉直，会是连接部分添加泪滴焊盘，便于制造。**

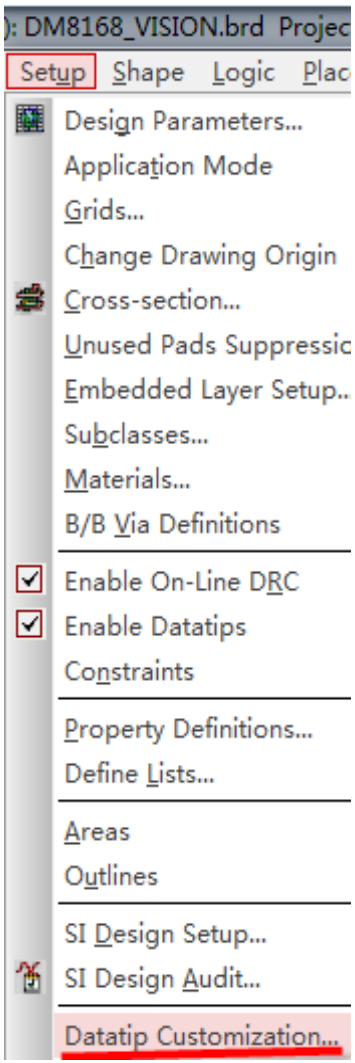


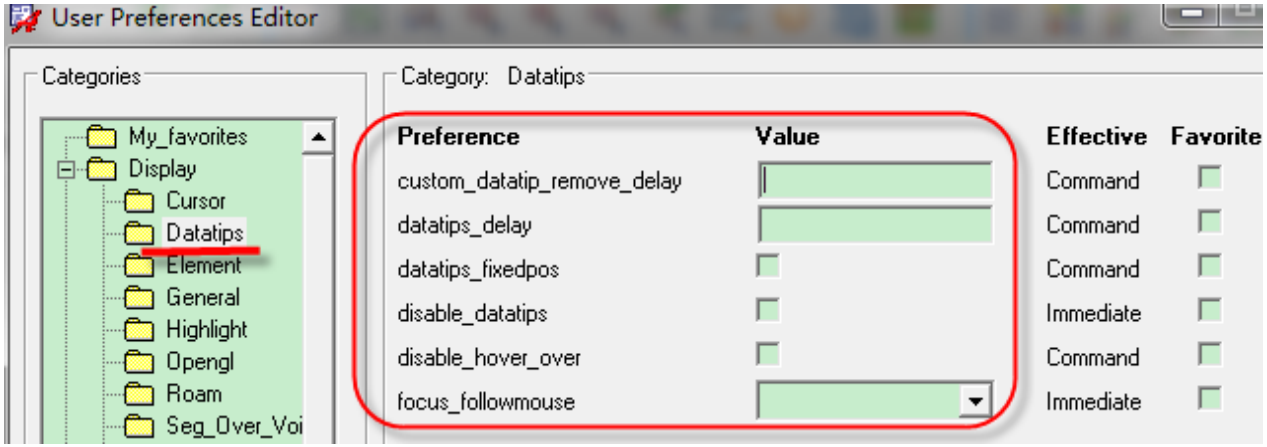


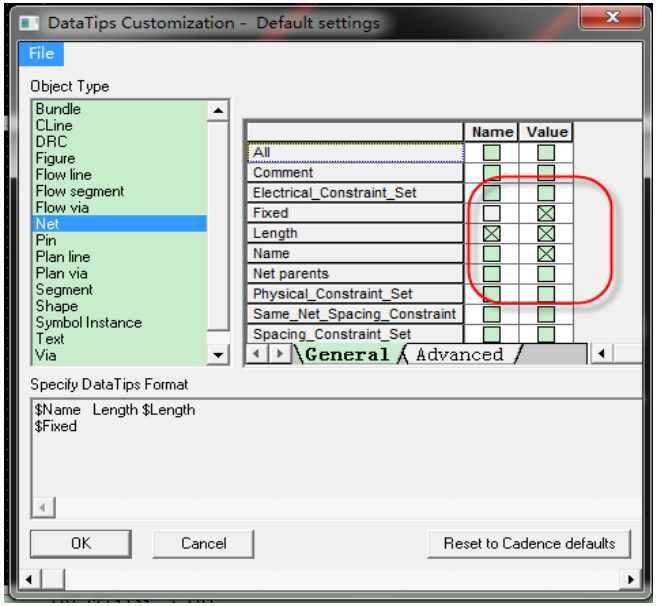


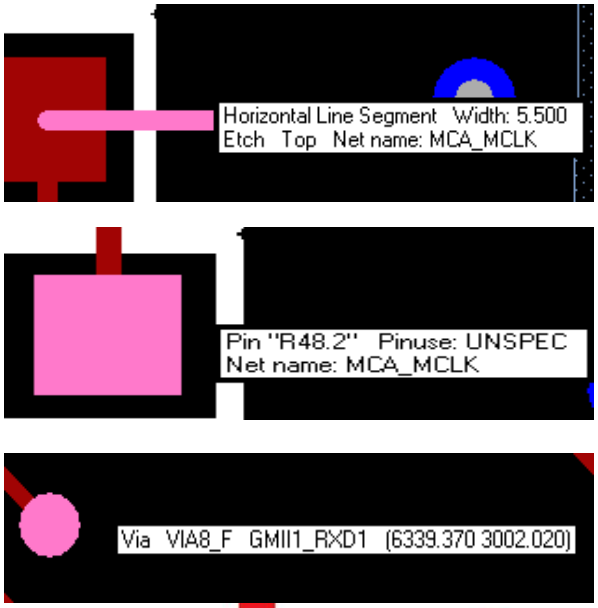
Data Tips

- **Data Tips是为了提示用户当前所选物体的具体属性。**

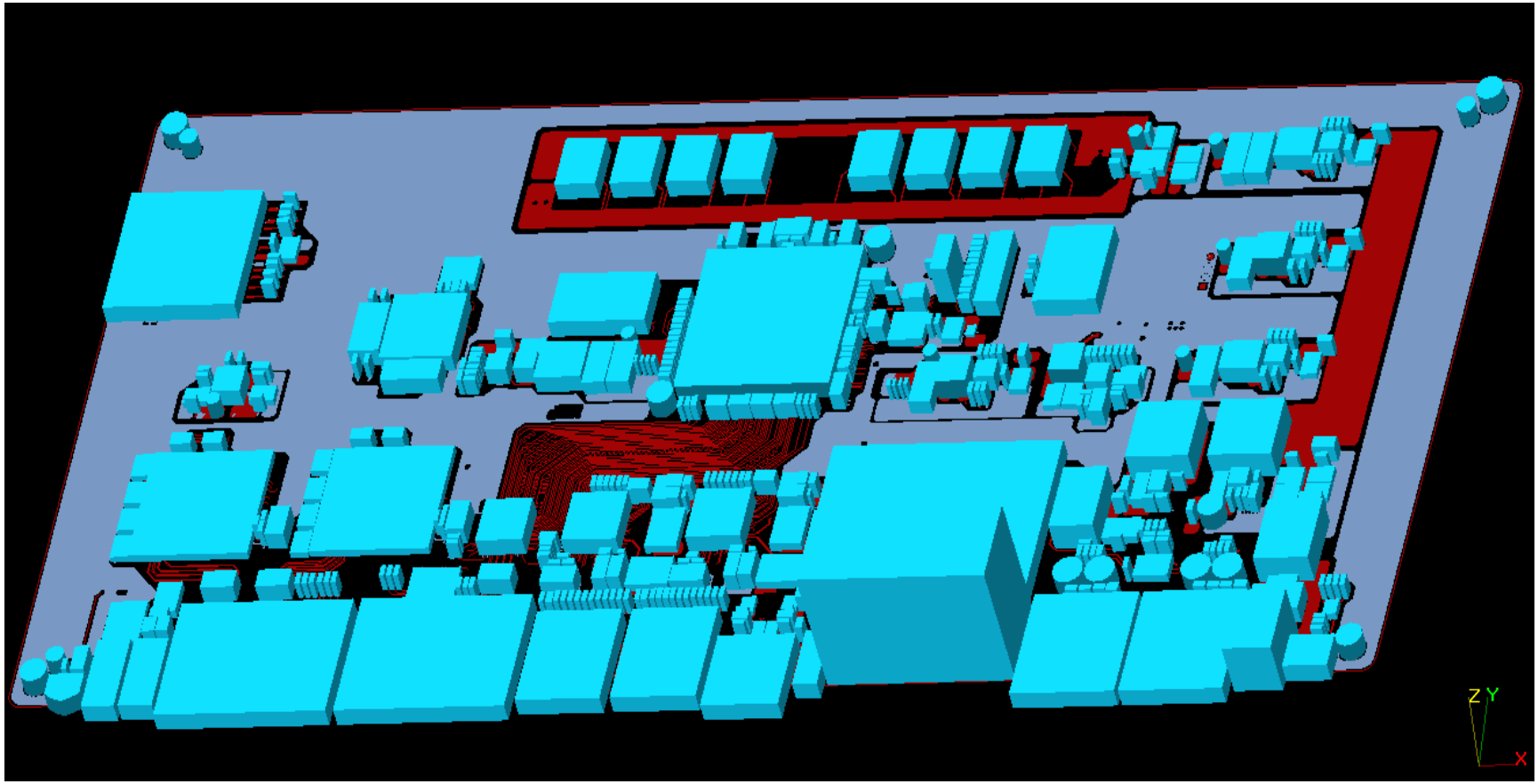






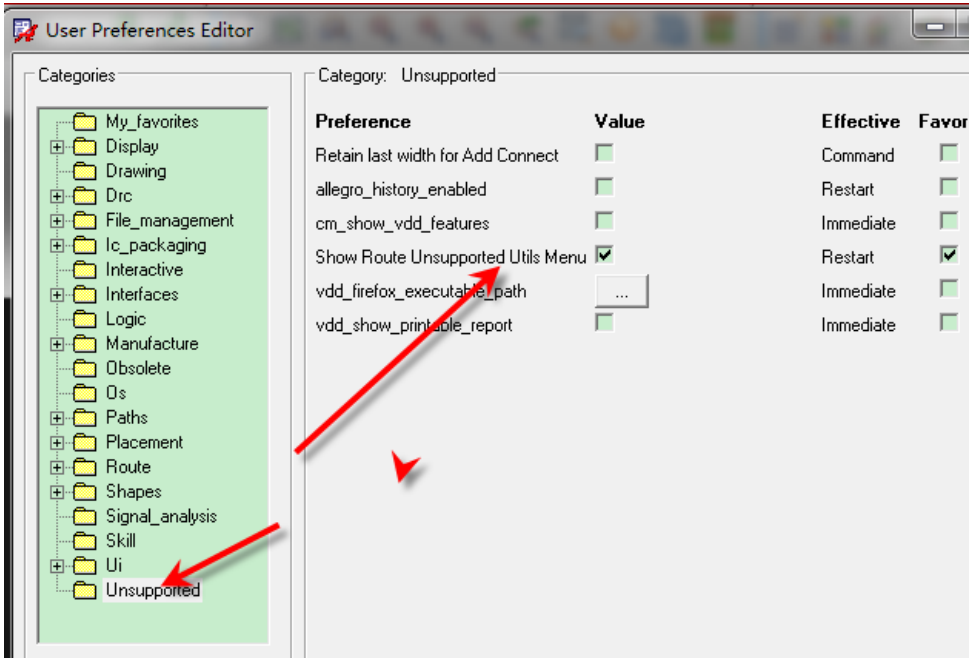


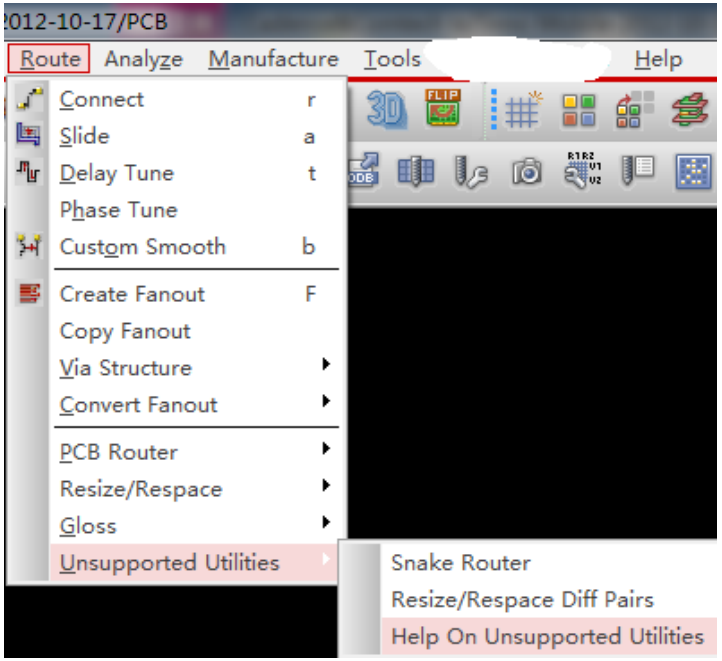
3D Viewer

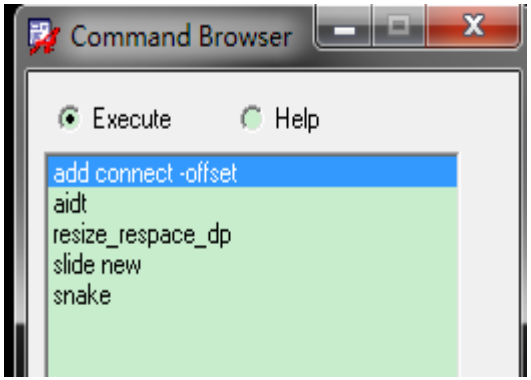


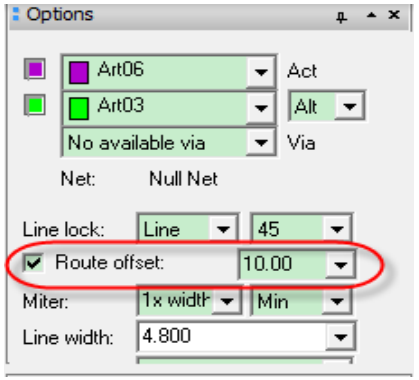
任意角度走线

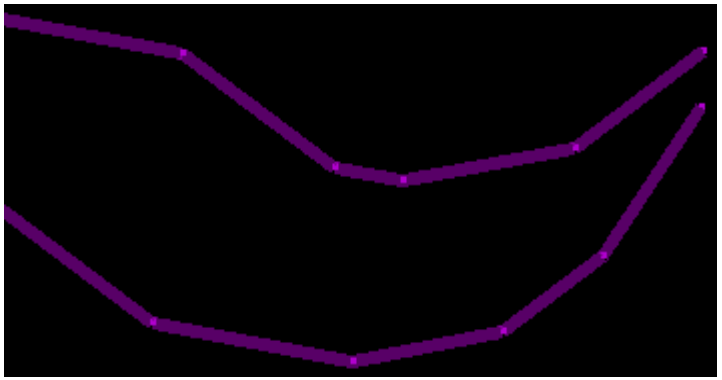
- 考虑材料对信号的影响





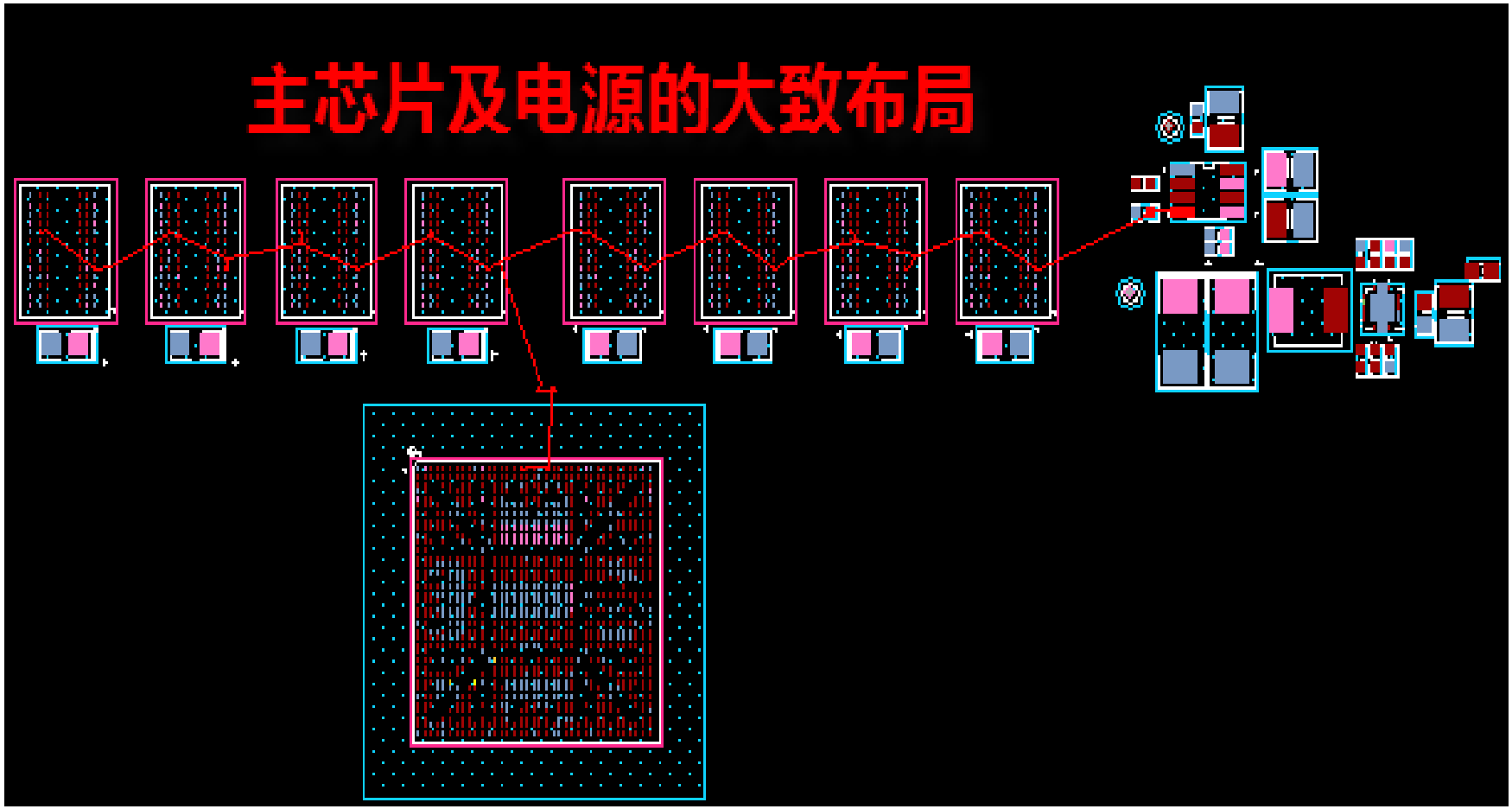






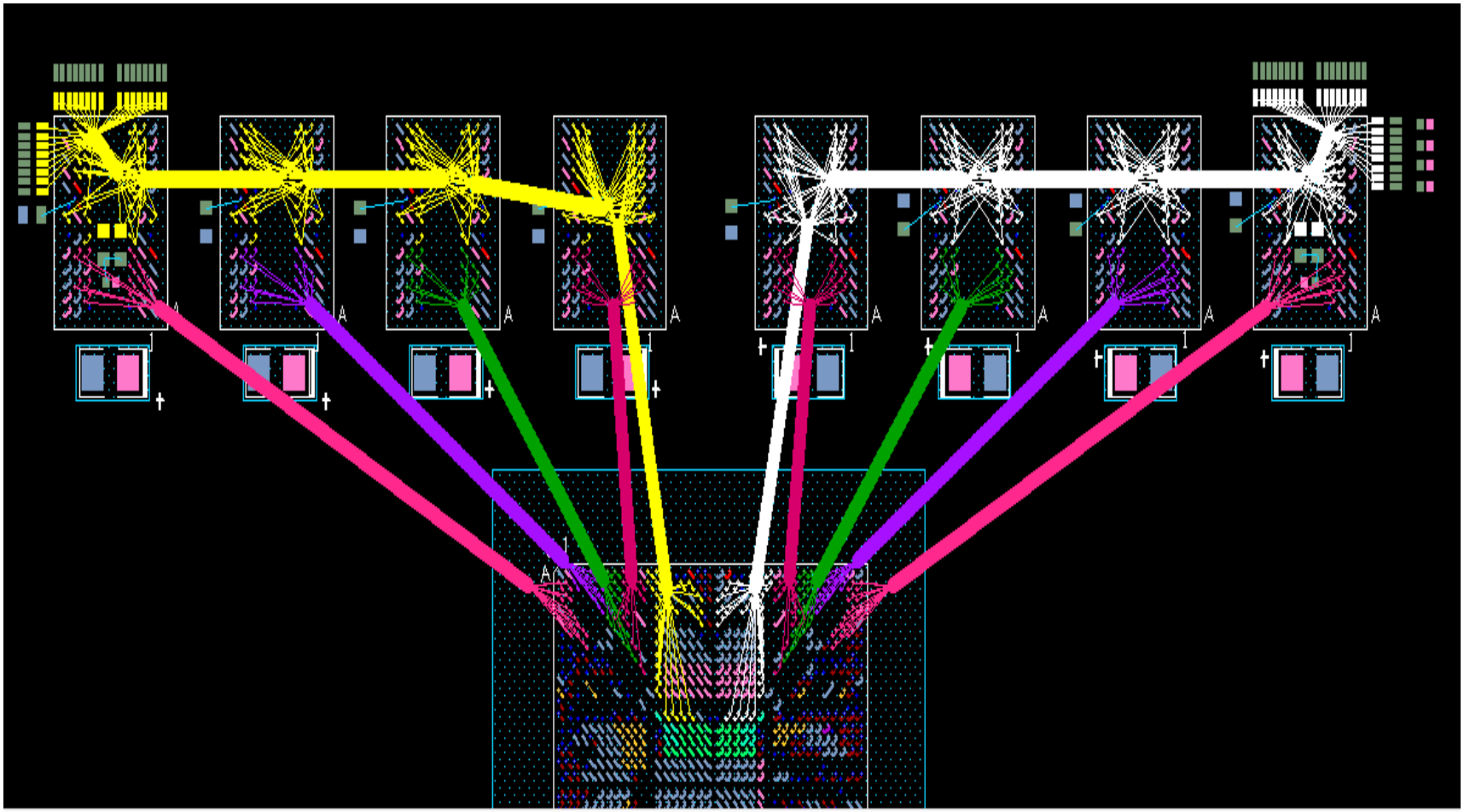
0.65 mm BGA带DDR3案例

- 主芯片布局（双通道Fly-By）



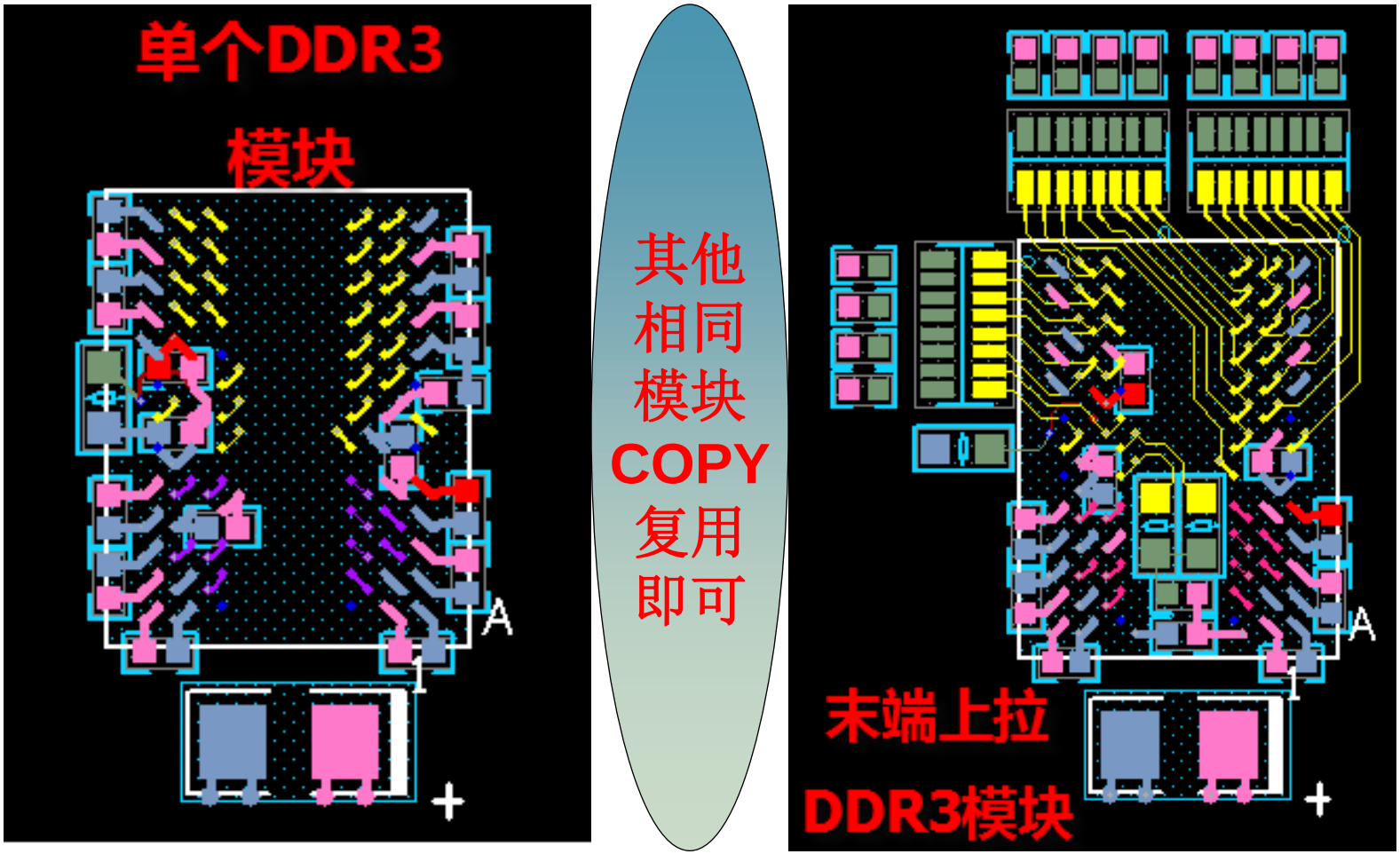
0.65 mm BGA带DDR3案例

- 主芯片Fanout（规则已经设置Ok）



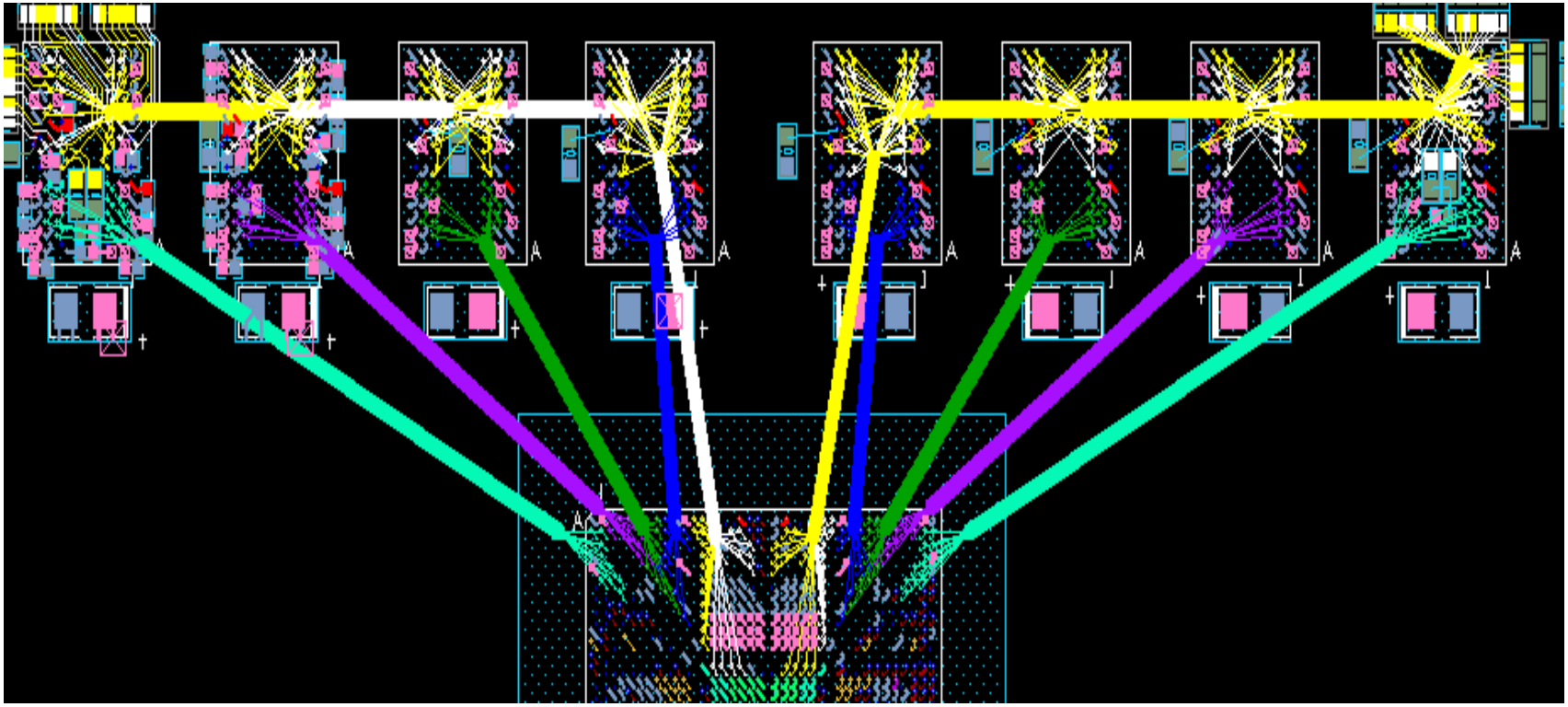
0.65 mm BGA带DDR3案例

- 滤波电容放置



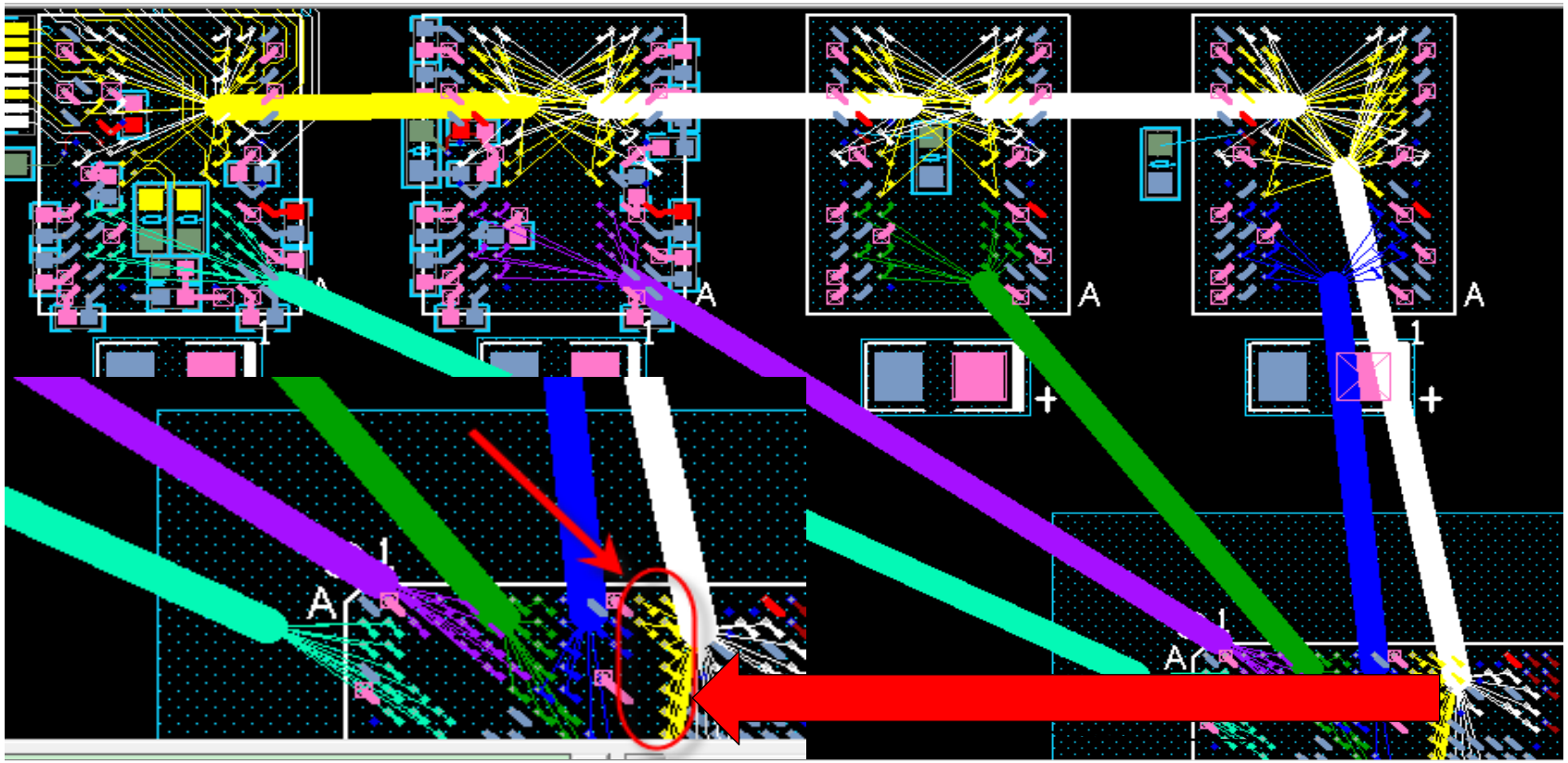
0.65 mm BGA带DDR3案例

- 布线规划
  - 首先我们把不同Bus高亮出来分析，左右两边对称且黄色和白色为地址、控制和命令Bus组，其他颜色为数据Bus。



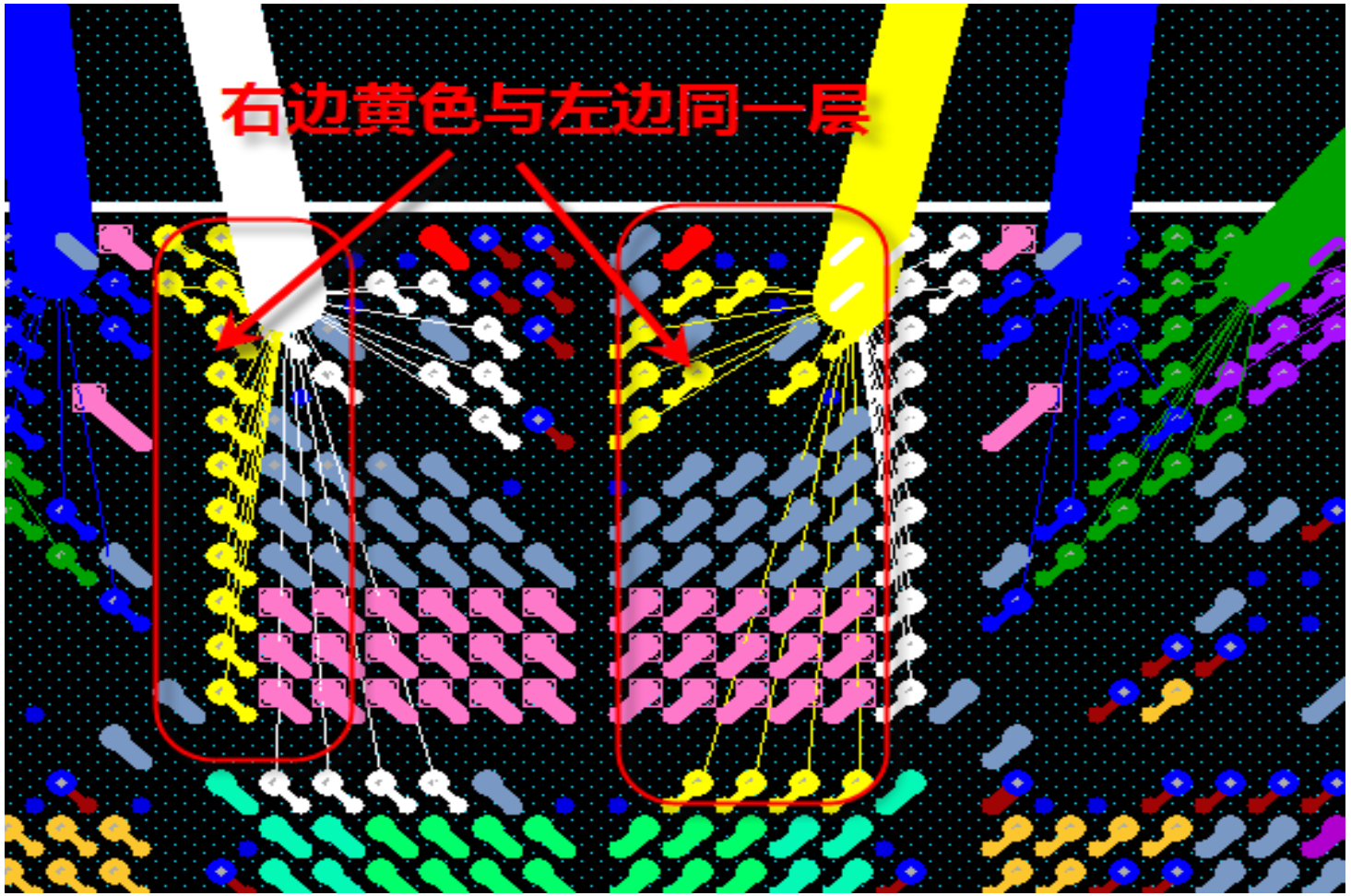
0.65 mm BGA带DDR3案例

- 布线规划
  - 其次，来分析单通道布线黄的和白色Bus计划用两个布线层可以布线完；黄色靠左边，所以规划数据组（天蓝&绿色）可以和黄色组共一层——黄色+绿色+天蓝共一层，其余另一层



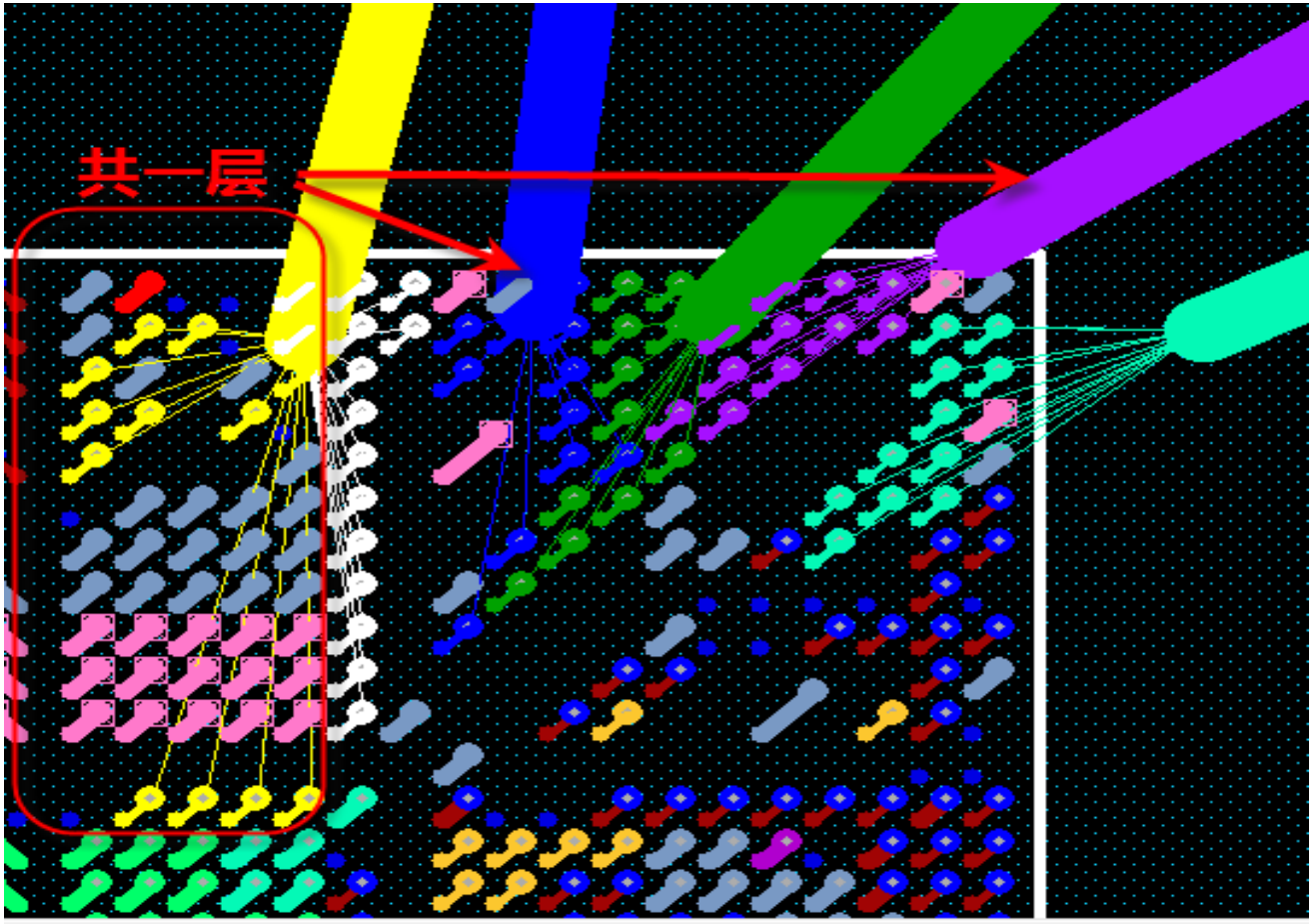
0.65 mm BGA带DDR3案例

- 布线规划
  - 最后考虑右边通道——从CPU这端考虑



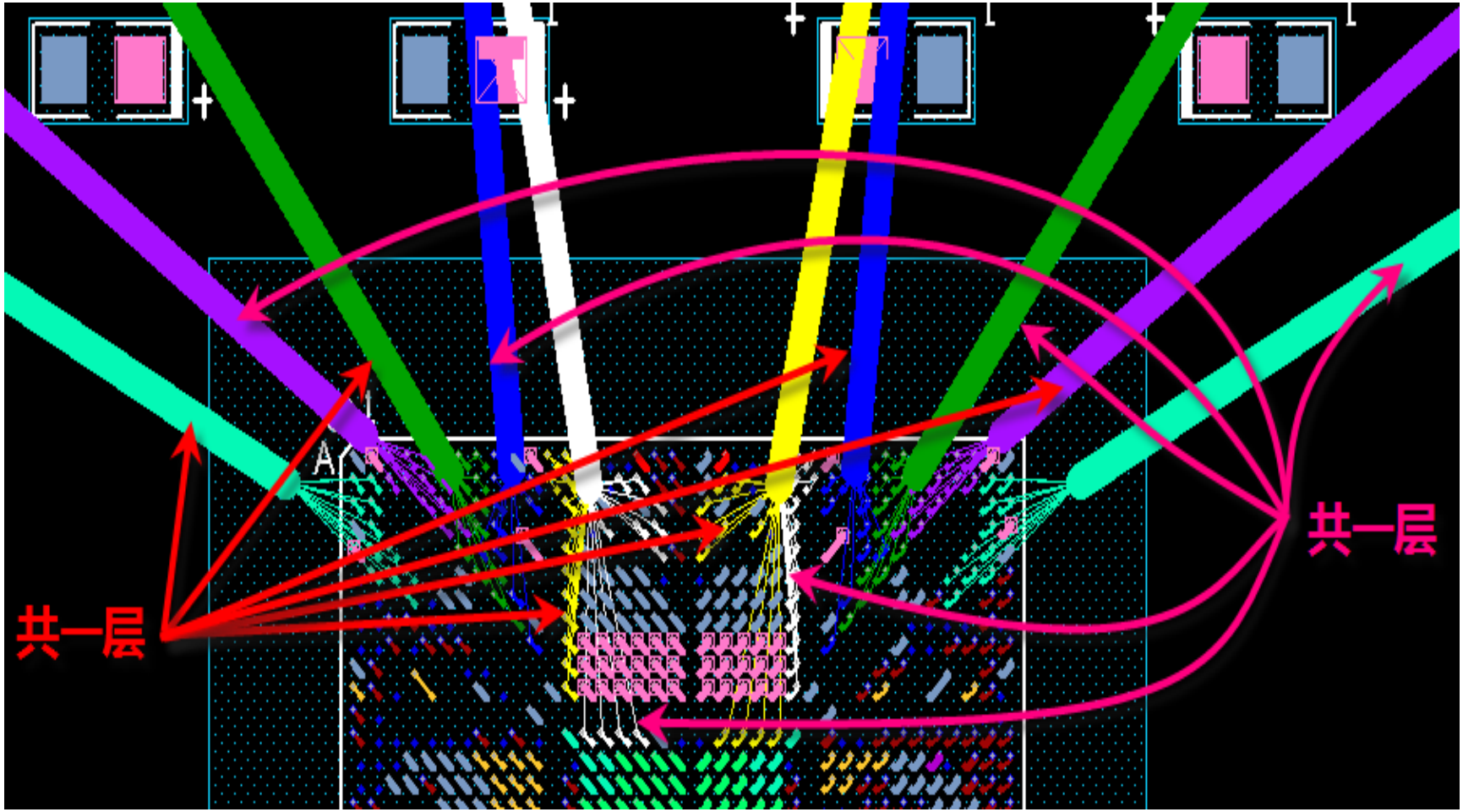
0.65 mm BGA带DDR3案例

- 布线规划
  - 有了前面的基础，这里就很容易规划了！
    - 黄色+深兰+紫色共一层，其他共一层。



0.65 mm BGA带DDR3案例

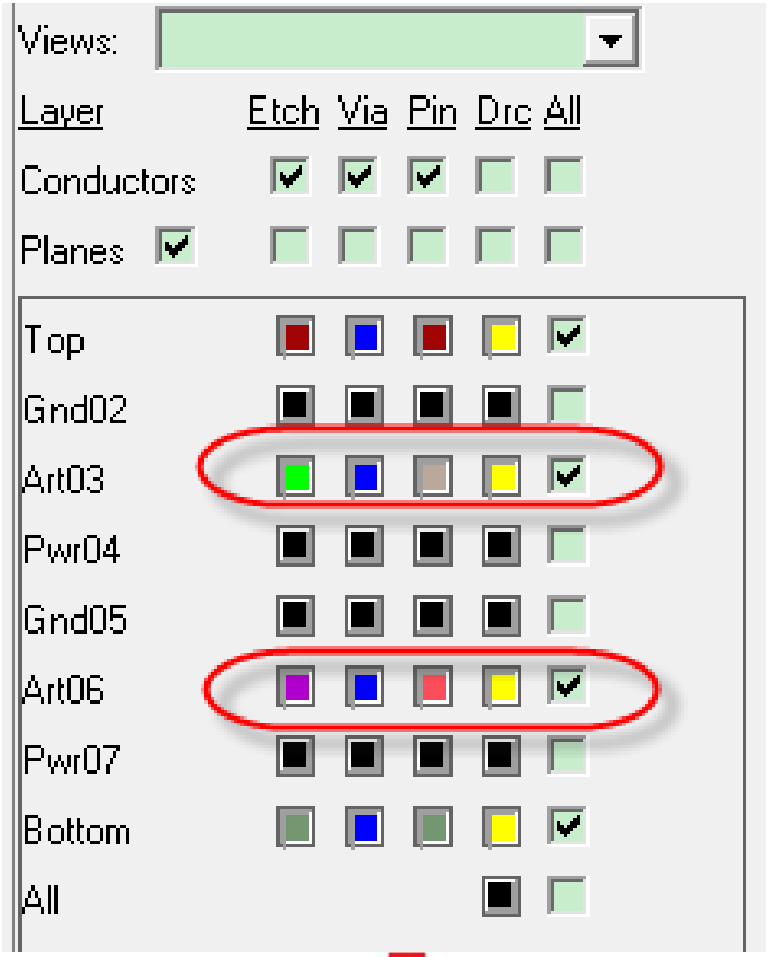
- 布线规划
  - 总结-布线内层需求



0.65 mm BGA带DDR3案例

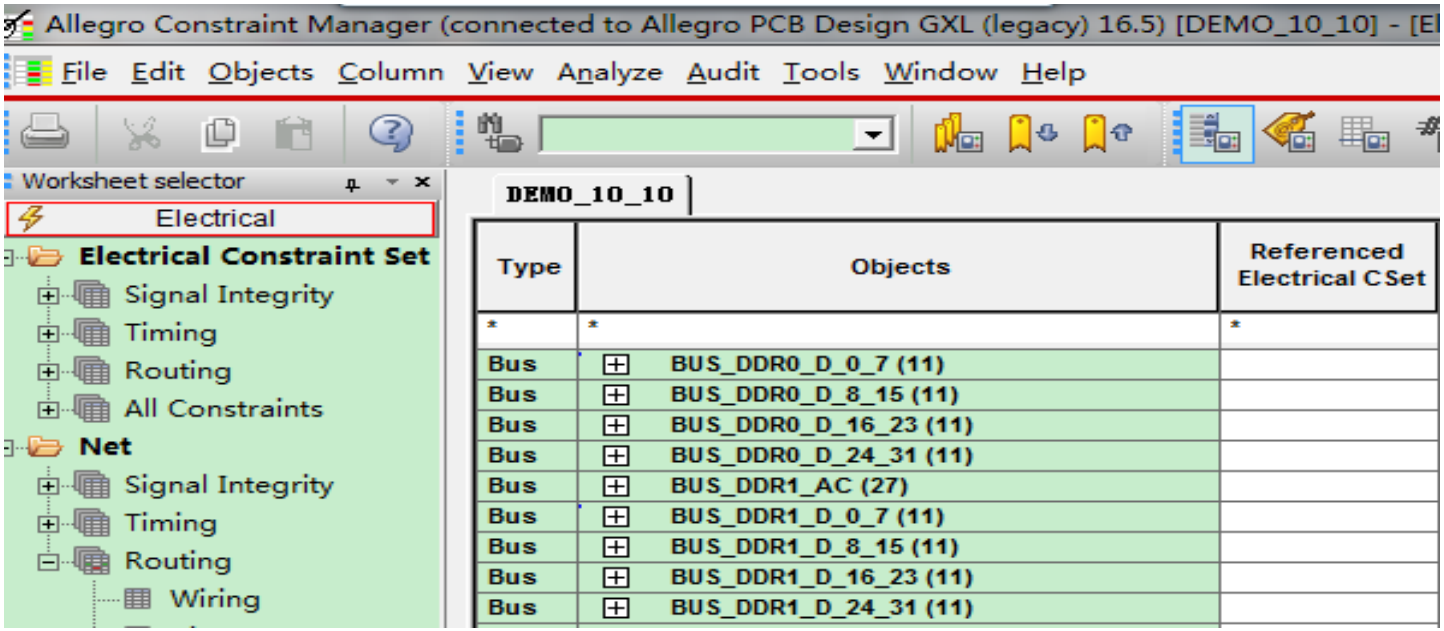
- 布线规划
  - 总结-叠层结构（2个布线内层）

Subclass Name	Type	Material
	SURFACE	AIR
TOP	CONDUCTOR	COPPER
	DIELECTRIC	FR-4
GND02	PLANE	COPPER
	DIELECTRIC	FR-4
ART03	CONDUCTOR	COPPER
	DIELECTRIC	FR-4
PWR04	PLANE	COPPER
	DIELECTRIC	FR-4
GND05	PLANE	COPPER
	DIELECTRIC	FR-4
ART06	CONDUCTOR	COPPER
	DIELECTRIC	FR-4
PWR07	PLANE	COPPER
	DIELECTRIC	FR-4
BOTTOM	CONDUCTOR	COPPER
	SURFACE	AIR



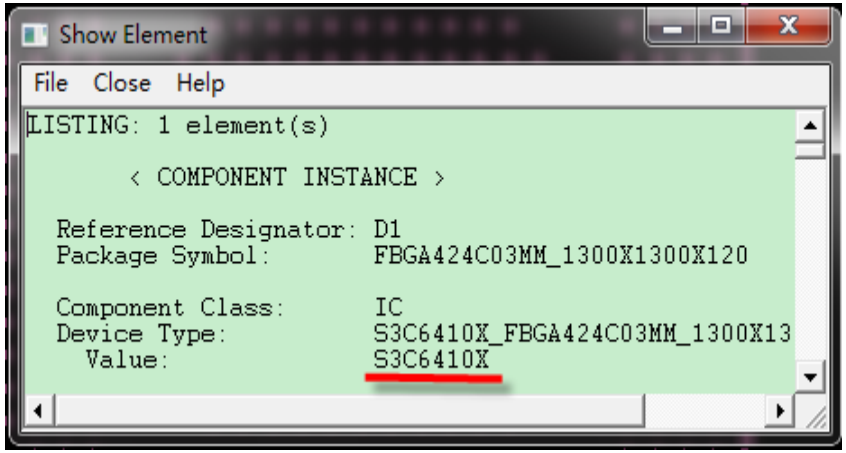
0.65 mm BGA带DDR3案例

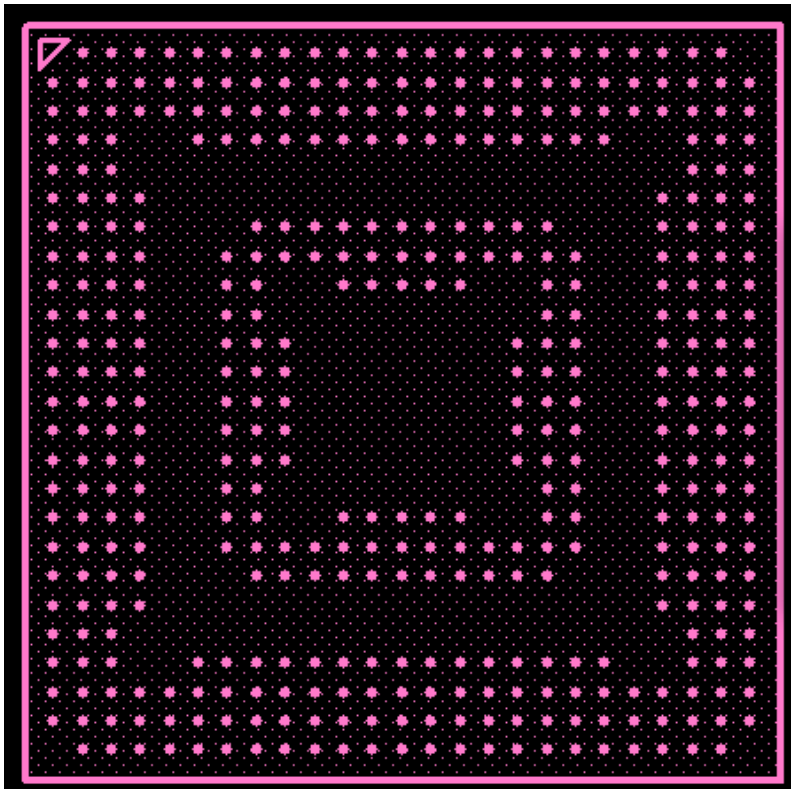
- 布线注意事项
  - 注意Fly-By拓扑结构
  - 0.65 mm BGA 可以采用无盘设计，以增加布线资源
  - DDR地址、控制、命令的上拉排阻可以调整pin，以便布线
  - DDR_VREF电源的滤波电容位置
  - 强烈建议建立好约束规则后再布线



HDI-0.5 mm BGA 盲埋孔设计案例

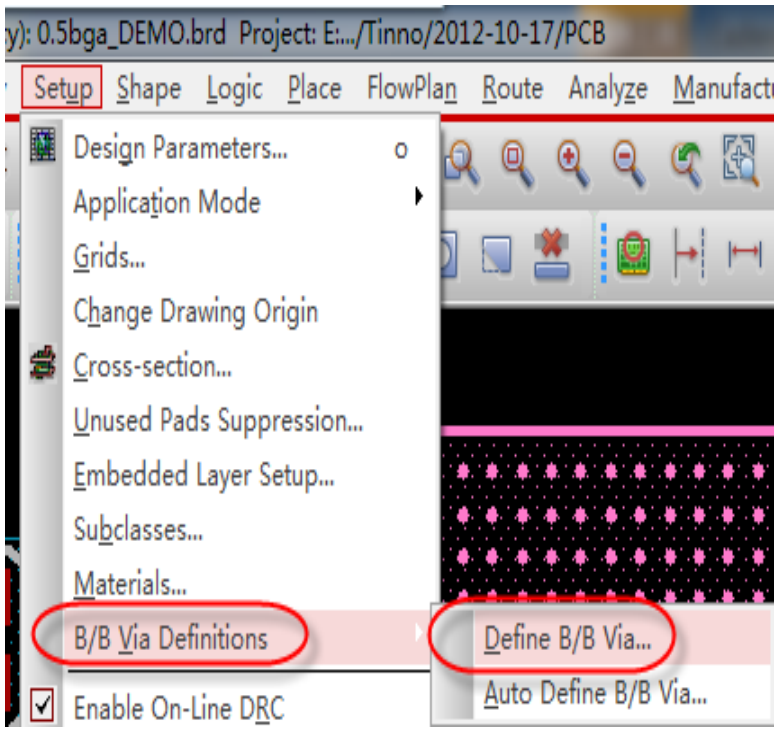
- HDI(High Density Interconnect，高密度互连)也就是通常所说的盲埋孔技术。
- IPC-2315对HDI的分类（按照激光孔深度）：
  - 一阶HDI
  - 二阶HDI
  - 三阶HDI
  - 任意阶HDI（ALIVH）
- S3C6410X 0.5mm设计分析

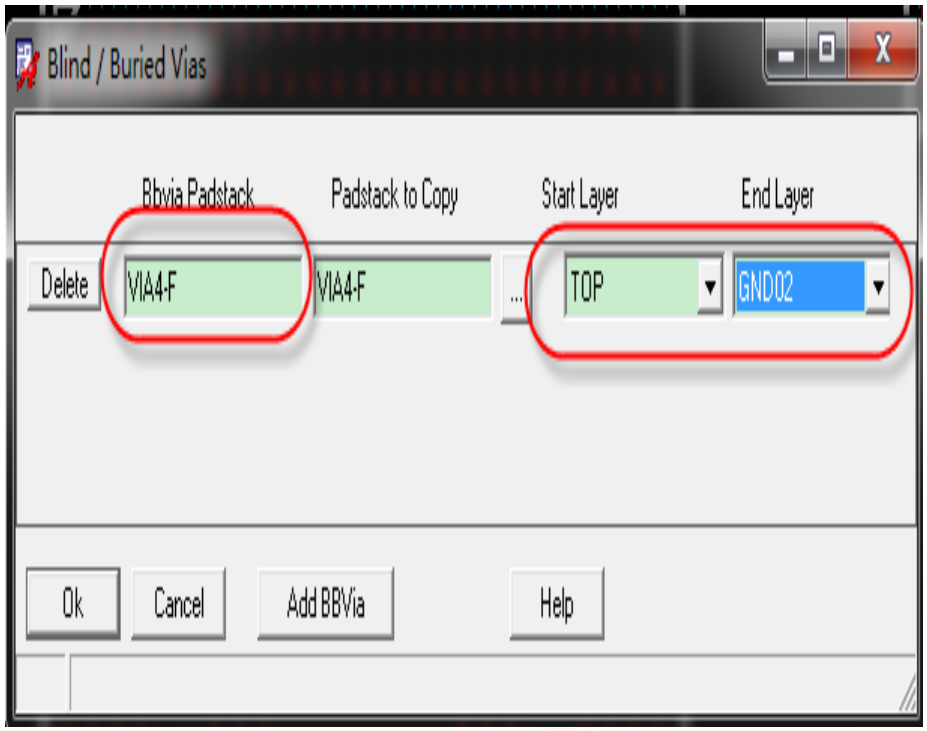




HDI-0.5 mm BGA 盲埋孔设计案例

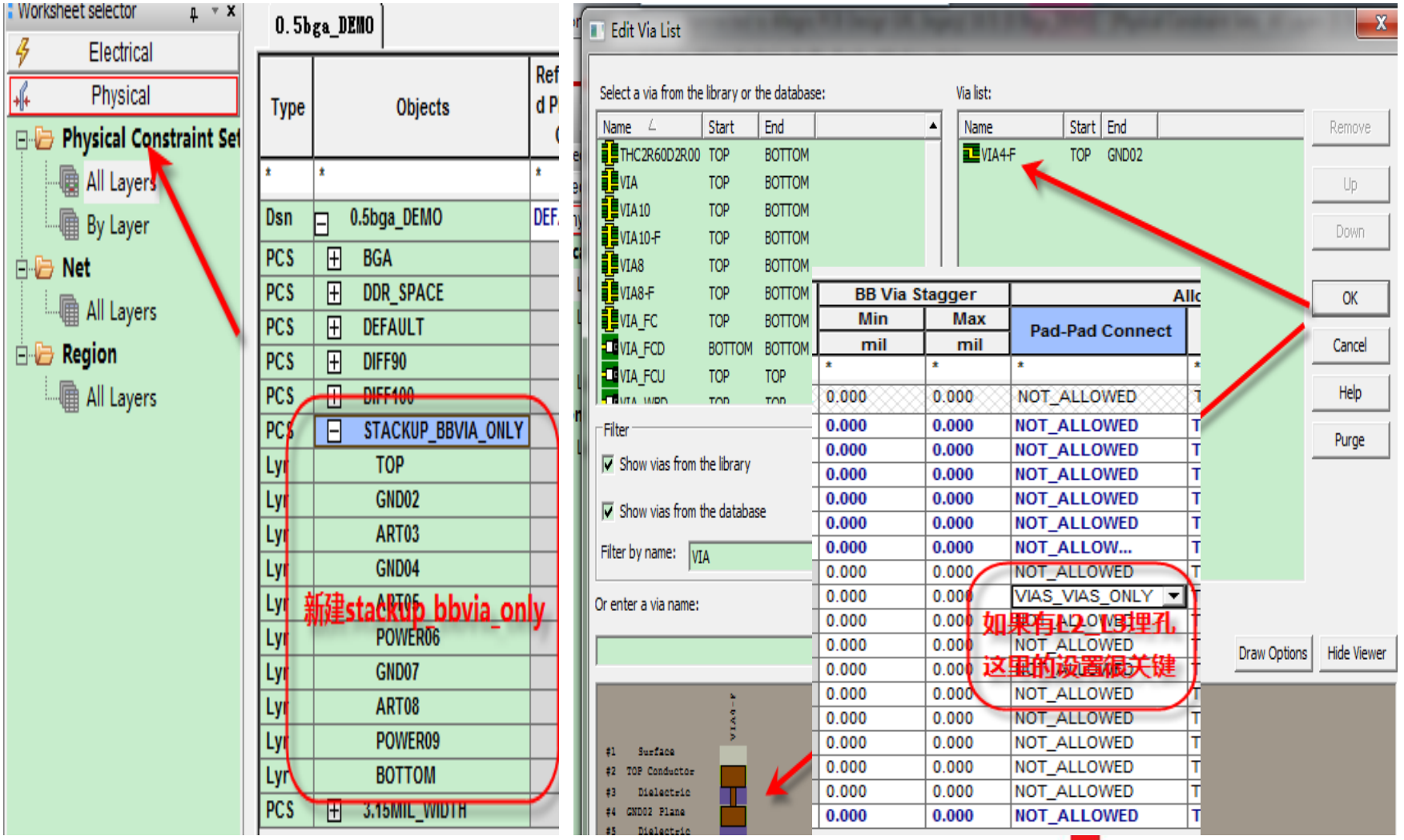
- **S3C6410X普遍应用于各类消费类产品（智能手机、Pad等），对此芯片的PCB设计无疑是对PCB 设计工程师的挑战。**
- 一阶盲孔设计为例
  - 定义盲埋孔





HDI-0.5 mm BGA 盲埋孔设计案例

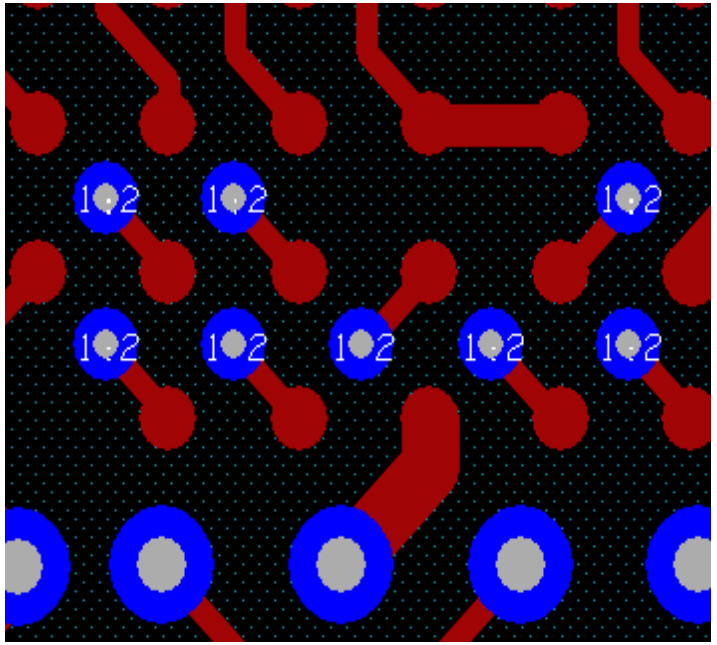
– 设置盲埋孔



HDI-0.5 mm BGA 盲埋孔设计案例

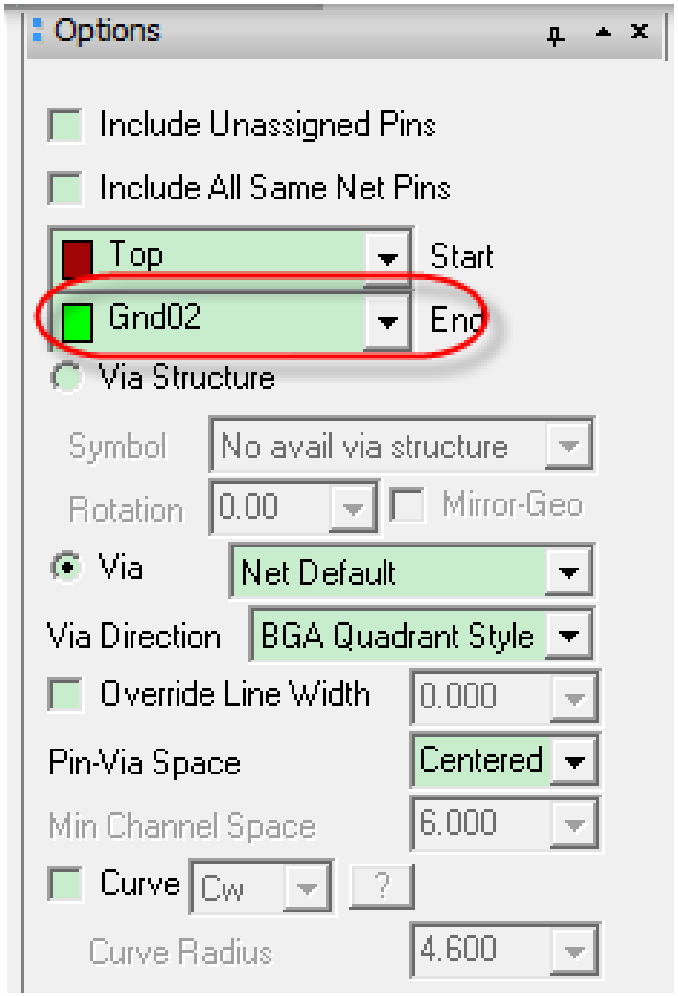
– 设置盲埋孔

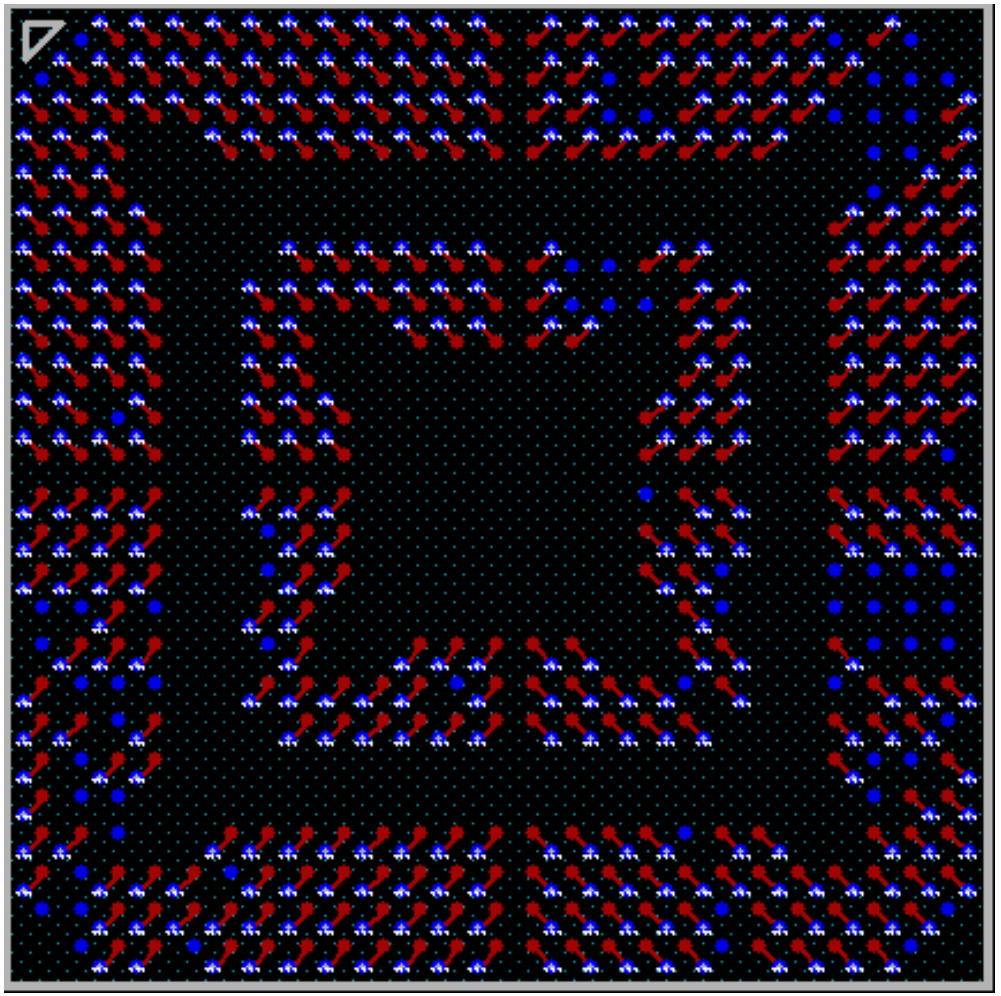
• 把设置好的**Stackup_Bbvia_Via**规则分配给相应的**Net**



HDI-0.5 mm BGA 盲埋孔设计案例

– **Fanout**

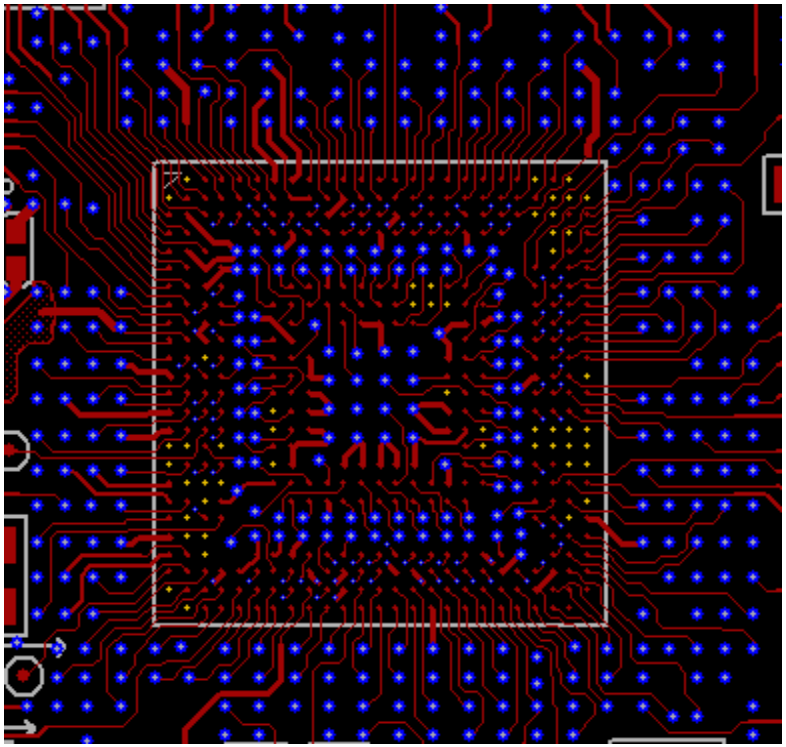


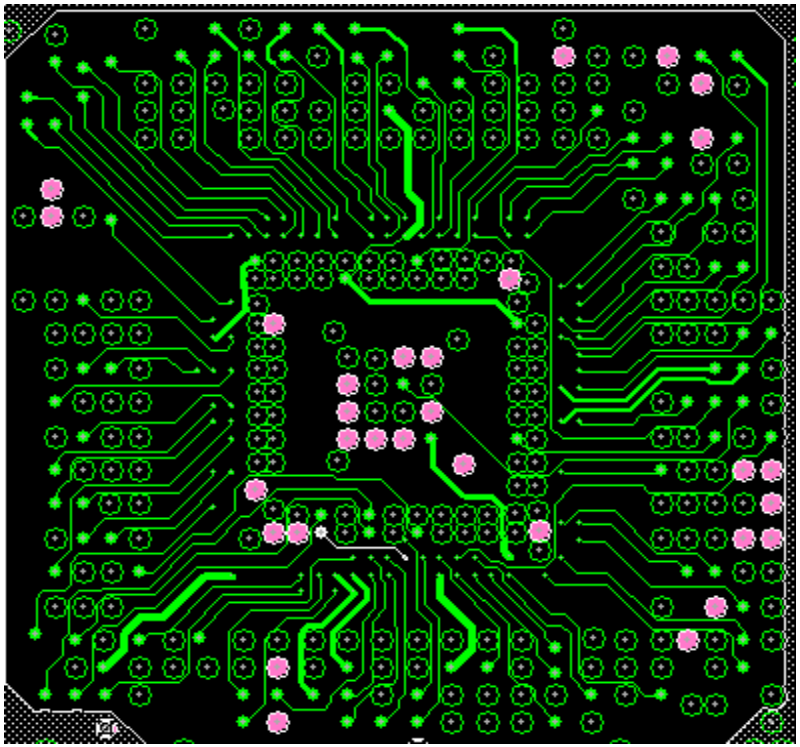


HDI-0.5 mm BGA 盲埋孔设计案例

– 注意事项

- 线宽/间距 3.5/3.5
- 焊盘0.23mm，保证表层能出线
- BGA盲孔的线(除GND、PWR)在02层引出来，设计难点就解决了





Q&A

- Q&A
- Summary

Thank you!

Oct 17，2012
By: Ausben Du
ausbendu@comtech.com.cn