

Allegro Constraint Manager

-----Channel Partner **COMTECH 科通**



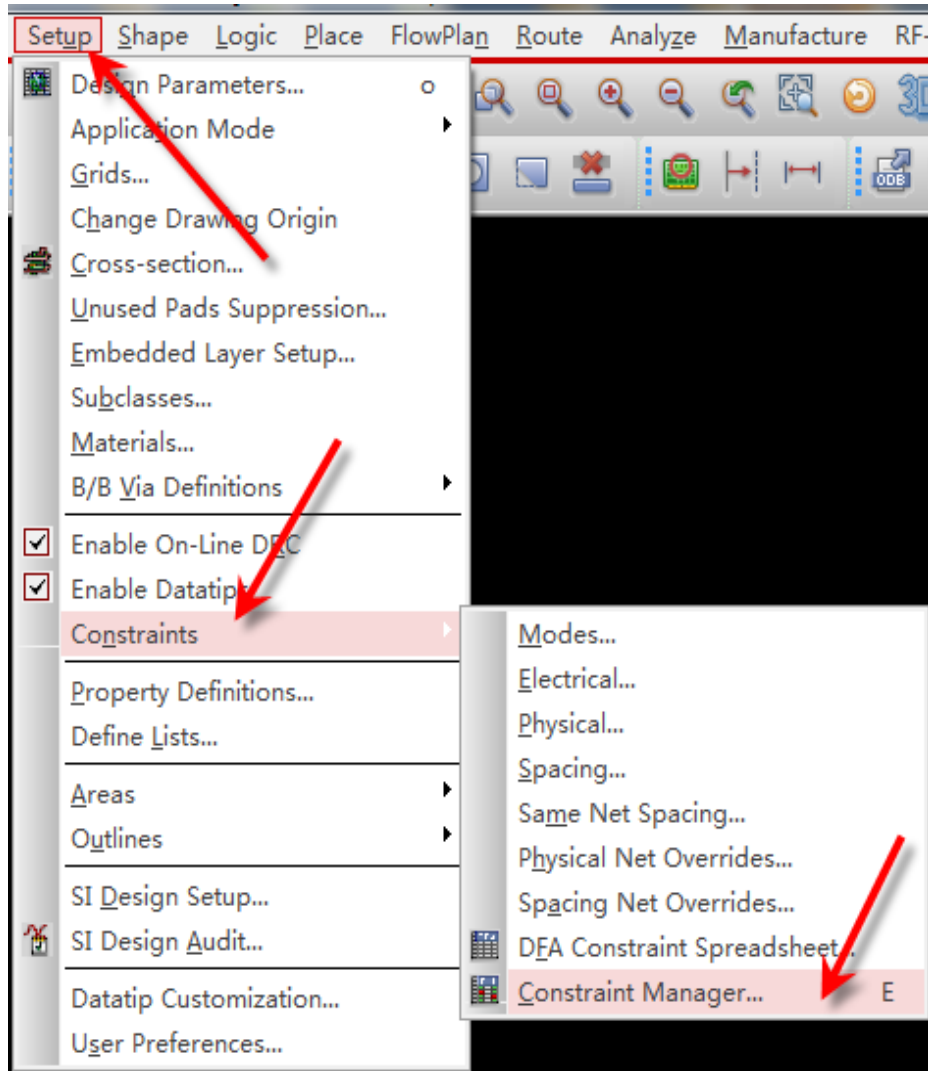
内容提要

- 约束管理器（**Constraint Manager**）介绍
- 物理约束 与间距约束
 - **Physical Constraint & Spacing Constraint** —介绍
 - 物理约束（**Physical Constraint**）
 - 间距约束（**Spacing Constraint**）
 - **Same Net Spacing Constraint**
 - 区域约束（**Region Constraint**）
 - **Net**属性
 - **Component**属性和**Pin**属性
 - **DRC**工作表
- 电气约束（**Electrical Constraint**）
 - **Relative Propagation Delay**工作表
 - **Differential Pair** 工作表
 - **Differential Pair**示例

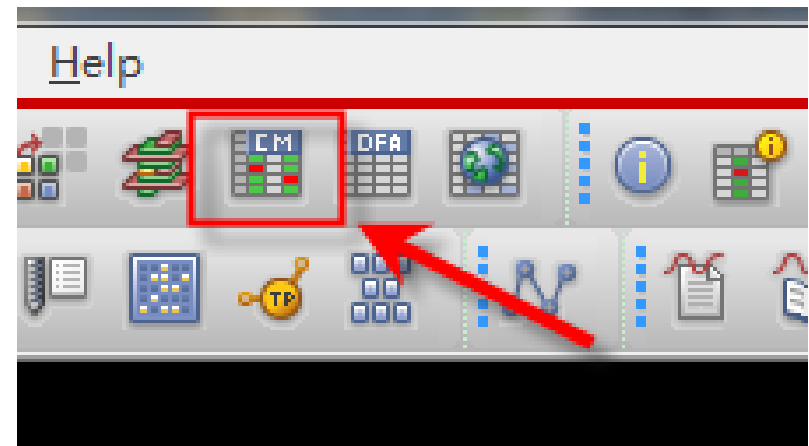
约束管理器（Constraint Manager）介绍

- 约束管理器(**CM**)是一个交叉的平台，以**工作簿**和**工作表**的形式管理**Cadence PCB**和**IC Package**设计流程中的所有工具的约束。
- 用户可以通过约束管理器在设计流程中的**任意**一个环节进行约束**定义**、**查看**和**验证**。
- 当约束设置完成后，**PCB**工具会自动根据定义 的约束对设计进行检查，不符合约束的地方会用**DRC Markers** 标记出来。

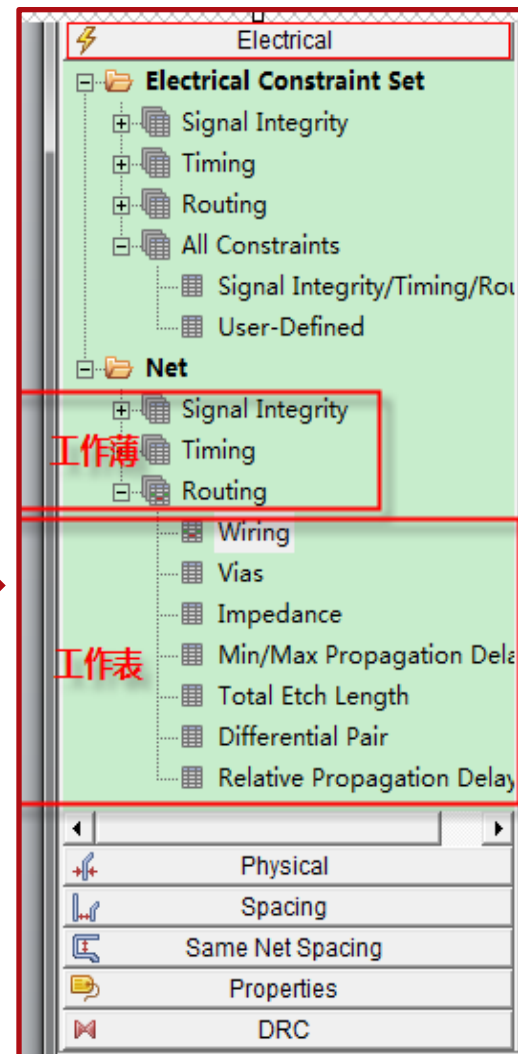
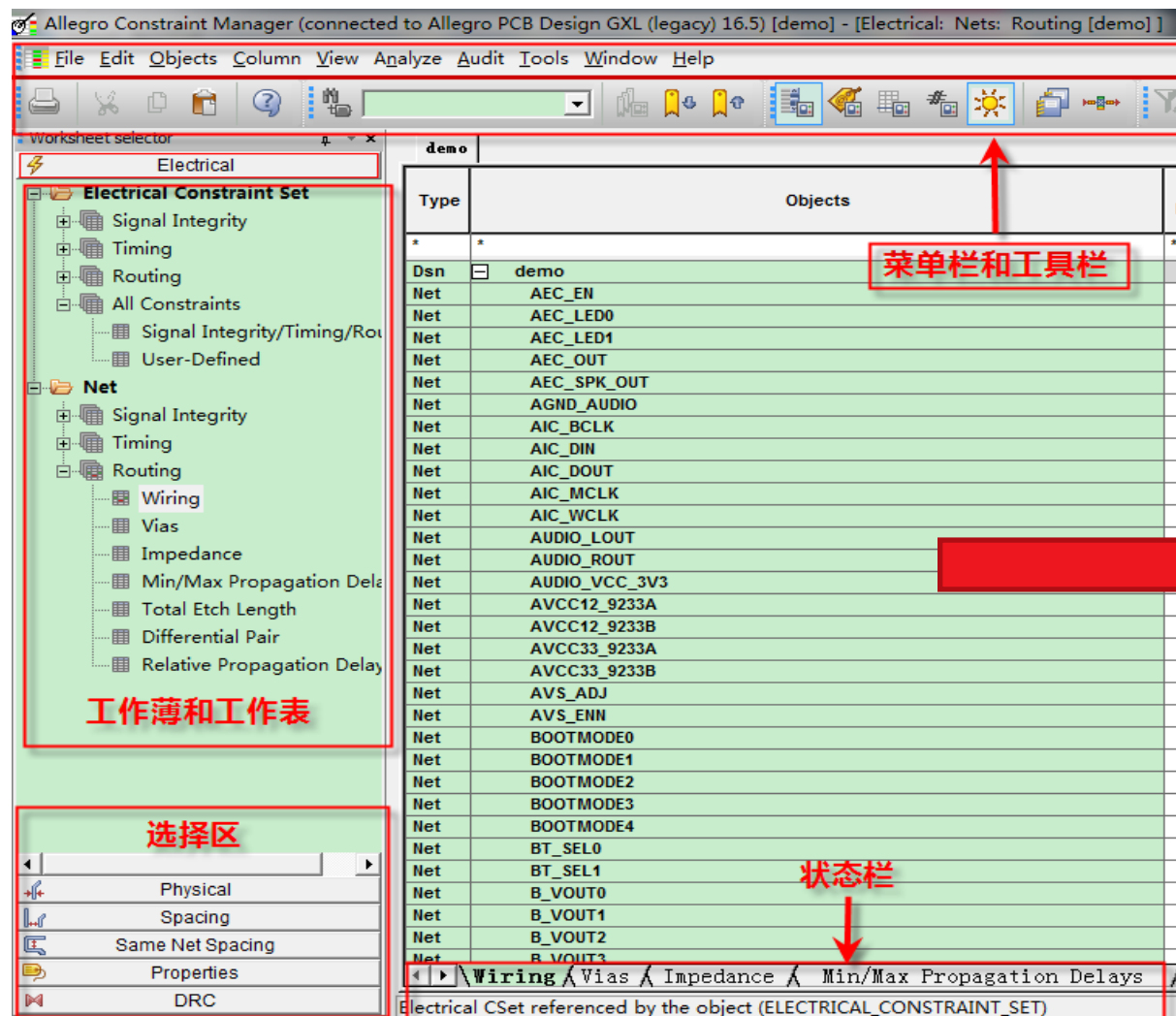
约束管理器（Constraint Manager）介绍



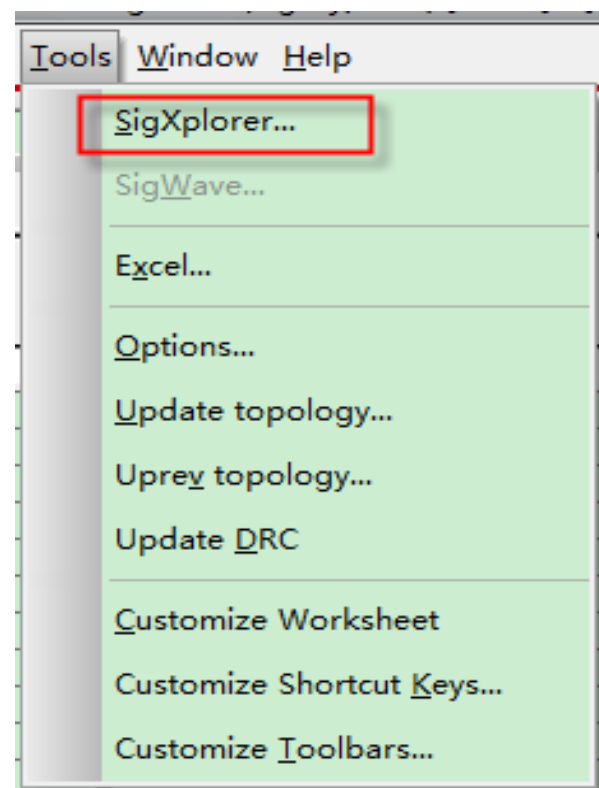
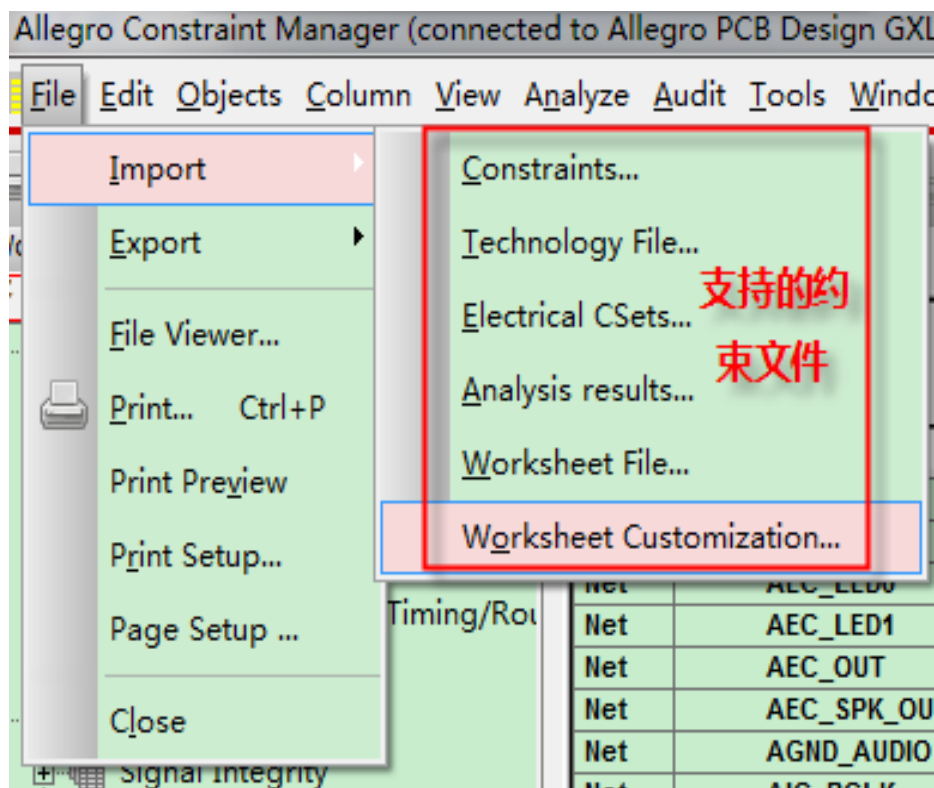
进入CM



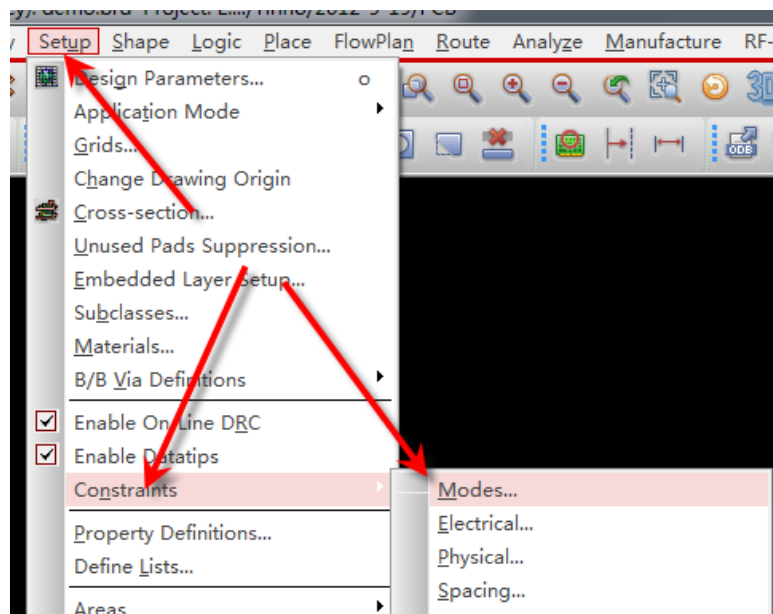
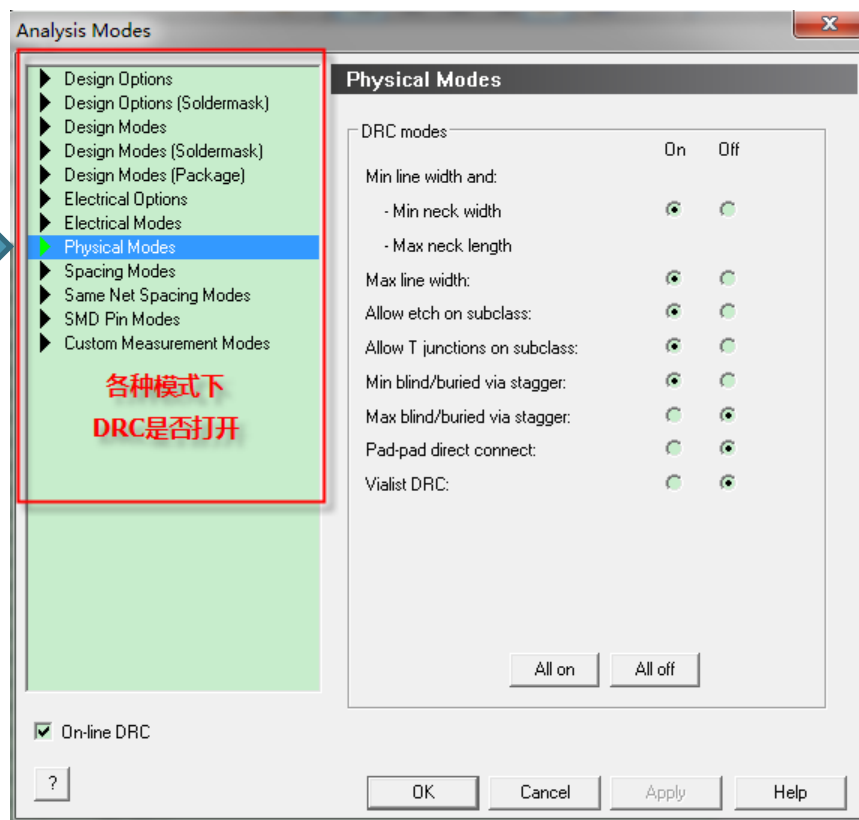
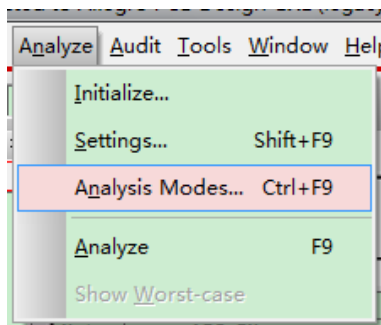
约束管理器 (Constraint Manager) 介绍



约束管理器（Constraint Manager）介绍



约束管理器 (Constraint Manager) 介绍



物理约束与间距约束——介绍

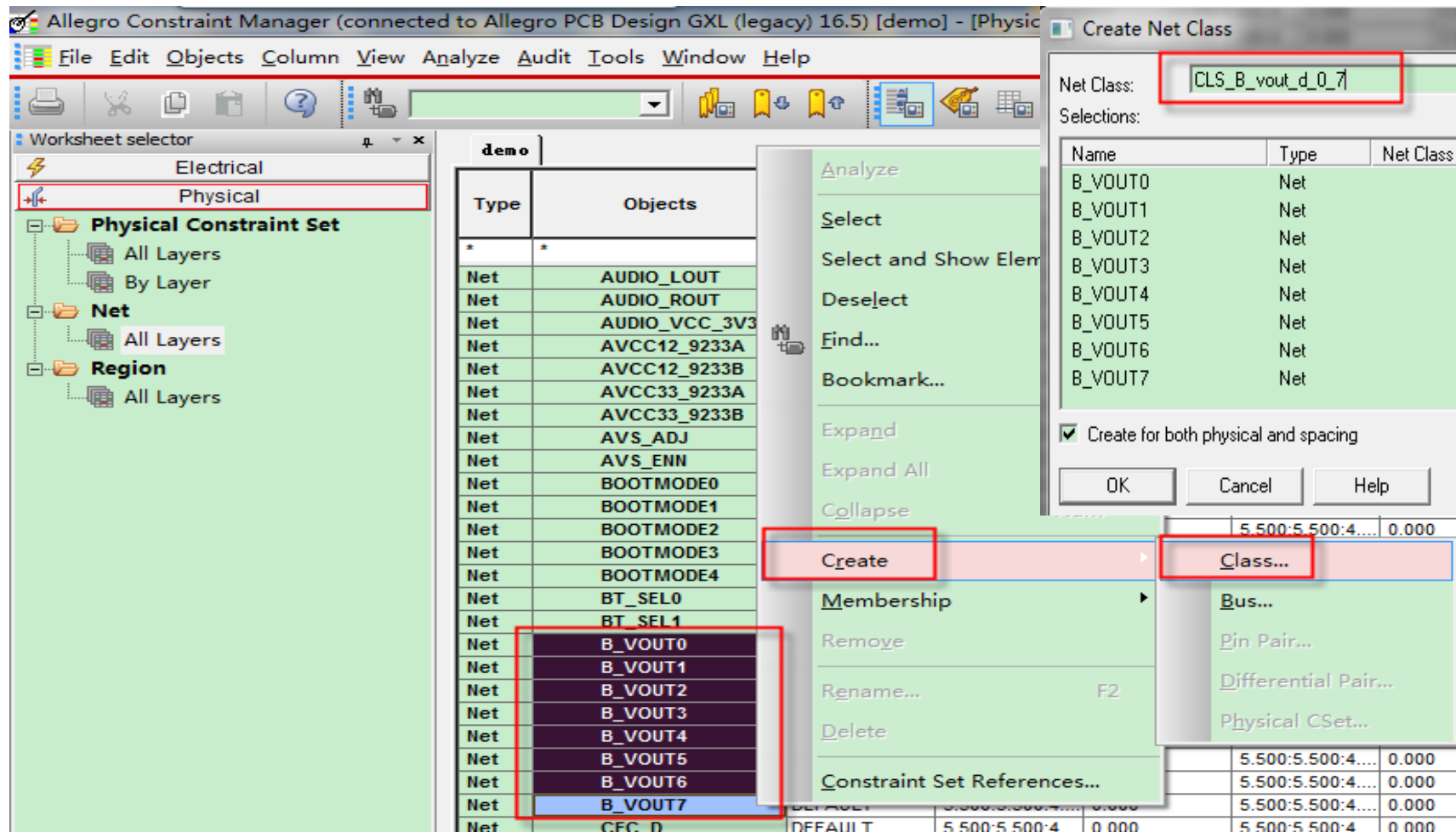
- 有四类关于**Net**的设计约束与规则：
 - **物理约束** (*Physical Constraint*)
 - **Line** (布线) 线宽和**Layer** (层) 约束
 - **间距约束** (*Spacing Constraint*)
 - 不同**Net** (网络) 的**Lines**、**Pads**、**Vias**、**Shapes**之间的间距
 - **相同网络间距约束** (*Same Net Spacing Constraint*)
 - 相同**Net**的**Lines**、**Pads**、**Vias**、**Shapes**之间的间距
 - **电气约束** (*Electrical Constraint*)
 - 管理电路信号特性 (**Cross Talk**、**Delay**...)
- 对于物理和间距规则主要分两类：
 - **默认规则** (*Default*规则)
 - **扩展规则**

物理约束与间距约束——介绍

- 在设计的初期，Allegro PCB Editor将**Physical、Spacing、Same Net Spacing**的**Default**规则赋予了设计中的所有网络。
- 若设计中有些**Net**的设计规则要不同于**Default**规则，用户需要先创建包含这些网络的**Net Class**，再建立扩展的**Physical、Spacing、Same Net Spacing**约束，最后将这些扩展的约束赋予**Net Class**。

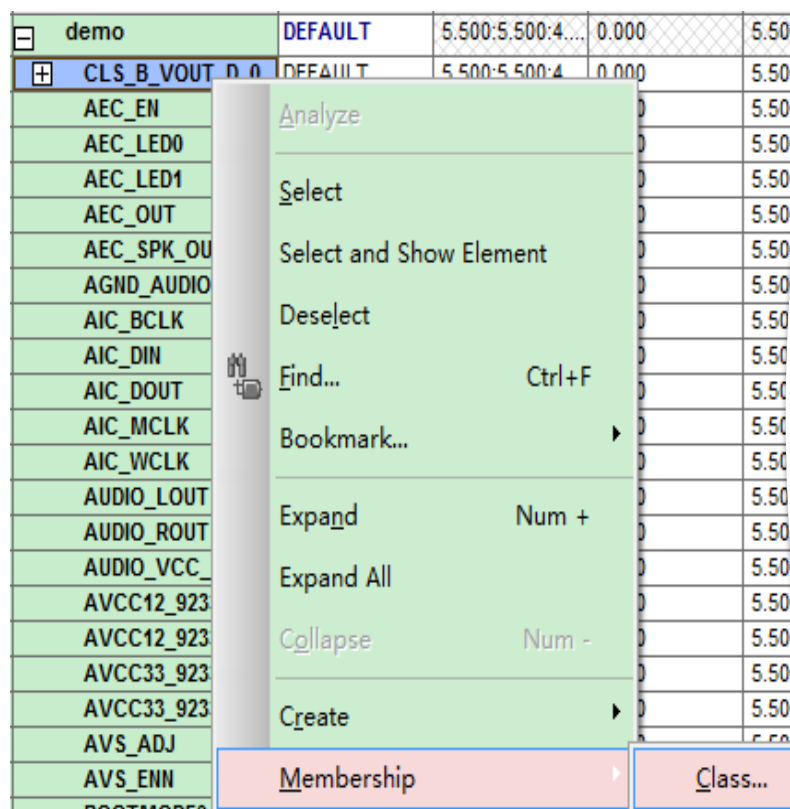
物理约束 (Physical Constraint)

• 建立Net Class

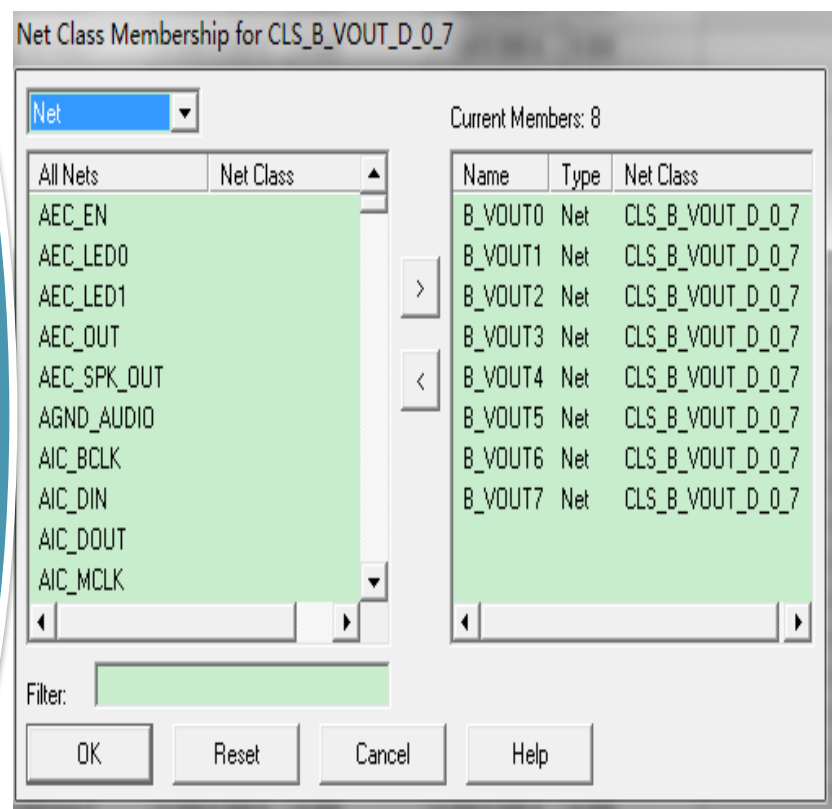


物理约束 (Physical Constraint)

- 为Class添加对象 (Assigning Objects to Classes)

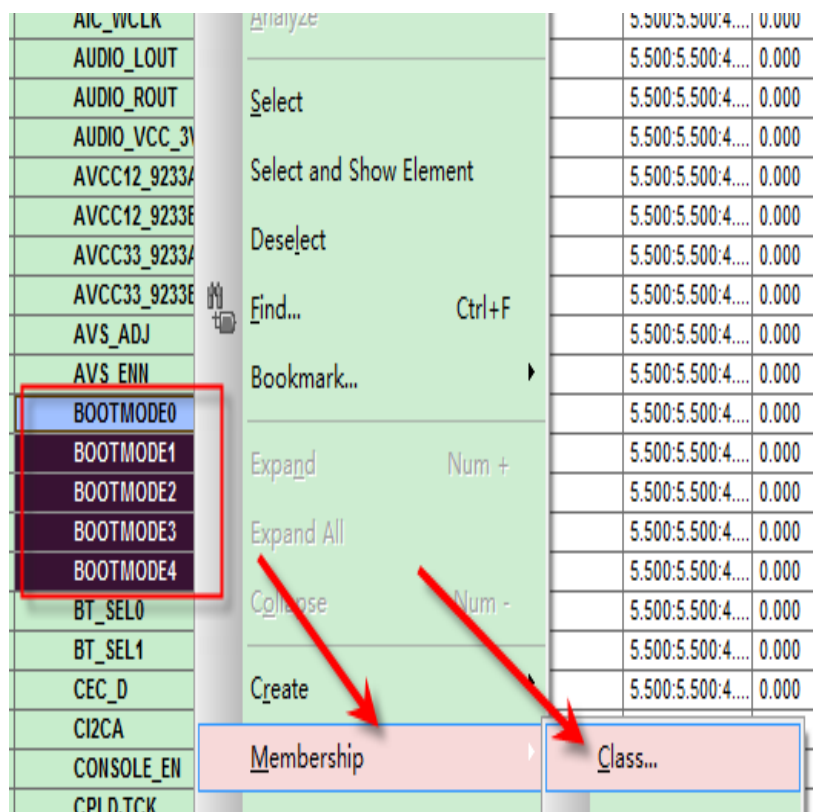


方法一

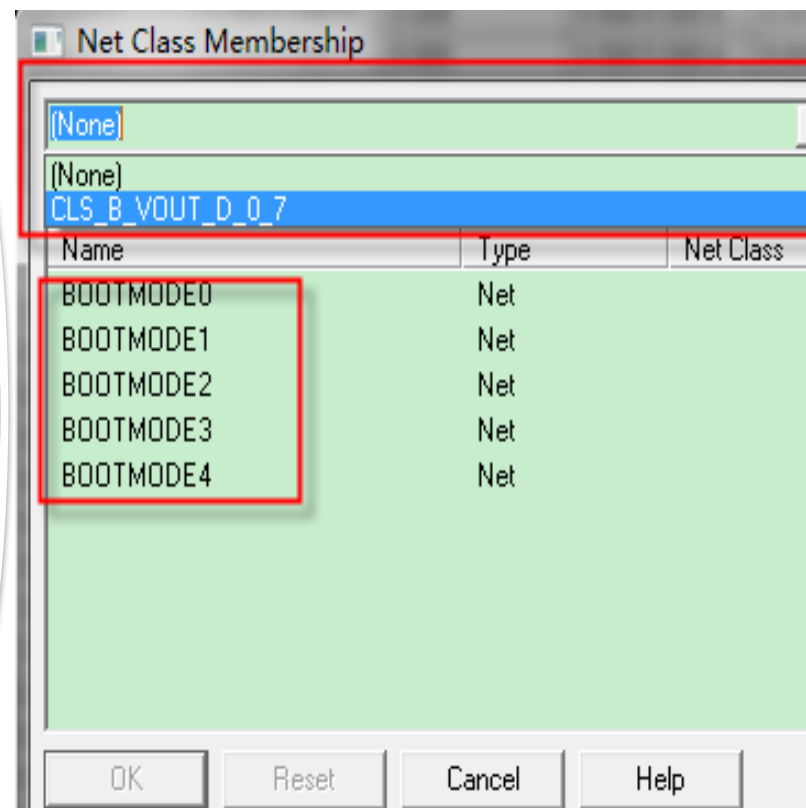


物理约束 (Physical Constraint)

- 为Class添加对象 (Assigning Objects to Classes)



方法二



物理约束 (Physical Constraint)

- 设置Default约束

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo] - [Physical Constraint Sets: All Layers [demo]]

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector

Electrical

Physical

Physical Constraint Set

- All Layers
- By Layer
- Net
 - All Layers
- Region
 - All Layers

demo

Type	Objects	Reference d Physical CSet	Line Width		Neck		Differential Pair				
			Min mil	Max mil	Min Wi mil	Max Len mil	Min mil	Pri mil	Nec mil	(+)T mil	(-)Toleranc mil
*	*	*	*	*	*	*	*	*	*	*	*
Dsn	<input checked="" type="checkbox"/> demo	DEFAULT	5.500:5.500	0.000	5.500:...	0.000	0.0..	0.0..	0.0..	0.0..	0.000
PCS	<input checked="" type="checkbox"/> DEFAULT		5.500:...	0.000	5.50...	0.000	...	0....	0....	0....	0.000
Lyr	TOP		5.500	0.000	5.500	0.000	0.0..	0.0..	0.0..	0.0..	0.000
Lyr	GND02		5.500	0.000	5.500	0.000	0.0..	0.0..	0.0..	0.0..	0.000
Lyr	ART03		4.800	0.000	4.800	0.000	4.0..	0.0..	0.0..	0.0..	0.000
Lyr	PWR04		5.500	0.000	5.500	0.000	0.0..	0.0..	0.0..	0.0..	0.000
Lyr	GND05		4.800	0.000	4.800	0.000	0.0..	0.0..	0.0..	0.0..	0.000
Lyr	ART06		4.800	0.000	4.800	0.000	4.0..	0.0..	0.0..	0.0..	0.000
Lyr	PWR07		5.500	0.000	5.500	0.000	0.0..	0.0..	0.0..	0.0..	0.000
Lyr	BOTTOM		5.500	0.000	5.500	0.000	0.0..	0.0..	0.0..	0.0..	0.000

物理约束 (Physical Constraint)

- 设置Default约束

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo] - [Physical Constraint Sets: All Layers [demo]]

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector

Electrical

Physical

Physical Constraint Set

- All Layers
- By Layer

Net

- All Layers

Region

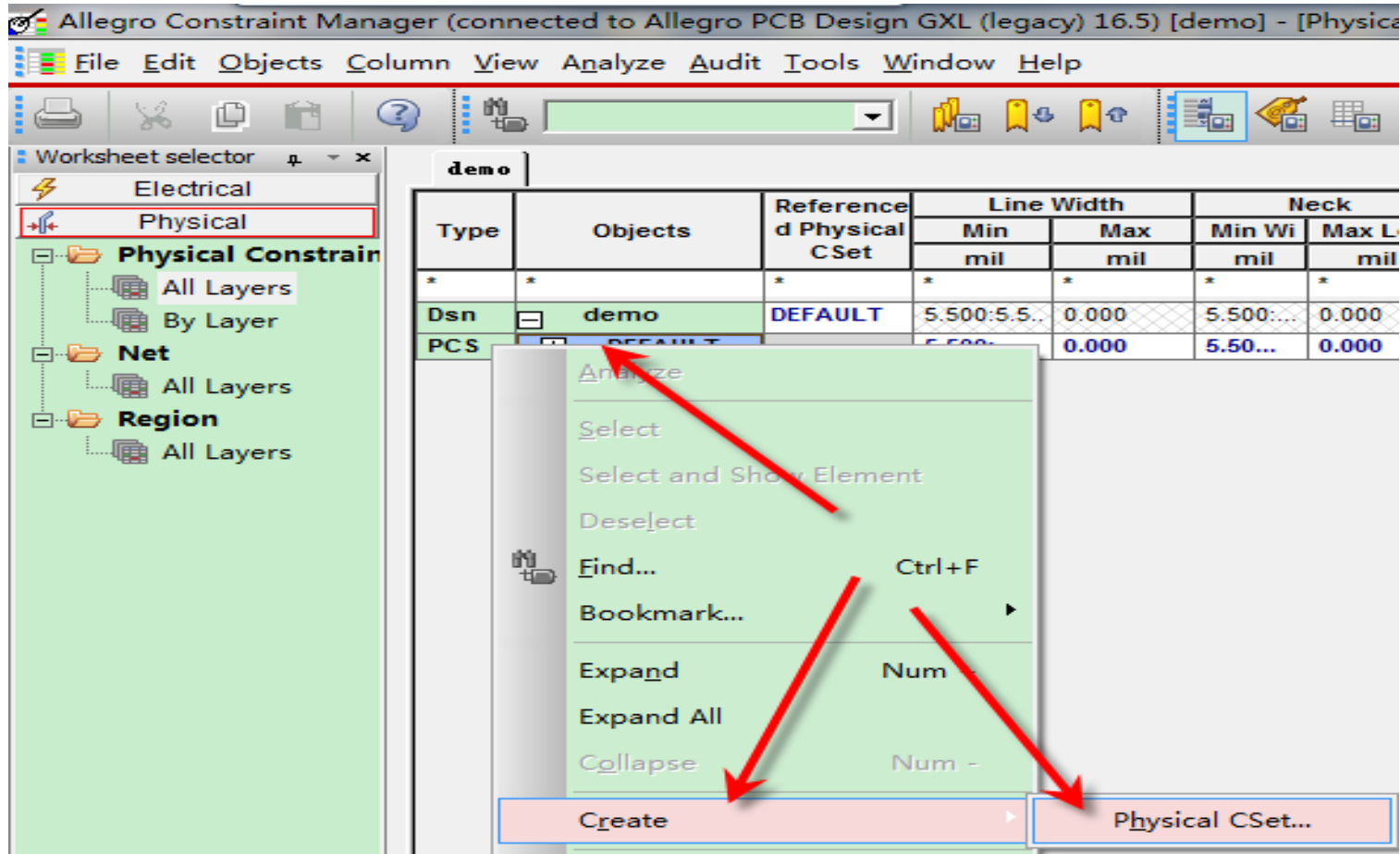
- All Layers

demo

Type	Objects	Vias	BB Via Stagger		Allow		
			Min	Max	Pad-Pad Connect	Etch	Ts
			mil	mil			
*	*	*	*	*	*	*	*
Dsn	demo	VIA10_F:VIA8_F..	5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE
PCS	DEFAULT	VIA10_F:VIA8...	5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE
Lyr	TOP		5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE
Lyr	GND02		5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE
Lyr	ART03		5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE
Lyr	PWR04		5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE
Lyr	GND05		5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE
Lyr	ART06		5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE
Lyr	PWR07		5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE
Lyr	BOTTOM		5.000	0.000	NOT_ALLOWED	TRUE	ANYWHERE

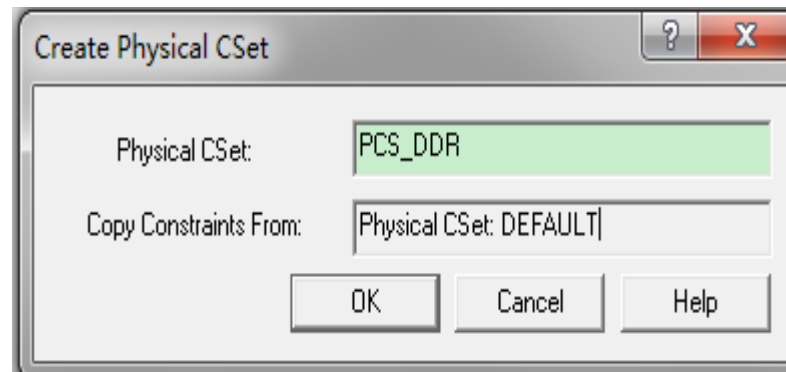
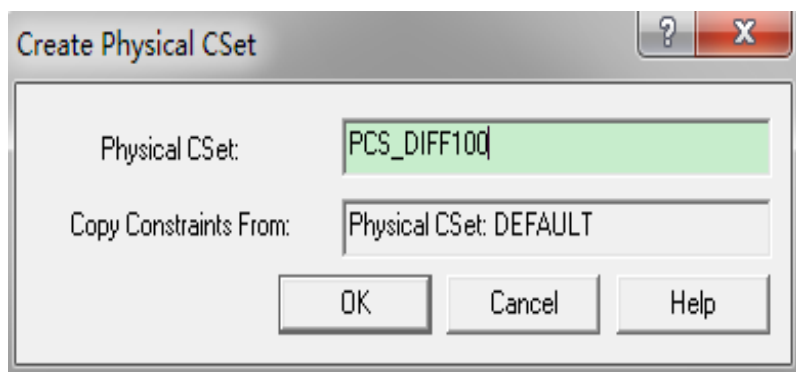
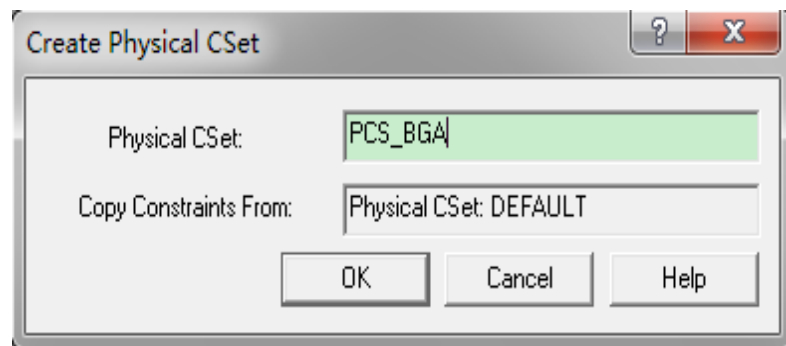
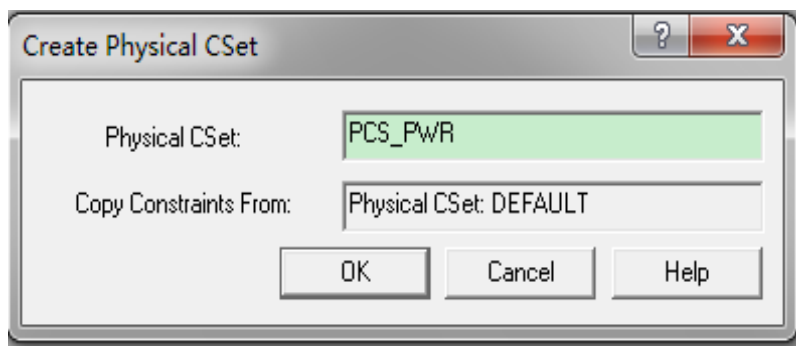
物理约束 (Physical Constraint)

- 建立扩展Physical约束



物理约束（Physical Constraint）

- 建立扩展Physical约束



物理约束 (Physical Constraint)

- 建立扩展Physical约束

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo] - [Physical Constraint Sets: All Layers [demo]]

File Edit Objects Column View Analyze Audit Tools Window Help

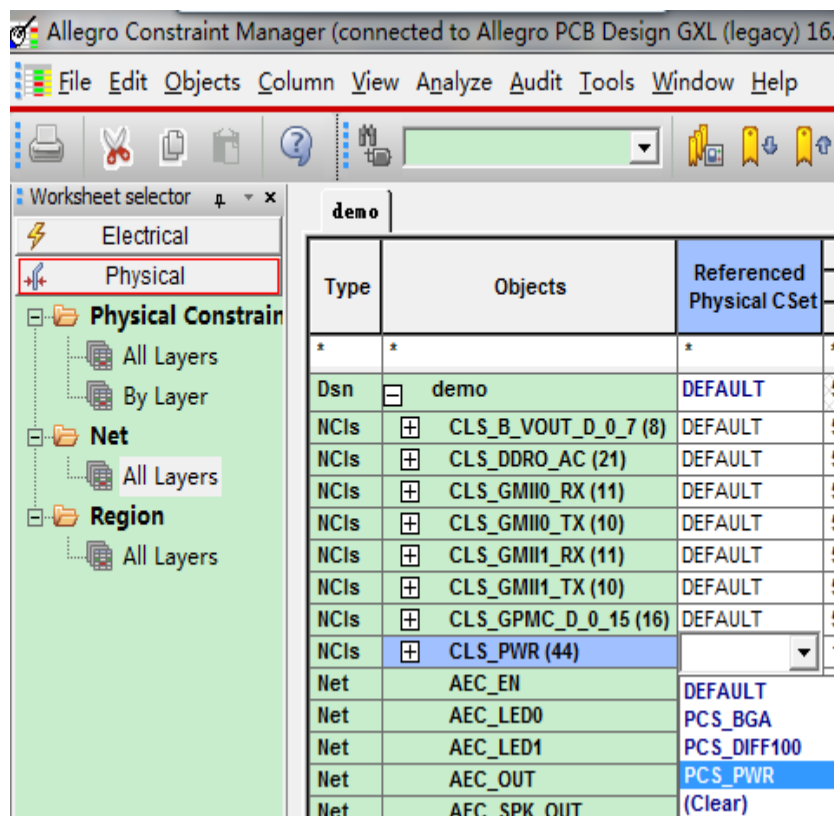
Worksheet selector: demo

Physical Constraint Manager Table:

Type	Objects	Reference d Physical CSet	Line Width		Neck		Differential Pair				
			Min	Max	Min Wi	Max Len	Min Li	Primary	Neck Ga	(+)Tolerance	(-)Tolerance
			mil	mil	mil	mil	mil	mil	mil	mil	mil
Dsn	demo	DEFAULT	5.500:5.5...	0.000	5.500:...	0.000	0.000:...	0.000	0.000	0.000	0.000
PCS	DEFAULT		5.500:...	0.000	5.50...	0.000	0.0...	0.000	0.000	0.000	0.000
PCS	PCS_BGA		5.500:...	0.000	5.50...	0.000	0.0...	0.000	0.000	0.000	0.000
Lyr	TOP		5.500	0.000	5.500	0.000	0.000	0.000	0.000	0.000	0.000
Lyr	GND02		5.500	0.000	5.500	0.000	0.000	0.000	0.000	0.000	0.000
Lyr	ART03		4.800	0.000	4.800	0.000	4.000	0.000	0.000	0.000	0.000
Lyr	PWR04		5.500	0.000	5.500	0.000	0.000	0.000	0.000	0.000	0.000
Lyr	GND05		4.800	0.000	4.800	0.000	0.000	0.000	0.000	0.000	0.000
Lyr	ART06		4.800	0.000	4.800	0.000	4.000	0.000	0.000	0.000	0.000
Lyr	PWR07		5.500	0.000	5.500	0.000	0.000	0.000	0.000	0.000	0.000
Lyr	BOTTOM		5.500	0.000	5.500	0.000	0.000	0.000	0.000	0.000	0.000

物理约束 (Physical Constraint)

- 为Net Class添加 Physical约束

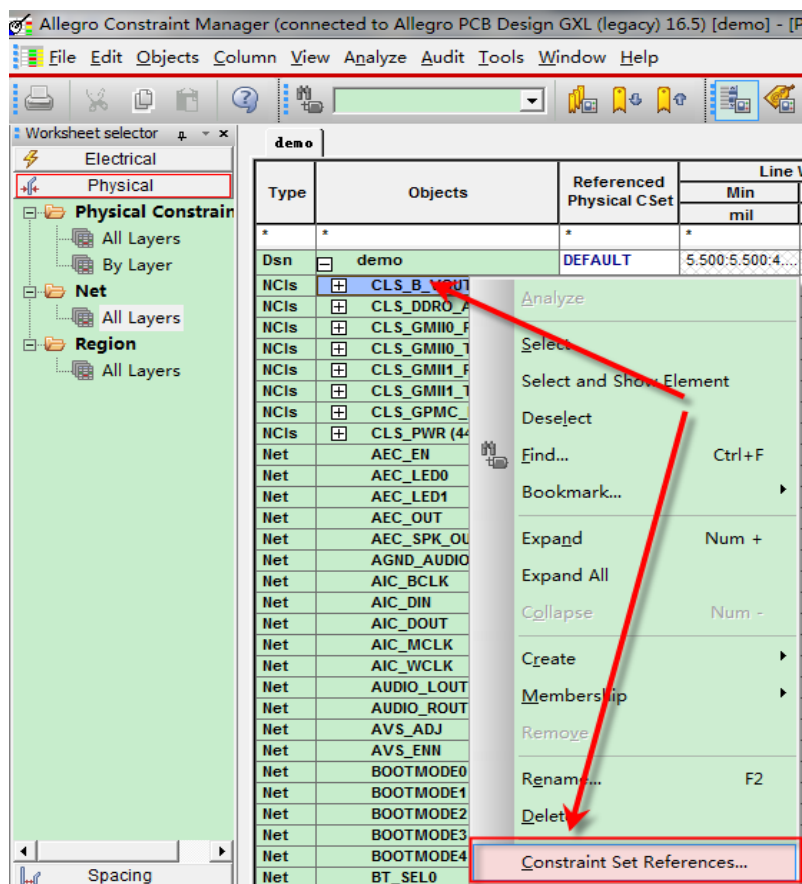


方法一

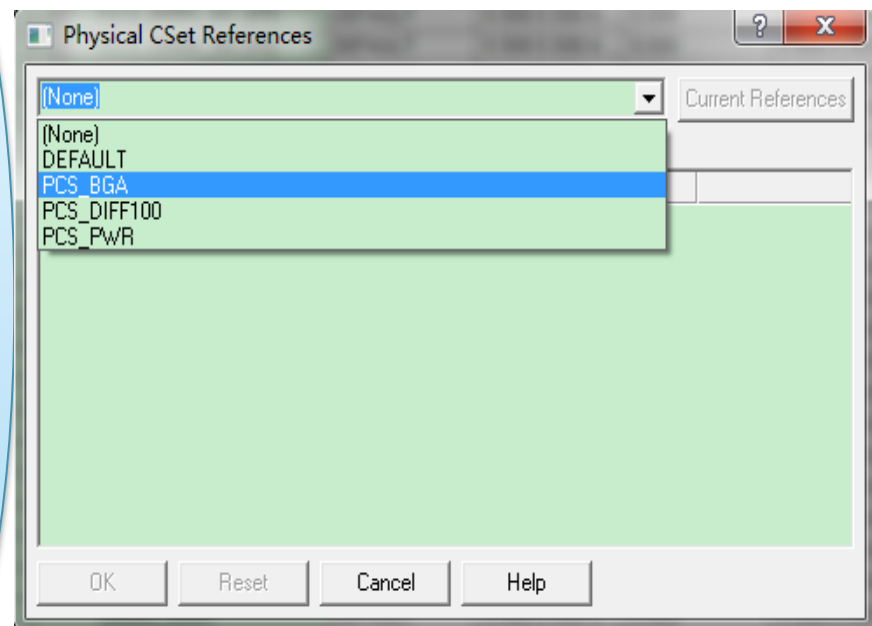
Type	Objects	Referenced Physical CSet	Line Width	
			Min mil	Max mil
*	*	*	*	*
Dsn	demo	DEFAULT	5.500:5.500:4....	0.000
NCIs	CLS_B_VOUT_D_0_7 (8)	DEFAULT	5.500:5.500:4....	0.000
NCIs	CLS_DDRO_AC (21)	DEFAULT	5.500:5.500:4....	0.000
NCIs	CLS_GMII0_RX (11)	DEFAULT	5.500:5.500:4....	0.000
NCIs	CLS_GMII0_TX (10)	DEFAULT	5.500:5.500:4....	0.000
NCIs	CLS_GMII1_RX (11)	DEFAULT	5.500:5.500:4....	0.000
NCIs	CLS_GMII1_TX (10)	DEFAULT	5.500:5.500:4....	0.000
NCIs	CLS_GPMC_D_0_15 (16)	DEFAULT	5.500:5.500:4....	0.000
NCIs	CLS_PWR (44)	PCS_PWR	10.000	0.000

物理约束 (Physical Constraint)

- 为Net Class添加 Physical约束



方法二



间距约束 (Spacing Constraint)

• 设置Default约束

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo] - [Spacing Constraint Sets: All Layers [demo]]

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector: demo

Electrical Physical **Spacing**

Spacing Constrain

All Layers Line

Type	Objects	Line To										
		Line mil	Thru Pin mil	SMD Pin mil	Test Pin mil	Thru Via mil	BB Via mil	Test Via mil	Microvia mil	Shape mil	Bond Finger mil	Hole mil
Dsn	demo	8.000:6.000	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
SCS	DEFAULT	8.000:...	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo] - [Spacing Constraint Sets: All Layers [demo]]

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector: demo

Electrical Physical **Spacing**

Spacing Constrain

All Layers Line Pins

Type	Objects	Thru Pin To									
		Line mil	Thru Pin mil	SMD Pin mil	Test Pin mil	Thru Via mil	BB Via mil	Test Via mil	Microvia mil	Shape mil	Bond Finger mil
Dsn	demo	4.000	8.000	8.000	8.000	5.000	5.000	5.000	5.000	10.000	5.000
SCS	DEFAULT	4.000	8.000	8.000	8.000	5.000	5.000	5.000	5.000	10.000	5.000

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo] - [Spacing Constraint Sets: All Layers [demo]]

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector: demo

Electrical Physical **Spacing**

Spacing Constrain

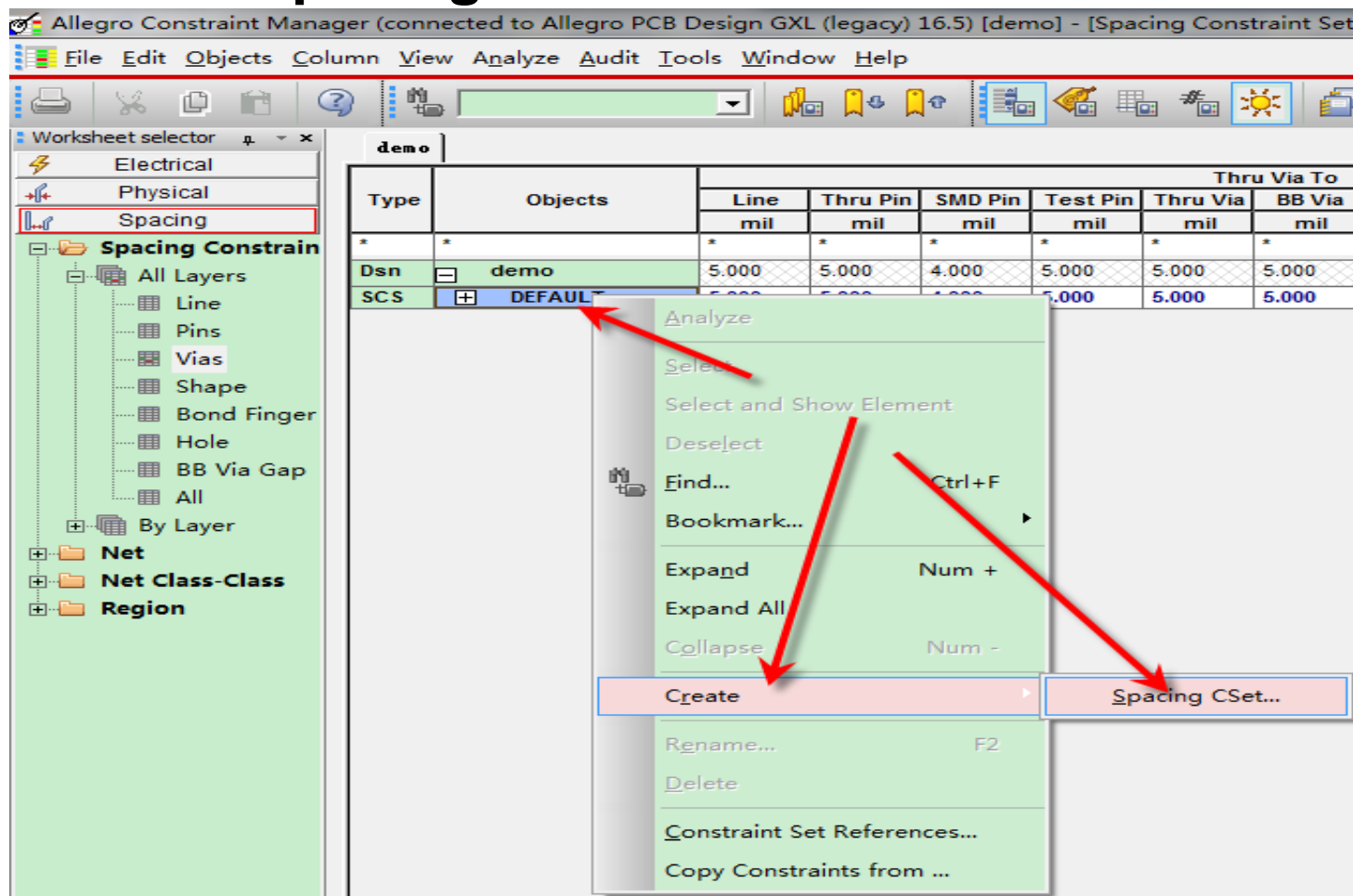
All Layers Line Pins Vias

Type	Objects	Thru Via To									
		Line mil	Thru Pin mil	SMD Pin mil	Test Pin mil	Thru Via mil	BB Via mil	Test Via mil	Microvia mil	Shape mil	Bond Finger mil
Dsn	demo	5.000	5.000	4.000	5.000	5.000	5.000	5.000	5.000	10.000	5.000
SCS	DEFAULT	5.000	5.000	4.000	5.000	5.000	5.000	5.000	5.000	10.000	5.000

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo] - [Spacing Constraint Sets: All Layers [demo]]

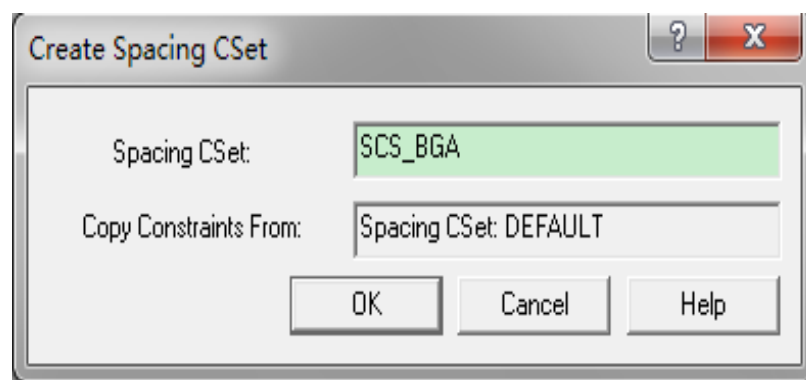
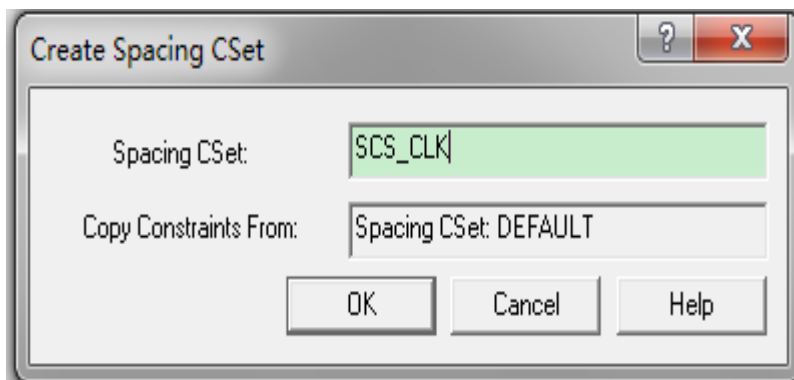
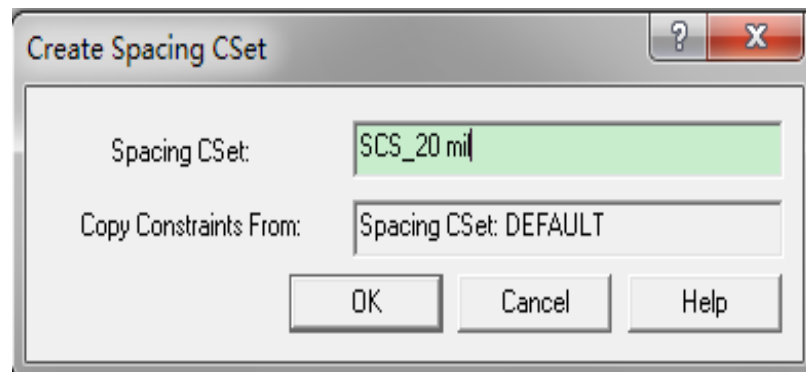
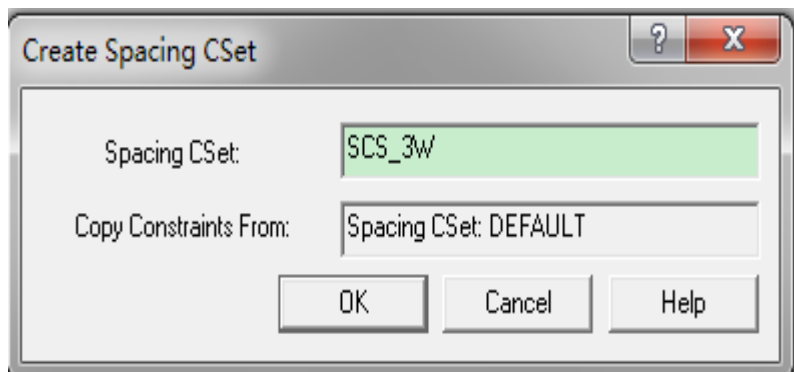
间距约束 (Spacing Constraint)

- 建立扩展Spacing约束



间距约束（Spacing Constraint）

- 建立扩展Spacing约束



间距约束 (Spacing Constraint)

- 建立扩展Spacing约束

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo] - [Spacing Constraint Sets: All Layers [demo]]

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector: demo

Electrical Physical **Spacing**

Spacing Constraint

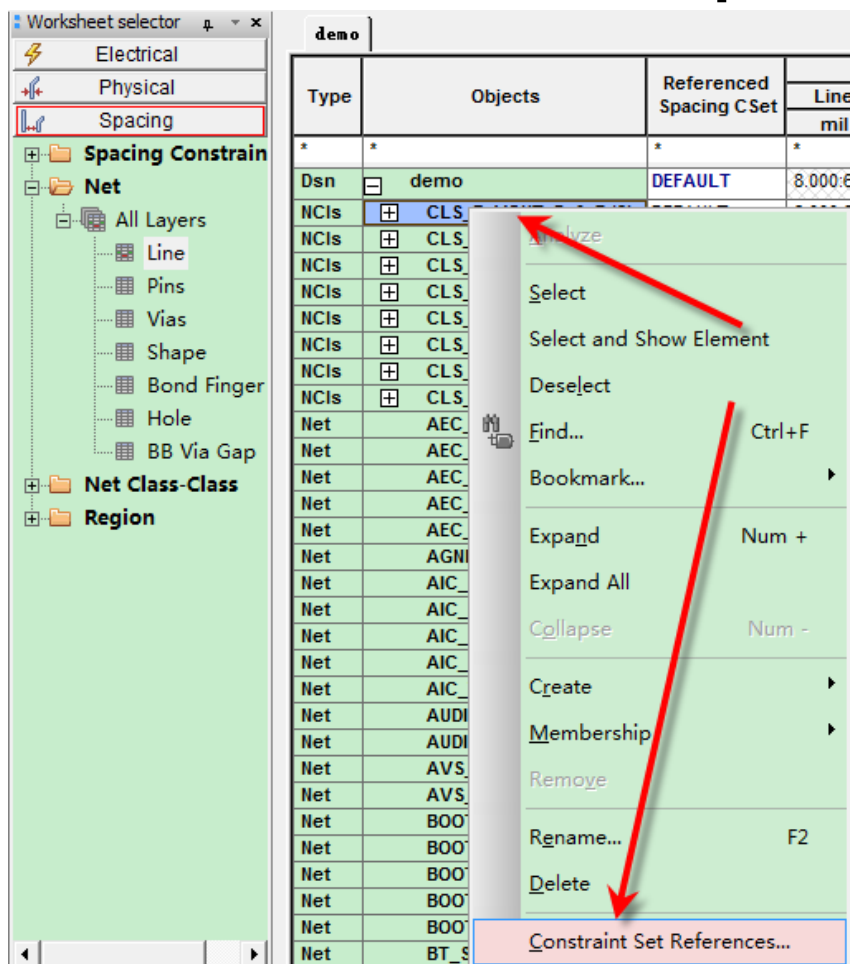
- All Layers
- Line
- Pins
- Vias
- Shape
- Bond Finger
- Hole
- BB Via Gap
- All
- By Layer
- Net
- Net Class Class

Type	Objects	Thru Via To									
		Line mil	Thru Pin mil	SMD Pin mil	Test Pin mil	Thru Via mil	BB Via mil	Test Via mil	Microvia mil	Shape mil	Bond Finger mil
Dsn	demo	5.000	5.000	4.000	5.000	5.000	5.000	5.000	5.000	10.000	5.000
SCS	DEFAULT	5.000	5.000	4.000	5.000	5.000	5.000	5.000	5.000	10.000	5.000
SCS	SCS_BGA	5.000	5.000	4.000	5.000	5.000	5.000	5.000	5.000	10.000	5.000
SCS	SCS_CLK	20.000	5.000	4.000	5.000	5.000	5.000	5.000	5.000	20.000	5.000
SCS	SCS_3W	5.000	5.000	4.000	5.000	5.000	5.000	5.000	5.000	10.000	5.000
SCS	SCS_20MIL	20.000	5.000	4.000	5.000	6.000	5.000	5.000	5.000	20.000	5.000
Lyr	TOP	20.000	5.000	4.000	5.000	6.000	5.000	5.000	5.000	20.000	5.000
Lyr	GND02	20.000	5.000	4.000	5.000	6.000	5.000	5.000	5.000	20.000	5.000
Lyr	ART03	20.000	5.000	4.000	5.000	6.000	5.000	5.000	5.000	20.000	5.000
Lyr	PWR04	20.000	5.000	4.000	5.000	6.000	5.000	5.000	5.000	20.000	5.000
Lyr	GND05	20.000	5.000	4.000	5.000	6.000	5.000	5.000	5.000	20.000	5.000
Lyr	ART06	20.000	5.000	4.000	5.000	6.000	5.000	5.000	5.000	20.000	5.000
Lyr	PWR07	20.000	5.000	4.000	5.000	6.000	5.000	5.000	5.000	20.000	5.000
Lyr	BOTTOM	20.000	5.000	4.000	5.000	6.000	5.000	5.000	5.000	20.000	5.000

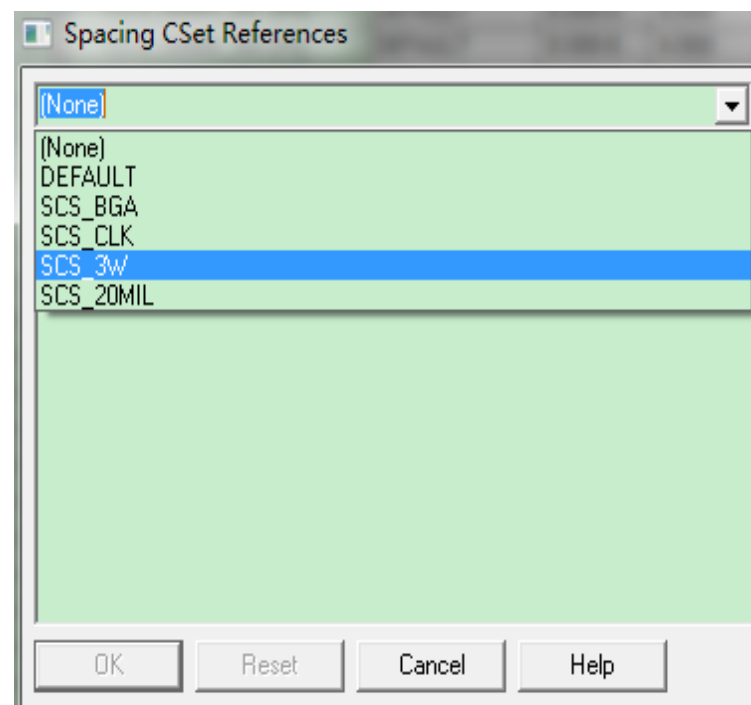
对任意层进行设置

间距约束 (Spacing Constraint)

- 为Net Class 添加 Spacing约束

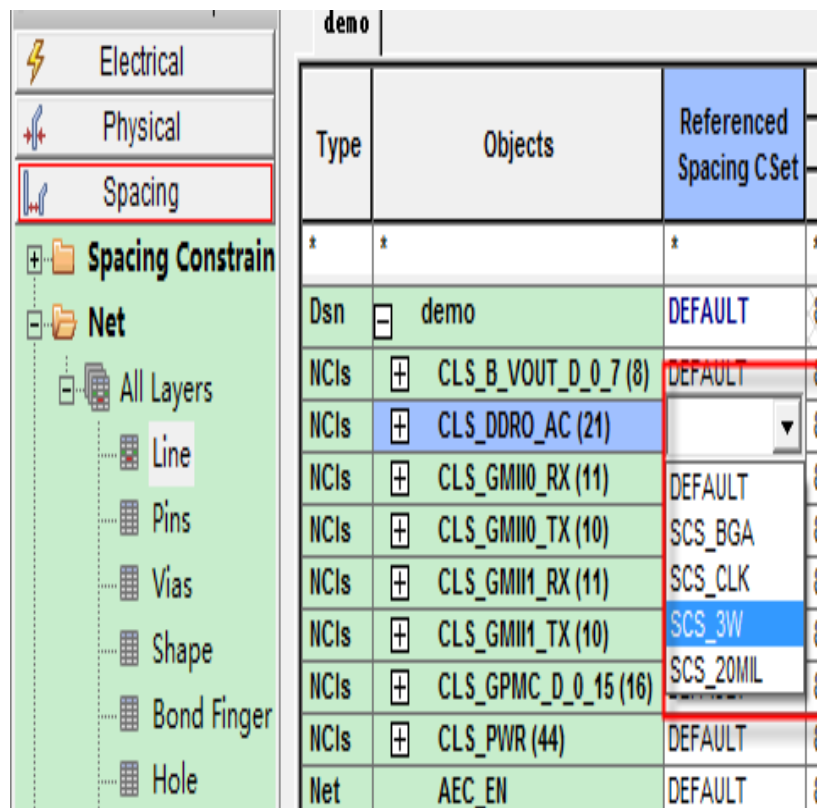


方法一



间距约束 (Spacing Constraint)

- 为Net Class 添加 Spacing约束

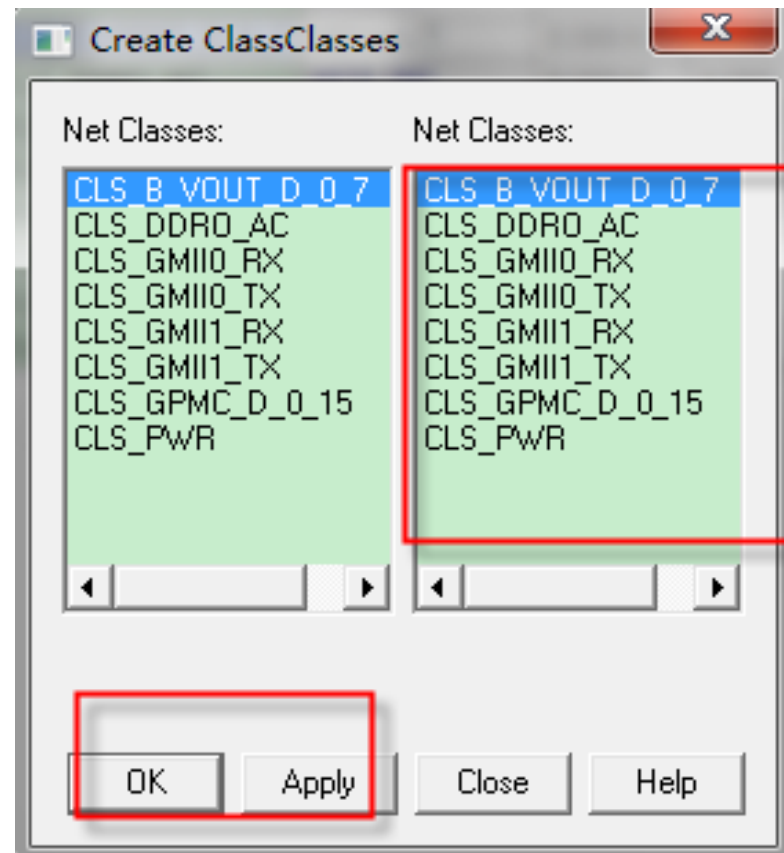
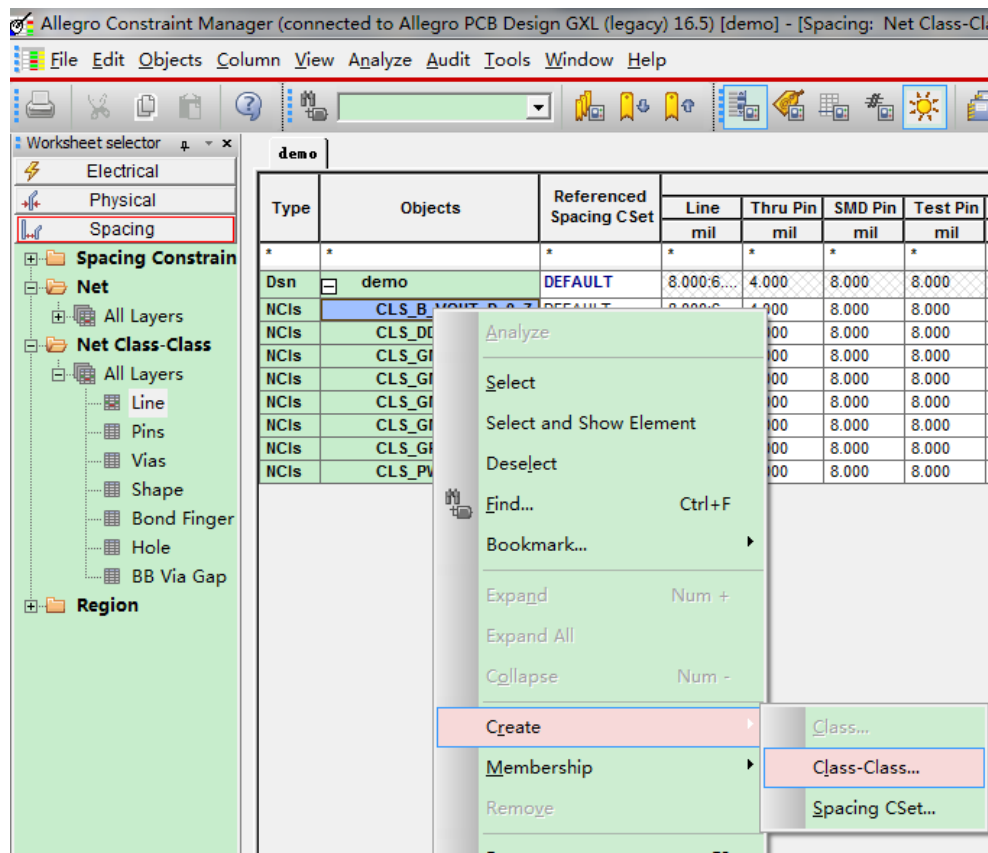


方法二

NCIs	CLS_DDRO_AC (21)	SCS_3W	8.000:6....	4.000
Net	DDR0_A0	SCS_3W	8.000:6....	4.000
Net	DDR0_A1	SCS_3W	8.000:6....	4.000
Net	DDR0_A2	SCS_3W	8.000:6....	4.000
Net	DDR0_A3	SCS_3W	8.000:6....	4.000
Net	DDR0_A4	SCS_3W	8.000:6....	4.000
Net	DDR0_A5	SCS_3W	8.000:6....	4.000
Net	DDR0_A6	SCS_3W	8.000:6....	4.000
Net	DDR0_A7	SCS_3W	8.000:6....	4.000
Net	DDR0_A8	SCS_3W	8.000:6....	4.000
Net	DDR0_A9	SCS_3W	8.000:6....	4.000
Net	DDR0_A10	SCS_3W	8.000:6....	4.000
Net	DDR0_A11	SCS_3W	8.000:6....	4.000
Net	DDR0_A12	SCS_3W	8.000:6....	4.000
Net	DDR0_A13	SCS_3W	8.000:6....	4.000
Net	DDR0_A14	SCS_3W	8.000:6....	4.000
Net	DDR0_BA0	SCS_3W	8.000:6....	4.000
Net	DDR0_BA1	SCS_3W	8.000:6....	4.000
Net	DDR0_BA2	SCS_3W	8.000:6....	4.000
Net	DDR0_CASN	SCS_3W	8.000:6....	4.000
Net	DDR0_CKE	SCS_3W	8.000:6....	4.000
Net	DDR0_CSN	SCS_3W	8.000:6....	4.000

间距约束 (Spacing Constraint)

- 建立Net Class-Class 间距约束



间距约束 (Spacing Constraint)

- 建立Net Class-Class 间距约束

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo] - [Spacing: Net Class-]

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector

Electrical

Physical

Spacing

Spacing Constrains

Net

All Layers

Net Class-Class

All Layers

Line

Pins

Vias

Shape

Bond Finger

demo

Type	Objects	Referenced Spacing CSet	Line mil	Thru Pin mil	SMD Pin mil	Test Pin mil
*	*	*	*	*	*	*
Dsn	demo	DEFAULT	8.000:6....	4.000	8.000	8.000
NCIs	CLS_B_VOUT_D_0_7	DEFAULT	8.000:6....	4.000	8.000	8.000
CCIs	CLS_DDRO_AC	SCS_3W	8.000:6....	4.000	8.000	8.000
CCIs	CLS_GMII0_RX	DEFAULT	8.000:6....	4.000	8.000	8.000
NCIs	CLS_DDRO_AC (1)	SCS_3W	8.000:6....	4.000	8.000	8.000
NCIs	CLS_GMII0_RX (1)	DEFAULT	8.000:6....	4.000	8.000	8.000
NCIs	CLS_GMII0_TX	DEFAULT	8.000:6....	4.000	8.000	8.000
NCIs	CLS_GMII1_RX	DEFAULT	8.000:6....	4.000	8.000	8.000
NCIs	CLS_GMII1_TX	DEFAULT	8.000:6....	4.000	8.000	8.000
NCIs	CLS_GPMC_D_0_15	DEFAULT	8.000:6....	4.000	8.000	8.000
NCIs	CLS_PWR	DEFAULT	8.000:6....	4.000	8.000	8.000

可以对新的 Net Class 添加约束

间距约束 (Spacing Constraint)

• 层间约束 (Constraint By Layer)

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo] - [Spacing Constraint Sets: By Layer [demo]]

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector: demo

Electrical
Physical
Spacing

Spacing Constraint

- All Layers
- By Layer
 - Line
 - Pins
 - Vias
 - Shape
 - Bond Finger
 - Hole
 - All
- Net
- Net Class-Class

Type	Objects	Line To										
		Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Microvia	Shape	Bond Finger	Hole
		mil	mil	mil	mil	mil	mil	mil	mil	mil	mil	mil
*	*	*	*	*	*	*	*	*	*	*	*	*
Dsn	demo	8.000:6...	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	TOP	8.000	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	GND02	6.000	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	ART03	9.600	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
SCS	DEFAULT	9.600	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
SCS	SCS_BGA	9.600	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
SCS	SCS_CLK	9.600	4.000	8.000	8.000	20.000	6.000	6.000	6.000	10.000	6.000	8.000
SCS	SCS_3W	9.600	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
SCS	SCS_20MIL	9.600	4.000	8.000	8.000	20.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	PWR04	6.000	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	GND05	9.600	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	ART06	9.600	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	PWR07	6.000	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	BOTTOM	8.000	4.000	8.000	8.000	5.000	6.000	6.000	6.000	10.000	6.000	8.000

Same Net Spacing Constraint

- 设置和Spacing约束操作一样，注意是相同网络的对象之间的间距。

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo] - [Same Net Spacing Constraint Sets: All Layers [demo]]

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector: demo

Electrical Physical Spacing **Same Net Spacing**

Same Net Spacing

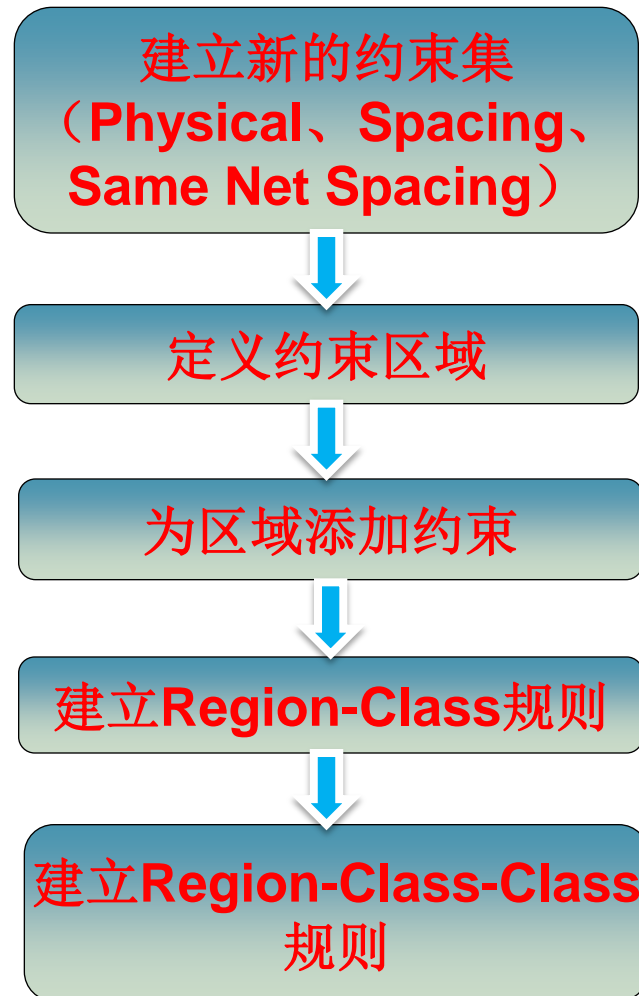
- All Layers
 - Line
 - Pins
 - Vias
 - Shape
 - Bond Fing
 - Hole
 - Options

Type	Objects	Line To										
		Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Microvia	Shape	Bond Finger	Hole
		mil	mil	mil	mil	mil	mil	mil	mil	mil	mil	mil
*	*	*	*	*	*	*	*	*	*	*	*	*
Dsn	demo	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000
SNSC	BGA	4.000	8.000	4.000	8.000	4.000	6.000	6.000	6.000	10.000	6.000	8.000
SNSC	DEFAULT	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	TOP	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	GND02	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	ART03	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	PWR04	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	GND05	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	ART06	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	PWR07	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000
Lyr	BOTTOM	6.000	4.000	8.000	8.000	6.000	6.000	6.000	6.000	10.000	6.000	8.000

区域约束（Region Constraint）

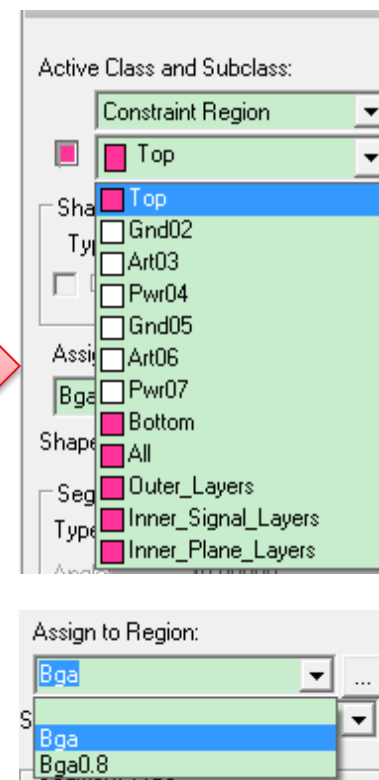
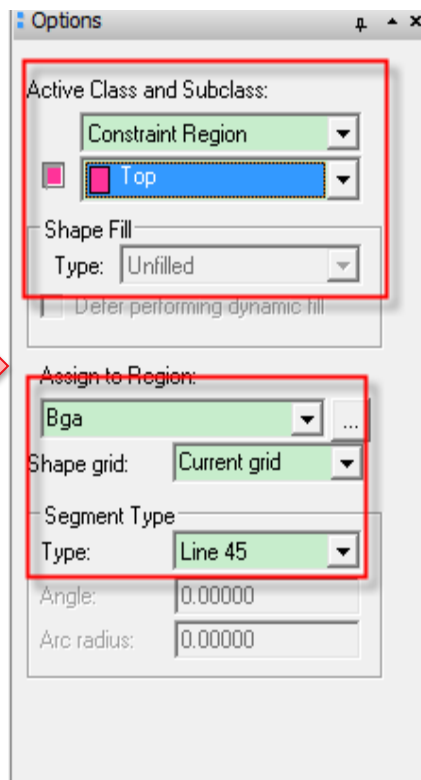
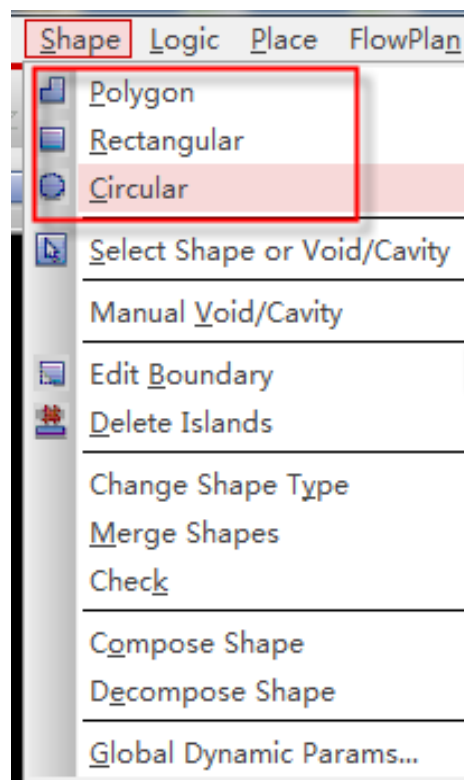
- 某些设计，用户会在部分区域使用特殊的设计规则，如 **BGA** 的附近区域需要用到更小的 **Line** 宽度和间距等。
- 首先，用户需要根据设计需求建立新的扩展（**Physical**、**Spacing**、**Same Net Spacing**）约束；
- 其次，用 **Shape命令** 来定义约束区域，随后为区域添加新的约束；
- 最后，如果约束区域中 **不同的Net Class** 需要不同的设计规则或者 **不同Net Class的网络** 之间需要不同的设计规则，则需要建立 **Region-Class** 或者 **Region-Class-Class**，并对其添加约束。

区域约束 (Region Constraint)



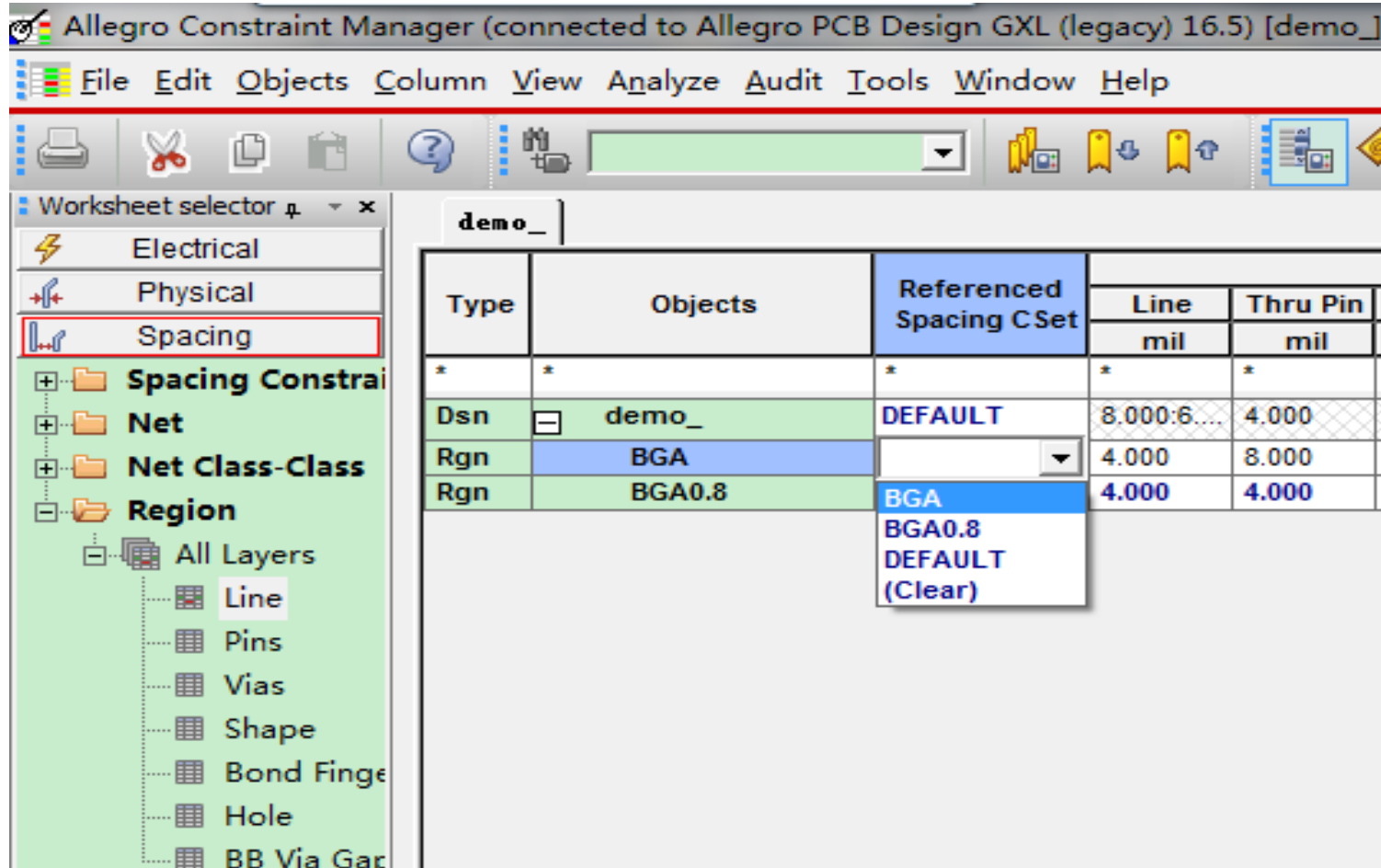
区域约束 (Region Constraint)

- 定义约束区域



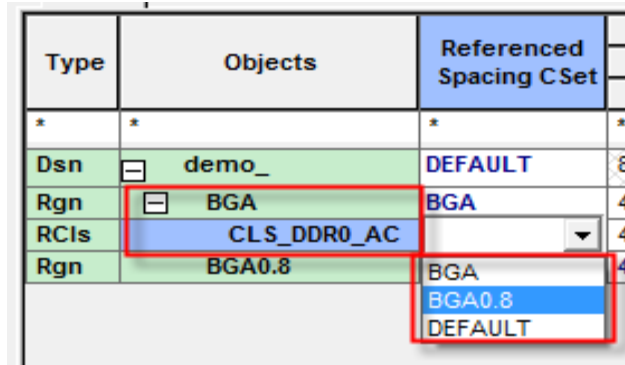
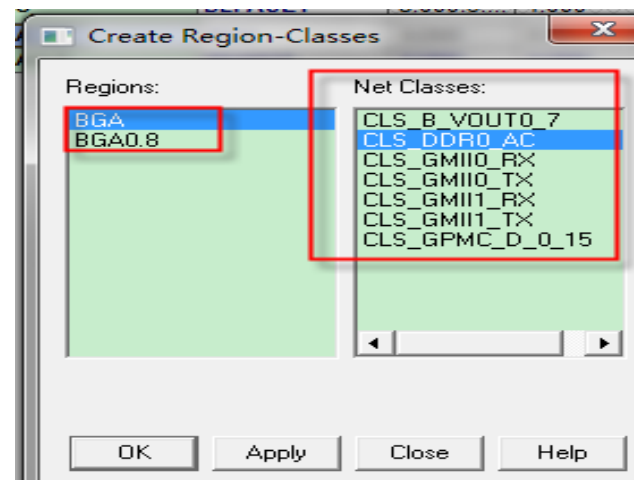
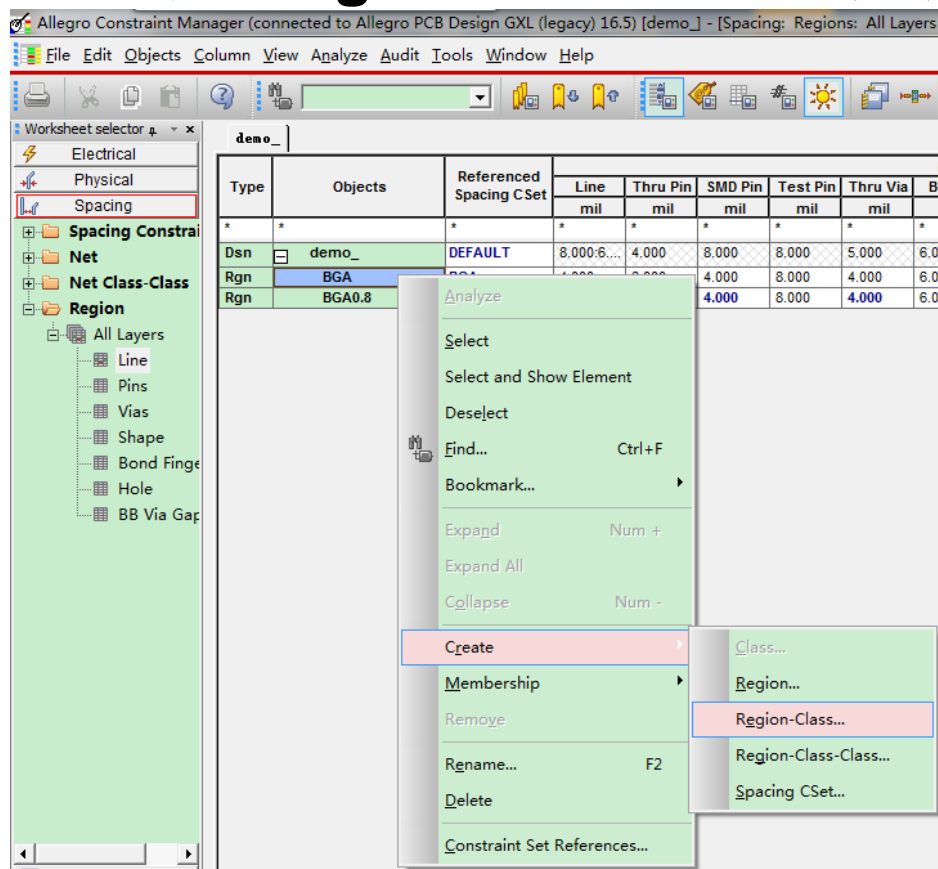
区域约束 (Region Constraint)

- 为区域添加约束



区域约束 (Region Constraint)

- 建立Region-Classes规则 (Net & Net Class都采用区域规则) Region-Class-Class类似



Net属性

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo_] - [Properties: Nets: Electrical Properties [demo_]]

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector p. x

demo_

Type	Objects	Referenced Electrical C Set	Frequency MHz	Period ns	Duty Cycle %	Jitter ps	Cycle to Measure	Offset ns
Dsn	demo_							
Net	AEC_EN							

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo_] - [Properties: Nets: General Properties [demo_]]

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector p. x

demo_

Type	Objects	Voltage V	Weight	No Rat	Route Priority	to Shape	Fixed	Route Restrictions No Route	No Ripup	No Pin Escape	Prohibit	Testpoints Quantity	Probe Number	Backdrill Max PTH Stub mil
Dsn	demo_													
Net	AEC_EN													
Net	AEC_LED0													
Net	AEC_LED1													
Net	AEC_OUT													

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo_] - [Properties: Nets: Ratsnest Bundle Properties [demo_]]

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector p. x

demo_

Type	Objects	Layer Transitions Layer Matching	Max Transition Count	Pattern	Min Wrap Gap mil	Min Amplitude mil	Max Amplitude mil	Corner Type	Corner Length mil
Dsn	demo_	FALSE	No limit	ACCORDION	3x width	No limit	No limit	45	1x width
Net	AEC_EN	TRUE							
Net	AEC_LED0	FALSE							
Net	AEC_LED1	(Clear)							
Net	AEC_OUT								
Net	AEC_SPK_OUT								

Component属性和Pin属性

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo_] - [Properties: Components: Pin Properties [demo_]]

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector

Electrical
Physical
Spacing
Same Net Spacing
Properties

Net

Component

- Component Properties
 - General
 - Thermal
 - Swapping
 - Reuse
- Pin Properties
 - General
 - Shapes
 - Manufacturing

demo_

Type	Objects	Backdrill		IDF Owner
		Exclude	Min Pin Plated Thru Hole	
*	*	*	*	*
Dsn	demo_			
PrtD	ACM1513_ACM1211_ACM1211			
Prtl	T1			
Pin	T1.1			
Pin	T1.2			
Pin	T1.3			
Pin	T1.4			
PrtD	ADG884BRMZ_MSOP10_ADG884BRMZ			
PrtD	BCP69T1_SOT-223_BCP69T1			
PrtD	CAP NP_C_EIA0402_0.1UF			
PrtD	CAP NP_C_EIA0402_0.01UF			
PrtD	CAP NP_C_EIA0402_0.22UF			
PrtD	CAP NP_C_EIA0402_1000PF			
PrtD	CAP NP_C_EIA0603_NO POP			
PrtD	CAP NP_C_EIA0603_0.1UF			
PrtD	CAP NP_C_EIA0603_0.1UF/100V			
PrtD	CAP NP_C_EIA0603_0.01UF			
PrtD	CAP NP_C_EIA0603_0.033UF			
PrtD	CAP NP_C_EIA0603_0.047UF			
PrtD	CAP NP_C_EIA0603_1UF			
PrtD	CAP NP_C_EIA0603_22PF			
PrtD	CAP NP_C_EIA0603_33PF			
PrtD	CAP NP_C_EIA0603_56PF			
PrtD	CAP NP_C_EIA0603_220PF			
PrtD	CAP NP_C_EIA0603_560PF			
PrtD	CAP NP_C_EIA0603_1000PF			
PrtD	CAP NP_C_EIA0603_1200PF			
PrtD	CAP NP_C_EIA0805_0.47UF			
PrtD	CAP NP_C_EIA0805_0.012UF			
PrtD	CAP NP_C_EIA0805_0.022UF			
PrtD	CAP NP_C_EIA0805_4.7UF			

DRC工作表

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo_] - [DRCs: Physical [demo_]]

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector

- Electrical
- Physical
- Spacing
- Same Net Spacing
- Properties
- DRC**
 - DRC
 - Electrical
 - Physical
 - Spacing
 - Same Net Spacing
 - Design
 - External

demo_

Objects	Constraint Set	DRC Subclass	Values	
			Required	Actual
*	*	*	*	*
demo_				

电气约束 (Electrical Constraint)

- 用户可以通过**Electrical**约束对设计中的高速信号进行约束设计。

The screenshot shows the Allegro Constraint Manager interface. On the left, the 'Electrical' constraint set is expanded, showing a tree structure with 'Routing' and 'Net' categories. The 'Routing' category is highlighted with a red box, and the 'Net' category is also highlighted with a red box. A red text overlay '6类&6张不同的工作表' (6 categories & 6 different worksheets) is placed over the 'Routing' and 'Net' categories. On the right, a table lists the objects for the 'demo_' worksheet.

Type	Objects	R	Elk
*	*	*	*
Dsn	demo_		
Net	AEC_EN		
Net	AEC_LED0		
Net	AEC_LED1		
Net	AEC_OUT		
Net	AEC_SPK_OUT		
Net	AGND_AUDIO		
Net	AIC_BCLK		
Net	AIC_DIN		
Net	AIC_DOUT		
Net	AIC_MCLK		
Net	AIC_WCLK		
Net	AUDIO_LOUT		
Net	AUDIO_ROUT		
Net	AUDIO_VCC_3V3		
Net	AVCC12_9233A		
Net	AVCC12_9233B		
Net	AVCC33_9233A		
Net	AVCC33_9233B		
Net	AVS_ADJ		
Net	AVS_ENN		
Net	BOOTMODE0		
Net	BOOTMODE1		
Net	BOOTMODE2		
Net	BOOTMODE3		
Net	BOOTMODE4		
Net	RT_SFI0		

电气约束 (Electrical Constraint)

Relative Propagation Delay工作表

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo_] - [Electrical: Nets: Routing [demo_]]

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector

Electrical

Electrical Constraint Set

- Signal Integrity
- Timing
- Routing
- All Constraints

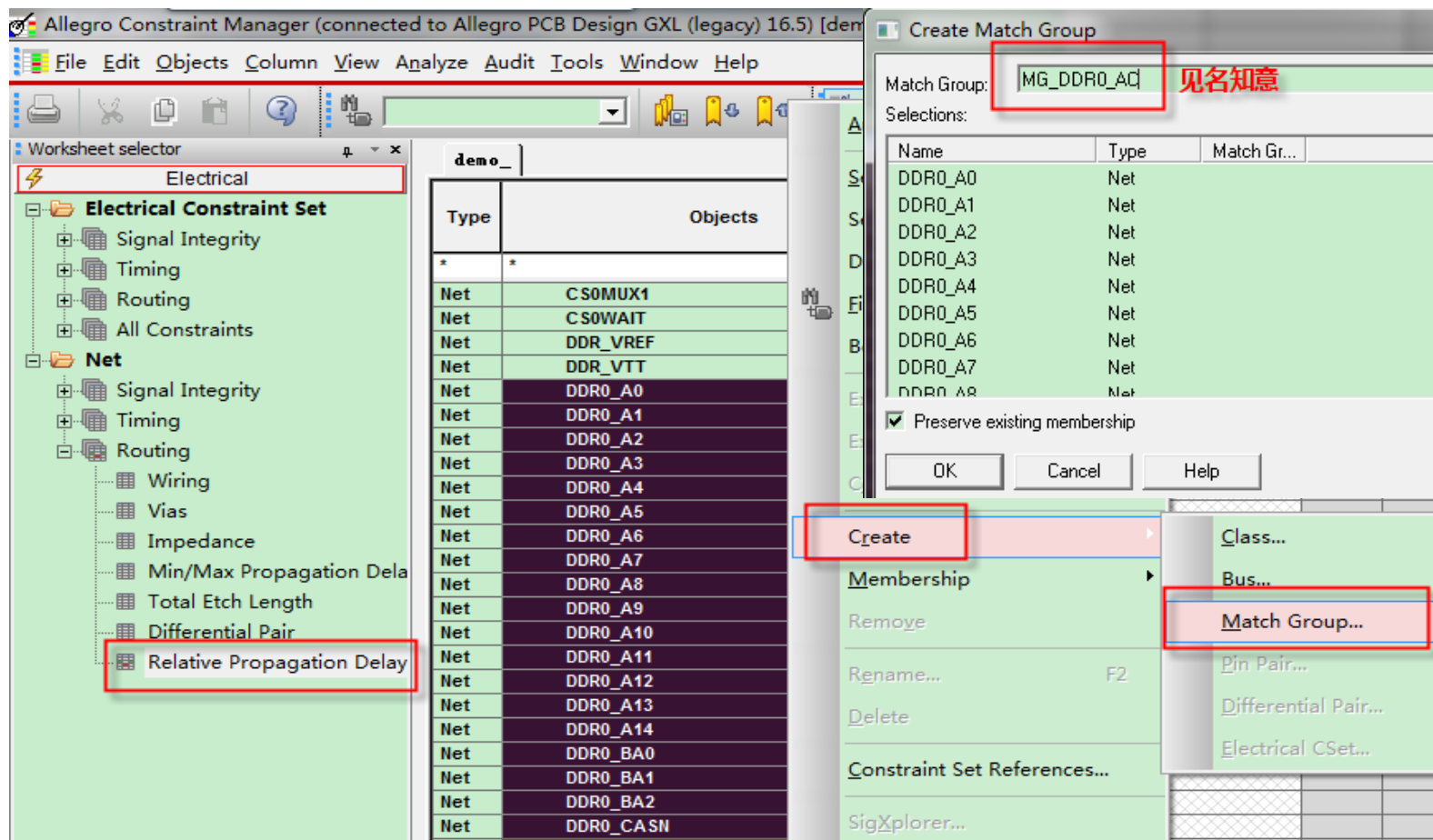
Net

- Signal Integrity
- Timing
- Routing
 - Wiring
 - Vias
 - Impedance
 - Min/Max Propagation Delay
 - Total Etch Length
 - Differential Pair
 - Relative Propagation Delay

Type	Objects	Referenced Electrical CSet	Pin Pairs	Pin Delay		Scope	Delta: T
				Pin 1 mil	Pin 2 mil		
*	*	*	*	*	*	*	*
Dsn	demo_						
MGrp	MG_DDR0_AC (21)		All Drivers/All Rece...			Global	0 mil:25 mil
Net	DDR0_A0		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A1		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A2		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A3		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A4		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A5		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A6		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A7		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A8		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A9		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A10		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A11		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A12		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A13		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_A14		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_BA0		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_BA1		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_BA2		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_CASN		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_CKE		All Drivers/All Receivers			Global	0 mil:25 mil
Net	DDR0_CSN		All Drivers/All Receivers			Global	0 mil:25 mil

电气约束 (Electrical Constraint)

- 创建Relative Propagation Delay约束 (方式一)

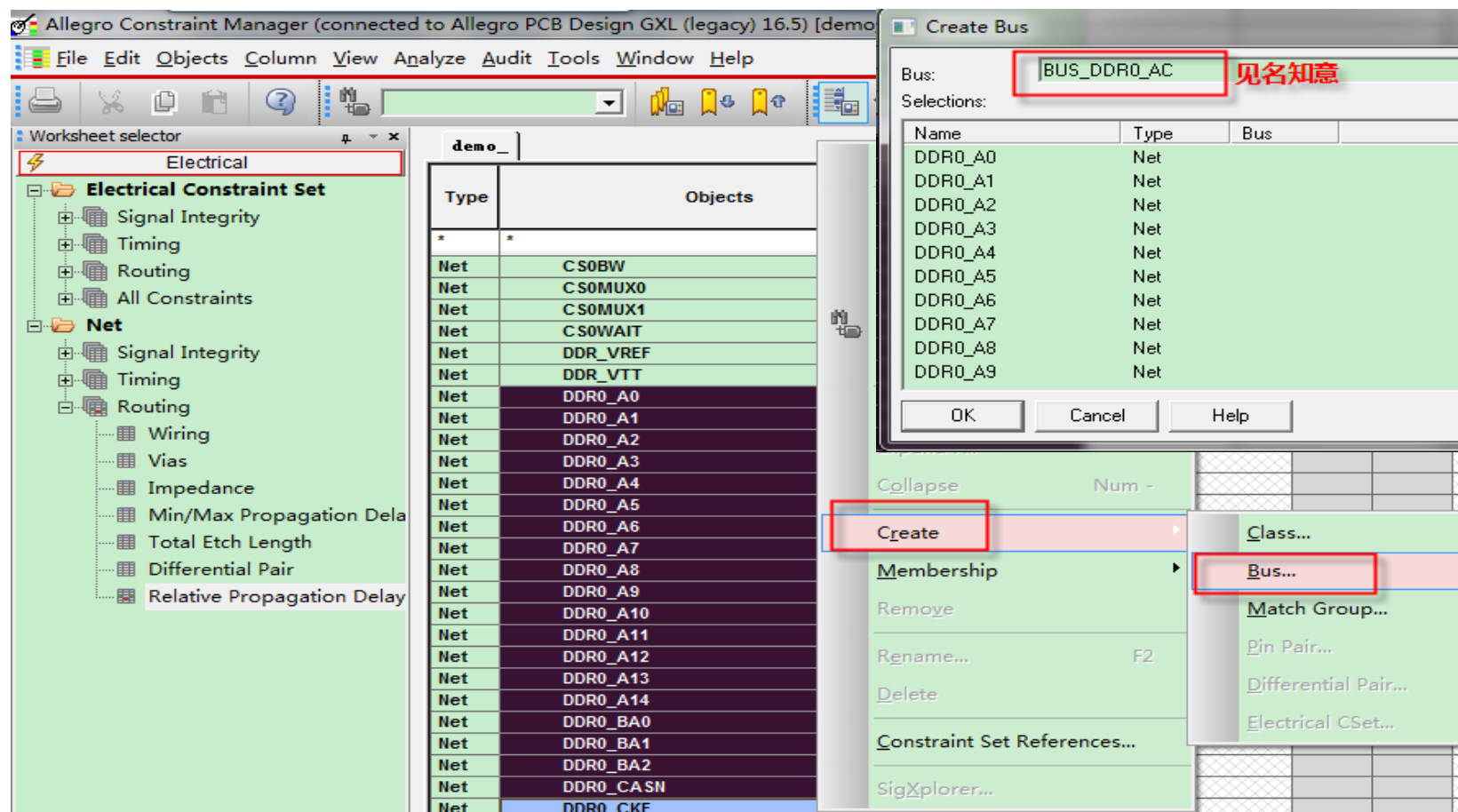


- 创建Relative Propagation Delay约束（方式一）

The screenshot shows the 'Propagation delay and tolerance' dialog box. The 'Delta' field is set to '0 mil' and the 'Tolerance' field is set to '25 mil'. A red box highlights these two fields. A blue arrow points from the 'Change...' option in the context menu to the dialog box. The context menu also shows options like 'Analyze', 'Go to source', 'Formula...', 'Dependencies...', 'Calculate', 'Set as target', 'Clear', 'Cut', 'Copy', 'Paste', 'Paste Special...', and 'Information...'.

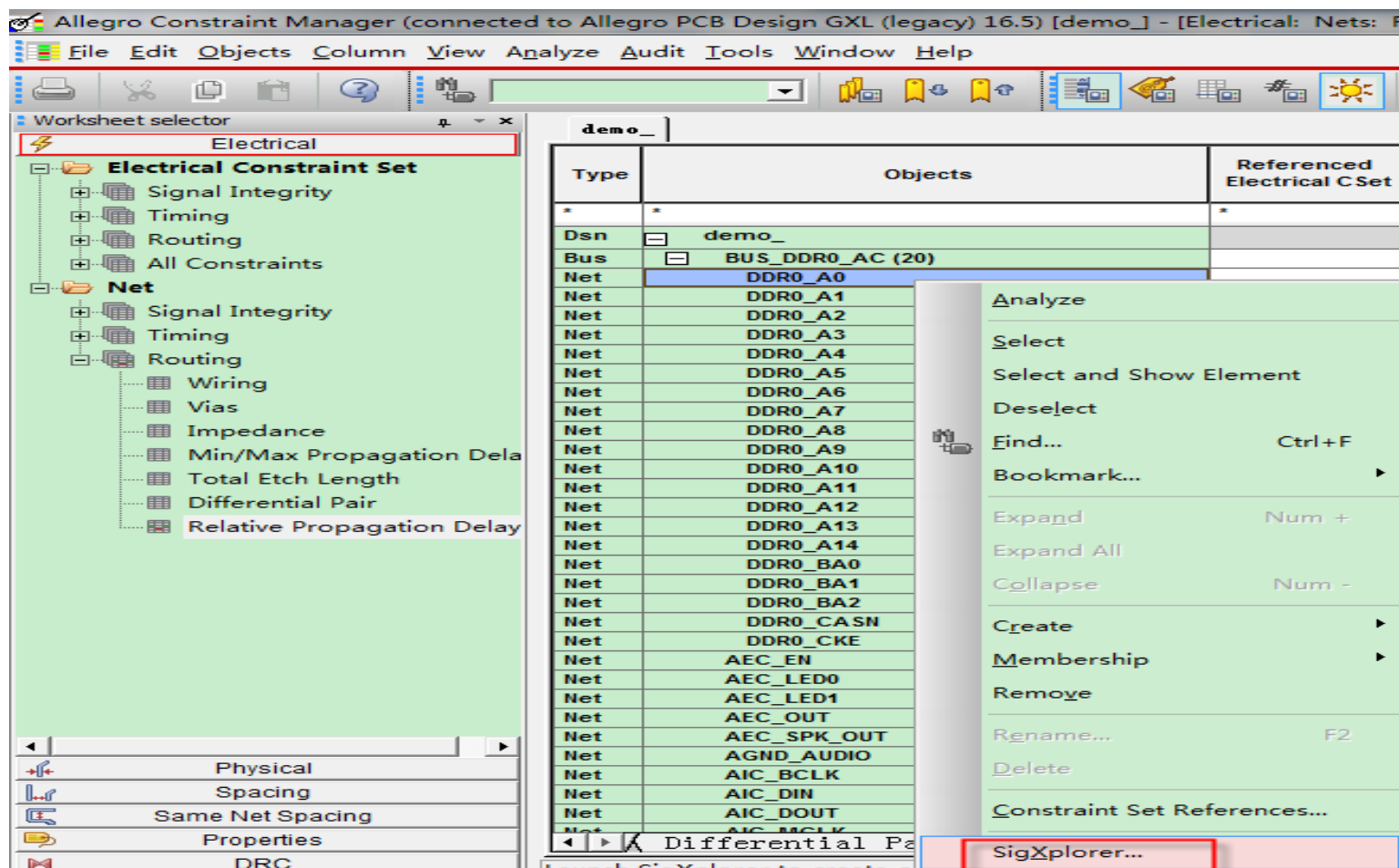
电气约束 (Electrical Constraint)

• 创建Relative Propagation Delay约束 (方式二)



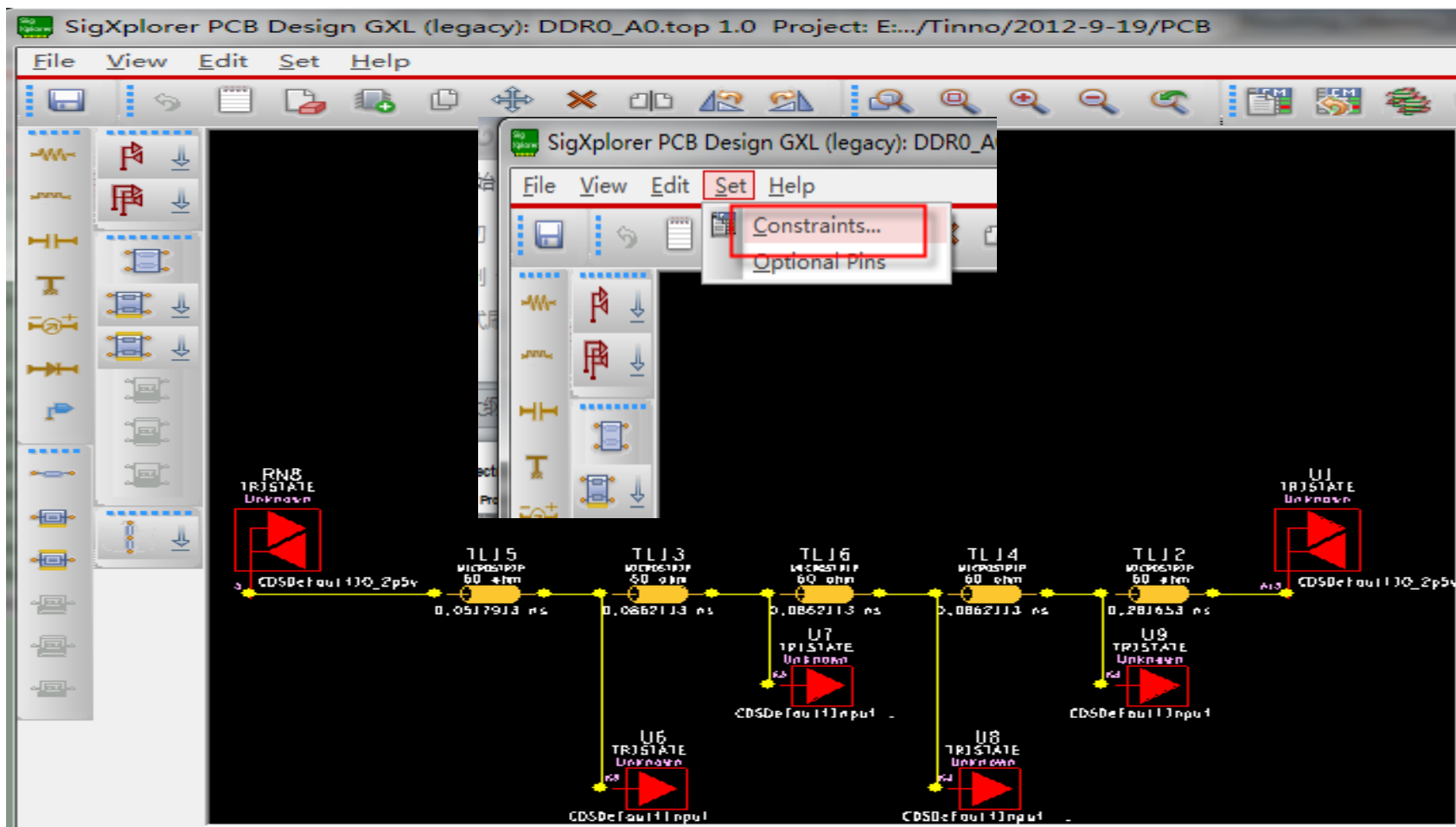
电气约束 (Electrical Constraint)

- 创建Relative Propagation Delay约束 (方式二)



电气约束 (Electrical Constraint)

- 创建Relative Propagation Delay约束 (方式二)



电气约束 (Electrical Constraint)

• 创建Relative Propagation Delay约束 (方式二)

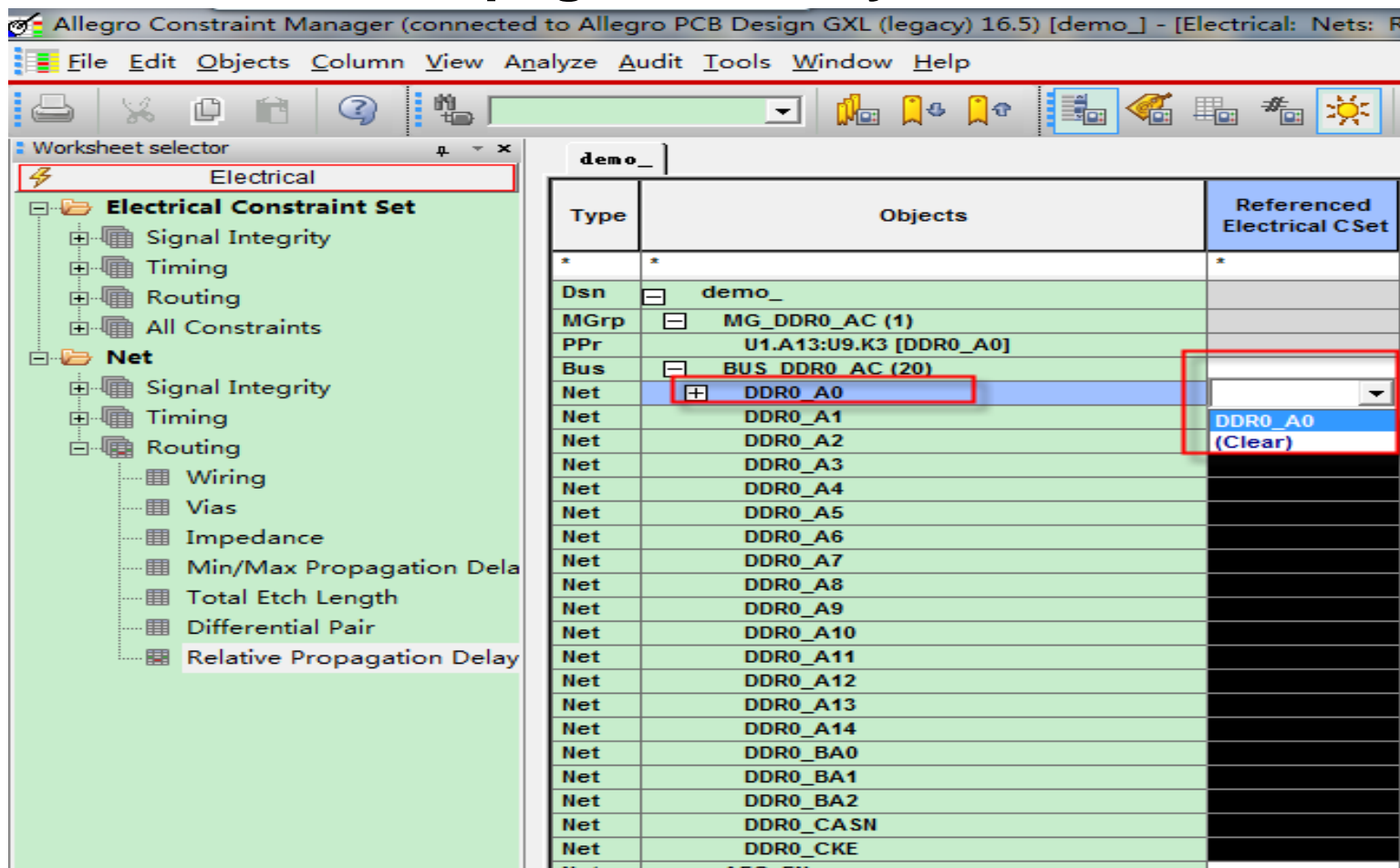
The screenshot illustrates the steps to create a Relative Propagation Delay constraint in SigXplorer PCB Design GXL. The 'Set' menu is open, and the 'Constraints...' option is selected. The 'Set Topology Constraints' dialog is shown, with the 'Rel Prop Delay' tab selected. The 'Rule Name' is 'MG_DDR0_AC', 'From' is 'U1.A13', 'To' is 'U9.K3', 'Scope' is 'Global', 'Delta Type' is 'Length', 'Delta' is '0.000 MIL', and 'Tol Type' is 'Length'. The 'Add' button is highlighted. The 'Pins/Tees' table lists various components and their usage.

Name	Usage
ALL DRVRS/RCVRS	
DRIVER/RECEIVER	
LONGEST	
RN8.5	IO
U1.A13	IO
U6.K3	IN
U7.K3	IN
U8.K3	IN
U9.K3	IN

一定记得 Update Cm

电气约束 (Electrical Constraint)

- 创建Relative Propagation Delay约束 (方式二)



电气约束 (Electrical Constraint)

• Differential Pair 工作表

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo_] - [Electrical: Nets: Routing [demo_]]

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector

Electrical

Electrical Constraint Set

- Signal Integrity
- Timing
- Routing
- All Constraints
- Net
 - Signal Integrity
 - Timing
 - Routing
 - Wiring
 - Vias
 - Impedance
 - Min/Max Propagation Delay
 - Total Etch Length
 - Differential Pair
 - Relative Propagation Delay

demo_

Type	Objects	Referenced Electrical CSet	Pin Delay		Gather Control	Uncoupled Length	
			Pin 1 mil	Pin 2 mil		Length Ignore mil	Max mil
*	*	*	*	*	*	*	*
Net	CPU_RESETN						
Net	CS0BW						
Net	CS0MUX0						
Net	CS0MUX1						
Net	CS0WAIT						
Net	DDR_VREF						
Net	DDR_VTT						
Net	DDR0_CLK0						
Net	DDR0_CLK0N						
Net	DDR0_CSN						
Net	DDR0_DQM0						
Net	DDR0_DQM1						
Net	DDR0_DQM2						
Net	DDR0_DQM3						
Net	DDR0_DQS0						
Net	DDR0_DQS0N						
Net	DDR0_DQS1						
Net	DDR0_DQS1N						
Net	DDR0_DQS2						
Net	DDR0_DQS2N						
Net	DDR0_DQS3						
Net	DDR0_DQS3N						
Net	DDR0_D0						
Net	DDR0_D1						
Net	DDR0_D2						
Net	DDR0_D3						
Net	DDR0_D4						
Net	DDR0_D5						

Analyze

Select

Select and Show Element

Deselect

Find... Ctrl+F

Bookmark...

Expand Num +

Expand All

Collapse Num -

Create

Membership

Remove

Rename... F2

Class...

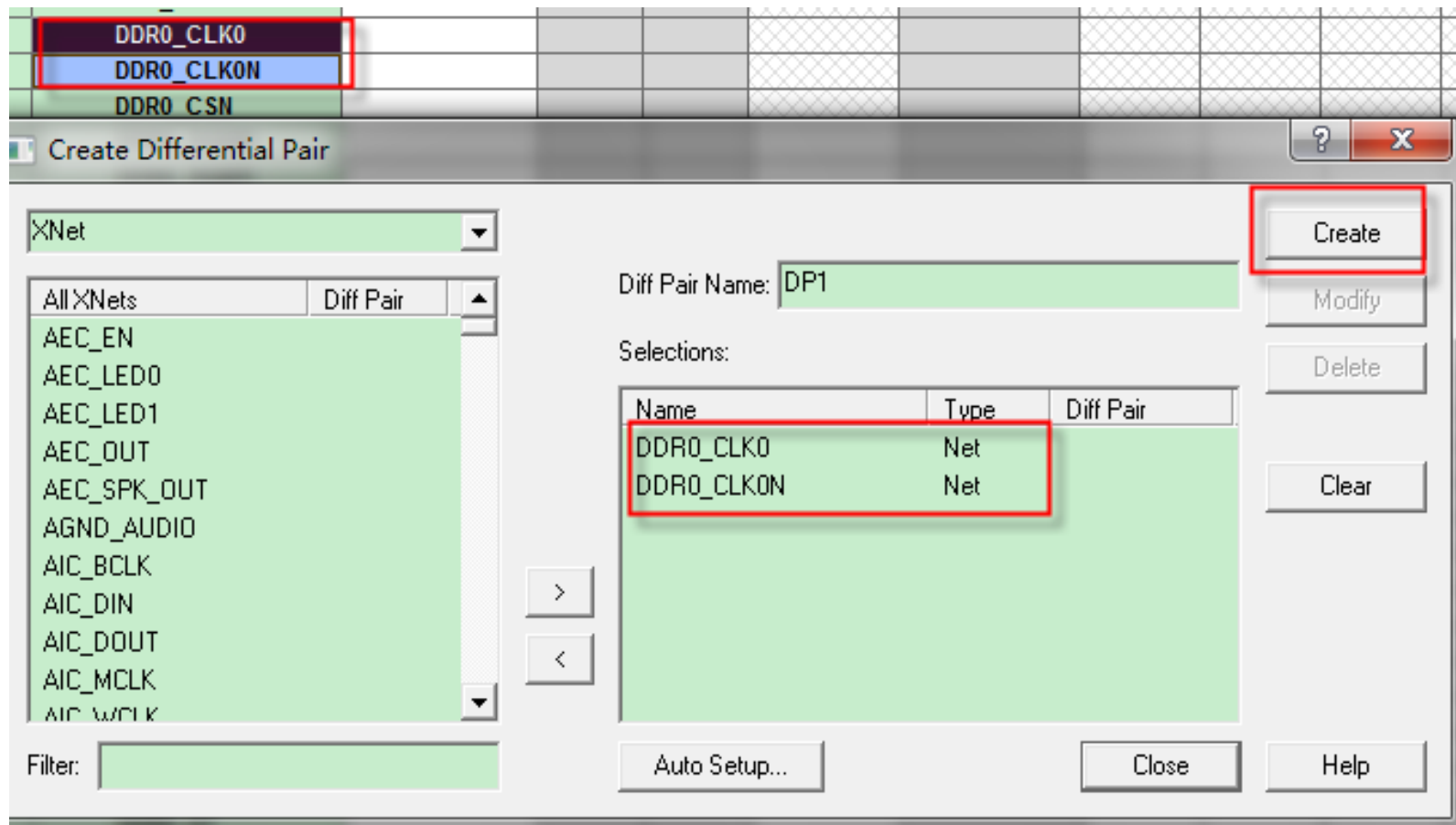
Bus...

Pin Pair...

Differential Pair...

电气约束 (Electrical Constraint)

- 创建Differential Pair



电气约束 (Electrical Constraint)

- 为Differential Pair添加约束

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo_] - [Physical: Nets: All Layers [de

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector

Physical

Physical Constraint Set

- All Layers
- By Layer
- Net
 - All Layers
- Region
 - All Layers

demo_

Type	Objects	Referenced Physical C Set	Line Width	
			Min mil	Max mil
Dsn	demo_	DEFAULT	5.500:5.500:4...	0.000
NCIs	CLS_B_VOUT0_7 (8)	DEFAULT	5.500:5.500:4...	0.000
NCIs	CLS_DDR0_AC (21)	DEFAULT	5.500:5.500:4...	0.000
NCIs	CLS_DIFF100 (33)		5.500:5.500:4...	0.000
DPr	DP1	BGA	5.500:5.500:4...	0.000
DPr	DP2	BGA0.8	5.500:5.500:4...	0.000
Net	DDR0_DQS0	DEFAULT	4.000	4.000
Net	DDR0_DQS0N	DIFF90	4.000	4.000
DPr	DP3	DIFF100	5.500:5.500:4...	0.000
Net	DDR0_DQS1	PWR	4.000	4.000

物理约束

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo_] - [Electrical: Net

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector

Electrical

Electrical Constraint Set

- Signal Integrity
- Timing
- Routing
- All Constraints
- Net
 - Signal Integrity
 - Timing
 - Routing
 - Wiring
 - Vias
 - Impedance
 - Min/Max Propagation Dela
 - Total Etch Length
 - Differential Pair
 - Relative Propagation Delay

demo_

Type	Objects	Referenced Electrical C Set	Pin Delay	
			Pin 1 mil	Pin 2 mil
Dsn	demo_			
Bus	BUS_DDR0_AC (20)	DDR0_A0		
DPr	DP1			
DPr	DP2	DDR0_A0		
DPr	DP3	ECS_DIFF100		
DPr	DP4			
DPr	DP5			
DPr	DP6			
DPr	DP7			
DPr	DP8			
DPr	DP9			
DPr	DP10			
DPr	DVI_IN0_CLK			
DPr	DVI_IN0_D0			
DPr	DVI_IN0_D1			
DPr	DVI_IN0_D2			

电气约束

电气约束 (Electrical Constraint)

- 为Differential Pair添加约束

Allegro Constraint Manager (connected to Allegro PCB Design GXL (legacy) 16.5) [demo_] - [Spacing: Nets: All Layers [demo_]]

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector

Electrical

Physical

Spacing

Spacing Constraint Set

Net

All Layers

Line

Pins

Vias

Shape

Bond Finger

Hole

BB Via Gap

Net Class-Class

Region

demo_

Type	Objects	Referenced Spacing CSet	Line To						
			Line mil	Thru Pin mil	SMD Pin mil	Test Pin mil	Thru Via mil	BB Via mil	Test Via mil
*	*	*	*	*	*	*	*	*	*
Dsn	demo_	DEFAULT	8.000:6....	4.000	8.000	8.000	5.000	6.000	6.000
NCIs	CLS_B_VOUT0_7 (8)	DEFAULT	8.000:6....	4.000	8.000	8.000	5.000	6.000	6.000
NCIs	CLS_DDR0_AC (21)	DEFAULT	8.000:6....	4.000	8.000	8.000	5.000	6.000	6.000
NCIs	CLS_DIFF100 (33)		8.000:6....	4.000	8.000	8.000	5.000	6.000	6.000
NCIs	CLS_GMII0_RX (11)	BGA	8.000:6....	4.000	8.000	8.000	5.000	6.000	6.000
NCIs	CLS_GMII0_TX (10)	BGA0.8	8.000:6....	4.000	8.000	8.000	5.000	6.000	6.000
NCIs	CLS_GMII1_RX (11)	DEFAULT	8.000:6....	4.000	8.000	8.000	5.000	6.000	6.000
NCIs	CLS_GMII1_TX (10)	SCS_DIFF100	8.000:6....	4.000	8.000	8.000	5.000	6.000	6.000
NCIs	CLS_GPMC_D_0_15 (16)	DEFAULT	8.000:6....	4.000	8.000	8.000	5.000	6.000	6.000
Bus	BUS_DDR0_AC (20)	DEFAULT	8.000:6....	4.000	8.000	8.000	5.000	6.000	6.000
Net	AEC_EN	DEFAULT	8.000:6....	4.000	8.000	8.000	5.000	6.000	6.000
Net	AEC_LED0	DEFAULT	8.000:6....	4.000	8.000	8.000	5.000	6.000	6.000
Net	AEC_LED1	DEFAULT	8.000:6....	4.000	8.000	8.000	5.000	6.000	6.000
Net	AEC_OUT	DEFAULT	8.000:6....	4.000	8.000	8.000	5.000	6.000	6.000
Net	AEC_SPK_OUT	DEFAULT	8.000:6....	4.000	8.000	8.000	5.000	6.000	6.000
Net	AGND_AUDIO	DEFAULT	8.000:6....	4.000	8.000	8.000	5.000	6.000	6.000

间距约束

电气约束 (Electrical Constraint)

- 为Differential Pair添加约束

The screenshot shows the Allegro Constraint Manager interface. The 'Physical' worksheet is selected in the 'Worksheet selector' pane. The 'Physical Constraint Set' is expanded, showing 'All Layers', 'By Layer', 'Net', and 'Region'. The 'Region' constraint is selected, and a dropdown menu shows 'BGA', 'BGA0.8', 'DEFAULT', 'DIFF90', 'DIFF100', 'PWR', and '(Clear)'. The 'DIFF100' option is highlighted.

The 'Analysis Modes' pane on the right shows 'Electrical Options' selected. The 'Electrical Options' pane is open, showing the following settings:

- DRC Unrouted**
 - ☐ Minimum Propagation Delay
 - ☐ Relative Propagation Delay
- Pin Delay**
 - ☐ Include in all Propagation Delays and in Differential Pair Phase checks
 - Propagation Velocity Factor: 1.524e+08 m/s
- Z Axis Delay**
 - ☐ Include in all Propagation Delays and in Differential Pair Phase checks
 - Propagation Velocity Factor: 1.524e+08 m/s
- Same Net Xtalk and Parallelism Checks**
 - ☐ Perform Xtalk and Parallelism checks within the same net
- Differential Pair Constraints**
 - ☒ Diff Pair width and gap properties (overrides) supersede Region constraints. (Maintains pre-16.2 constraint resolution).

The 'On-line DRC' checkbox is checked.

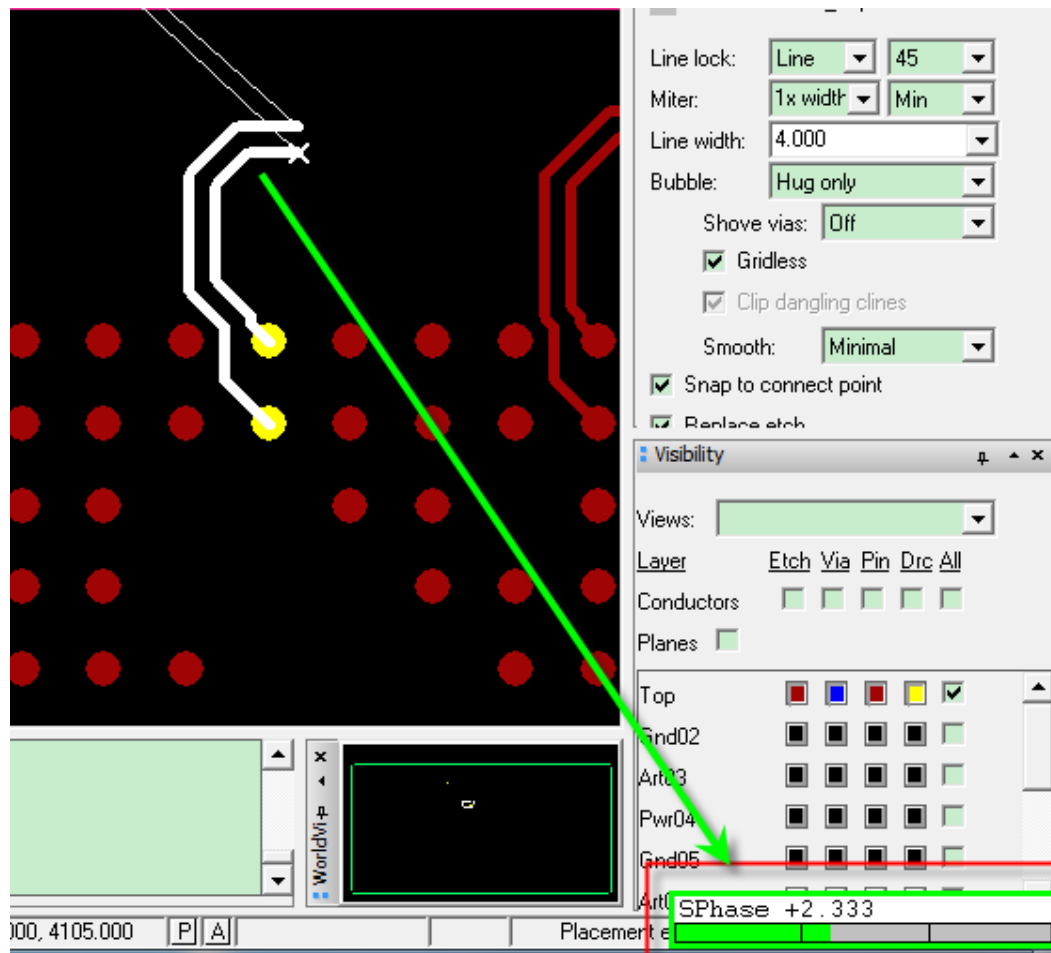
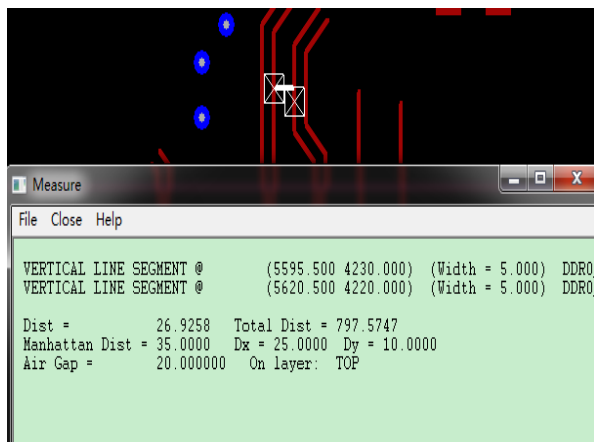
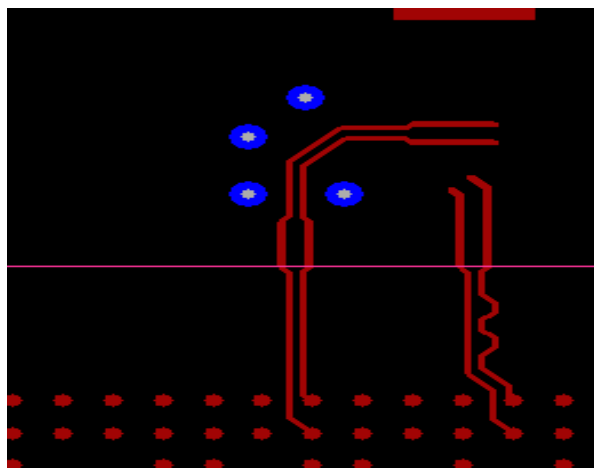
The 'demo_' table shows the following data:

Type	Objects	Referenced Physical CSet	
Dsn	demo_	DEFAULT	5.9
Rgn	BGA	BGA	4.0
RCIs	CLS_DDR0_AC	BGA	4.0
RCIs	CLS_DIFF100	BGA	4.0
Rgn	BGA0.8	BGA0.8	4.0
Rgn	RGN_DIFF100		4.0

A red box highlights the 'DIFF100' option in the dropdown menu, and a red box highlights the 'Differential Pair Constraints' section in the 'Electrical Options' pane. A red box also highlights the 'Physical' worksheet in the 'Worksheet selector' pane.

电气约束 (Electrical Constraint)

• Differential Pair约束示例



Q&A

- Q&A
- Summary

Thank you!

SEP 19, 2012

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