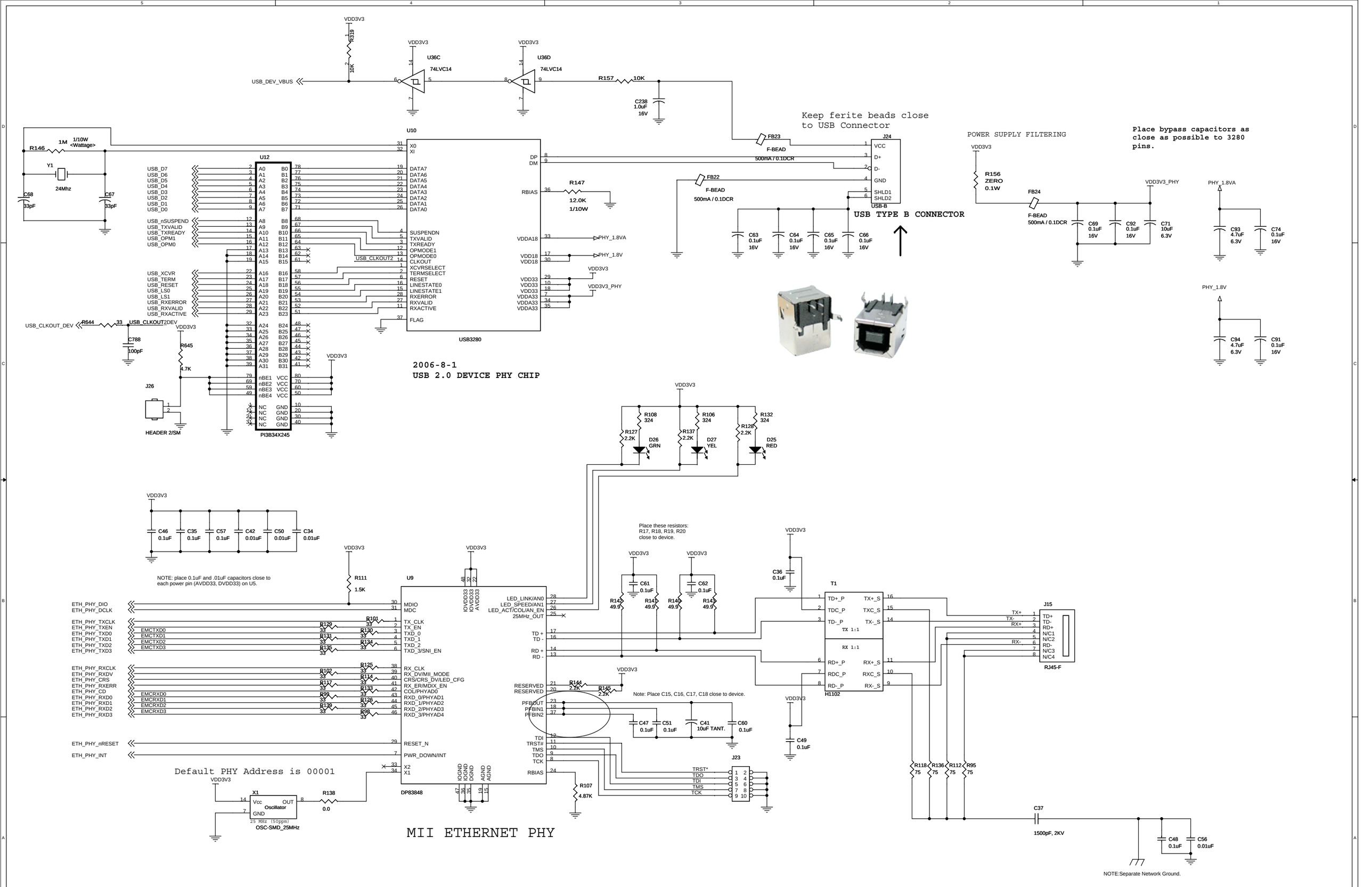

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Size A2	Document Number <Doc>	Rev 1.0
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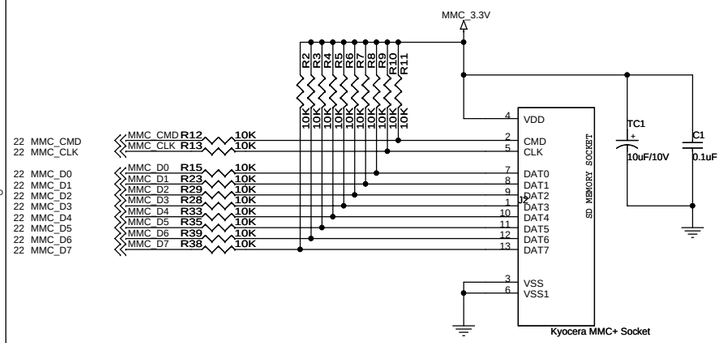
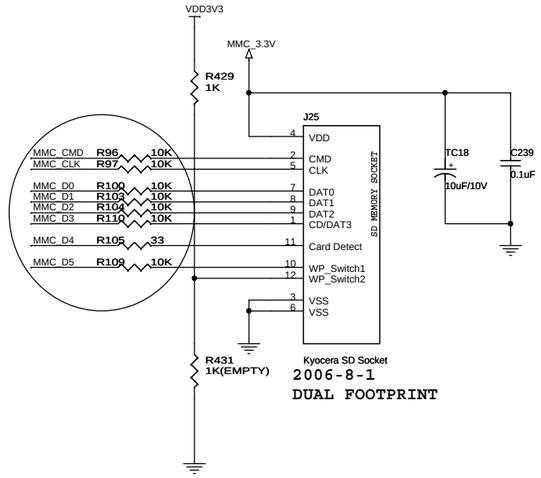
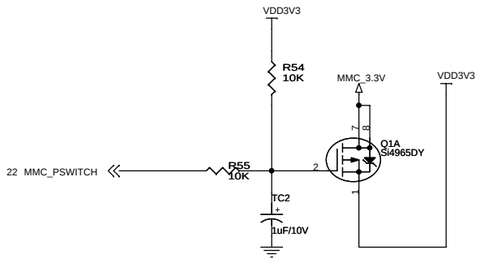
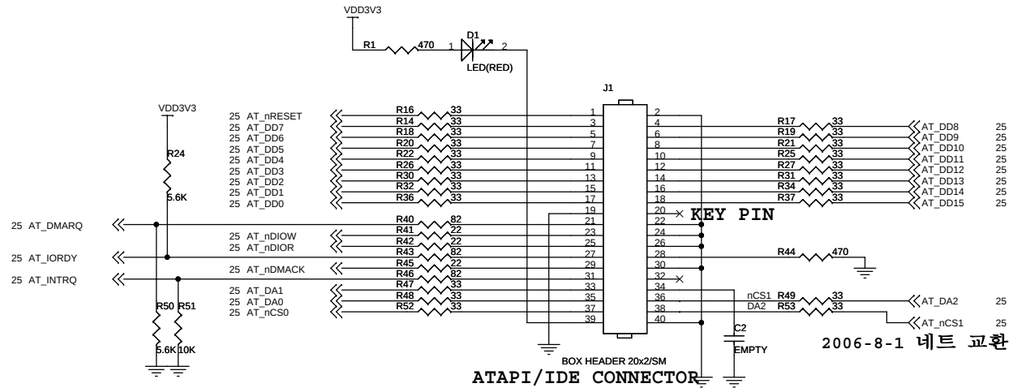
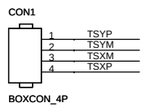




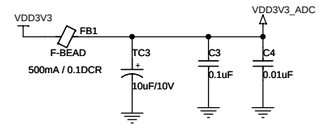


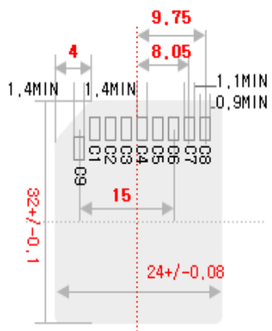
SD/HS-MMC SOCKET



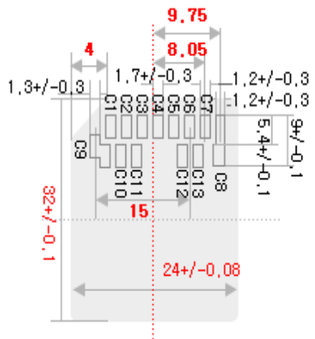


TOUCHSCREEN CONN.
MITSHMI
M60-04-30-134P

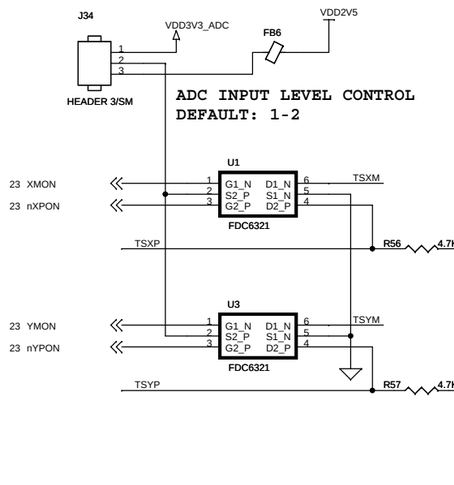


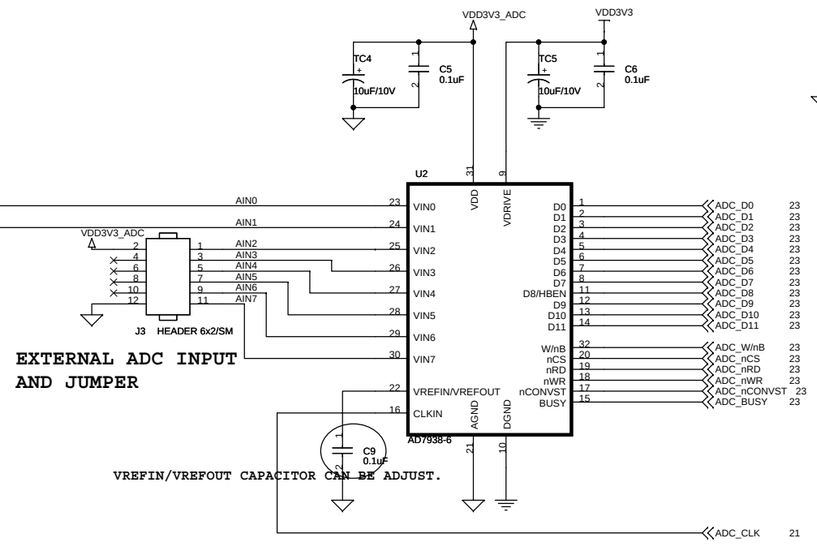


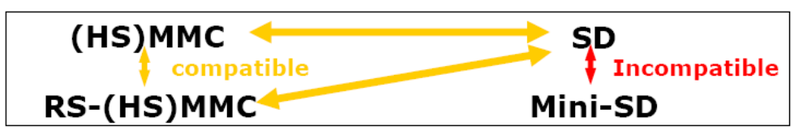
SD Card

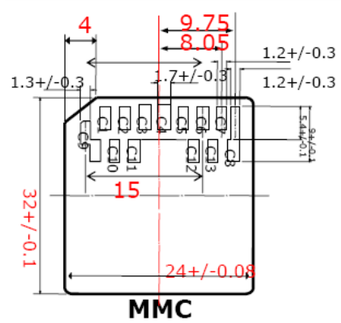


HS-MMC









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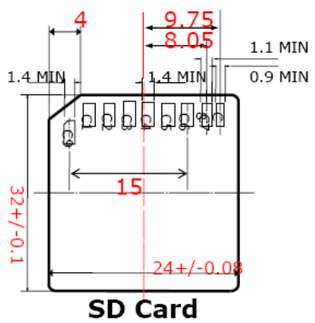

SD Card

SANGHWA FPGA PLATFORM

Title: SD/MMC/IDE/TOUCH SCREEN

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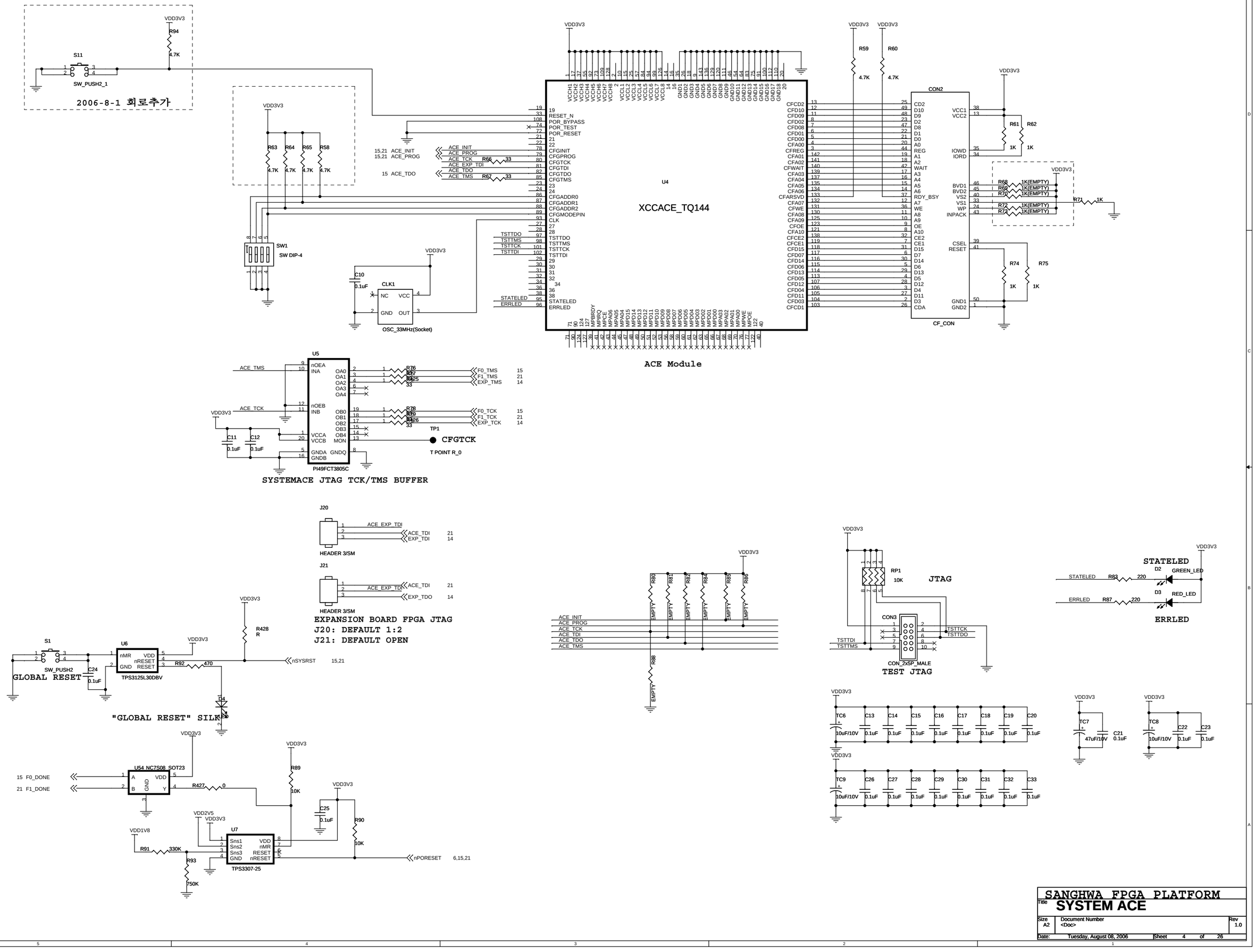

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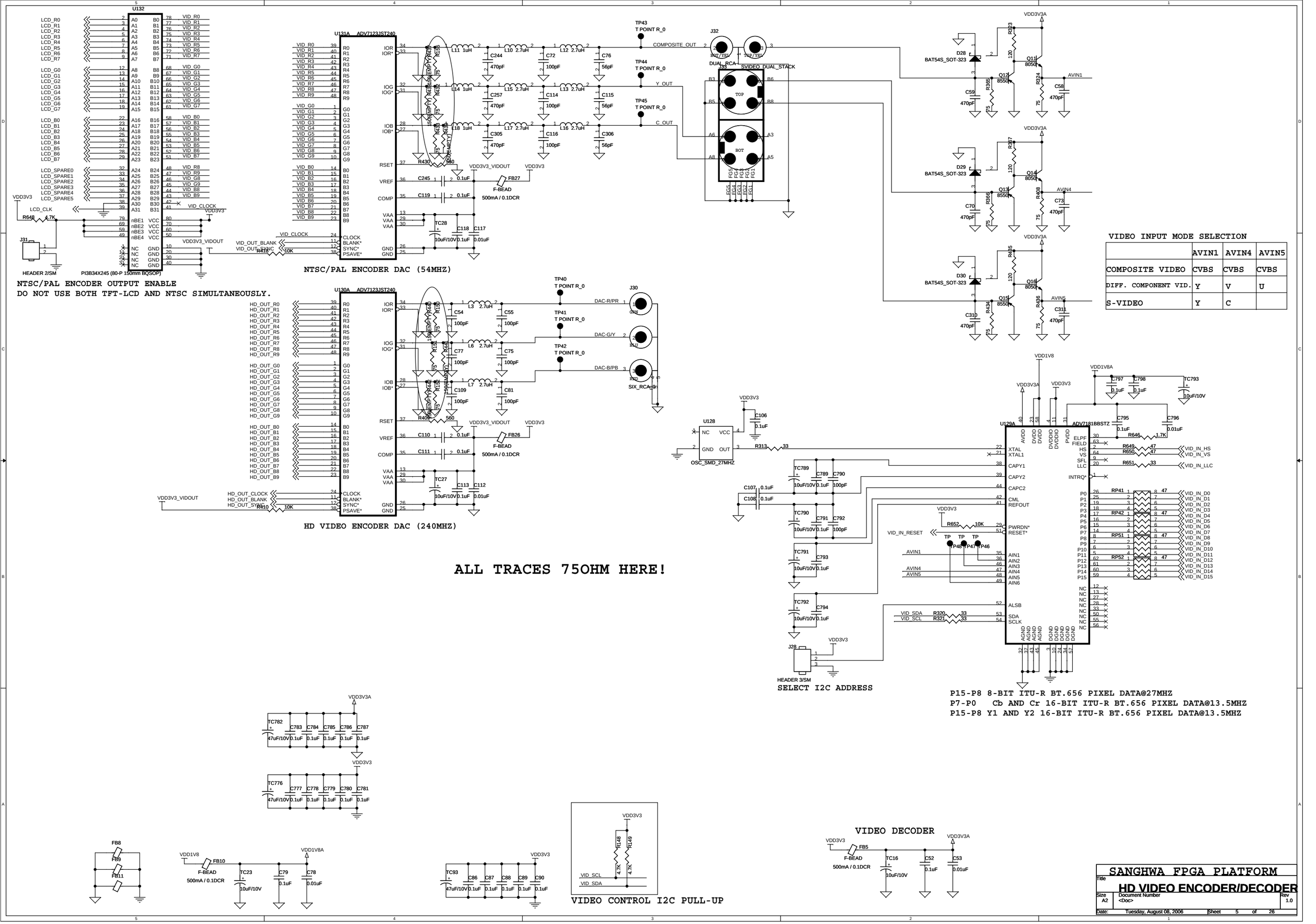
Size A2	Document Number <Doc>		Rev 1.0
Date: Tuesday, August 08, 2006	Sheet 4 of 26		


U132
PI3B34X245 (80-P 150mm BQSOP)
J31
HEADER 2/SM
NTSC/PAL ENCODER OUTPUT ENABLE
DO NOT USE BOTH TFT-LCD AND NTSC SIMULTANEOUSLY.
U131A ADV7123JST240
NTSC/PAL ENCODER DAC (54MHZ)
U130A ADV7123JST240
HD VIDEO ENCODER DAC (240MHZ)
ALL TRACES 75OHM HERE!
TP43 T POINT R_0
TP44 T POINT R_0
TP45 T POINT R_0
COMPOSITE_OUT
Y_OUT
C_OUT
J32
J33
SVIDEO_DUAL_STACK
DUAL_RCA
TP40 T POINT R_0
TP41 T POINT R_0
TP42 T POINT R_0
DAC-R/PR
DAC-G/Y
DAC-B/PB
J30
SIX_RCA
VIDEO INPUT MODE SELECTION
AVIN1
AVIN4
AVIN5
U128
OSC_SMD_27MHZ
U129A ADV7181BBSTZ
VIDEO DECODER
J28
HEADER 3/SM
SELECT I2C ADDRESS
P15-P8 8-BIT ITU-R BT.656 PIXEL DATA@27MHZ
P7-P0 Cb AND Cr 16-BIT ITU-R BT.656 PIXEL DATA@13.5MHZ
P15-P8 Y1 AND Y2 16-BIT ITU-R BT.656 PIXEL DATA@13.5MHZ
VIDEO CONTROL I2C PULL-UP
SANGHWA FPGA PLATFORM
HD VIDEO ENCODER/DECODER
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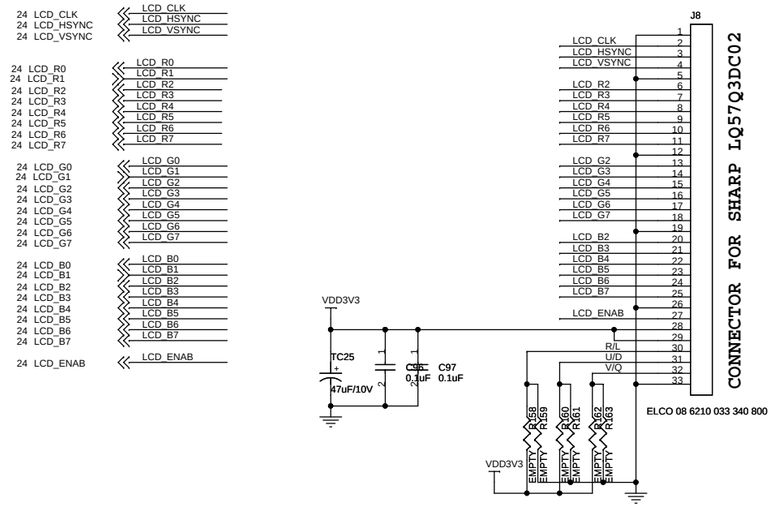
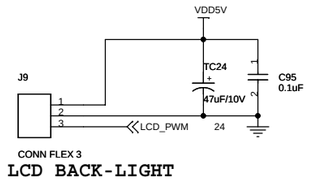
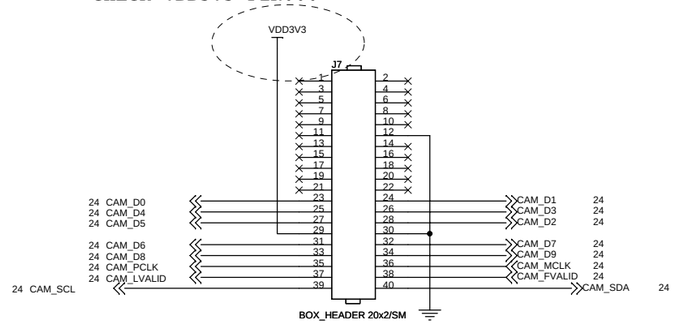




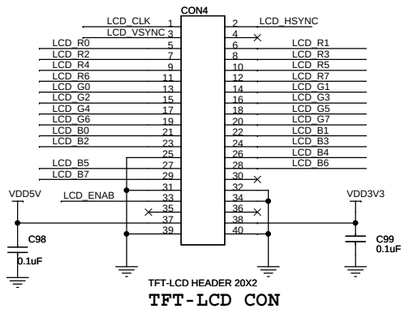
LCD BACK-LIGHT

CHECK VDD3V3 PIN!!!

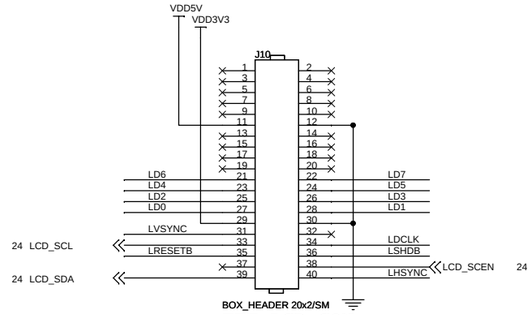


CMOS IMAGE SENSOR SOCKET

TERASIC, INC. (TRDB_DC2 BOARD)



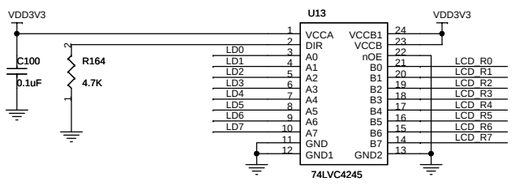
TFT-LCD CON

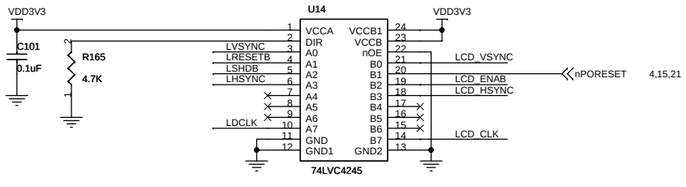


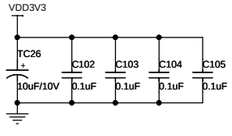
TFT-LCD CON

TERASIC, INC. (TRDB_LCM BOARD)

7-SEGMENT INTERFACE







SANGHWA FPGA PLATFORM

Title: CIS/TFT-LCD

Size: A2 | Document Number: <Doc> | Rev: 1.0

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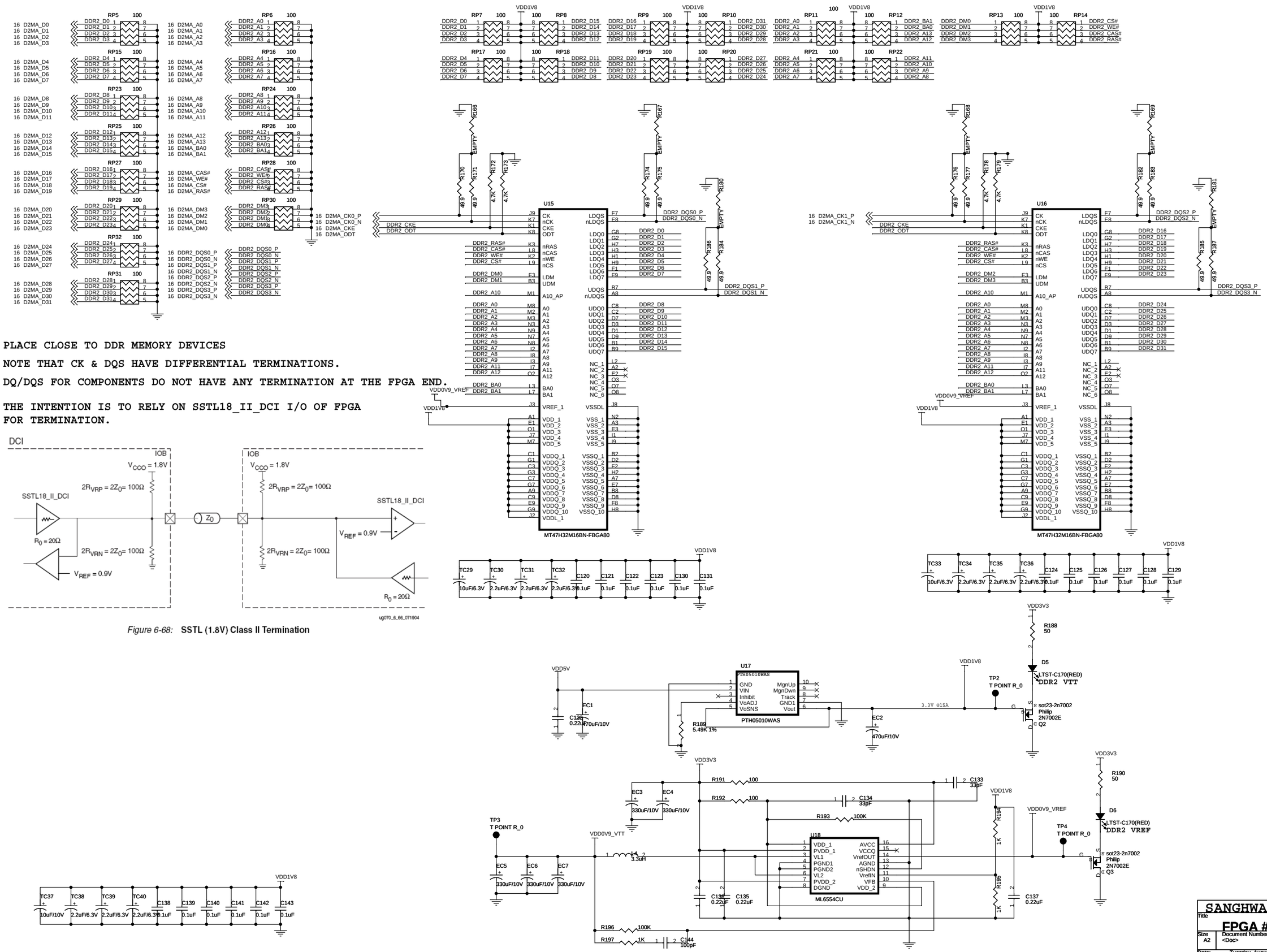

PLACE CLOSE TO DDR MEMORY DEVICES

NOTE THAT CK & DQS HAVE DIFFERENTIAL TERMINATIONS.

DQ/DQS FOR COMPONENTS DO NOT HAVE ANY TERMINATION AT THE FPGA END.

THE INTENTION IS TO RELY ON SSTL18_II_DCI I/O OF FPGA FOR TERMINATION.

Figure 6-68: **SSTL (1.8V) Class II Termination**

SANGHWA FPGA PLATFORM

Title: FPGA #0 DDR2 SDRAM

Size: A2 | Document Number: <Doc> | Rev: 1.0

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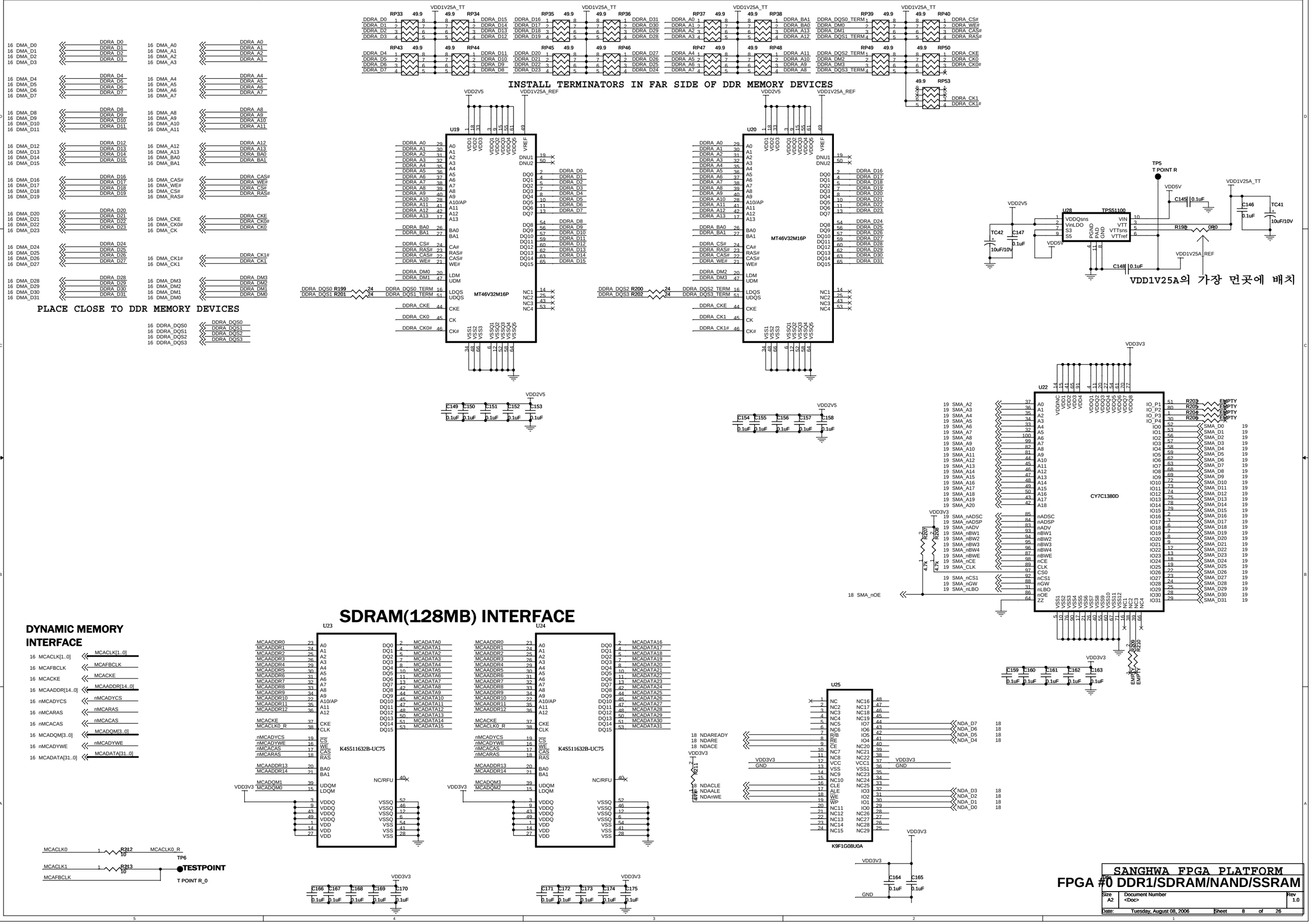
INSTALL TERMINATORS IN FAR SIDE OF DDR MEMORY DEVICES
PLACE CLOSE TO DDR MEMORY DEVICES
VDD1V25A의 가장 먼곳에 배치
SDRAM(128MB) INTERFACE
DYNAMIC MEMORY INTERFACE
U19 MT46V32M16P
U20 MT46V32M16P
U22 CY7C1380D
U23 K4S511632B-UC75
U24 K4S511632B-UC75
U25 K9F1G08U0A
U28 TPS51100
TESTPOINT
SANGHWA FPGA PLATFORM
FPGA #0 DDR1/SDRAM/NAND/SSRAM
Document Number
<Doc>
Rev
1.0
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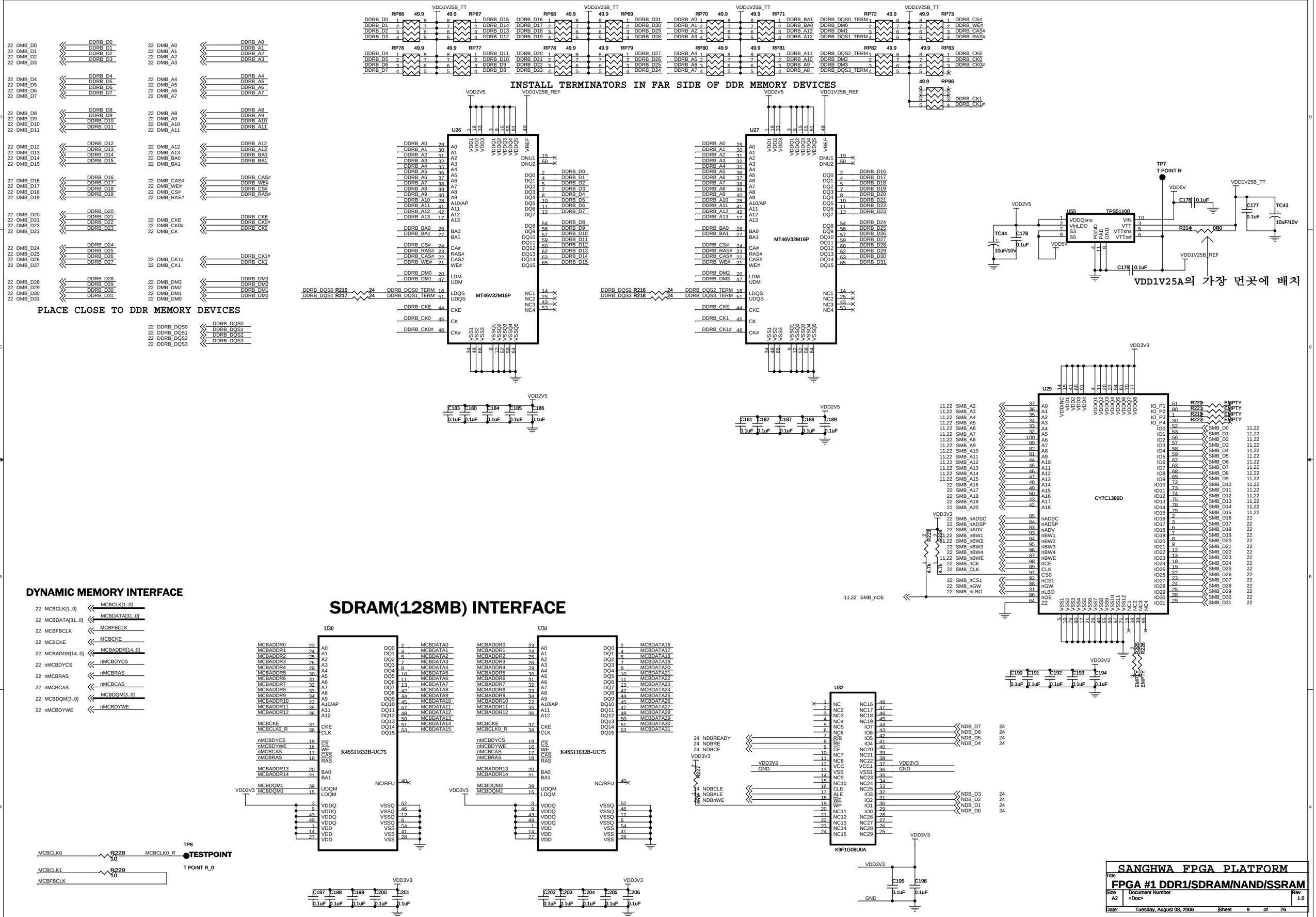
Sheet 8 of 26


INSTALL TERMINATORS IN FAR SIDE OF DDR MEMORY DEVICES
PLACE CLOSE TO DDR MEMORY DEVICES
VDD1V25A의 가장 먼곳에 배치
DYNAMIC MEMORY INTERFACE
SDRAM(128MB) INTERFACE
U26
MT46V32M16P
U27
MT46V32M16P
U29
CY7C1380D
U30
K4S511632B-UC75
U31
K4S511632B-UC75
U32
K9F1G08U0A
U55
TPS51100
TP7
T POINT R
TP8
TESTPOINT
T POINT R_0
SANGHWA FPGA PLATFORM
FPGA #1 DDR1/SDRAM/NAND/SSRAM
Size A2
Document Number <Doc>
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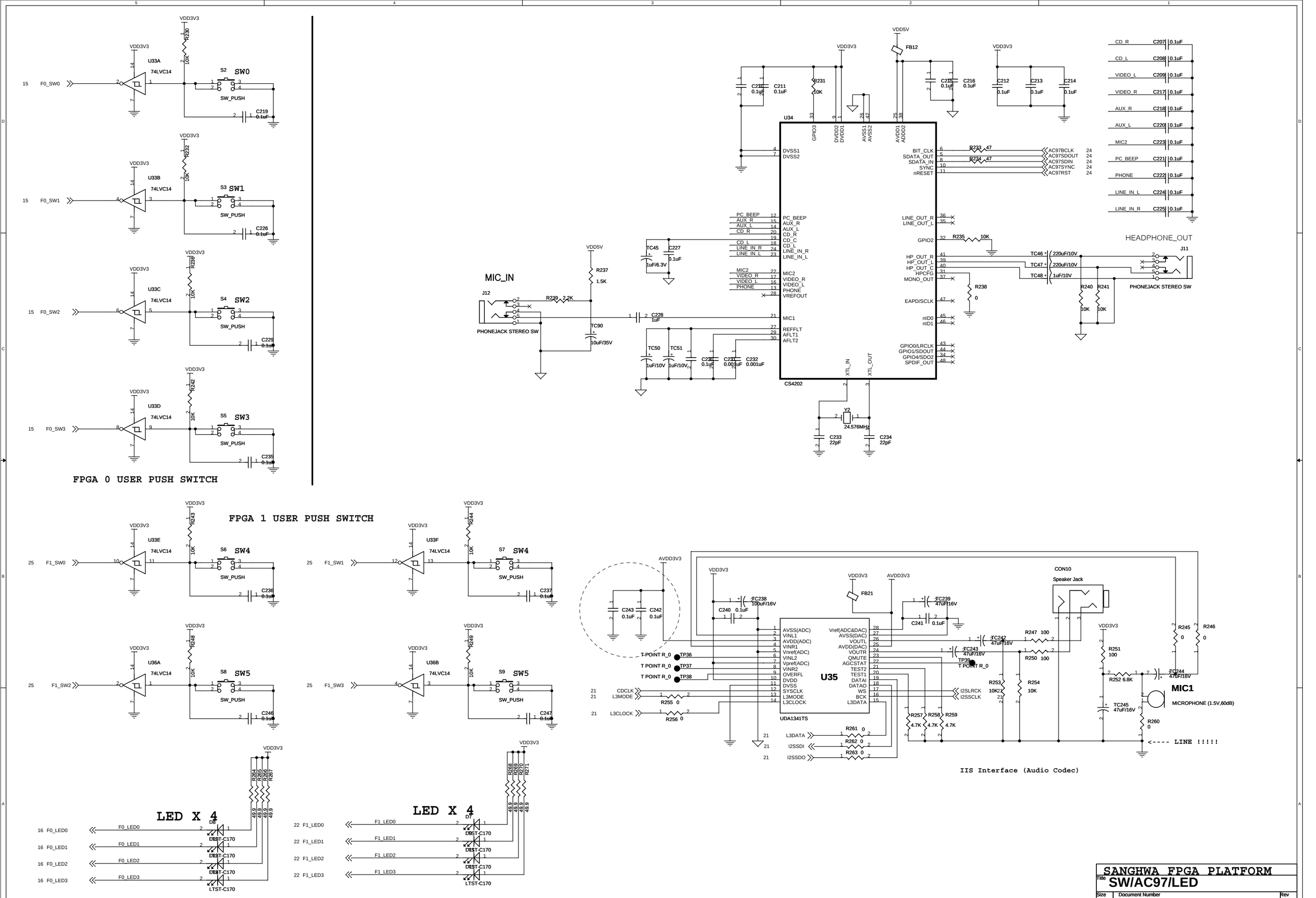
FPGA 0 USER PUSH SWITCH
FPGA 1 USER PUSH SWITCH
U33A 74LVC14 F0_SW0 S2 SW0 R230 10K C219 0.1uF
U33B 74LVC14 F0_SW1 S3 SW1 R232 10K C226 0.1uF
U33C 74LVC14 F0_SW2 S4 SW2 R236 10K C229 0.1uF
U33D 74LVC14 F0_SW3 S5 SW3 R242 10K C235 0.1uF
U33E 74LVC14 F1_SW0 S6 SW4 R243 10K C236 0.1uF
U33F 74LVC14 F1_SW1 S7 SW4 R244 10K C237 0.1uF
U36A 74LVC14 F1_SW2 S8 SW5 R248 10K C246 0.1uF
U36B 74LVC14 F1_SW3 S9 SW5 R249 10K C247 0.1uF
SW_PUSH
LED X 4
D8 D7 DIST-C170 LTST-C170
F0_LED0 F0_LED1 F0_LED2 F0_LED3
F1_LED0 F1_LED1 F1_LED2 F1_LED3
R264 R265 R266 R267 R268 R269 R270 R271 49.9
MIC_IN
J12 PHONEJACK STEREO SW
R239 2.2K R237 1.5K TC90 10uF/35V
TC45 1uF/6.3V C227 0.1uF
C228 1uF
TC50 1uF/10V TC51 1uF/10V C230 0.1uF C231 0.001uF C232 0.001uF
U34 CS4202
DVSS1 DVSS2 GPIO3 DVDD2 DVDD1 AVSS1 AVSS2 AVDD1 ADDD2
PC_BEPE AUX_R AUX_L CD_R CD_C CD_L LINE_IN_R LINE_IN_L
MIC2 VIDEO_R VIDEO_L PHONE VREFOUT MIC1 REFFLT AFLT1 AFLT2
BIT_CLK SDATA_OUT SDATA_IN SYNC nRESET
AC97BCLK AC97SDOUT AC97SDIN AC97SYNC AC97RST
LINE_OUT_R LINE_OUT_L GPIO2 HP_OUT_R HP_OUT_L HP_OUT_C HPCFG MONO_OUT EAPD/SCLK nID0 nID1 GPIO0/LRCLK GPIO1/SDOUT GPIO4/SDO2 SPDIF_OUT
XTL_IN XTL_OUT Y2 24.576MHz C233 22pF C234 22pF
FB12 C211 0.1uF C215 0.1uF C216 0.1uF C212 0.1uF C213 0.1uF C214 0.1uF
R231 10K R233 47 R234 47 R235 10K R238 0 R240 10K R241 10K
TC46 220uF/10V TC47 220uF/10V TC48 1uF/10V
HEADPHONE_OUT J11 PHONEJACK STEREO SW
CD_R CD_L VIDEO_L VIDEO_R AUX_R AUX_L MIC2 PC_BEPE PHONE LINE_IN_L LINE_IN_R
C207 C208 C209 C217 C218 C220 C223 C221 C222 C224 C225 0.1uF
U35 UDA1341TS
AVSS(ADC) VINL1 AVDD(ADC) VINR1 Vref(ADC) VINL2 Vref(ADC) VINR2 OVERFL DVDD DVSS SYSCLK L3MODE L3CLOCK
Vref(ADC&DAC) AVSS(DAC) VOUTL AVDD(DAC) VOUTR QMUTE AGCSTAT TEST2 TEST1 DATAI DATAO WS BCK L3DATA
T POINT R_0 TP36 TP37 TP38 TP39
CDCLK L3MODE L3CLOCK L3DATA I2SSDI I2SSDO I2SLRCK I2SSCLK
R255 0 R256 0 R261 0 R262 0 R263 0
TC238 100uF/16V C240 0.1uF C241 0.1uF C243 0.1uF C242 0.1uF
FB21 TC239 47uF/16V TC242 47uF/16V TC243 47uF/16V
CON10 Speaker Jack
R247 100 R250 100 R253 10K R254 10K R257 4.7K R258 4.7K R259 4.7K
R245 0 R246 0 R251 100 R252 6.8K TC244 47uF/16V TC245 47uF/16V R260 0
MIC1 MICROPHONE (1.5V,60dB)
<---- LINE !!!!!
IIS Interface (Audio Codec)
SANGHWA FPGA PLATFORM
Title SW/AC97/LED
Size A2 Document Number <Doc> Rev 1.0
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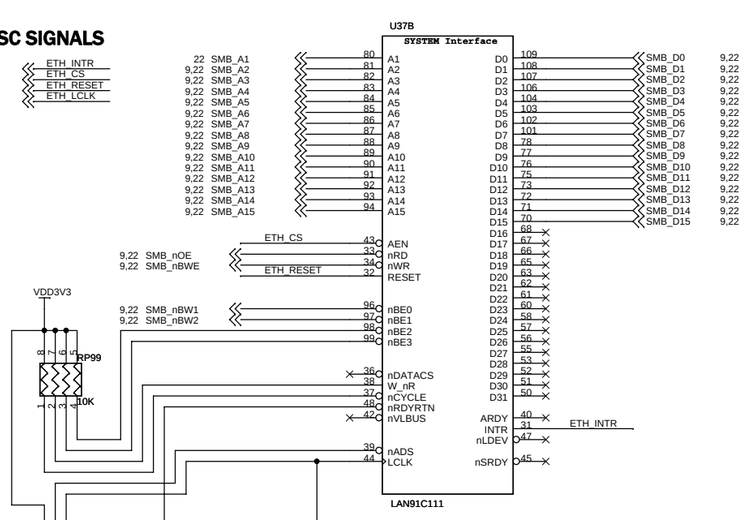
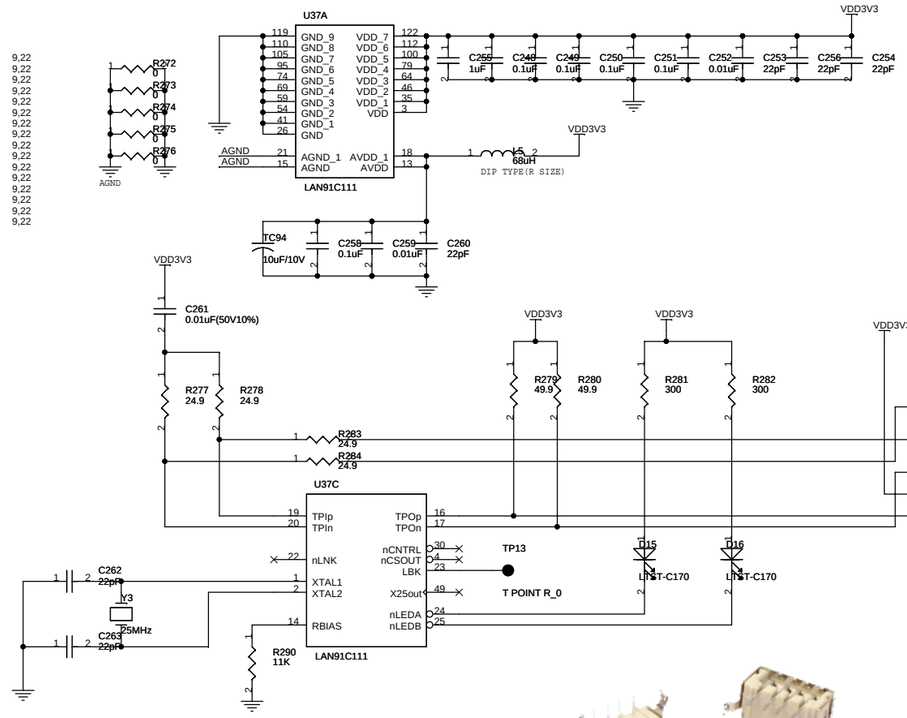
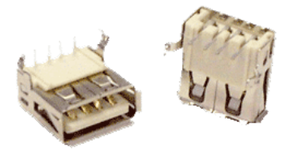
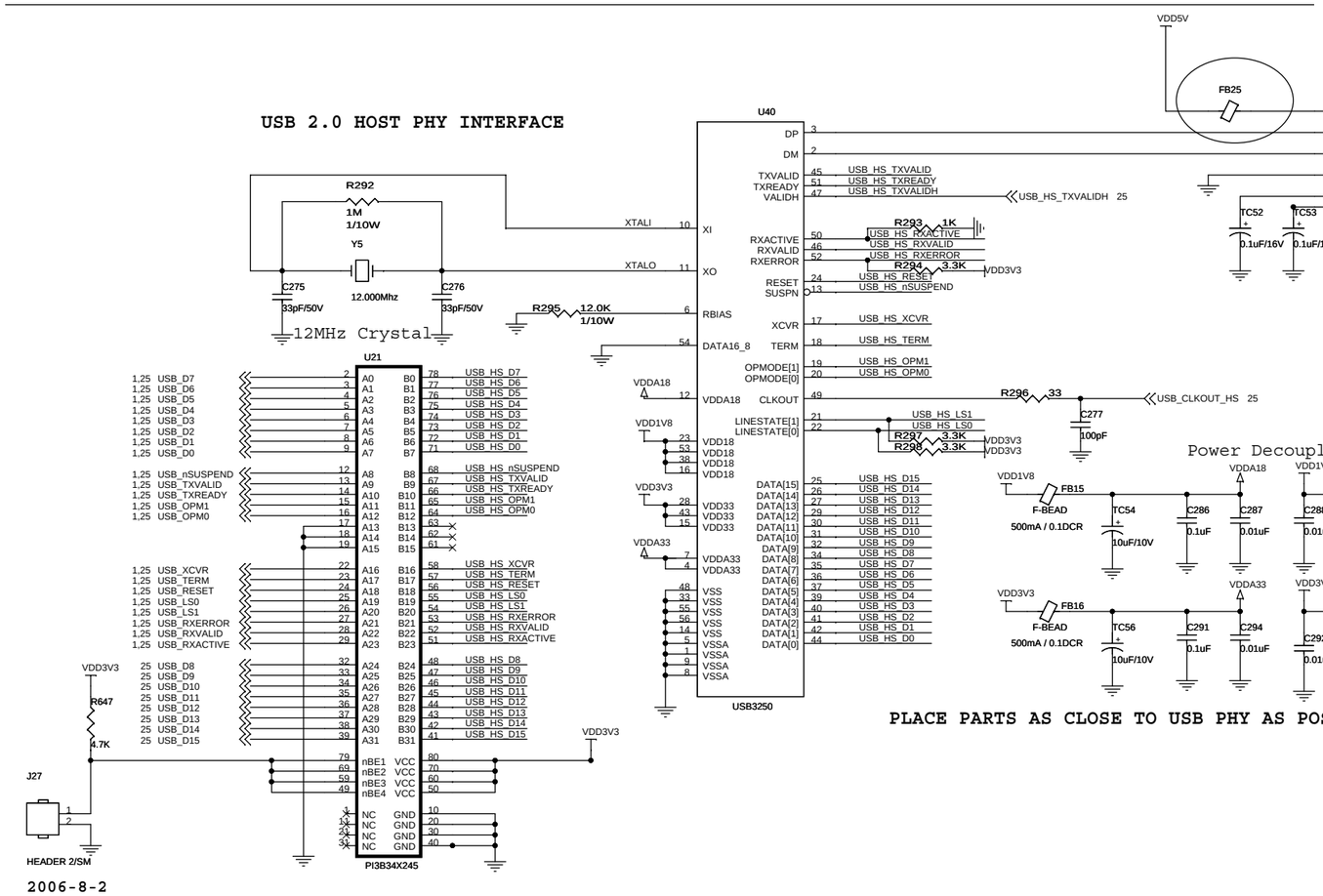
ETH MISC SIGNALS



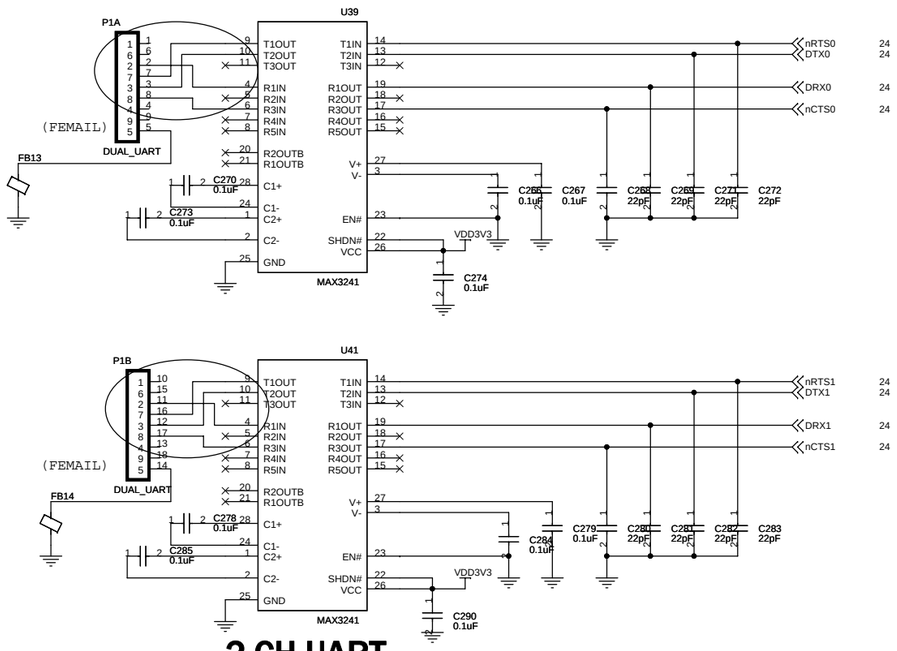




USB 2.0 HOST PHY INTERFACE



PLACE PARTS AS CLOSE TO USB PHY AS POSSIBLE



2-CH UART

2006-8-2

USB HOST UTMI ENABLE

Title	SANGHWA FPGA PLATFORM ETH/USB/UART
Size A2	Document Number <Doc>
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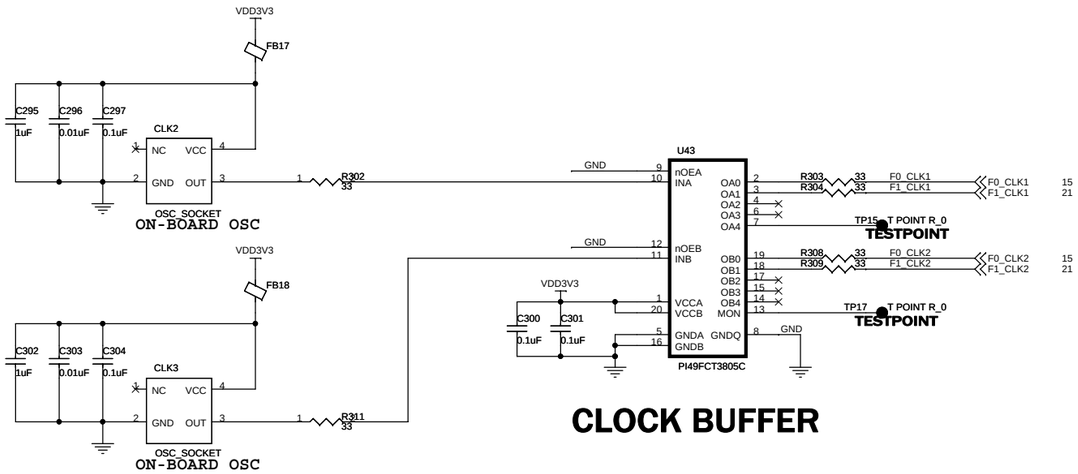

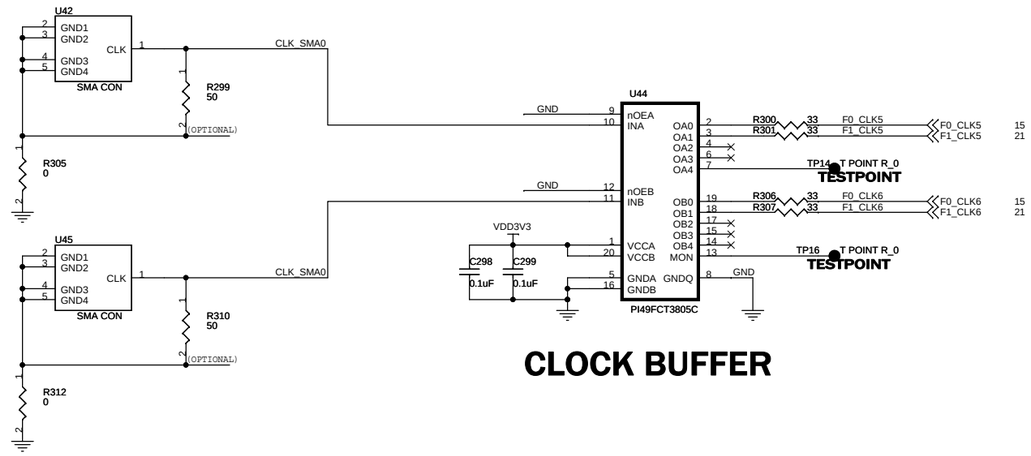

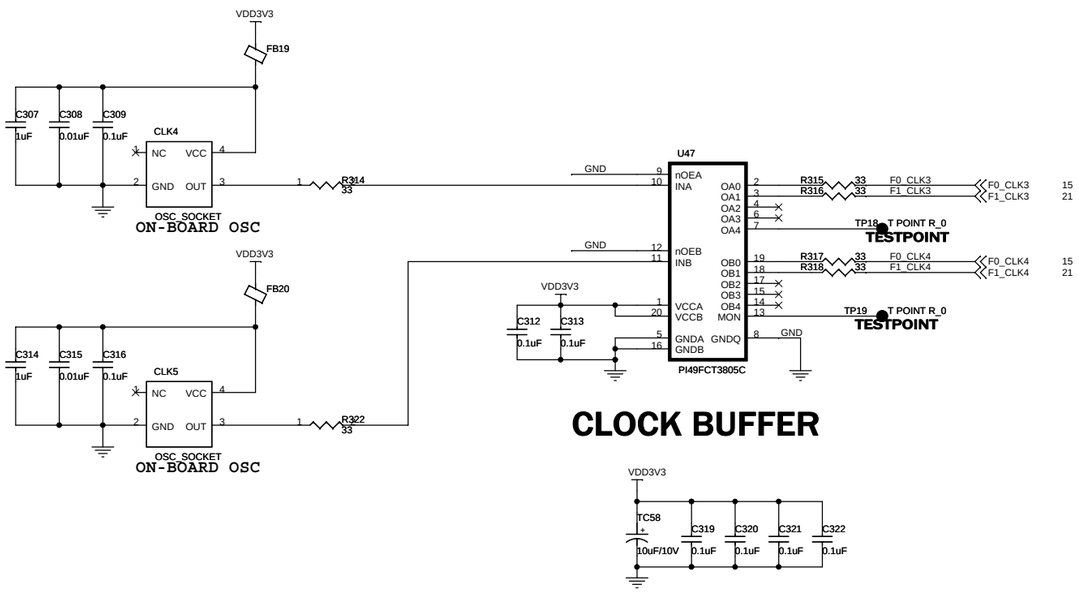

SANGHWA FPGA PLATFORM

Title **CLOCK/PLL/MULTIPLEXOR**

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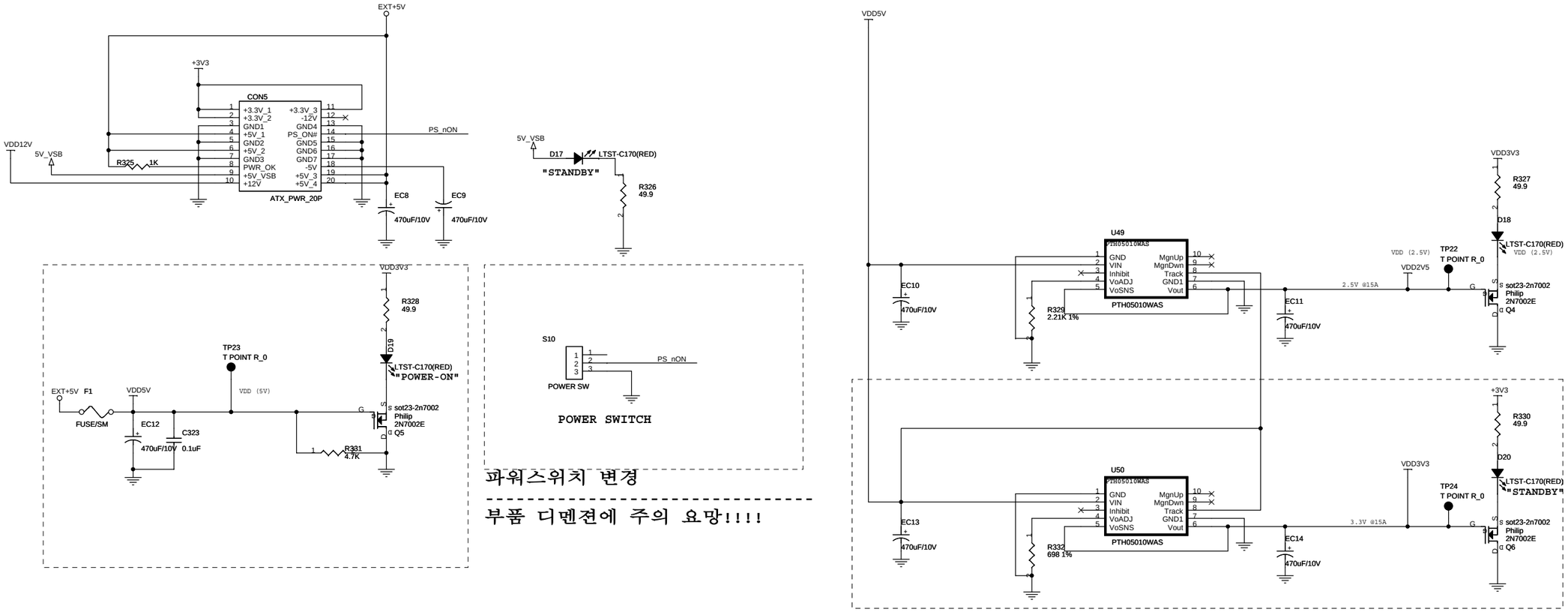
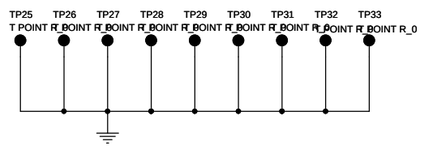
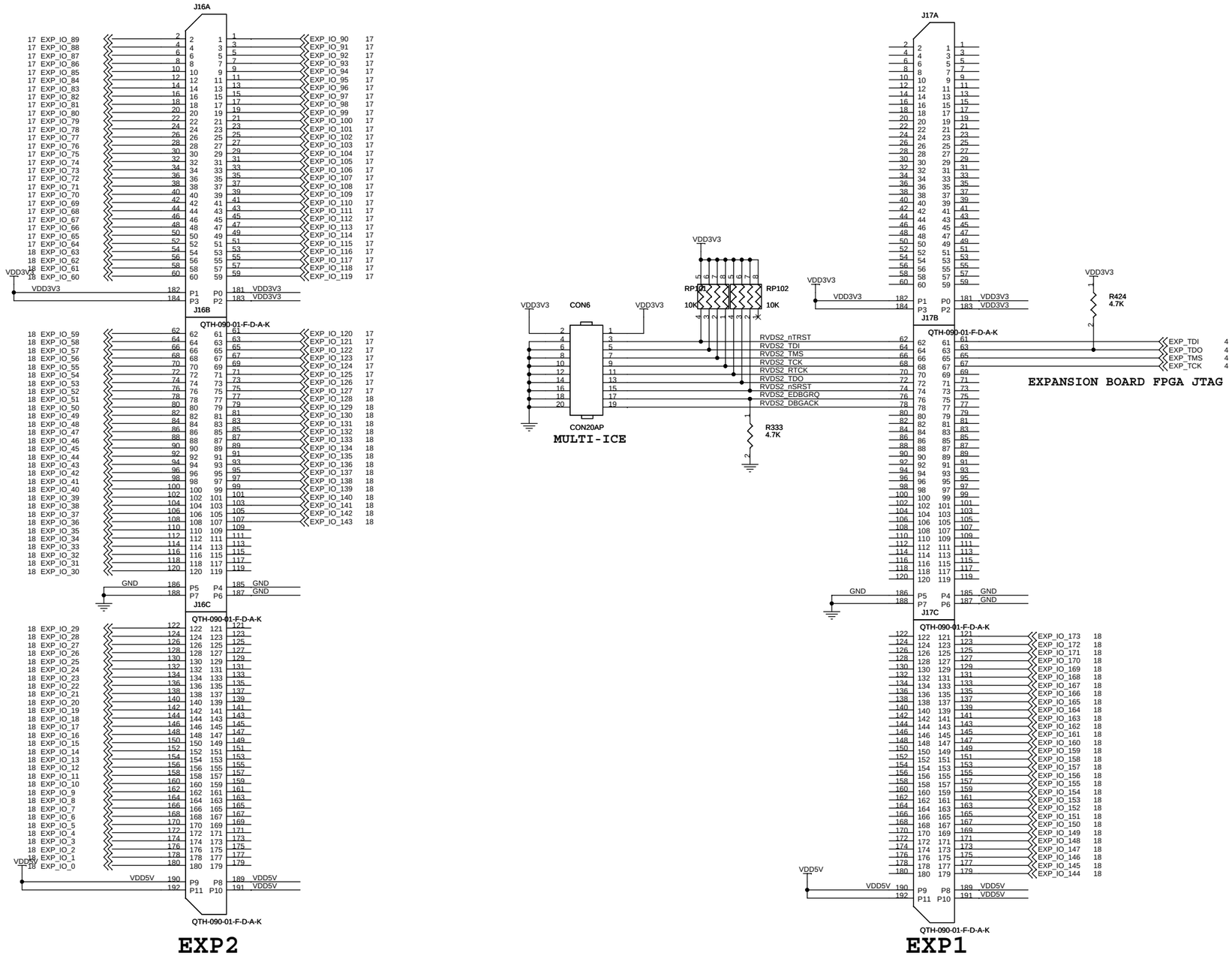


GND Point



SANGHWA FPGA PLATFORM		
Title: SYSTEM POWER		
Size: A2	Document Number: <Doc>	Rev: 1.0
Date: Tuesday, August 08, 2006	Sheet 13 of 26	

EXPANSION SLOT FOR FPGA #0



SANGHWA FPGA PLATFORM	
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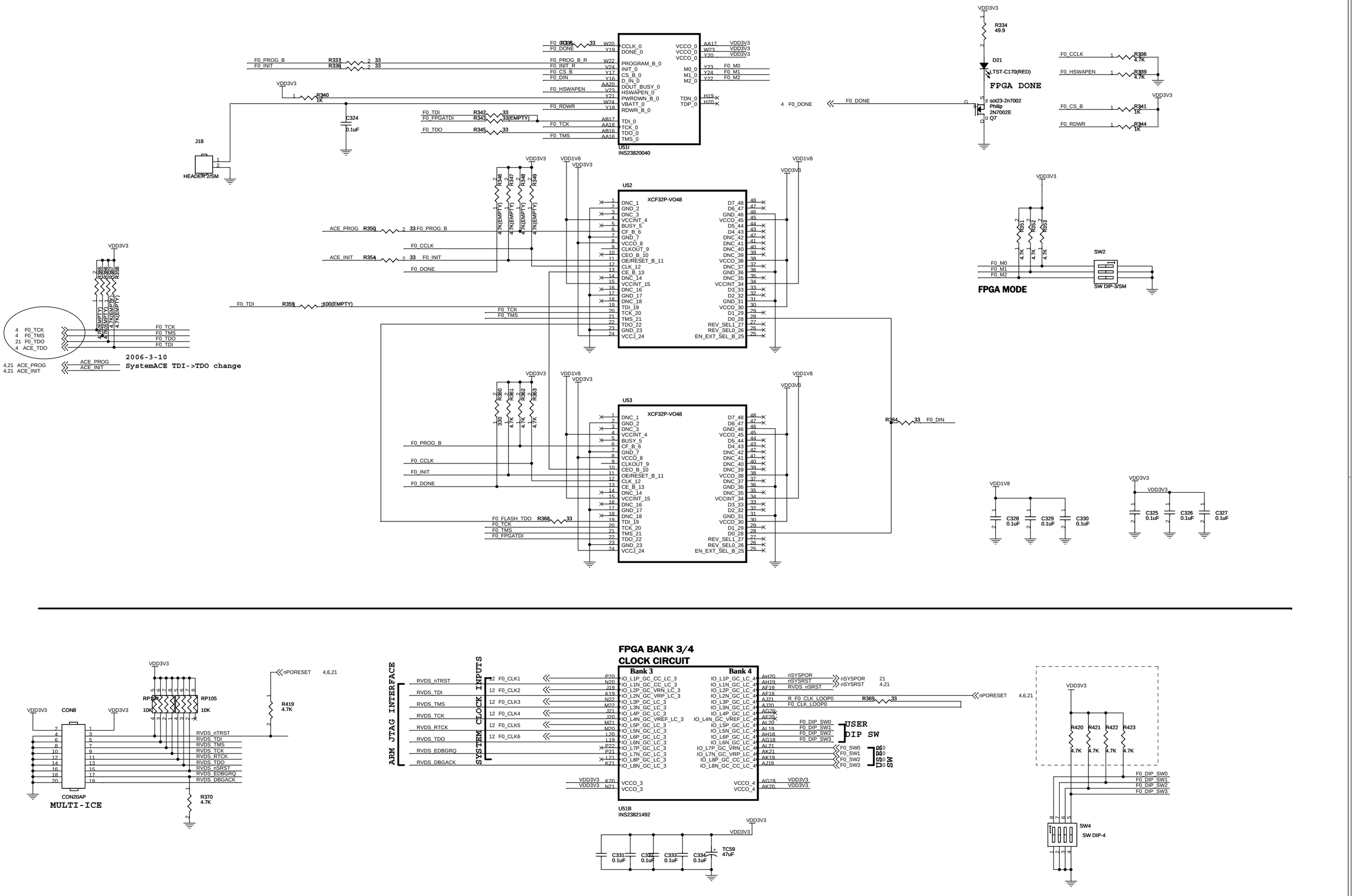
Size A2	Document Number <Doc>
Rev	1.0
Date: Tuesday, August 08, 2006	Sheet 14 of 26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U52
XCF32P-VO48
U53
XCF32P-VO48
J18
HEADER 2/SM
FPGA DONE
D21
LTST-C170(RED)
Q7
2N7002E
FPGA MODE
SW2
SW DIP-3/SM
2006-3-10
SystemACE TDI->TDO change
FPGA BANK 3/4
CLOCK CIRCUIT
Bank 3
Bank 4
U51B
INS23821492
ARM JTAG INTERFACE
SYSTEM CLOCK INPUTS
USER
DIP SW
USER
SW
MULTI-ICE
CON8
CON20AP
SW4
SW DIP-4
SANGHWA FPGA PLATFORM
FPGA0 CONFIG/CLOCK
Size A2
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<Doc>
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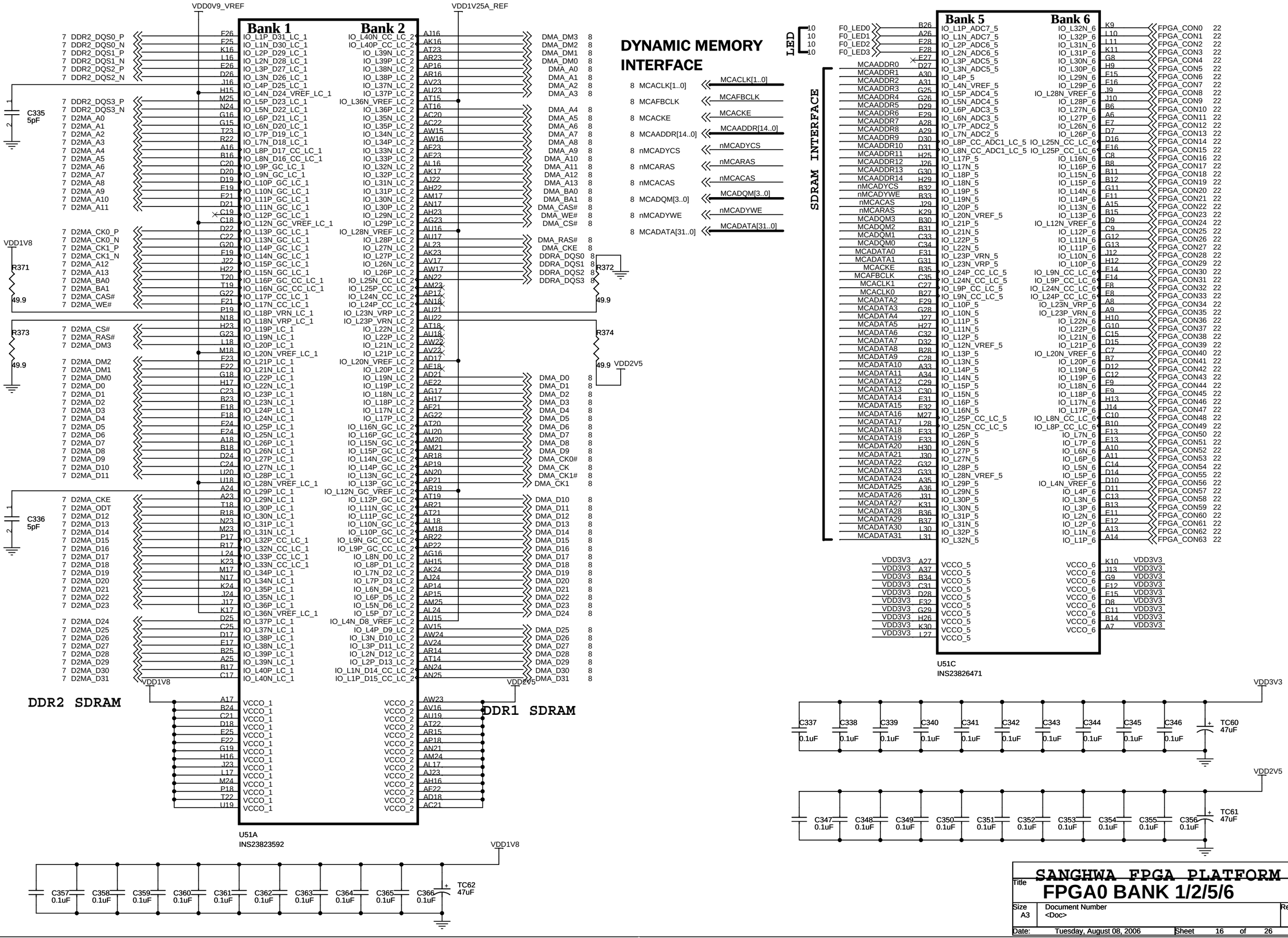
DYNAMIC MEMORY INTERFACE
Bank 1
Bank 2
Bank 5
Bank 6
DDR2 SDRAM
DDR1 SDRAM
SDRAM INTERFACE
LED
VDD0V9_VREF
VDD1V25A_REF
VDD1V8
VDD2V5
VDD3V3
C335 5pF
C336 5pF
R371 49.9
R372 49.9
R373 49.9
R374 49.9
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MCAFBCLK
MCACKE
MCAADDR[14..0]
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nMCARAS
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INS23823592
U51C
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TC62 47uF
TC60 47uF
TC61 47uF
SANGHWA FPGA PLATFORM
FPGA0 BANK 1/2/5/6
Title
Size A3
Document Number <Doc>
Rev 1.0
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FPGA INTERCONNECTION

Bank 7 / Bank 8

23	FPGA_CON384	AT33	IO_L1P_7	IO_L32N_8	AW10	FPGA_CON320	23
23	FPGA_CON385	AR33	IO_L1N_7	IO_L32P_8	AW11	FPGA_CON321	23
23	FPGA_CON386	AJ30	IO_L2P_7	IO_L31N_8	AV14	FPGA_CON322	23
23	FPGA_CON387	AK31	IO_L2N_7	IO_L31P_8	AW14	FPGA_CON323	23
23	FPGA_CON388	AM30	IO_L3P_7	IO_L30N_8	AU10	FPGA_CON324	23
23	FPGA_CON389	AL30	IO_L3N_7	IO_L30P_8	AV10	FPGA_CON325	23
23	FPGA_CON390	AM31	IO_L4P_7	IO_L29N_8	AR13	FPGA_CON326	23
23	FPGA_CON391	AL31	IO_L4N_VREF_7	IO_L29P_8	AT13	FPGA_CON327	23
23	FPGA_CON392	AP24	IO_L5P_7	IO_L28N_VREF_8	AR11	FPGA_CON328	23
23	FPGA_CON393	AR24	IO_L5N_7	IO_L28P_8	AT11	FPGA_CON329	23
23	FPGA_CON394	AP32	IO_L6P_7	IO_L27N_8	AM13	FPGA_CON330	23
23	FPGA_CON395	AN32	IO_L6N_7	IO_L27P_8	AN14	FPGA_CON331	23
23	FPGA_CON396	AN30	IO_L7P_7	IO_L26N_8	AV9	FPGA_CON332	23
23	FPGA_CON397	AP31	IO_L7N_7	IO_L26P_8	AW9	FPGA_CON333	23
23	FPGA_CON398	AK29	IO_L8P_CC_LC_7	IO_L25N_CC_LC_8	AV12	FPGA_CON334	23
23	FPGA_CON399	AJ29	IO_L8N_CC_LC_7	IO_L25P_CC_LC_8	AW12	FPGA_CON335	23
23	FPGA_CON400	AT24	IO_L9P_CC_LC_7	IO_L24N_CC_LC_8	AV7	FPGA_CON336	23
23	FPGA_CON401	AT25	IO_L9N_CC_LC_7	IO_L24P_CC_LC_8	AV8	FPGA_CON337	23
23	FPGA_CON402	AW34	IO_L10P_7	IO_L23N_VRP_8	AU11	FPGA_CON338	23
23	FPGA_CON403	AV34	IO_L10N_7	IO_L23P_VRN_8	AU12	FPGA_CON339	23
23	FPGA_CON404	AW30	IO_L11P_7	IO_L22N_8	AT9	FPGA_CON340	23
23	FPGA_CON405	AW31	IO_L11N_7	IO_L22P_8	AT10	FPGA_CON341	23
23	FPGA_CON406	AV33	IO_L12P_7	IO_L21N_8	AU13	FPGA_CON342	23
23	FPGA_CON407	AU33	IO_L12N_VREF_7	IO_L21P_8	AV13	FPGA_CON343	23
23	FPGA_CON408	AP25	IO_L13P_7	IO_L20N_VREF_8	AP9	FPGA_CON344	23
23	FPGA_CON409	AP26	IO_L13N_7	IO_L20P_8	AR9	FPGA_CON345	23
23	FPGA_CON410	AT31	IO_L14P_7	IO_L19N_8	AP12	FPGA_CON346	23
23	FPGA_CON411	AT30	IO_L14N_7	IO_L19P_8	AR12	FPGA_CON347	23
23	FPGA_CON412	AU25	IO_L15P_7	IO_L18N_8	AT8	FPGA_CON348	23
23	FPGA_CON413	AV25	IO_L15N_7	IO_L18P_8	AU8	FPGA_CON349	23
23	FPGA_CON414	AR31	IO_L16P_7	IO_L17N_8	AL13	FPGA_CON350	23
23	FPGA_CON415	AR32	IO_L16N_7	IO_L17P_8	AL14	FPGA_CON351	23
23	FPGA_CON416	AL26	IO_L17P_7	IO_L16N_8	AU6	FPGA_CON352	23
23	FPGA_CON417	AM27	IO_L17N_7	IO_L16P_8	AU7	FPGA_CON353	23
23	FPGA_CON418	AU31	IO_L18P_7	IO_L15N_8	AP11	FPGA_CON354	23
23	FPGA_CON419	AU32	IO_L18N_7	IO_L15P_8	AN12	FPGA_CON355	23
23	FPGA_CON420	AV28	IO_L19P_7	IO_L14N_8	AJ12	FPGA_CON356	23
23	FPGA_CON421	AU28	IO_L19N_7	IO_L14P_8	AH13	FPGA_CON357	23
23	FPGA_CON422	AW32	IO_L20P_7	IO_L13N_8	AN10	FPGA_CON358	23
23	FPGA_CON423	AV32	IO_L20N_VREF_7	IO_L13P_8	AM11	FPGA_CON359	23
23	FPGA_CON424	AW25	IO_L21P_7	IO_L12N_VREF_8	AL10	FPGA_CON360	23
23	FPGA_CON425	AW26	IO_L21N_7	IO_L12P_8	AM10	FPGA_CON361	23
23	FPGA_CON426	AP29	IO_L22P_7	IO_L11N_8	AW6	FPGA_CON362	23
23	FPGA_CON427	AN29	IO_L22N_7	IO_L11P_8	AW7	FPGA_CON363	23
23	FPGA_CON428	AN27	IO_L23P_VRN_7	IO_L10N_8	AW4	FPGA_CON364	23
23	FPGA_CON429	AN28	IO_L23N_VRP_7	IO_L10P_8	AW5	FPGA_CON365	23
23	FPGA_CON430	AL28	IO_L24P_CC_LC_7	IO_L9N_CC_LC_8	AK11	FPGA_CON366	23
23	FPGA_CON431	AM28	IO_L24N_CC_LC_7	IO_L9P_CC_LC_8	AL11	FPGA_CON367	23
23	FPGA_CON432	AP27	IO_L25P_CC_SM7_LC_7	IO_L8N_CC_LC_8	AV3	FPGA_CON368	23
23	FPGA_CON433	AR27	IO_L25N_CC_SM7_LC_7	IO_L8P_CC_LC_8	AV4	FPGA_CON369	23
23	FPGA_CON434	AV30	IO_L26P_SM6_7	IO_L7N_8	AR7	FPGA_CON370	23
23	FPGA_CON435	AU30	IO_L26N_SM6_7	IO_L7P_8	AR8	FPGA_CON371	23
23	FPGA_CON436	AR26	IO_L27P_SM5_7	IO_L6N_8	AN7	FPGA_CON372	23
23	FPGA_CON437	AT26	IO_L27N_SM5_7	IO_L6P_8	AP7	FPGA_CON373	23
23	FPGA_CON438	AW29	IO_L28P_7	IO_L5N_8	AN15	FPGA_CON374	23
23	FPGA_CON439	AV29	IO_L28N_VREF_7	IO_L5P_8	AM15	FPGA_CON375	23
23	FPGA_CON440	AV27	IO_L29P_SM4_7	IO_L4N_VREF_8	AK9	FPGA_CON376	23
23	FPGA_CON441	AW27	IO_L29N_SM4_7	IO_L4P_8	AL9	FPGA_CON377	23
23	FPGA_CON442	AT29	IO_L30P_SM3_7	IO_L3N_8	AN8	FPGA_CON378	23
23	FPGA_CON443	AR29	IO_L30N_SM3_7	IO_L3P_8	AN9	FPGA_CON379	23
23	FPGA_CON444	AU26	IO_L31P_SM2_7	IO_L2N_8	AJ9	FPGA_CON380	23
23	FPGA_CON445	AU27	IO_L31N_SM2_7	IO_L2P_8	AJ10	FPGA_CON381	23
23	FPGA_CON446	AT28	IO_L32P_SM1_7	IO_L1N_8	AU5	FPGA_CON382	23
23	FPGA_CON447	AR28	IO_L32N_SM1_7	IO_L1P_8	AV5	FPGA_CON383	23

VDD3V3	AK30	VCCO_7	VCCO_8	AW3	VDD3V3
VDD3V3	AL27	VCCO_7	VCCO_8	AW13	VDD3V3
VDD3V3	AN31	VCCO_7	VCCO_8	AV6	VDD3V3
VDD3V3	AP28	VCCO_7	VCCO_8	AU9	VDD3V3
VDD3V3	AR25	VCCO_7	VCCO_8	AT12	VDD3V3
VDD3V3	AT32	VCCO_7	VCCO_8	AP8	VDD3V3
VDD3V3	AU29	VCCO_7	VCCO_8	AN11	VDD3V3
VDD3V3	AV26	VCCO_7	VCCO_8	AM14	VDD3V3
VDD3V3	AW33	VCCO_7	VCCO_8	AK10	VDD3V3
			VCCO_8	AJ13	VDD3V3

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Bank 9 / Bank 10

14	EXP_IO_64	D34	IO_L1P_9	IO_L32N_10	T11	FPGA_CON64	23
14	EXP_IO_65	D35	IO_L1N_9	IO_L32P_10	U12	FPGA_CON65	23
14	EXP_IO_66	C37	IO_L2P_9	IO_L31N_10	R8	FPGA_CON66	23
14	EXP_IO_67	C38	IO_L2N_9	IO_L31P_10	R9	FPGA_CON67	23
14	EXP_IO_68	E34	IO_L3P_9	IO_L30N_10	P7	FPGA_CON68	23
14	EXP_IO_69	E34	IO_L3N_9	IO_L30P_10	N7	FPGA_CON69	23
14	EXP_IO_70	E35	IO_L4P_9	IO_L29N_10	M6	FPGA_CON70	23
14	EXP_IO_71	G35	IO_L4N_VREF_9	IO_L29P_10	L6	FPGA_CON71	23
14	EXP_IO_72	D36	IO_L5P_9	IO_L28N_VREF_10	N8	FPGA_CON72	23
14	EXP_IO_73	D37	IO_L5N_9	IO_L28P_10	P9	FPGA_CON73	23
14	EXP_IO_74	H33	IO_L6P_9	IO_L27N_10	M7	FPGA_CON74	23
14	EXP_IO_75	H34	IO_L6N_9	IO_L27P_10	M8	FPGA_CON75	23
14	EXP_IO_76	E36	IO_L7P_9	IO_L26N_10	U13	FPGA_CON76	23
14	EXP_IO_77	E36	IO_L7N_9	IO_L26P_10	T13	FPGA_CON77	23
14	EXP_IO_78	C39	IO_L8P_CC_LC_9	IO_L25N_CC_LC_10	R11	FPGA_CON78	23
14	EXP_IO_79	D39	IO_L8N_CC_LC_9	IO_L25P_CC_LC_10	P11	FPGA_CON79	23
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14	EXP_IO_81	K32	IO_L9N_CC_LC_9	IO_L24P_CC_LC_10	F1	FPGA_CON81	23
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14	EXP_IO_89	M31	IO_L13N_9	IO_L20P_10	K7	FPGA_CON89	23
14	EXP_IO_90	E39	IO_L14P_9	IO_L19N_10	R12	FPGA_CON90	23
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14	EXP_IO_92	J34	IO_L15P_9	IO_L18N_10	E1	FPGA_CON92	23
14	EXP_IO_93	K34	IO_L15N_9	IO_L18P_10	E2	FPGA_CON93	23
14	EXP_IO_94	E38	IO_L16P_9	IO_L17N_10	T14	FPGA_CON94	23
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14	EXP_IO_98	H37	IO_L18P_9	IO_L15N_10	E3	FPGA_CON98	23
14	EXP_IO_99	H38	IO_L18N_9	IO_L15P_10	E4	FPGA_CON99	23
14	EXP_IO_100	N30	IO_L19P_9	IO_L14N_10	N10	FPGA_CON100	23
14	EXP_IO_101	P29	IO_L19N_9	IO_L14P_10	M10	FPGA_CON101	23
14	EXP_IO_102	L34	IO_L20P_9	IO_L13N_10	T15	FPGA_CON102	23
14	EXP_IO_103	L35	IO_L20N_VREF_9	IO_L13P_10	R16	FPGA_CON103	23
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14	EXP_IO_105	J37	IO_L21N_9	IO_L12P_10	F4	FPGA_CON105	23
14	EXP_IO_106	K36	IO_L22P_9	IO_L11N_10	N12	FPGA_CON106	23
14	EXP_IO_107	L36	IO_L22N_9	IO_L11P_10	M11	FPGA_CON107	23
14	EXP_IO_108	H39	IO_L23P_VRN_9	IO_L10N_10	G5	FPGA_CON108	23
14	EXP_IO_109	J39	IO_L23N_VRP_9	IO_L10P_10	F5	FPGA_CON109	23
14	EXP_IO_110	M33	IO_L24P_CC_LC_9	IO_L9N_CC_LC_10	G6	FPGA_CON110	23
14	EXP_IO_111	N32	IO_L24N_CC_LC_9	IO_L9P_CC_LC_10	G7	FPGA_CON111	23
14	EXP_IO_112	R28	IO_L25P_CC_LC_9	IO_L8N_CC_LC_10	J7	FPGA_CON112	23
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14	EXP_IO_114	M35	IO_L26P_9	IO_L7N_10	F6	FPGA_CON114	23
14	EXP_IO_115	N35	IO_L26N_9	IO_L7P_10	F6	FPGA_CON115	23
14	EXP_IO_116	K37	IO_L27P_9	IO_L6N_10	C2	FPGA_CON116	23
14	EXP_IO_117	K38	IO_L27N_9	IO_L6P_10	C3	FPGA_CON117	23
14	EXP_IO_118	N33	IO_L28P_9	IO_L5N_10	D5	FPGA_CON118	23
14	EXP_IO_119	N34	IO_L28N_VREF_9	IO_L5P_10	D6	FPGA_CON119	23
14	EXP_IO_120	P31	IO_L29P_9	IO_L4N_VREF_10	D4	FPGA_CON120	23
14	EXP_IO_121	P32	IO_L29N_9	IO_L4P_10	C4	FPGA_CON121	23
14	EXP_IO_122	K39	IO_L30P_9	IO_L3N_10	C5	FPGA_CON122	23
14	EXP_IO_123	L39	IO_L30N_9	IO_L3P_10	B5	FPGA_CON123	23
14	EXP_IO_124	L38	IO_L31P_9	IO_L2N_10	B3	FPGA_CON124	23
14	EXP_IO_125	M38	IO_L31N_9	IO_L2P_10	A3	FPGA_CON125	23
14	EXP_IO_126	M36	IO_L32P_9	IO_L1N_10	A4	FPGA_CON126	23
14	EXP_IO_127	M37	IO_L32N_9	IO_L1P_10	A5	FPGA_CON127	23

VDD3V3	D38	VCCO_9	VCCO_10	T12	VDD3V3
VDD3V3	E35	VCCO_9	VCCO_10	R15	VDD3V3
VDD3V3	G39	VCCO_9	VCCO_10	P8	VDD3V3
VDD3V3	H36	VCCO_9	VCCO_10	N11	VDD3V3
VDD3V3	J33	VCCO_9	VCCO_10	L7	VDD3V3
VDD3V3	L37	VCCO_9	VCCO_10	H6	VDD3V3
VDD3V3	M34	VCCO_9	VCCO_10	F2	VDD3V3
VDD3V3	N31	VCCO_9	VCCO_10	E5	VDD3V3
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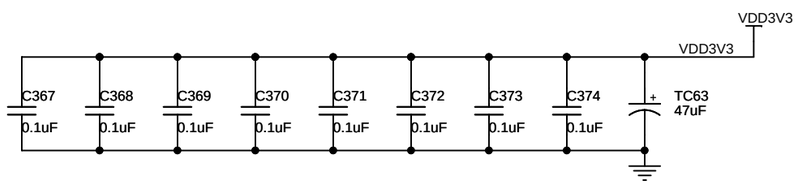

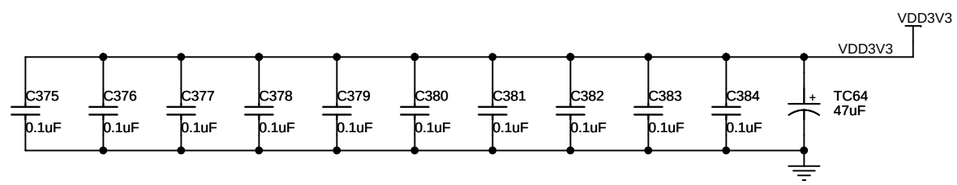

SANGHWA FPGA PLATFORM

Title: FPGA0 BANK 7/8/9/10

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A3	<Doc>	1.0

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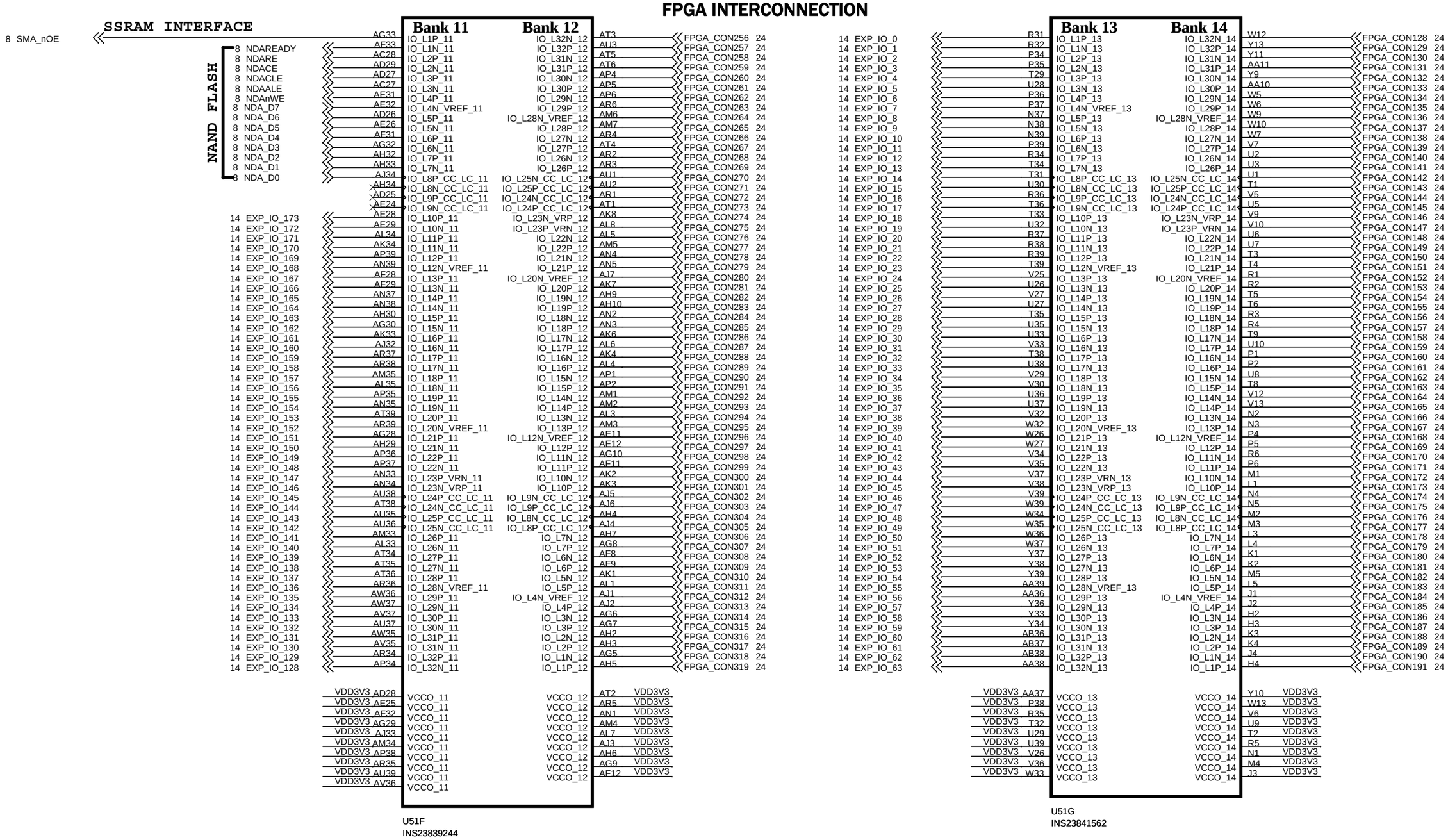
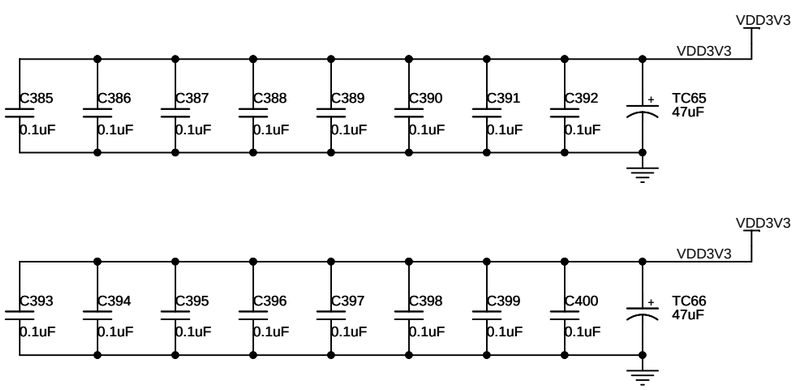
FPGA INTERCONNECTION





Title	SANGHWA FPGA PLATFORM FPGA0 BANK 11/12/13/14		
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VIRTEX-4 FPGA
POWER GROUND

GND	D13	GND	J28
GND	K13	GND	N28
GND	M13	GND	W28
GND	P13	GND	AJ28
GND	AD13	GND	AW28
GND	AF13	GND	B29
GND	AK13	GND	M29
GND	AP13	GND	AB29
GND	G14	GND	AM29
GND	L14	GND	E30
GND	N14	GND	R30
GND	U14	GND	AF30
GND	W14	GND	AR30
GND	AF14	GND	H31
GND	AG14	GND	V31
GND	AJ14	GND	AH31
GND	AU14	GND	AV31
GND	K15	GND	A32
GND	M15	GND	L32
GND	P15	GND	AA32
GND	V15	GND	AL32
GND	Y15	GND	D33
GND	AD15	GND	P33
GND	AF15	GND	AD33
GND	AK15	GND	AP33
GND	C16	GND	G34
GND	N16	GND	U34
GND	U16	GND	AG34
GND	W16	GND	AU34
GND	AC16	GND	K35
GND	AE16	GND	Y35
GND	AN16	GND	AK35
GND	F17	GND	C36
GND	T17	GND	N36
GND	V17	GND	AC36
GND	AF17	GND	AN36
GND	AT17	GND	F37
GND	J18	GND	T37
GND	W18	GND	AF37
GND	AC18	GND	AT37
GND	AJ18	GND	A38
GND	AW18	GND	J38
GND	B19	GND	W38
GND	M19	GND	AJ38
GND	V19	GND	AW38
GND	AB19	GND	B39
GND	AD19	GND	M39
GND	AM19	GND	AB39
GND	E20	GND	AM39
GND	R20	GND	AV39
GND	AE20	GND	B1
GND	AR20	GND	H1
GND	H21	GND	V1
GND	T21	GND	AH1
GND	V21	GND	AV1
GND	AB21	GND	A2
GND	AH21	GND	L2
GND	AV21	GND	AA2
GND	A22	GND	AL2
GND	L22	GND	AW2
GND	U22	GND	D3
GND	AA22	GND	P3
GND	AL22	GND	AD3
GND	D23	GND	AP3
GND	P23	GND	G4
GND	AB23	GND	U4
GND	AD23	GND	AG4
GND	AP23	GND	AU4
GND	G24	GND	K5
GND	R24	GND	Y5
GND	U24	GND	AK5
GND	AA24	GND	C6
GND	AC24	GND	N6
GND	AG24	GND	AC6
GND	AU24	GND	AN6
GND	K25	GND	F7
GND	P25	GND	T7
GND	T25	GND	AF7
GND	Y25	GND	AT7
GND	AB25	GND	J8
GND	AF25	GND	W8
GND	AH25	GND	AJ8
GND	AK25	GND	AW8
GND	C26	GND	B9
GND	L26	GND	M9
GND	N26	GND	AB9
GND	R26	GND	AM9
GND	AA26	GND	E10
GND	AC26	GND	R10
GND	AG26	GND	AF10
GND	AJ26	GND	AR10
GND	AN26	GND	H11
GND	F27	GND	V11
GND	K27	GND	AH11
GND	P27	GND	AV11
GND	T27	GND	A12
GND	AF27	GND	L12
GND	AH27	GND	AA12
GND	AK27	GND	AG12
GND	AT27	GND	AL12

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SSRAM INTERFACE

8	SMA_A2	Y27	IO_L1P_15	IO_L32N_16	AF3	FPGA_CON192	25
8	SMA_A3	AA28	IO_L1N_15	IO_L32P_16	AG3	FPGA_CON193	25
8	SMA_A4	W29	IO_L2P_15	IO_L31N_16	AF8	FPGA_CON194	25
8	SMA_A5	W30	IO_L2N_15	IO_L31P_16	AF9	FPGA_CON195	25
8	SMA_A6	AA34	IO_L3P_15	IO_L30N_16	AG1	FPGA_CON196	25
8	SMA_A7	AA35	IO_L3N_15	IO_L30P_16	AG2	FPGA_CON197	25
8	SMA_A8	Y29	IO_L4P_15	IO_L29N_16	AF5	FPGA_CON198	25
8	SMA_A9	AA30	IO_L4N_VREF_15	IO_L29P_16	AF6	FPGA_CON199	25
8	SMA_A10	AC38	IO_L5P_15	IO_L28N_VREF_16	AD6	FPGA_CON200	25
8	SMA_A11	AC39	IO_L5N_15	IO_L28P_16	AE6	FPGA_CON201	25
8	SMA_A12	AA31	IO_L6P_15	IO_L27N_16	AE4	FPGA_CON202	25
8	SMA_A13	Y31	IO_L6N_15	IO_L27P_16	AE4	FPGA_CON203	25
8	SMA_A14	AC35	IO_L7P_15	IO_L26N_16	AE1	FPGA_CON204	25
8	SMA_A15	AB35	IO_L7N_15	IO_L26P_16	AE1	FPGA_CON205	25
8	SMA_A16	AB33	IO_L8P_CC_LC_15	IO_L25N_CC_LC_16	AD11	FPGA_CON206	25
8	SMA_A17	AA33	IO_L8N_CC_LC_15	IO_L25P_CC_LC_16	AC12	FPGA_CON207	25
8	SMA_A18	AC33	IO_L9P_CC_LC_15	IO_L24N_CC_LC_16	AE2	FPGA_CON208	25
8	SMA_A19	AC34	IO_L9N_CC_LC_15	IO_L24P_CC_LC_16	AE3	FPGA_CON209	25
8	SMA_A20	AD37	IO_L10P_15	IO_L23N_VRP_16	AC7	FPGA_CON210	25
8	SMA_nADSC	AC37	IO_L10N_15	IO_L23P_VRN_16	AD7	FPGA_CON211	25
8	SMA_nADSP	AC32	IO_L11P_15	IO_L22N_16	AD9	FPGA_CON212	25
8	SMA_nADV	AB31	IO_L11N_15	IO_L22P_16	AC10	FPGA_CON213	25
8	SMA_nBW1	AE39	IO_L12P_15	IO_L21N_16	AC14	FPGA_CON214	25
8	SMA_nBW2	AD39	IO_L12N_VREF_15	IO_L21P_16	AB15	FPGA_CON215	25
8	SMA_nBW3	AE38	IO_L13P_15	IO_L20N_VREF_16	AC13	FPGA_CON216	25
8	SMA_nBW4	AE39	IO_L13N_15	IO_L20P_16	AB13	FPGA_CON217	25
8	SMA_nBWE	AD35	IO_L14P_15	IO_L19N_16	AD4	FPGA_CON218	25
8	SMA_nCE	AD36	IO_L14N_15	IO_L19P_16	AD5	FPGA_CON219	25
8	SMA_CLK	AC30	IO_L15P_15	IO_L18N_16	AD1	FPGA_CON220	25
8	SMA_nCS1	AB30	IO_L15N_15	IO_L18P_16	AD2	FPGA_CON221	25
8	SMA_nGW	AE37	IO_L16P_15	IO_L17N_16	AB8	FPGA_CON222	25
8	SMA_nLBO	AE38	IO_L16N_15	IO_L17P_16	AC8	FPGA_CON223	25
8	SMA_D31	AB27	IO_L17P_15	IO_L16N_16	AC4	FPGA_CON224	25
8	SMA_D30	AB28	IO_L17N_15	IO_L16P_16	AC5	FPGA_CON225	25
8	SMA_D29	AE34	IO_L18P_15	IO_L15N_16	AB10	FPGA_CON226	25
8	SMA_D28	AD34	IO_L18N_15	IO_L15P_16	AB11	FPGA_CON227	25
8	SMA_D27	AD31	IO_L19P_15	IO_L14N_16	AA8	FPGA_CON228	25
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8	SMA_D23	AJ39	IO_L21P_15	IO_L12N_VREF_16	AB1	FPGA_CON232	25
8	SMA_D22	AH39	IO_L21N_15	IO_L12P_16	AB2	FPGA_CON233	25
8	SMA_D21	AG37	IO_L22P_15	IO_L11N_16	AB5	FPGA_CON234	25
8	SMA_D20	AG38	IO_L22N_15	IO_L11P_16	AB6	FPGA_CON235	25
8	SMA_D19	AH37	IO_L23P_VRN_15	IO_L10N_16	AA5	FPGA_CON236	25
8	SMA_D18	AH38	IO_L23N_VRP_15	IO_L10P_16	AA6	FPGA_CON237	25
8	SMA_D17	AE34	IO_L24P_CC_LC_15	IO_L9N_CC_LC_16	AA13	FPGA_CON238	25
8	SMA_D16	AE35	IO_L24N_CC_LC_15	IO_L9P_CC_LC_16	AA14	FPGA_CON239	25
8	SMA_D15	AJ36	IO_L25P_CC_LC_15	IO_L8N_CC_LC_16	AA1	FPGA_CON240	25
8	SMA_D14	AJ37	IO_L25N_CC_LC_15	IO_L8P_CC_LC_16	Y1	FPGA_CON241	25
8	SMA_D13	AG35	IO_L26P_15	IO_L7N_16	AB3	FPGA_CON242	25
8	SMA_D12	AG36	IO_L26N_15	IO_L7P_16	AA3	FPGA_CON243	25
8	SMA_D11	AJ35	IO_L27P_15	IO_L6N_16	Y2	FPGA_CON244	25
8	SMA_D10	AH35	IO_L27N_15	IO_L6P_16	Y3	FPGA_CON245	25
8	SMA_D9	AK38	IO_L28P_15	IO_L5N_16	AA4	FPGA_CON246	25
8	SMA_D8	AK39	IO_L28N_VREF_15	IO_L5P_16	Y4	FPGA_CON247	25
8	SMA_D7	AM37	IO_L29P_15	IO_L4N_VREF_16	Y6	FPGA_CON248	25
8	SMA_D6	AM38	IO_L29N_15	IO_L4P_16	Y7	FPGA_CON249	25
8	SMA_D5	AL38	IO_L30P_15	IO_L3N_16	W1	FPGA_CON250	25
8	SMA_D4	AL39	IO_L30N_15	IO_L3P_16	W2	FPGA_CON251	25
8	SMA_D3	AM36	IO_L31P_15	IO_L2N_16	V2	FPGA_CON252	25
8	SMA_D2	AL36	IO_L31N_15	IO_L2P_16	V3	FPGA_CON253	25
8	SMA_D1	AK36	IO_L32P_15	IO_L1N_16	W4	FPGA_CON254	25
8	SMA_D0	AK37	IO_L32N_15	IO_L1P_16	V4	FPGA_CON255	25

Bank 15 **Bank 16**

VDD3V3	AA27	VCCO_15	VCCO_16	W3	VDD3V3
VDD3V3	AB34	VCCO_15	VCCO_16	AF2	VDD3V3
VDD3V3	AC31	VCCO_15	VCCO_16	AF5	VDD3V3
VDD3V3	AD38	VCCO_15	VCCO_16	AD8	VDD3V3
VDD3V3	AE35	VCCO_15	VCCO_16	AC11	VDD3V3
VDD3V3	AG39	VCCO_15	VCCO_16	AC1	VDD3V3
VDD3V3	AH36	VCCO_15	VCCO_16	AB4	VDD3V3
VDD3V3	AL37	VCCO_15	VCCO_16	AB14	VDD3V3
VDD3V3	Y30	VCCO_15	VCCO_16	AA7	VDD3V3

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VDD3V3

C401	C402	C403	C404	C405	C406	C407	C408	TC67
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	47uF

Title
SANGHWA FPGA PLATFORM
FPGA0 BANK 15/16/GND

Size	Document Number	Rev
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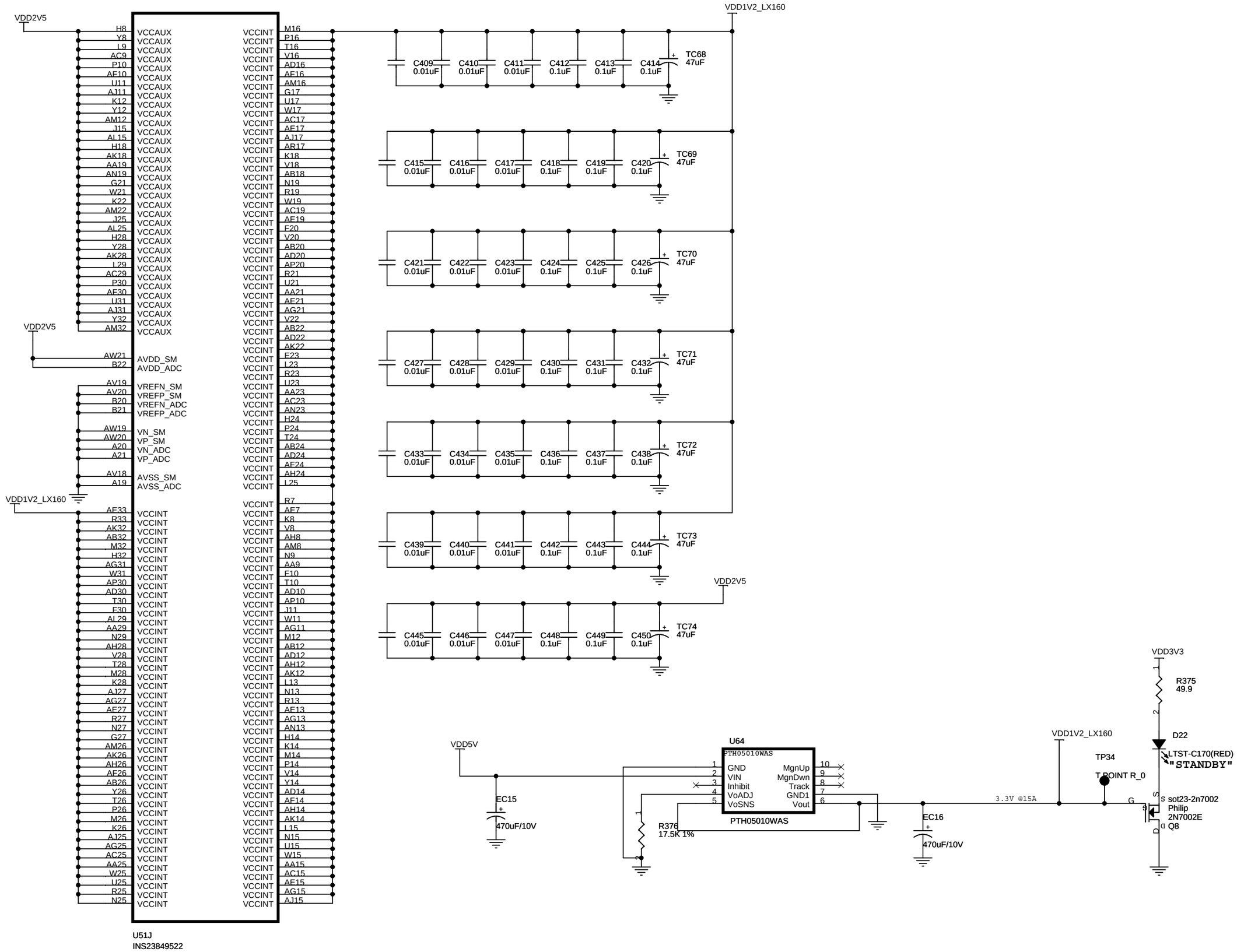

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Size A3	Document Number <Doc>	Rev 1.0
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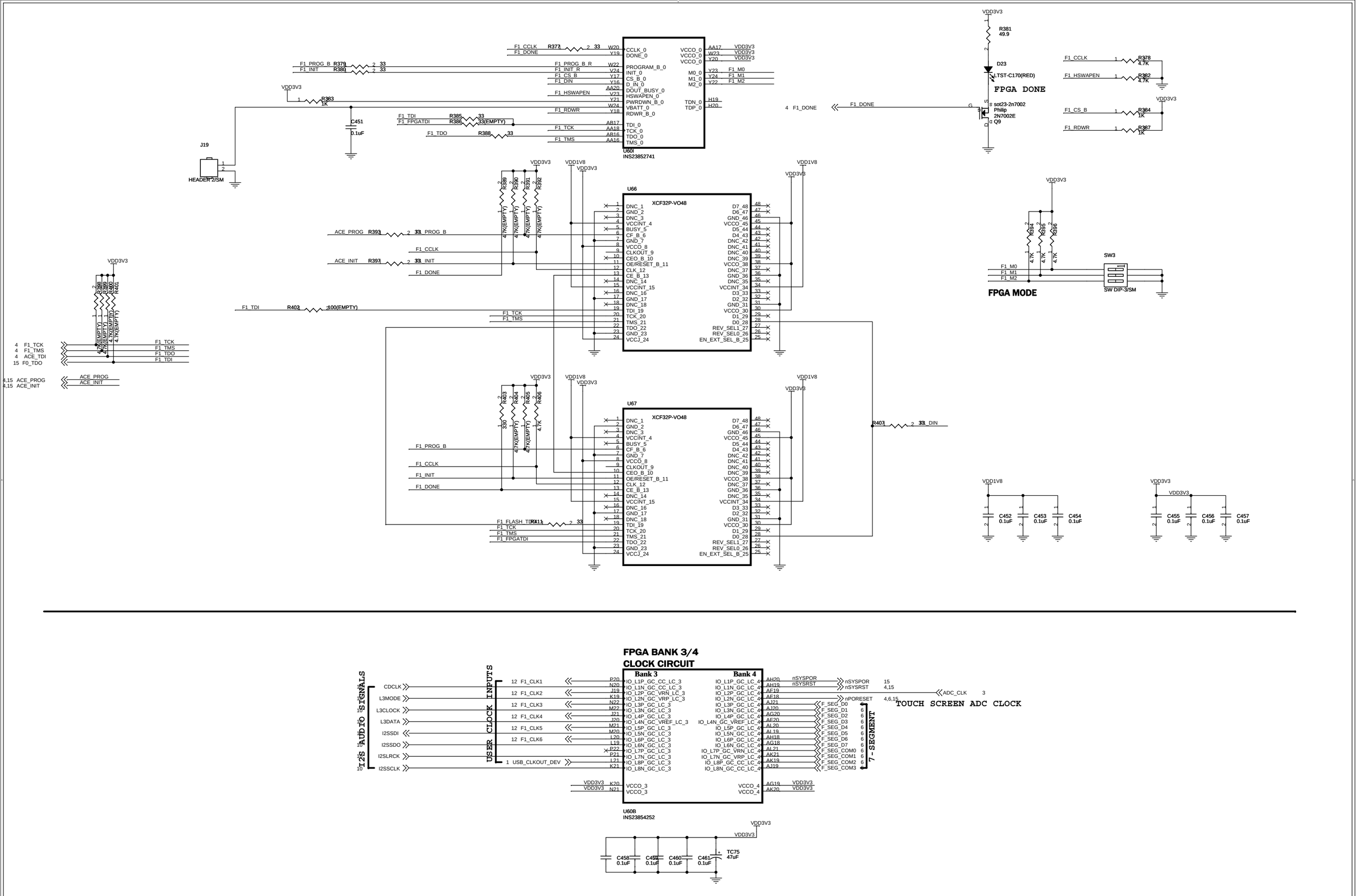
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FPGA DONE
FPGA MODE
SW3
SW DIP-3/SM
FPGA BANK 3/4
CLOCK CIRCUIT
Bank 3
Bank 4
U60B
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USER CLOCK INPUTS
7 - SEGMENT
TOUCH SCREEN ADC CLOCK
SANGHWA FPGA PLATFORM
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Size A2
Document Number
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Rev 1.0
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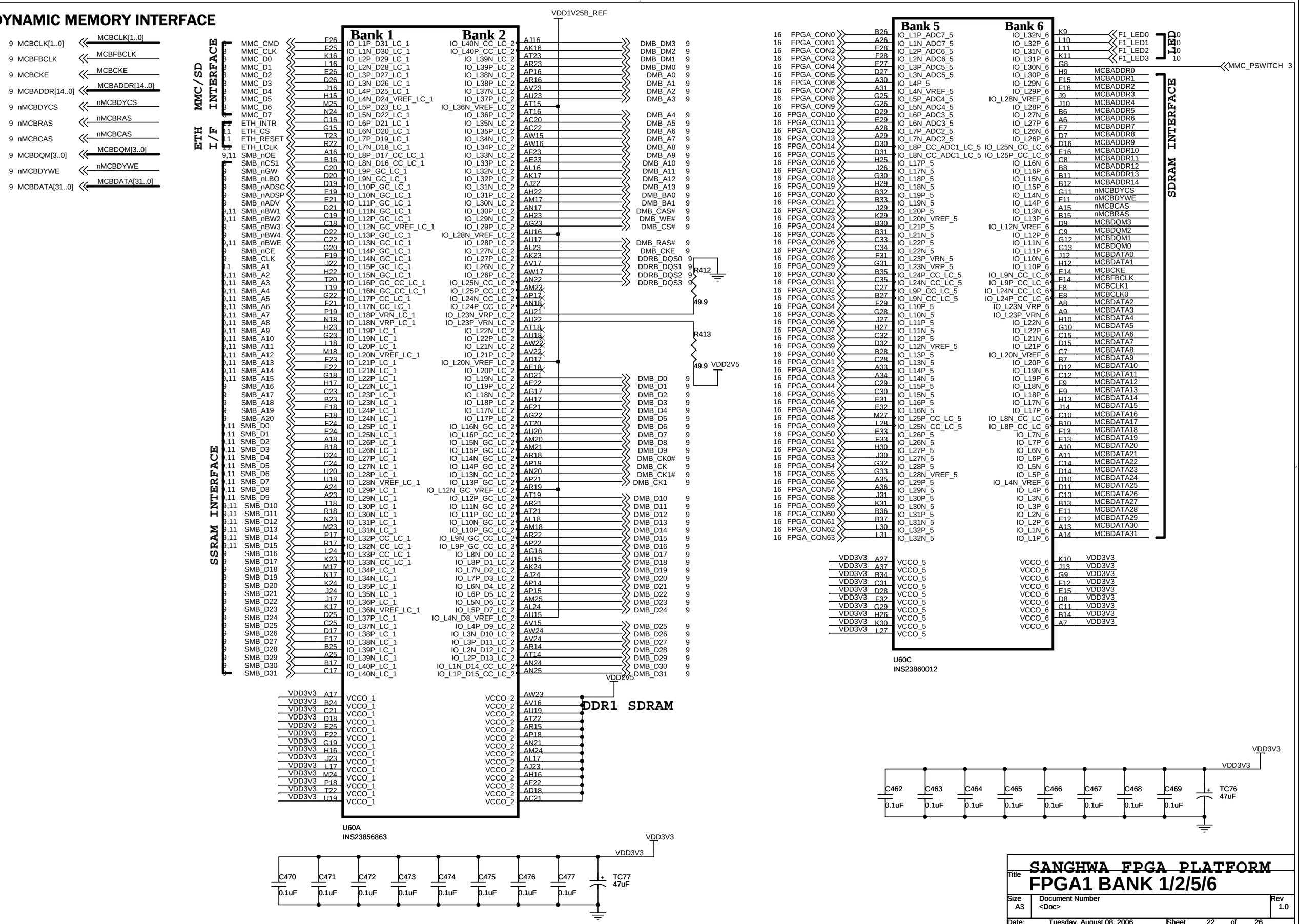
DYNAMIC MEMORY INTERFACE



SANGHWA FPGA PLATFORM

Title: FPGA1 BANK 1/2/5/6

Size	Document Number	Rev
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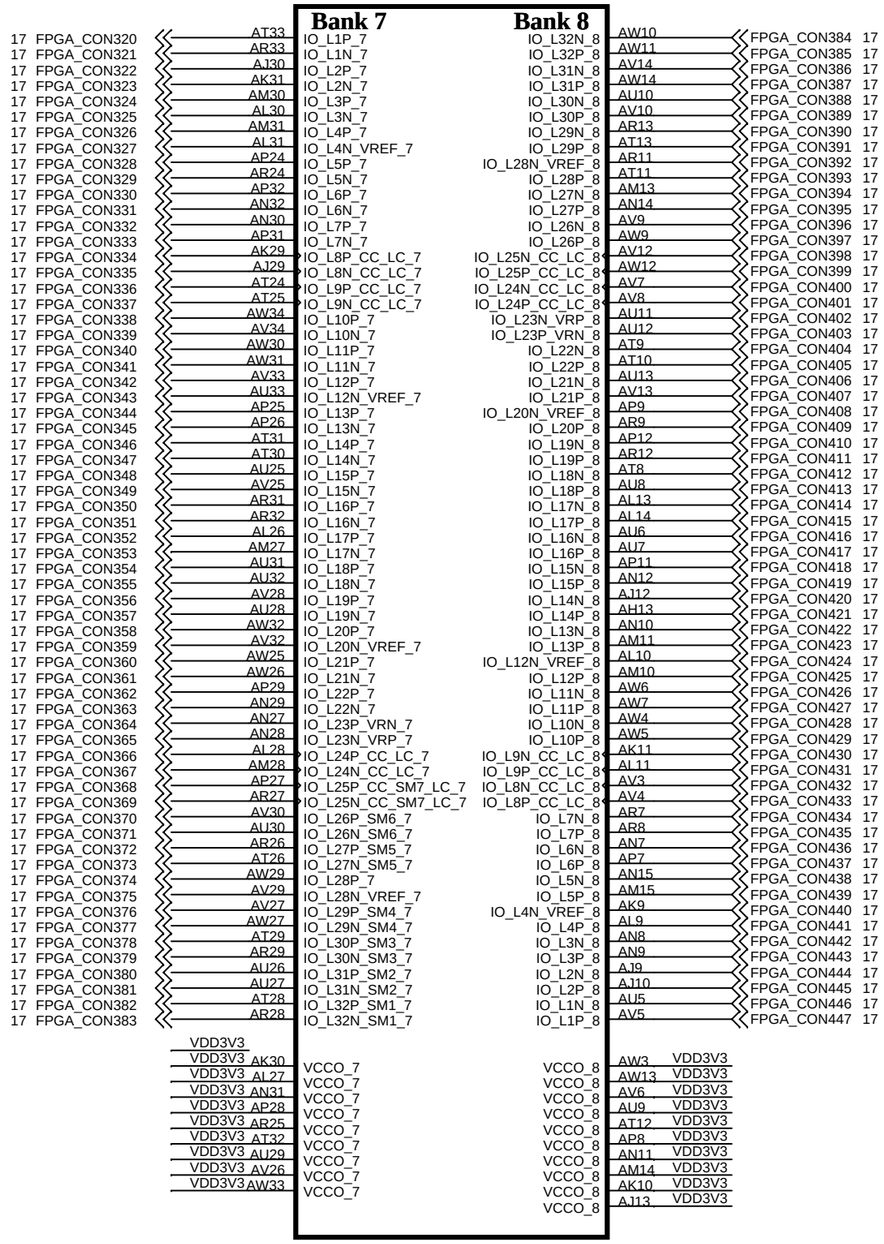

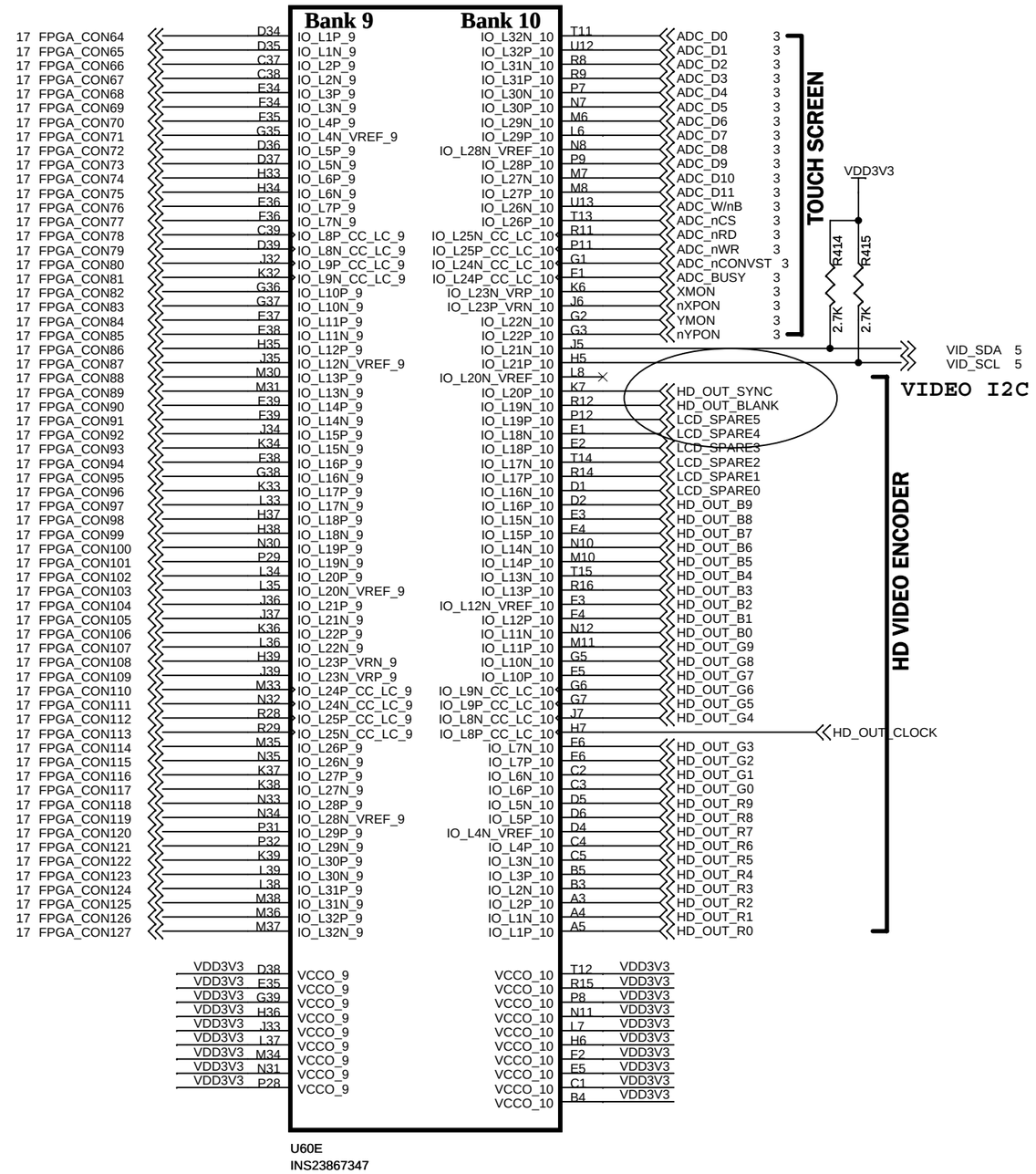

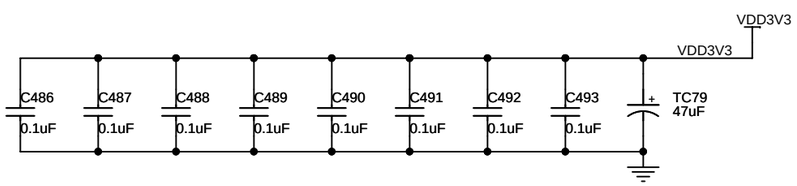

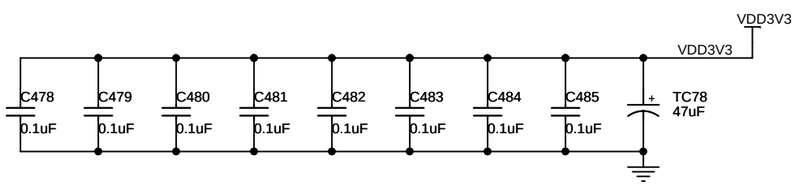

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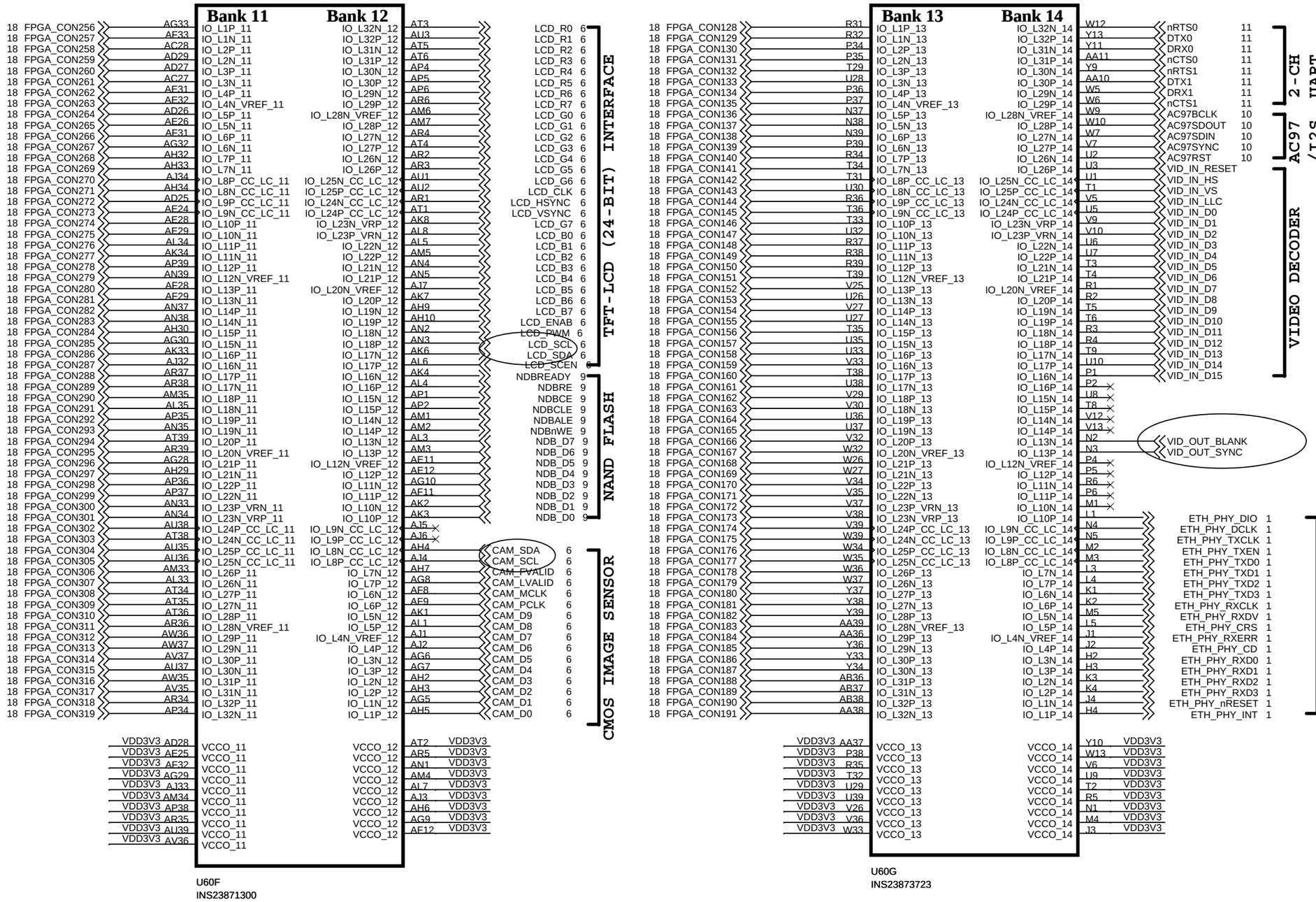

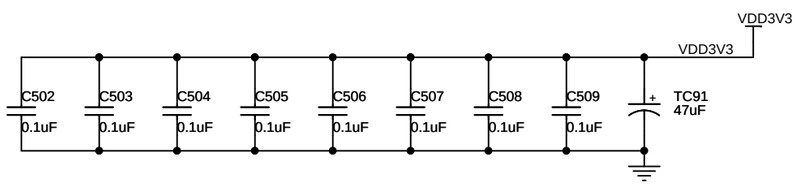

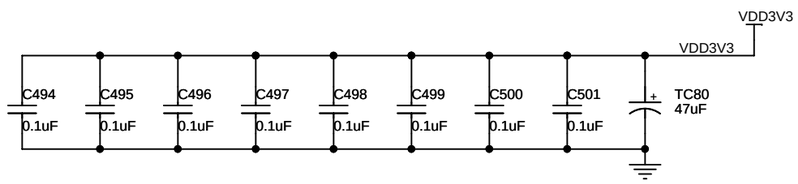

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Size A3	Document Number <Doc>
Rev	1.0
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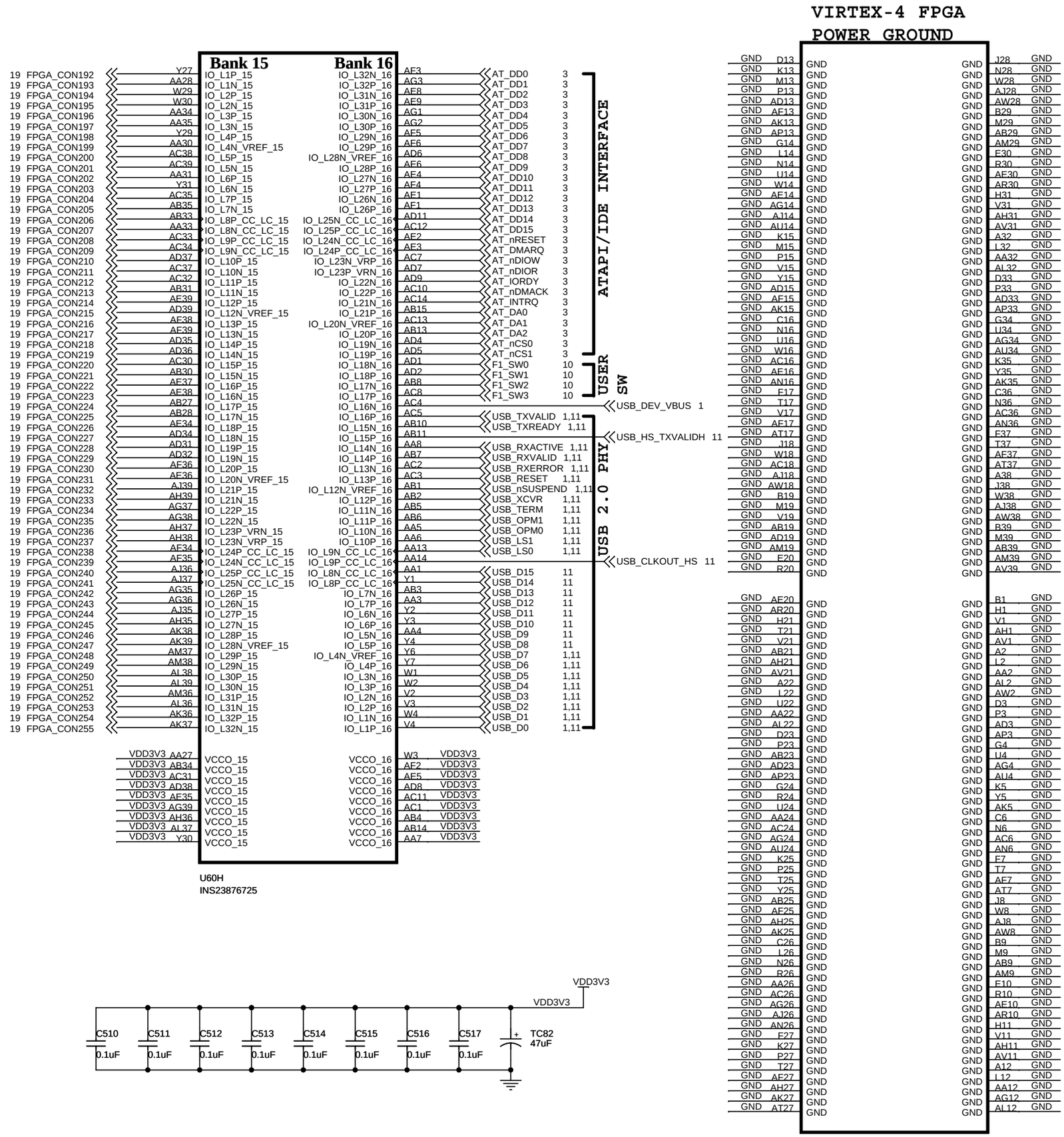

SANGHWA FPGA PLATFORM

Title: FPGA1 BANK 15/16/GND

Size	Document Number	Rev
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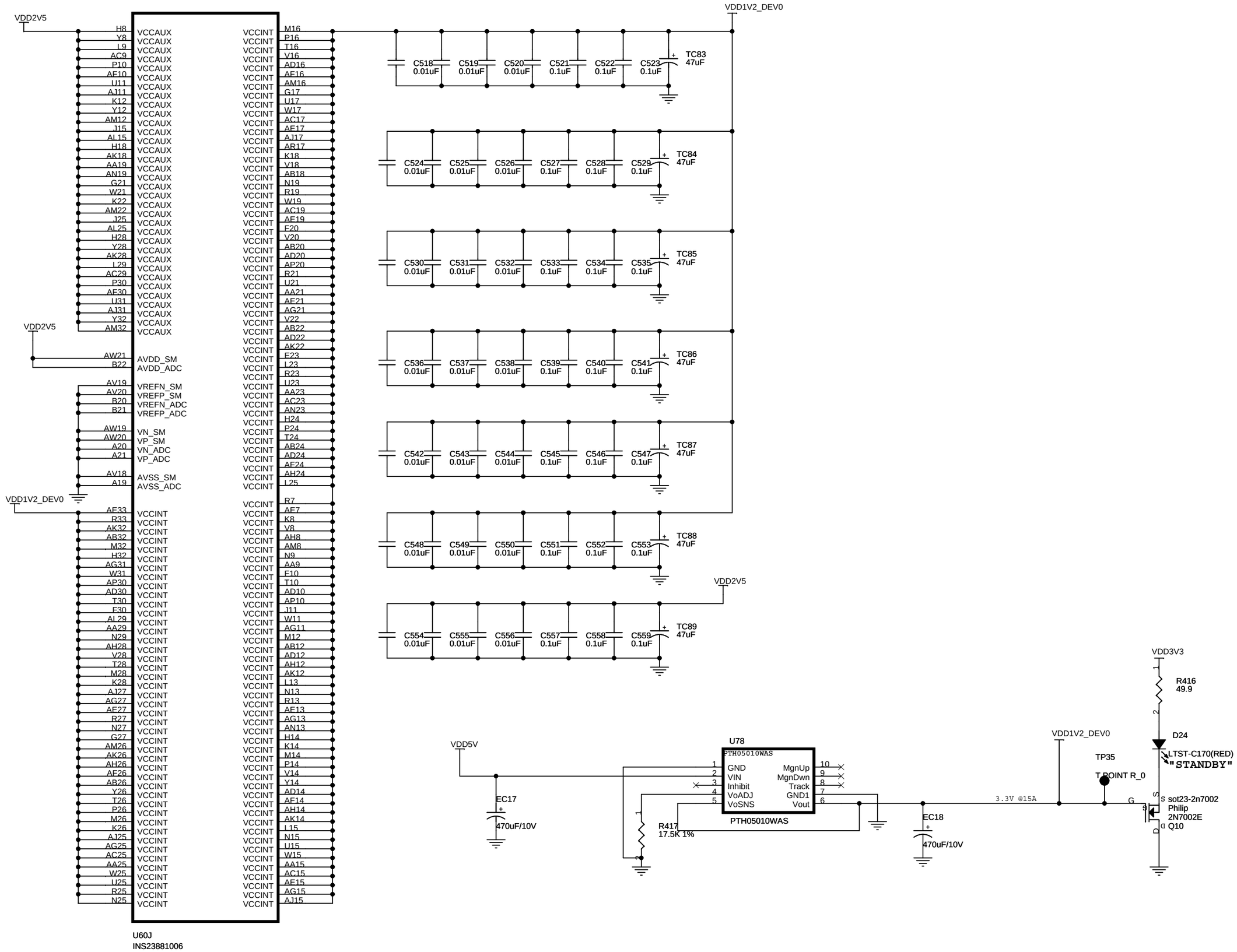

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Size A3	Document Number <Doc>	Rev 1.0
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