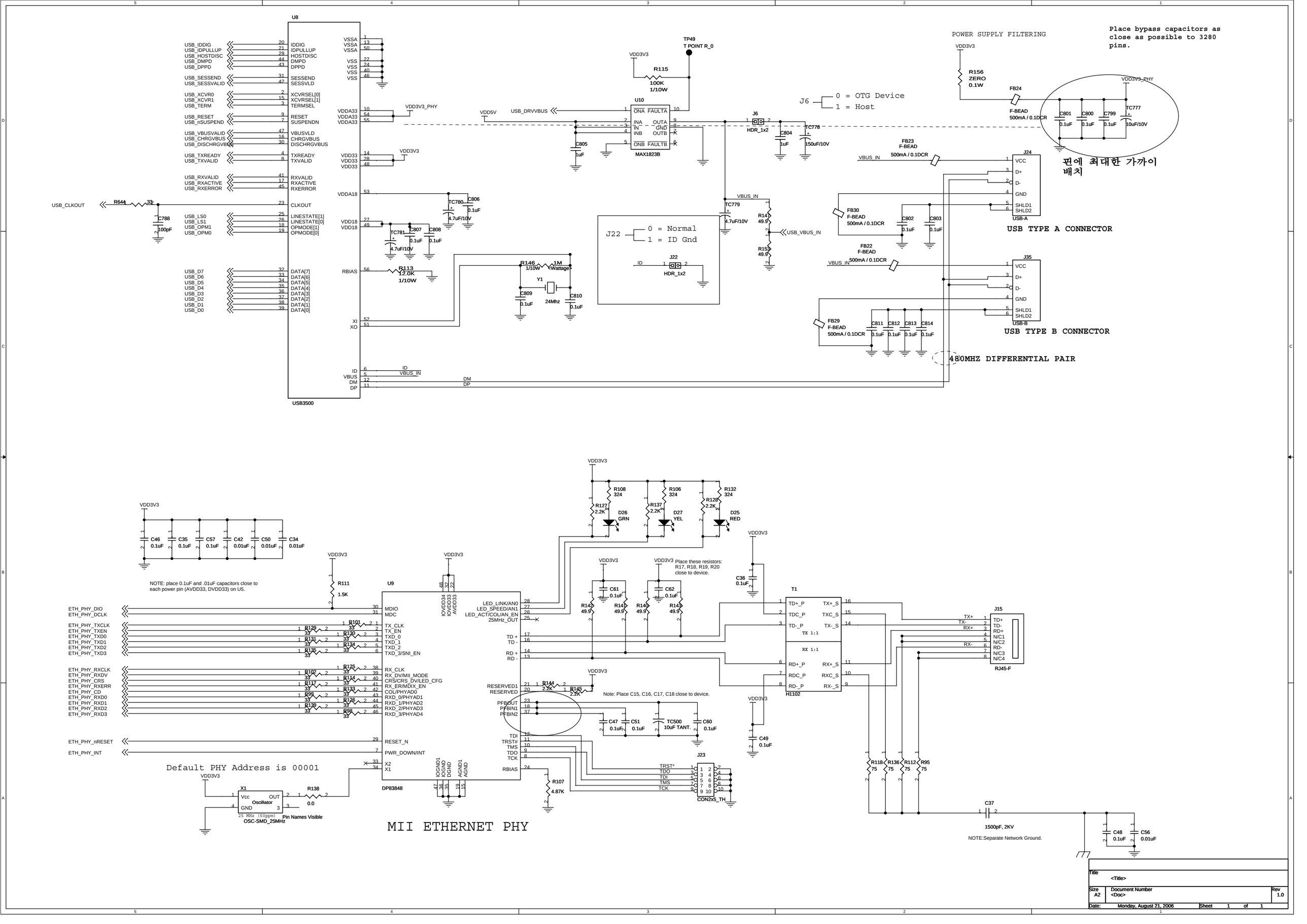

U8
USB3500
USB_IDDIG
USB_IDPULLUP
USB_HOSTDISC
USB_DMPD
USB_DPPD
USB_SESSEND
USB_SESSVALID
USB_XCVR0
USB_XCVR1
USB_TERM
USB_RESET
USB_nSUSPEND
USB_VBUSVALID
USB_CHRGVBUS
USB_DISCHRGVBUS
USB_TXREADY
USB_TXVALID
USB_RXVALID
USB_RXACTIVE
USB_RXERROR
USB_CLKOUT
USB_LS0
USB_LS1
USB_OPM1
USB_OPM0
USB_D7
USB_D6
USB_D5
USB_D4
USB_D3
USB_D2
USB_D1
USB_D0
R644
33
C788
100pF
VDD3V3_PHY
VDD3V3
TC780
C806
4.7uF/10V
0.1uF
TC781
C807
C808
R113
12.0K
1/10W
R146
1M
Wattage
Y1
24Mhz
C809
C810
TP49
T POINT R_0
R115
100K
1/10W
U10
MAX1823B
VDD5V
USB_DRVVBUS
C805
1uF
J6
HDR_1x2
C804
TC778
150uF/10V
J6
0 = OTG Device
1 = Host
J22
0 = Normal
1 = ID Gnd
TC779
R147
49.9
R153
USB_VBUS_IN
POWER SUPPLY FILTERING
R156
ZERO
0.1W
FB24
F-BEAD
500mA / 0.1DCR
C801
C800
C799
TC777
10uF/10V
Place bypass capacitors as close as possible to 3280 pins.
핀에 최대한 가까이 배치
FB23
FB30
FB22
FB29
J24
J35
USB-A
USB-B
USB TYPE A CONNECTOR
USB TYPE B CONNECTOR
C802
C803
C811
C812
C813
C814
480MHZ DIFFERENTIAL PAIR
C46
C35
C57
C42
C50
C34
0.01uF
NOTE: place 0.1uF and .01uF capacitors close to each power pin (AVDD33, DVDD33) on U5.
R111
1.5K
U9
DP83848
ETH_PHY_DIO
ETH_PHY_DCLK
ETH_PHY_TXCLK
ETH_PHY_TXEN
ETH_PHY_TXD0
ETH_PHY_TXD1
ETH_PHY_TXD2
ETH_PHY_TXD3
ETH_PHY_RXCLK
ETH_PHY_RXDV
ETH_PHY_CRS
ETH_PHY_RXERR
ETH_PHY_CD
ETH_PHY_RXD0
ETH_PHY_RXD1
ETH_PHY_RXD2
ETH_PHY_RXD3
ETH_PHY_nRESET
ETH_PHY_INT
Default PHY Address is 00001
X1
Oscillator
25 MHz (50ppm)
OSC-SMD_25MHz
R138
0.0
Pin Names Visible
R108
324
R106
R132
R127
2.2K
R137
R128
D26
GRN
D27
YEL
D25
RED
Place these resistors: R17, R18, R19, R20 close to device.
C61
C62
0.1uF
R142
R141
R140
R143
49.9
C36
T1
TX 1:1
RX 1:1
H1102
J15
RJ45-F
TX+
TX-
RX+
RX-
Note: Place C15, C16, C17, C18 close to device.
C47
C51
TC500
10uF TANT.
C60
C49
R144
2.2K
R145
J23
CON2x5_TH
TRST*
TDO
TDI
TMS
TCK
R107
4.87K
R118
R136
R112
R95
75
C37
1500pF, 2KV
NOTE:Separate Network Ground.
C48
C56
0.01uF
MII ETHERNET PHY
Title
<Title>
Size
A2
Document Number
<Doc>
Rev
1.0
Date:
Monday, August 21, 2006
Sheet
1
of
1

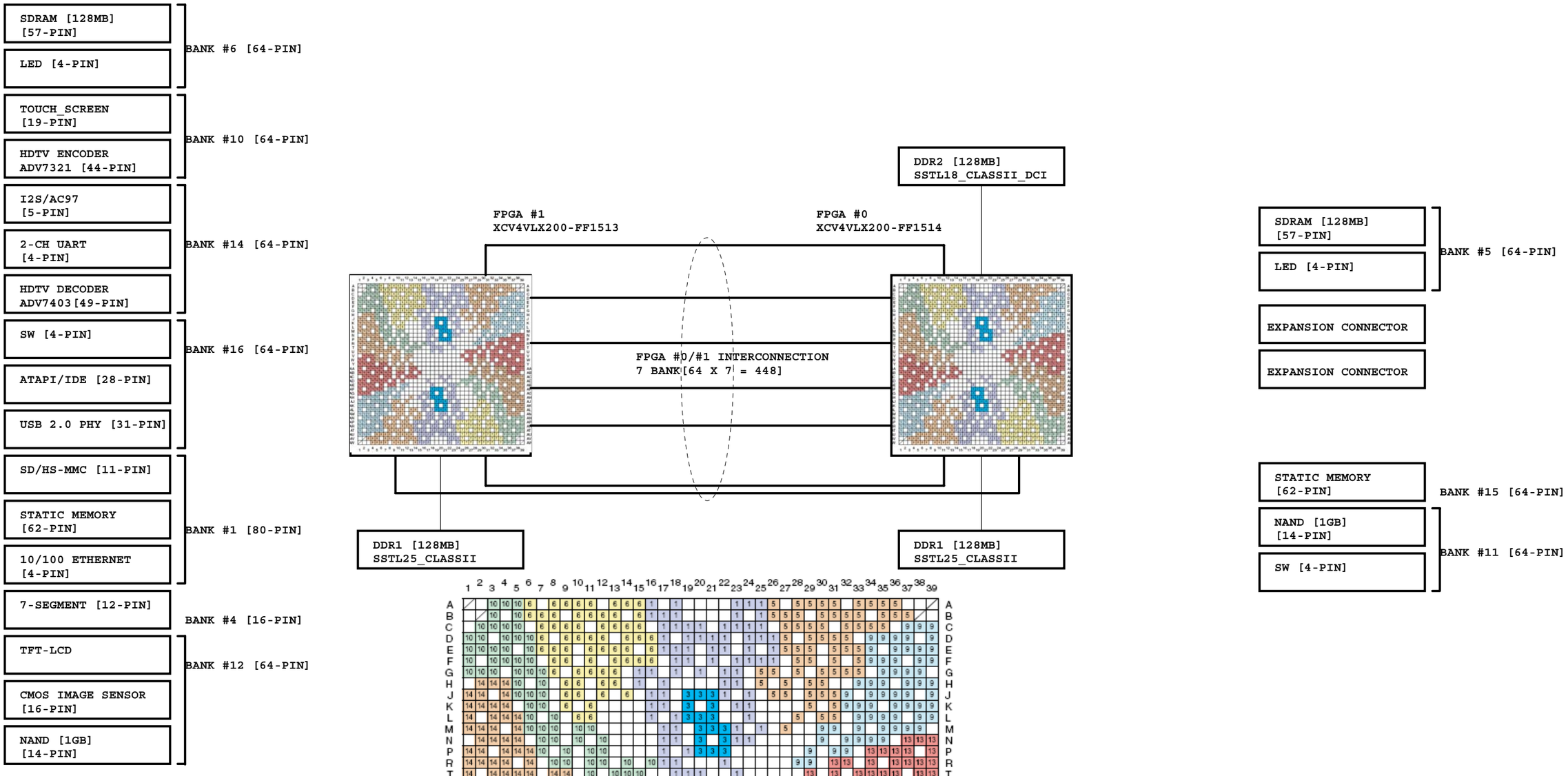
SANGHWA FPGA PLATFORM

PAGE #	DESCRIPTION
P00	TITLE PAGE (THIS)
P01	SD/MMC/TOUCH
P02	SYSTEM ACE (FPGA CONFIGURATION)
P03	NONE
P04	VIDEO
P05	MEMORY BLOCK
P06	SW/AC97
P07	ETH/USB/UART
P08	CLOCK/PLL/MULTIPLEXOR
P09	SYSTEM POWER
P10	FPGA TEST MICTOR
P11	F0 CONFIG/CLOCK
P12	F0 BANK 1/2/5/6
P13	F0 BANK 7/8/9/10
P14	F0 BANK 11/12/13/14
P15	F0 BANK 15/16/GND
P16	F0 POWER VCCO
P17	F1 CONFIG/CLOCK
P18	F1 BANK 1/2/5/7
P19	F1 BANK 7/8/9/11
P20	F1 BANK 11/12/13/15
P21	F1 BANK 15/16/GND
P22	F1 POWER VCCO

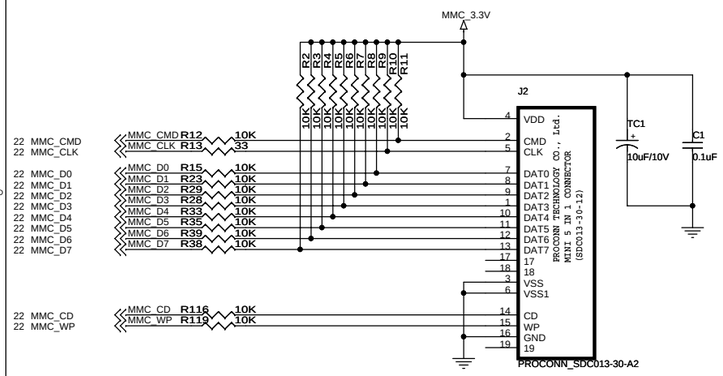
2006-7-20
DESIGNED BY DDSMURF

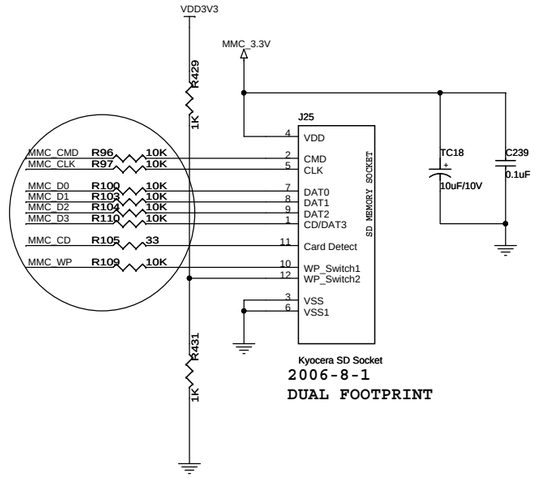
SANGHWA FPGA PLATFORM

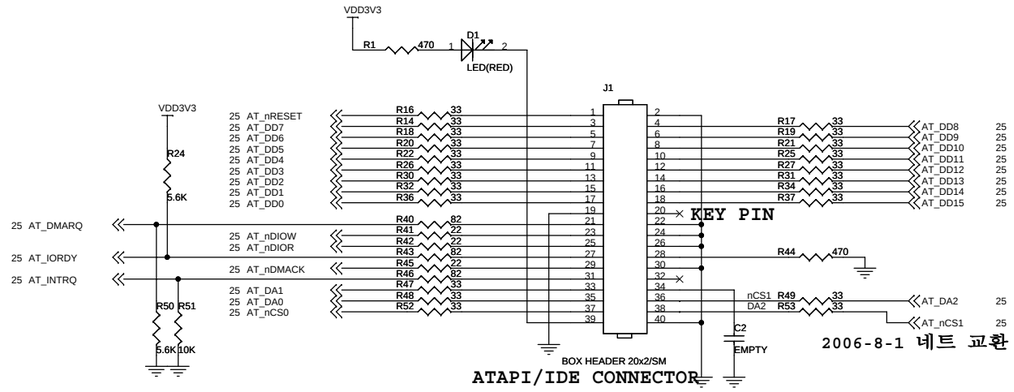
Title	SANGHWA FPGA PLATFORM	
Size A3	Document Number <Doc>	Rev 1.0
Date: Monday, August 21, 2006	Sheet 1 of 26	

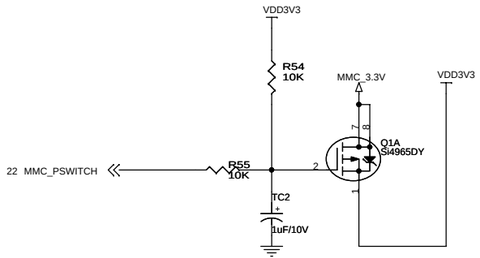


Title	SANGHWA FPGA PLATFORM PART PLACEMENT
Size A2	Document Number <Doc>
Rev 1.0	
Date: Monday, August 21, 2006	Sheet 2 of 26

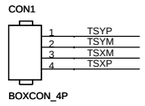




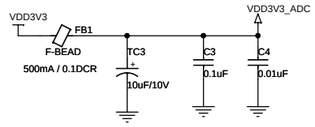


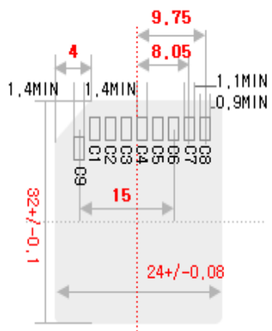


SD/HS-MMC SOCKET

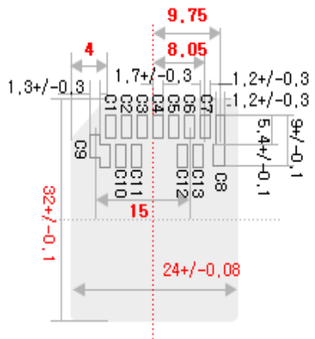


TOUCHSCREEN CONN.
MITSHMI
M60-04-30-134P

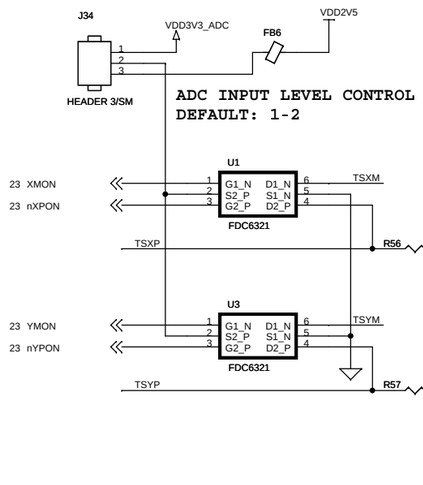


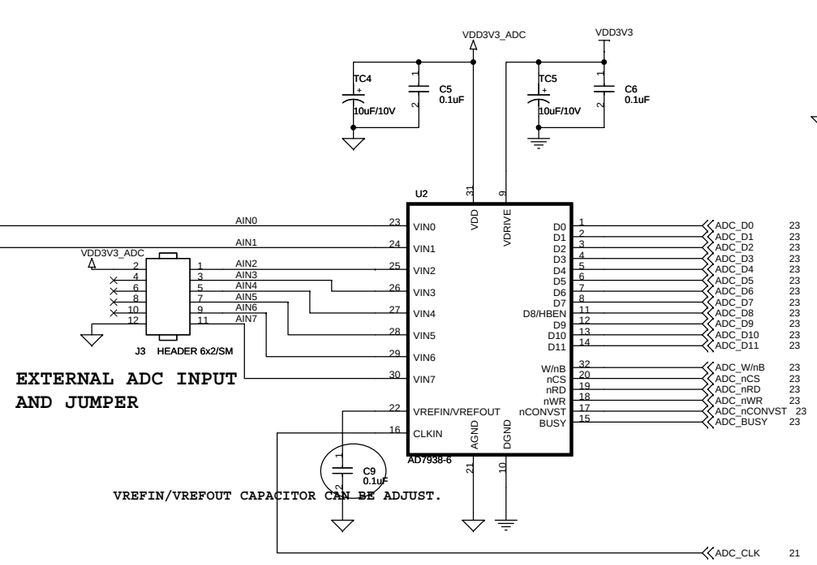


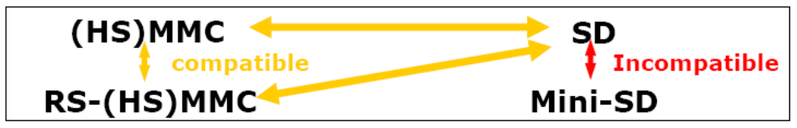
SD Card

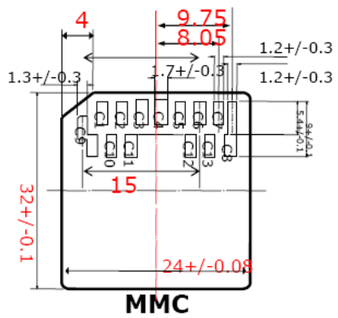


HS-MMC

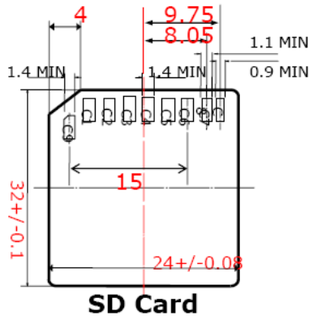








MMC



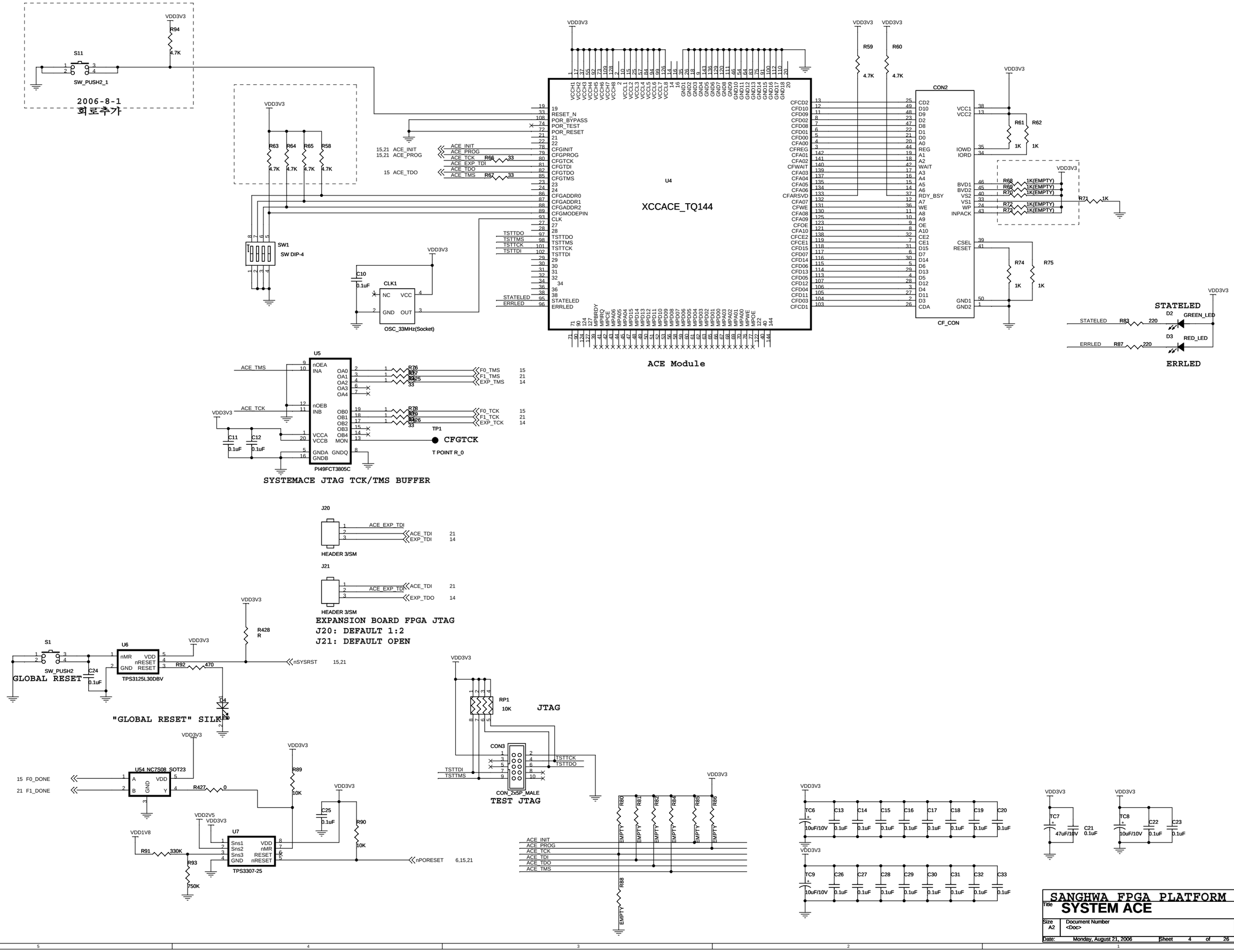
SD Card

SANGHWA FPGA PLATFORM

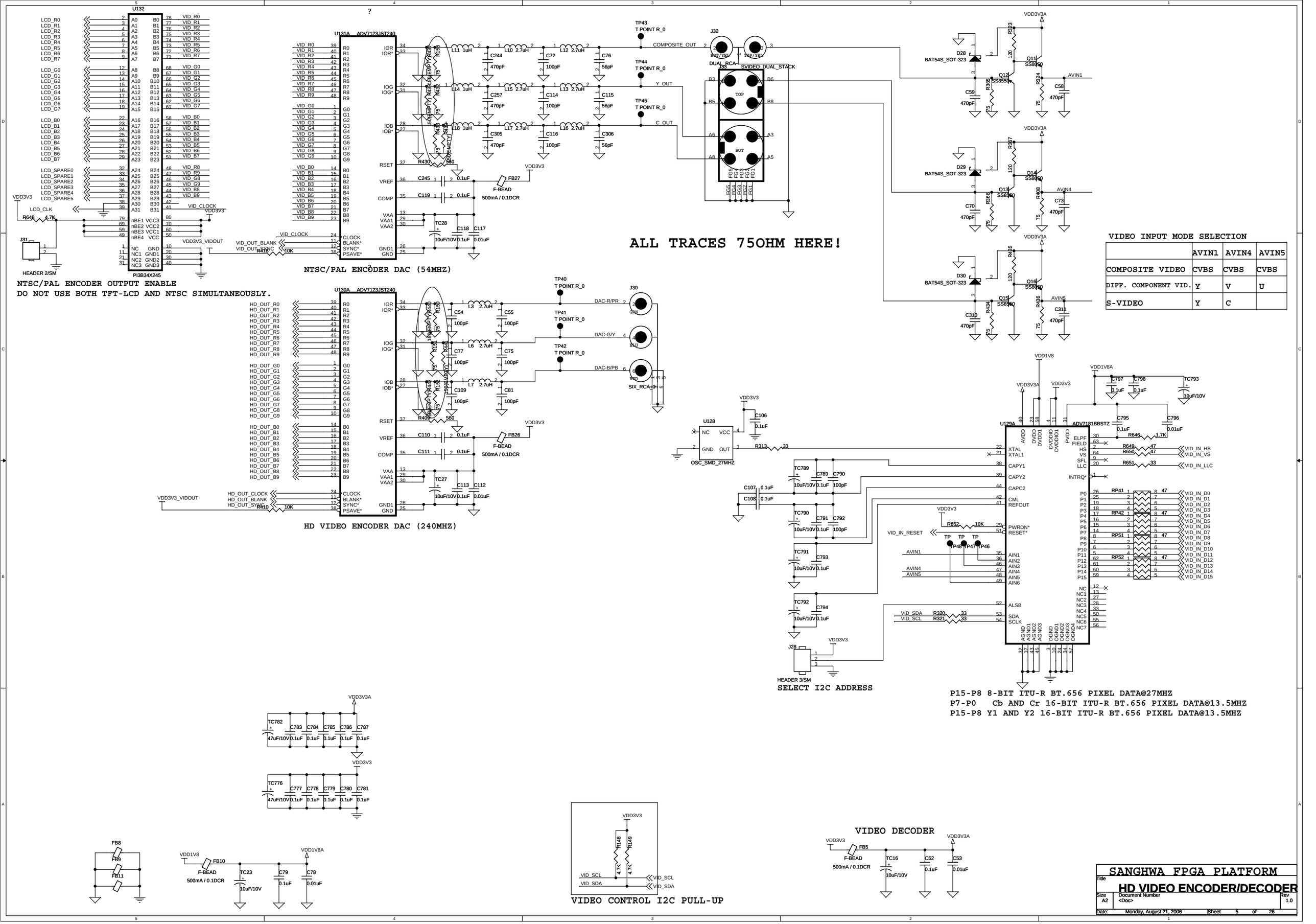
Title: SD/MMC/IDE/TOUCH SCREEN

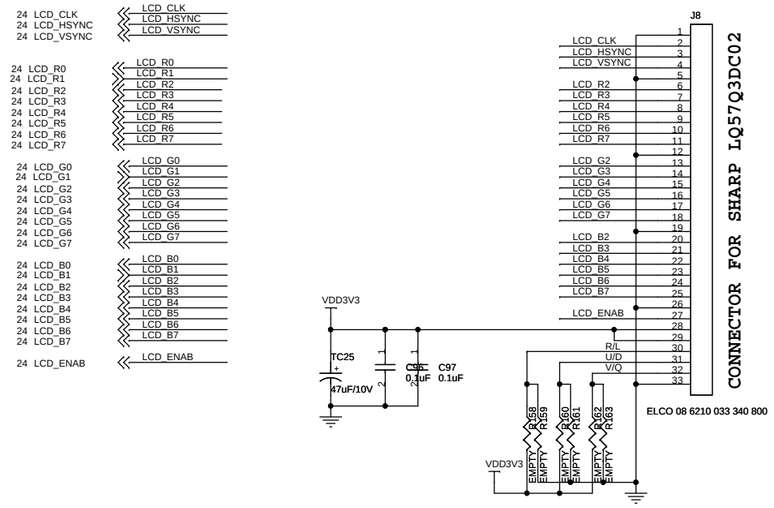
Size	Document Number	Rev
A2	<Doc>	1.0

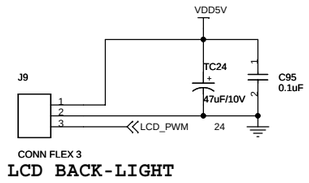
Date: Wednesday, August 16, 2006 Sheet 3 of 26



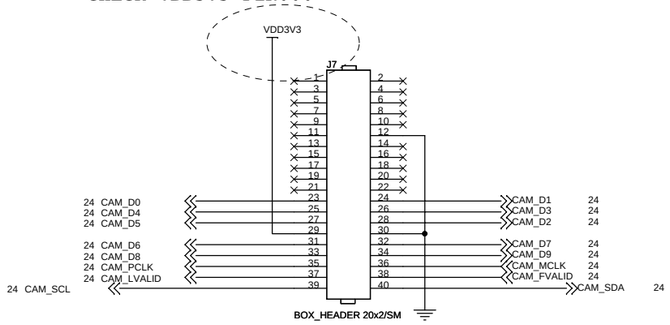
Title	SANGHWA FPGA PLATFORM SYSTEM ACE
Size A2	Document Number <Doc>
Rev	1.0
Date:	Monday, August 21, 2006
Sheet	4 of 26


U132
PI3B34X245
U131A ADV7123JST240
NTSC/PAL ENCODER DAC (54MHZ)
NTSC/PAL ENCODER OUTPUT ENABLE
DO NOT USE BOTH TFT-LCD AND NTSC SIMULTANEOUSLY.
ALL TRACES 75OHM HERE!
J32
DUAL_RCA
J33
SVIDEO_DUAL_STACK
VIDEO INPUT MODE SELECTION
U130A ADV7123JST240
HD VIDEO ENCODER DAC (240MHZ)
J30
SIX_RCA
U128
OSC_SMD_27MHZ
U129A ADV7181BBSTZ
SELECT I2C ADDRESS
P15-P8 8-BIT ITU-R BT.656 PIXEL DATA@27MHZ
P7-P0 Cb AND Cr 16-BIT ITU-R BT.656 PIXEL DATA@13.5MHZ
P15-P8 Y1 AND Y2 16-BIT ITU-R BT.656 PIXEL DATA@13.5MHZ
VIDEO DECODER
VIDEO CONTROL I2C PULL-UP
SANGHWA FPGA PLATFORM
HD VIDEO ENCODER/DECODER
Size A2
Document Number <Doc>
Rev 1.0
Date: Monday, August 21, 2006
Sheet 5 of 26



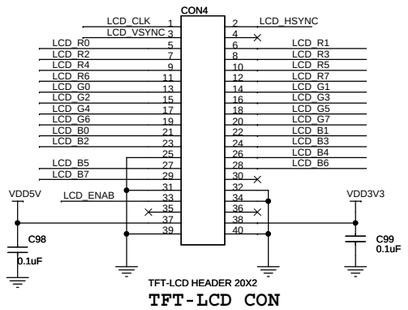


CHECK VDD3V3 PIN!!!

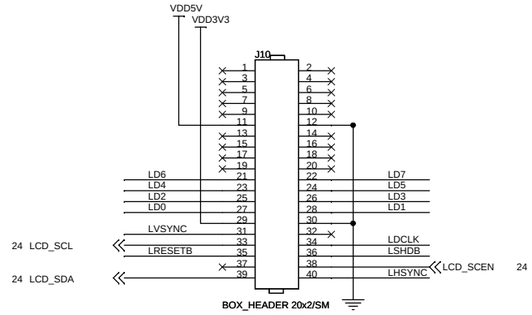


CMOS IMAGE SENSOR SOCKET

TERASIC, INC. (TRDB_DC2 BOARD)



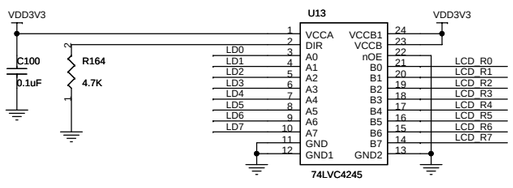
TFT-LCD CON

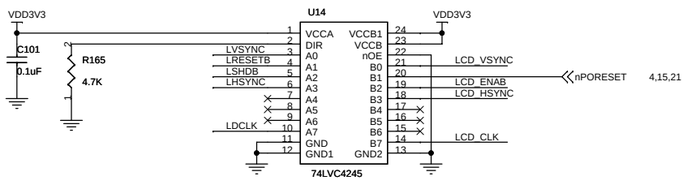


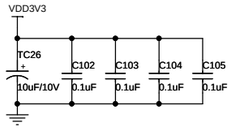
TFT-LCD CON

TERASIC, INC. (TRDB_LCM BOARD)

7-SEGMENT INTERFACE







SANGHWA FPGA PLATFORM

Title: CIS/TFT-LCD

Size	Document Number	Rev
A2	<Doc>	1.0

Date: Wednesday, August 16, 2006 Sheet 6 of 26

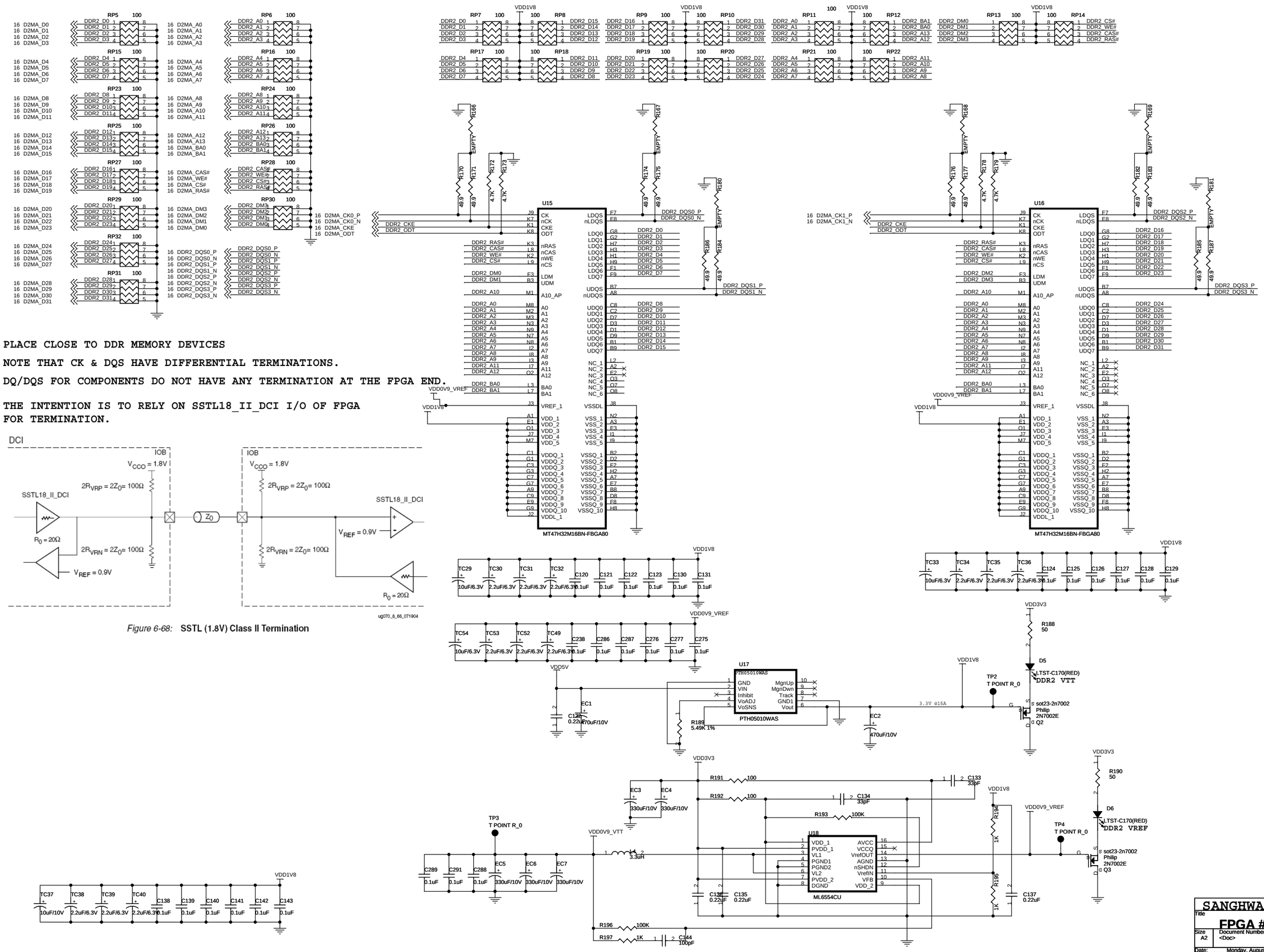


Figure 6-68: **SSTL (1.8V) Class II Termination**

PLACE CLOSE TO DDR MEMORY DEVICES

NOTE THAT CK & DQS HAVE DIFFERENTIAL TERMINATIONS.

DQ/DQS FOR COMPONENTS DO NOT HAVE ANY TERMINATION AT THE FPGA END.

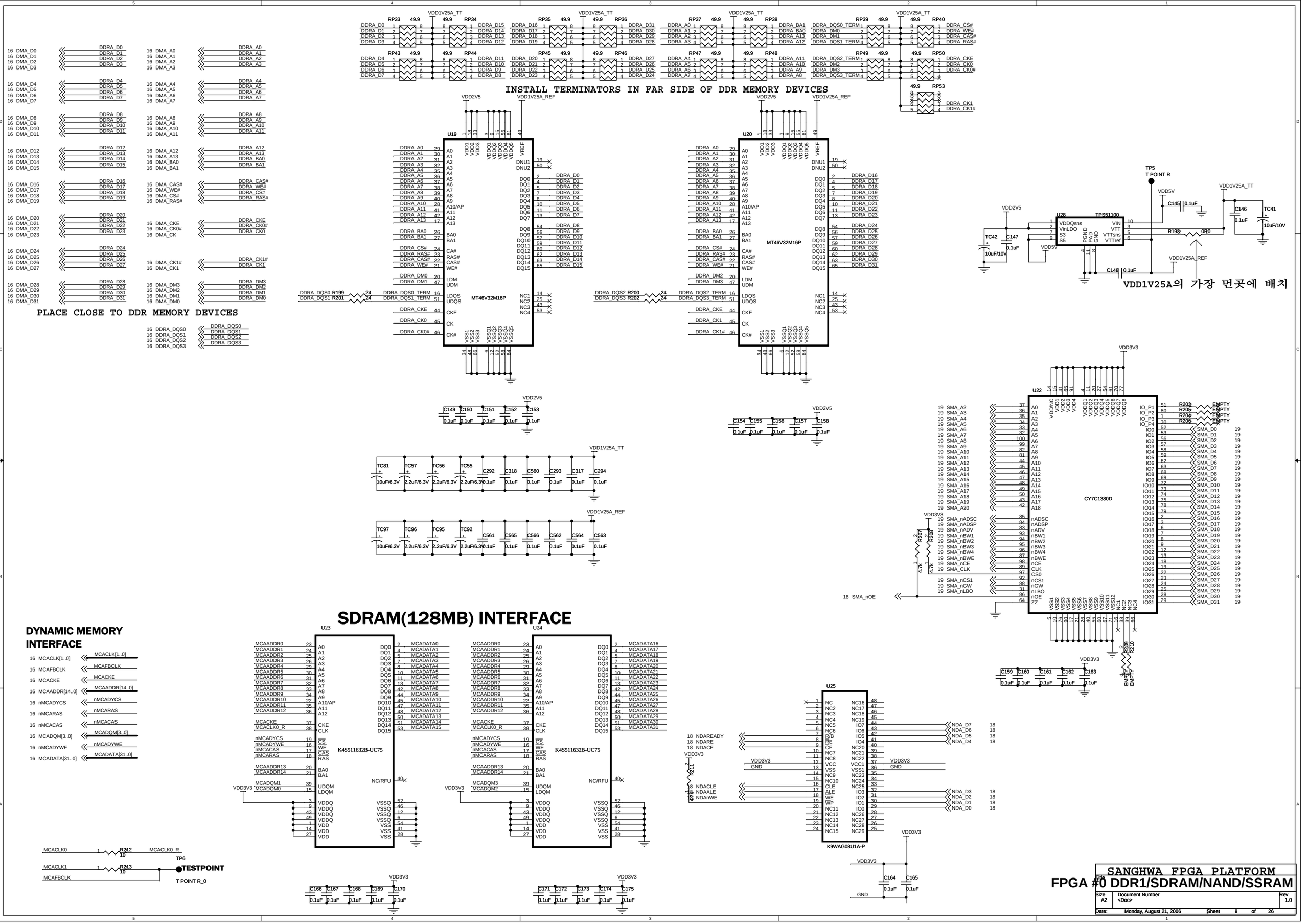
THE INTENTION IS TO RELY ON SSTL18_II_DCI I/O OF FPGA FOR TERMINATION.

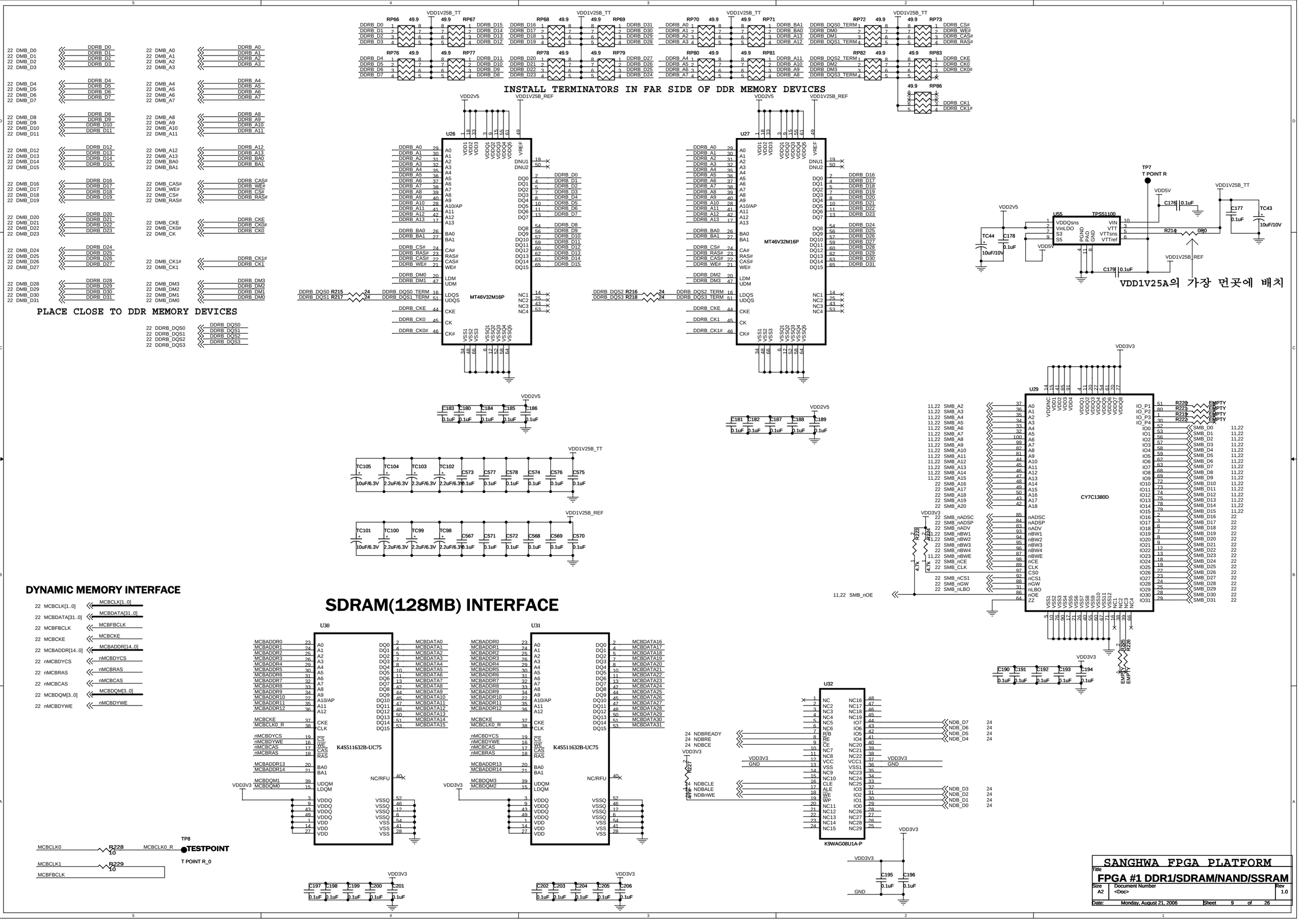
SANGHWA FPGA PLATFORM

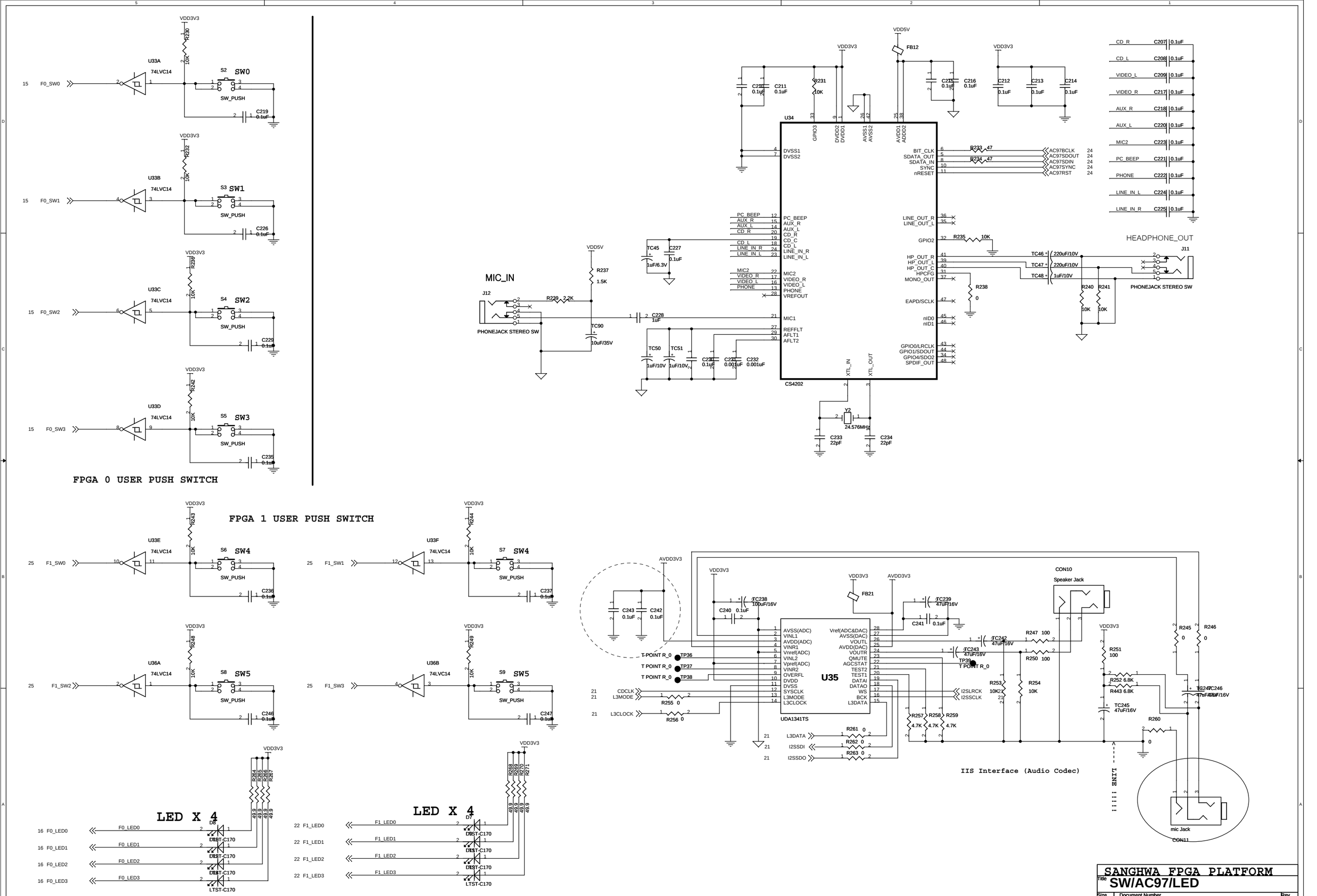
Title: **FPGA #0 DDR2 SDRAM**

Size	Document Number	Rev
A2	<Doc>	1.0

Date: Monday, August 21, 2006 Sheet 7 of 26

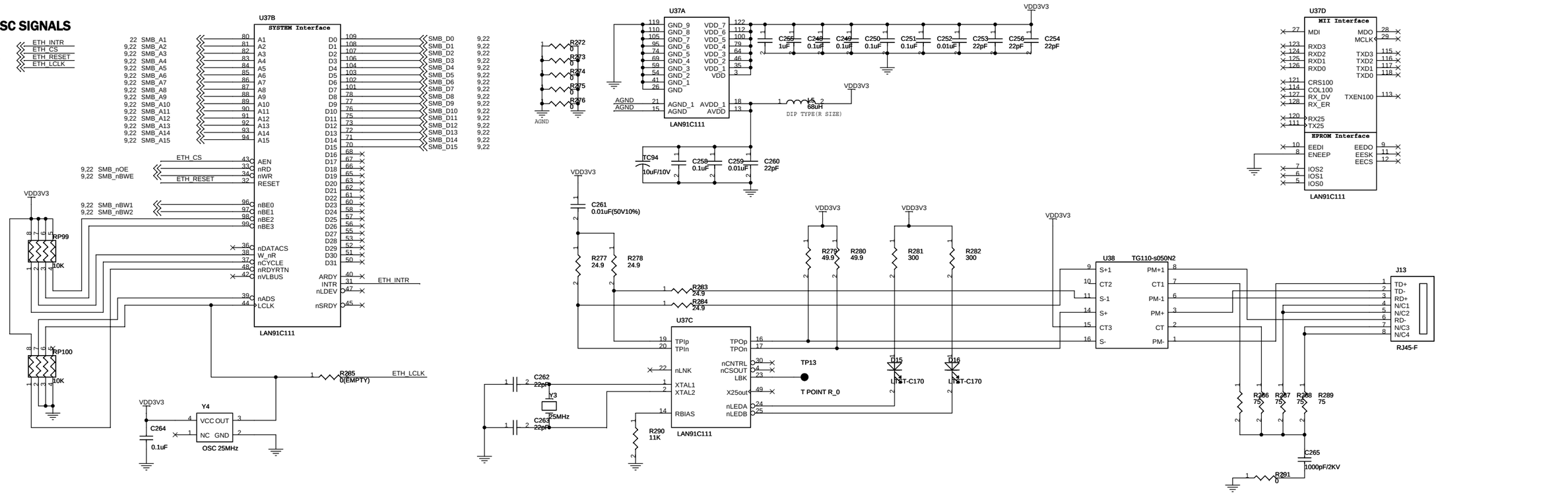

INSTALL TERMINATORS IN FAR SIDE OF DDR MEMORY DEVICES
PLACE CLOSE TO DDR MEMORY DEVICES
VDD1V25A의 가장 먼곳에 배치
SDRAM(128MB) INTERFACE
DYNAMIC MEMORY INTERFACE
U19
U20
MT46V32M16P
U28
TPS51100
U22
CY7C1380D
U23
U24
K4S511632B-UC75
U25
K9WAG08U1A-P
TESTPOINT
SANGHWA FPGA PLATFORM
FPGA #0 DDR1/SDRAM/NAND/SSRAM
Document Number
<Doc>
Rev
1.0
Monday, August 21, 2006
Sheet 8 of 26

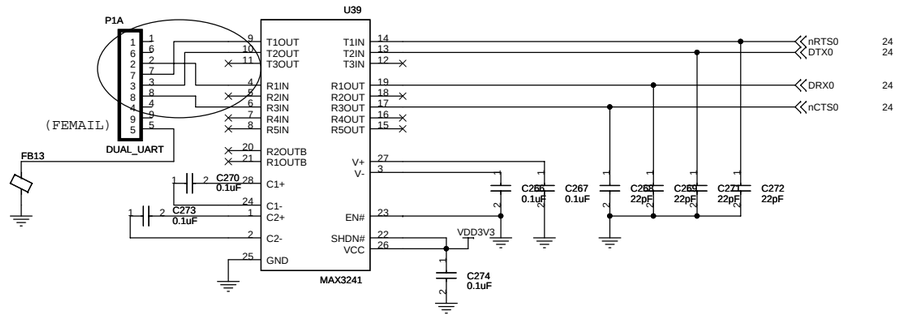

INSTALL TERMINATORS IN FAR SIDE OF DDR MEMORY DEVICES
PLACE CLOSE TO DDR MEMORY DEVICES
VDD1V25A의 가장 먼곳에 배치
DYNAMIC MEMORY INTERFACE
SDRAM(128MB) INTERFACE
U26
U27
MT46V32M16P
U29
CY7C1380D
U30
U31
K4S511632B-UC75
U32
K9WAG08U1A-P
U55
TPS51100
TP7
T POINT R
TP8
TESTPOINT
T POINT R_0
SANGHWA FPGA PLATFORM
FPGA #1 DDR1/SDRAM/NAND/SSRAM
Size A2
Document Number <Doc>
Rev 1.0
Date: Monday, August 21, 2006
Sheet 9 of 26

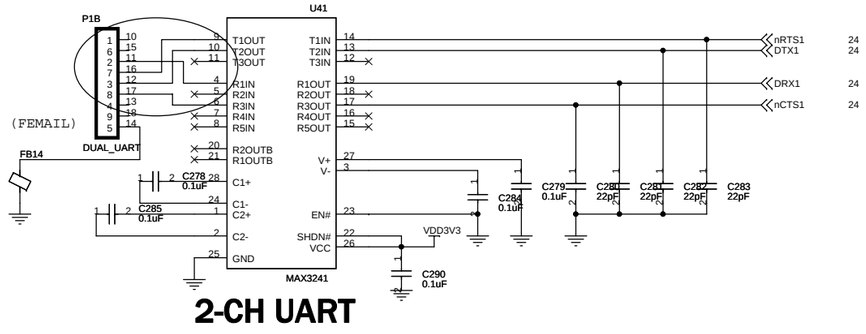


Title	SANGHWA FPGA PLATFORM SW/AC97/LED
Size A2	Document Number <Doc>
Rev	1.0
Date: Monday, August 21, 2006	Sheet 10 of 26

ETH MISC SIGNALS

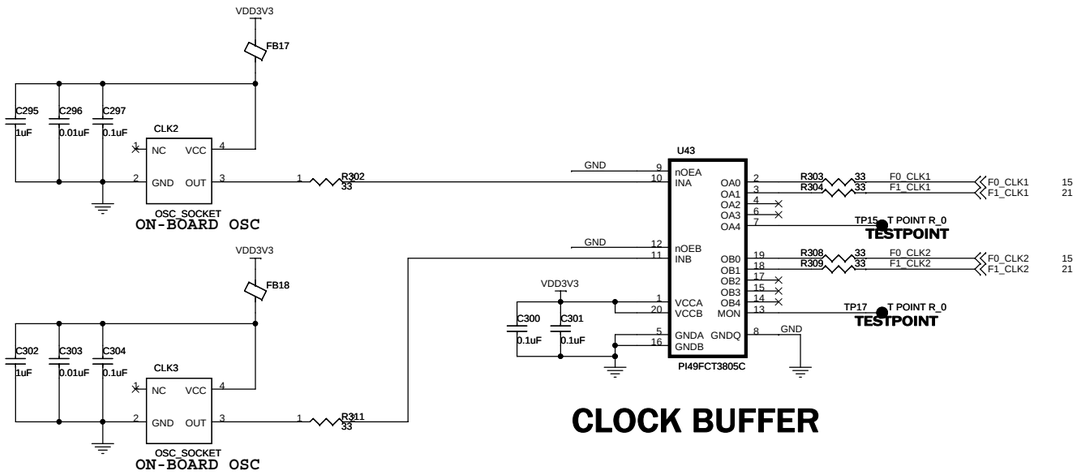


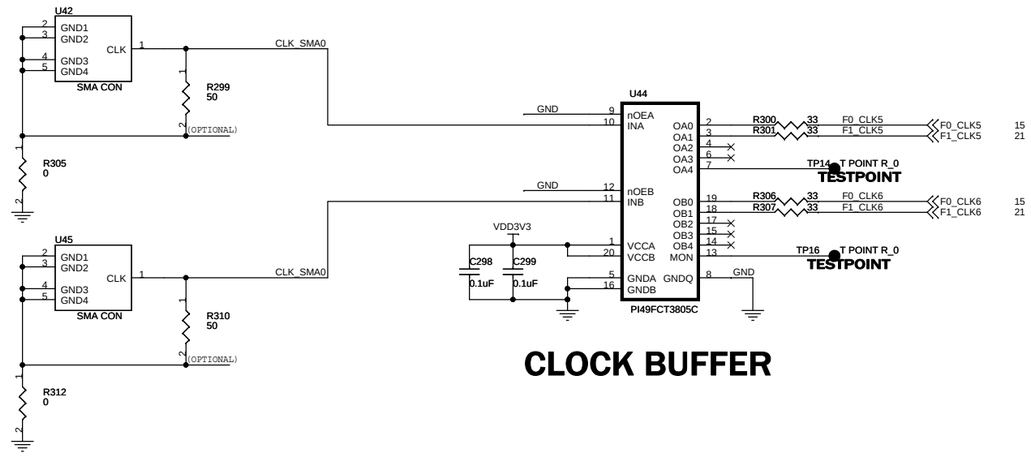


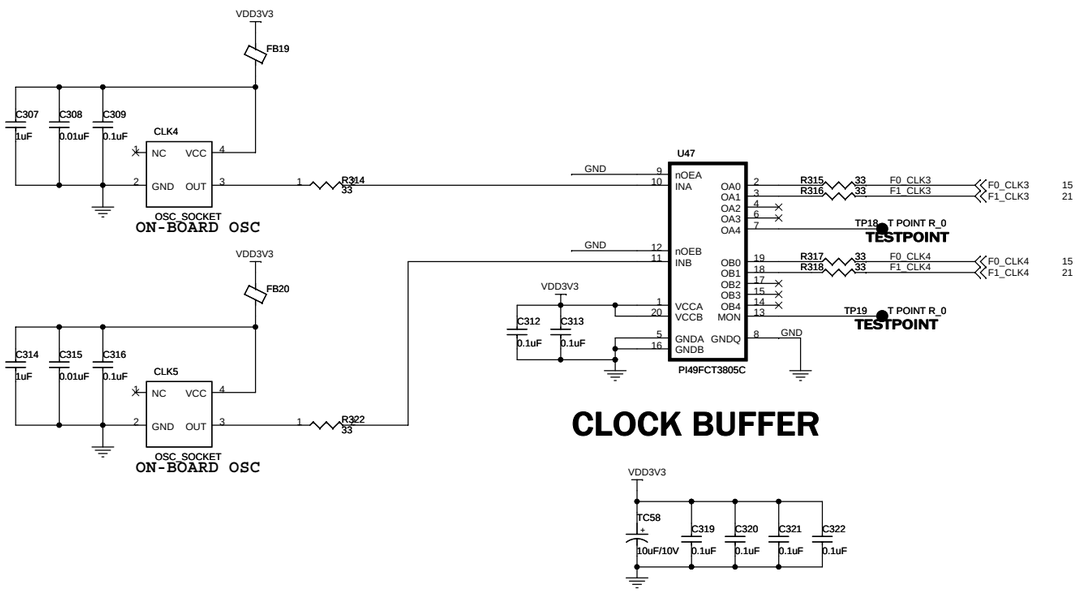


2-CH UART

SANGHWA FPGA PLATFORM		
Title: ETH/USB/UART		
Size: A2	Document Number: <Doc>	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 11 of 26	





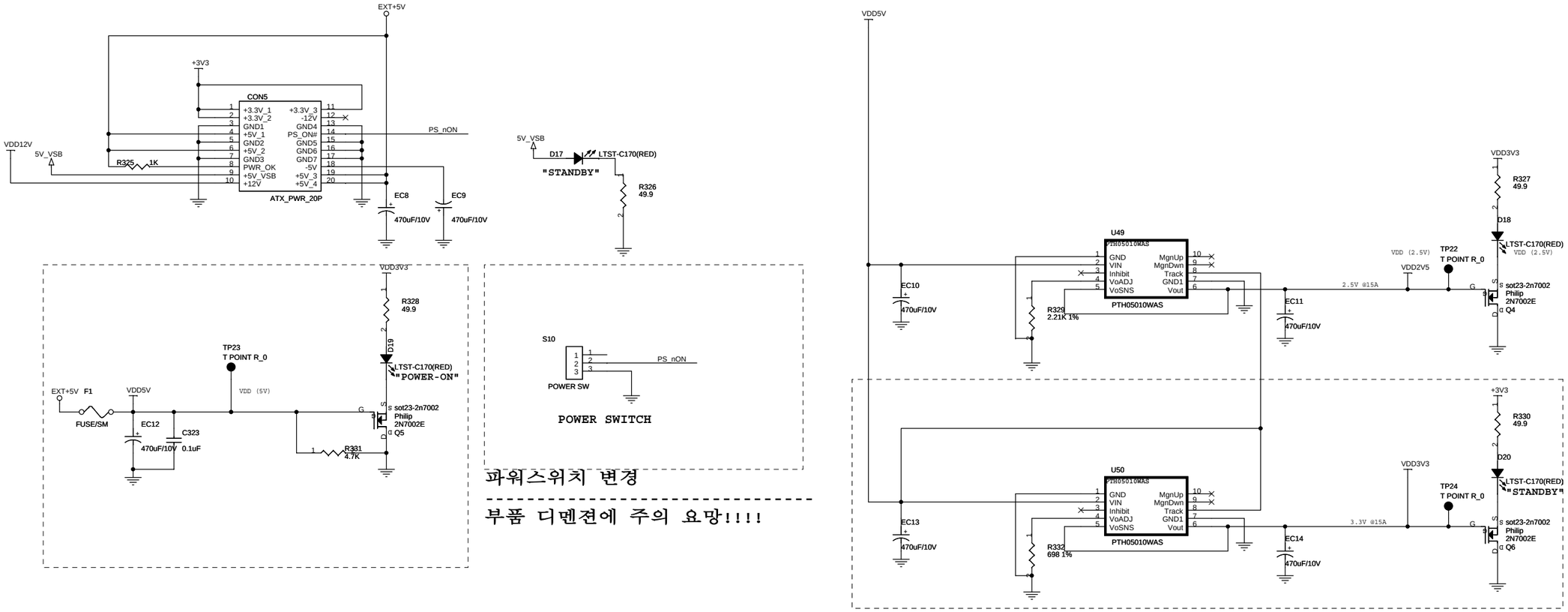


SANGHWA FPGA PLATFORM

Title **CLOCK/PLL/MULTIPLEXOR**

Size	Document Number	Rev
A2	<Doc>	1.0

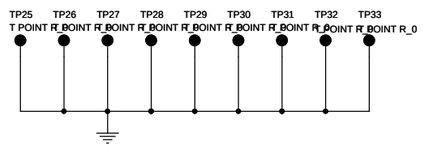
Date: Monday, August 21, 2006 Sheet 12 of 26



파워스위치 변경

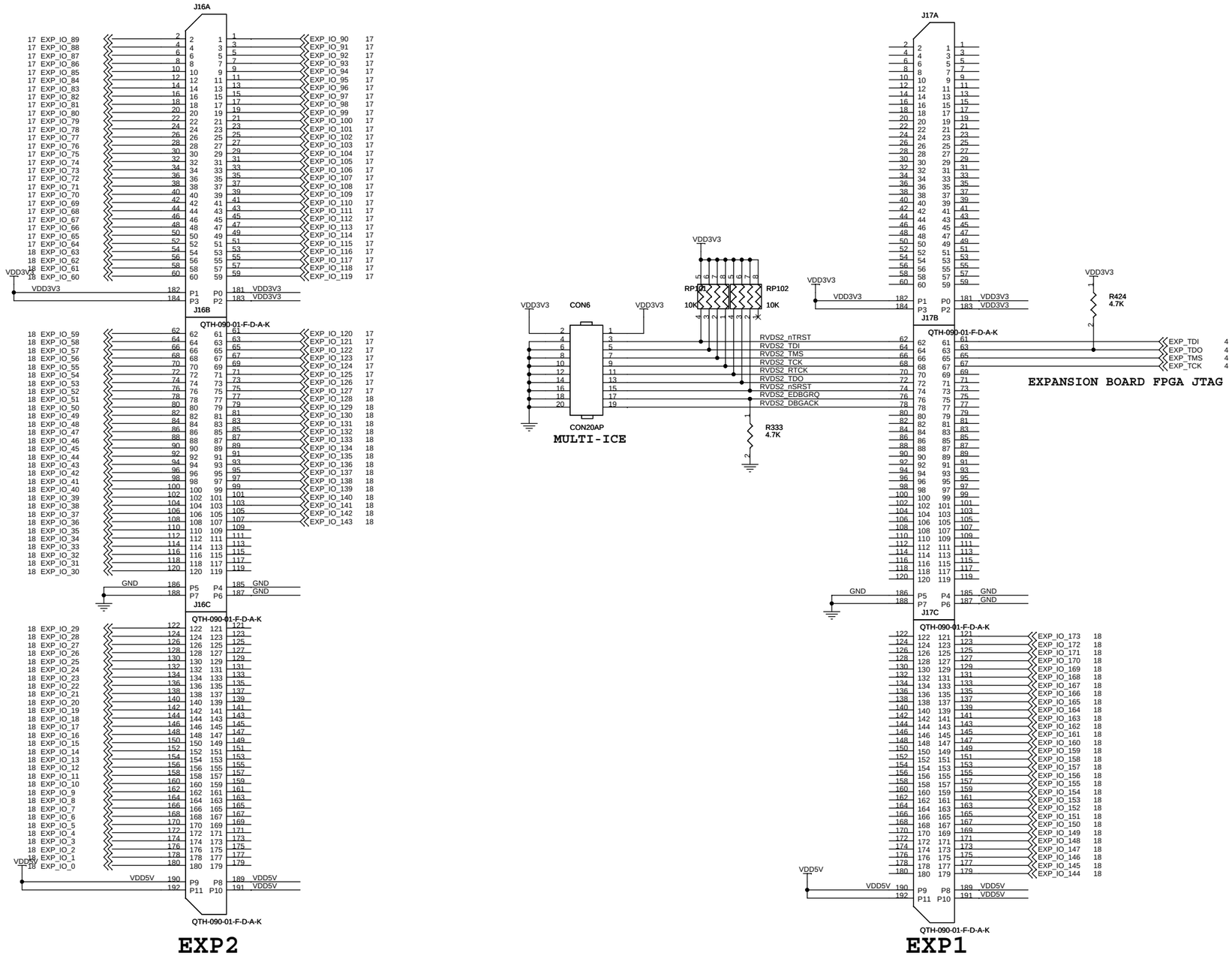
부품 디멘젼에 주의 요망!!!!

GND Point

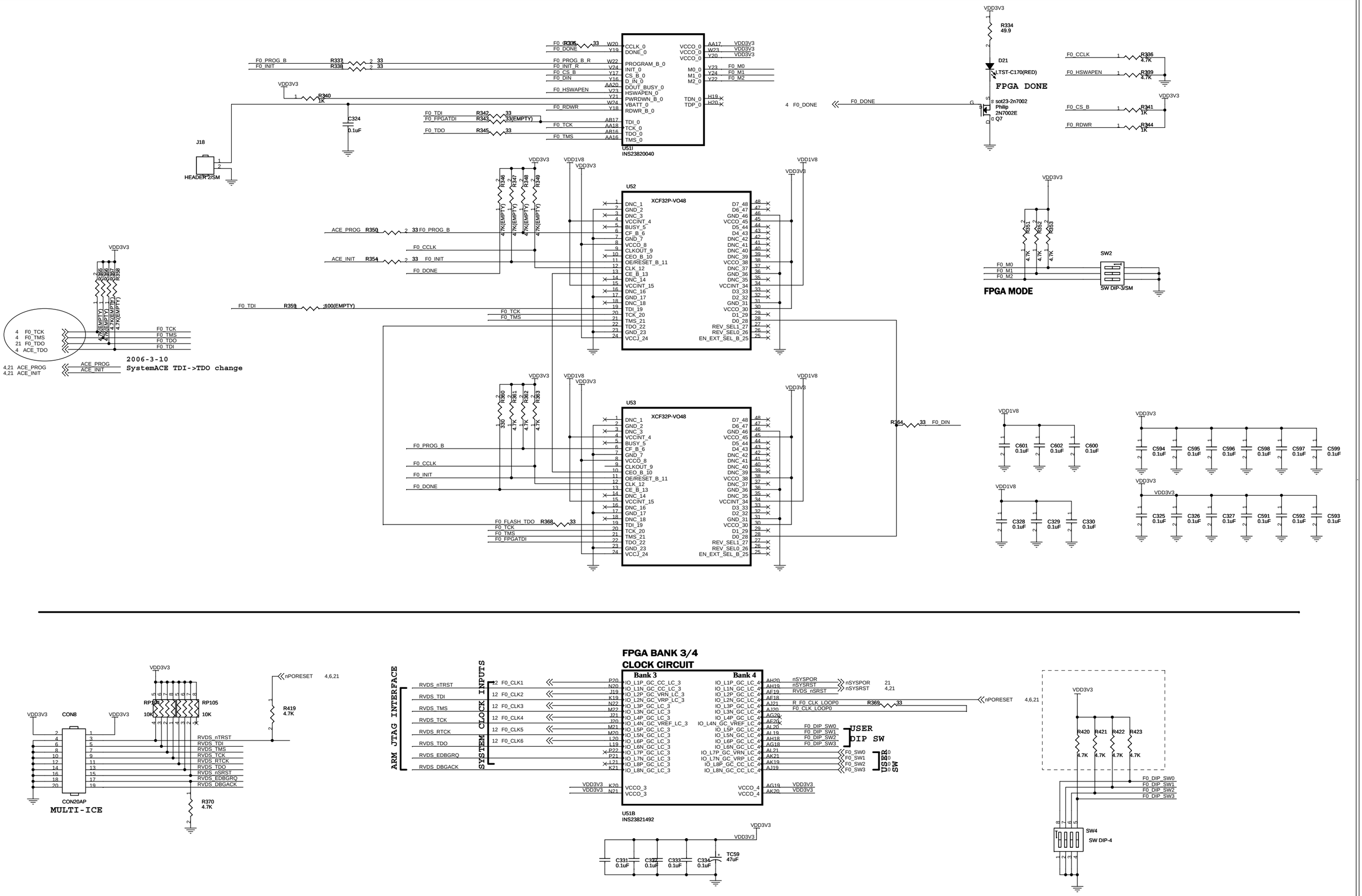


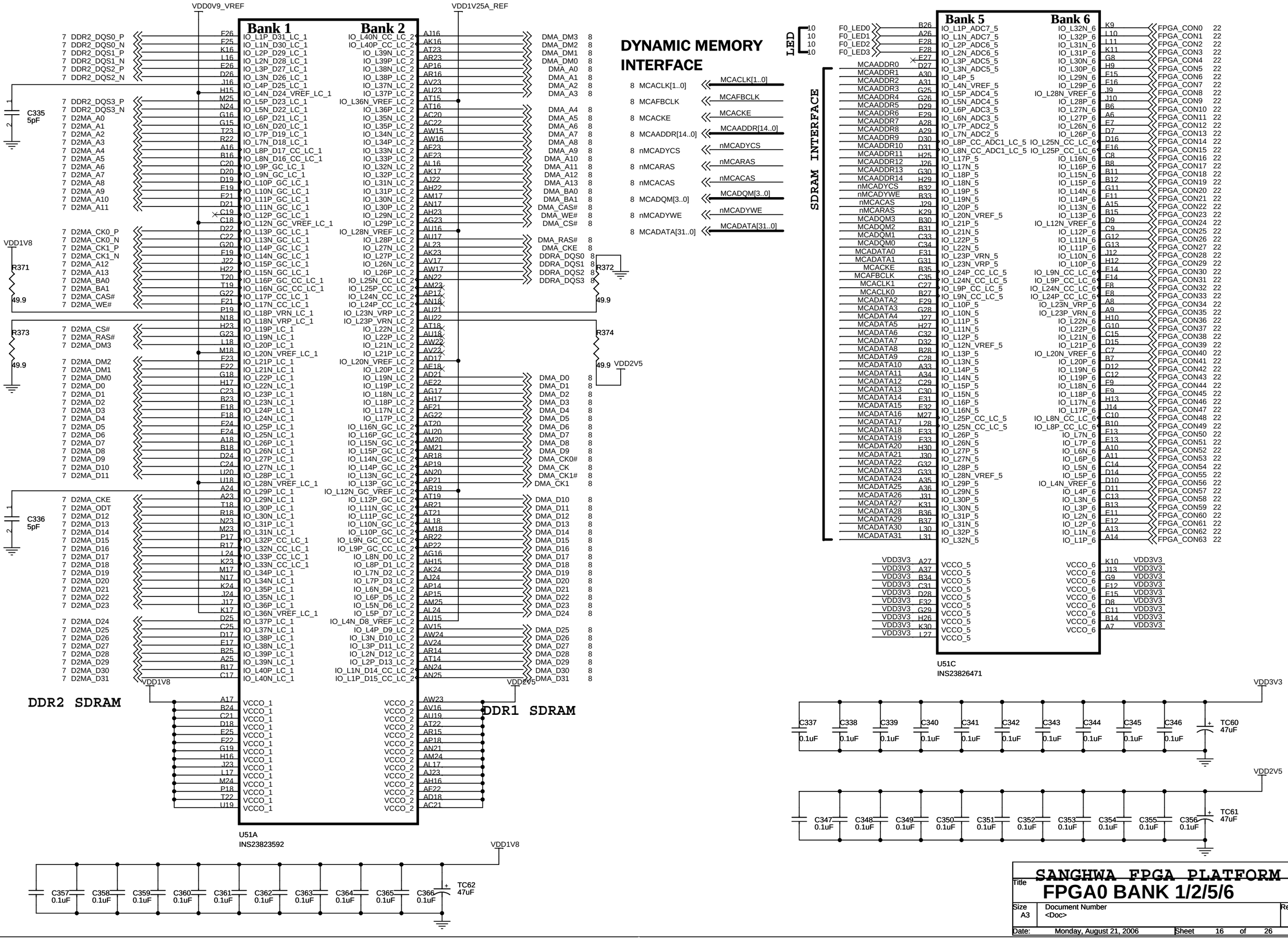
Title	SANGHWA FPGA PLATFORM SYSTEM POWER	
Size A2	Document Number <Doc>	Rev 1.0
Date: Monday, August 21, 2006	Sheet 13 of 26	

EXPANSION SLOT FOR FPGA #0



SANGHWA FPGA PLATFORM	
Title	FPGA #0 EXPANSION CONNECTOR
Size A2	Document Number <Doc>
Rev	1.0
Date: Monday, August 21, 2006	Sheet 14 of 26


U51I
INS23820040
U52
XCF32P-VO48
U53
XCF32P-VO48
J18
HEADER 2/SM
FPGA DONE
D21
LTST-C170(RED)
Q7
2N7002E
FPGA MODE
SW2
SW DIP-3/SM
2006-3-10
SystemACE TDI->TDO change
CON8
CON20AP
MULTI-ICE
FPGA BANK 3/4
CLOCK CIRCUIT
Bank 3
Bank 4
U51B
INS23821492
ARM JTAG INTERFACE
SYSTEM CLOCK INPUTS
USER DIP SW
SW4
SW DIP-4
SANGHWA FPGA PLATFORM
FPGA0 CONFIG/CLOCK
Size A2
Document Number <Doc>
Rev 1.0
Date: Monday, August 21, 2006
Sheet 15 of 26


DYNAMIC MEMORY INTERFACE
Bank 1
Bank 2
Bank 5
Bank 6
SDRAM INTERFACE
LED
DDR2 SDRAM
DDR1 SDRAM
U51A
INS23823592
U51C
INS23826471
VDD0V9_VREF
VDD1V25A_REF
VDD1V8
VDD2V5
VDD3V3
C335 5pF
C336 5pF
R371 49.9
R372 49.9
R373 49.9
R374 49.9
TC60 47uF
TC61 47uF
TC62 47uF
SANGHWA FPGA PLATFORM
FPGA0 BANK 1/2/5/6
Title
Size A3
Document Number <Doc>
Rev 1.0
Date: Monday, August 21, 2006
Sheet 16 of 26

FPGA INTERCONNECTION

Bank 7 / Bank 8

23	FPGA_CON384	AT33	IO_L1P_7	IO_L32N_8	AW10	FPGA_CON320	23
23	FPGA_CON385	AR33	IO_L1N_7	IO_L32P_8	AW11	FPGA_CON321	23
23	FPGA_CON386	AJ30	IO_L2P_7	IO_L31N_8	AV14	FPGA_CON322	23
23	FPGA_CON387	AK31	IO_L2N_7	IO_L31P_8	AW14	FPGA_CON323	23
23	FPGA_CON388	AM30	IO_L3P_7	IO_L30N_8	AU10	FPGA_CON324	23
23	FPGA_CON389	AL30	IO_L3N_7	IO_L30P_8	AV10	FPGA_CON325	23
23	FPGA_CON390	AM31	IO_L4P_7	IO_L29N_8	AR13	FPGA_CON326	23
23	FPGA_CON391	AL31	IO_L4N_VREF_7	IO_L29P_8	AT13	FPGA_CON327	23
23	FPGA_CON392	AP24	IO_L5P_7	IO_L28N_VREF_8	AR11	FPGA_CON328	23
23	FPGA_CON393	AR24	IO_L5N_7	IO_L28P_8	AT11	FPGA_CON329	23
23	FPGA_CON394	AP32	IO_L6P_7	IO_L27N_8	AM13	FPGA_CON330	23
23	FPGA_CON395	AN32	IO_L6N_7	IO_L27P_8	AN14	FPGA_CON331	23
23	FPGA_CON396	AN30	IO_L7P_7	IO_L26N_8	AV9	FPGA_CON332	23
23	FPGA_CON397	AP31	IO_L7N_7	IO_L26P_8	AW9	FPGA_CON333	23
23	FPGA_CON398	AK29	IO_L8P_CC_LC_7	IO_L25N_CC_LC_8	AV12	FPGA_CON334	23
23	FPGA_CON399	AJ29	IO_L8N_CC_LC_7	IO_L25P_CC_LC_8	AW12	FPGA_CON335	23
23	FPGA_CON400	AT24	IO_L9P_CC_LC_7	IO_L24N_CC_LC_8	AV7	FPGA_CON336	23
23	FPGA_CON401	AT25	IO_L9N_CC_LC_7	IO_L24P_CC_LC_8	AV8	FPGA_CON337	23
23	FPGA_CON402	AW34	IO_L10P_7	IO_L23N_VRP_8	AU11	FPGA_CON338	23
23	FPGA_CON403	AV34	IO_L10N_7	IO_L23P_VRN_8	AU12	FPGA_CON339	23
23	FPGA_CON404	AW30	IO_L11P_7	IO_L22N_8	AT9	FPGA_CON340	23
23	FPGA_CON405	AW31	IO_L11N_7	IO_L22P_8	AT10	FPGA_CON341	23
23	FPGA_CON406	AV33	IO_L12P_7	IO_L21N_8	AU13	FPGA_CON342	23
23	FPGA_CON407	AU33	IO_L12N_VREF_7	IO_L21P_8	AV13	FPGA_CON343	23
23	FPGA_CON408	AP25	IO_L13P_7	IO_L20N_VREF_8	AP9	FPGA_CON344	23
23	FPGA_CON409	AP26	IO_L13N_7	IO_L20P_8	AR9	FPGA_CON345	23
23	FPGA_CON410	AT31	IO_L14P_7	IO_L19N_8	AP12	FPGA_CON346	23
23	FPGA_CON411	AT30	IO_L14N_7	IO_L19P_8	AR12	FPGA_CON347	23
23	FPGA_CON412	AU25	IO_L15P_7	IO_L18N_8	AT8	FPGA_CON348	23
23	FPGA_CON413	AV25	IO_L15N_7	IO_L18P_8	AU8	FPGA_CON349	23
23	FPGA_CON414	AR31	IO_L16P_7	IO_L17N_8	AL13	FPGA_CON350	23
23	FPGA_CON415	AR32	IO_L16N_7	IO_L17P_8	AL14	FPGA_CON351	23
23	FPGA_CON416	AL26	IO_L17P_7	IO_L16N_8	AU6	FPGA_CON352	23
23	FPGA_CON417	AM27	IO_L17N_7	IO_L16P_8	AU7	FPGA_CON353	23
23	FPGA_CON418	AU31	IO_L18P_7	IO_L15N_8	AP11	FPGA_CON354	23
23	FPGA_CON419	AU32	IO_L18N_7	IO_L15P_8	AN12	FPGA_CON355	23
23	FPGA_CON420	AV28	IO_L19P_7	IO_L14N_8	AJ12	FPGA_CON356	23
23	FPGA_CON421	AU28	IO_L19N_7	IO_L14P_8	AH13	FPGA_CON357	23
23	FPGA_CON422	AW32	IO_L20P_7	IO_L13N_8	AN10	FPGA_CON358	23
23	FPGA_CON423	AV32	IO_L20N_VREF_7	IO_L13P_8	AM11	FPGA_CON359	23
23	FPGA_CON424	AW25	IO_L21P_7	IO_L12N_VREF_8	AL10	FPGA_CON360	23
23	FPGA_CON425	AW26	IO_L21N_7	IO_L12P_8	AM10	FPGA_CON361	23
23	FPGA_CON426	AP29	IO_L22P_7	IO_L11N_8	AW6	FPGA_CON362	23
23	FPGA_CON427	AN29	IO_L22N_7	IO_L11P_8	AW7	FPGA_CON363	23
23	FPGA_CON428	AN27	IO_L23P_VRN_7	IO_L10N_8	AW4	FPGA_CON364	23
23	FPGA_CON429	AN28	IO_L23N_VRP_7	IO_L10P_8	AW5	FPGA_CON365	23
23	FPGA_CON430	AL28	IO_L24P_CC_LC_7	IO_L9N_CC_LC_8	AK11	FPGA_CON366	23
23	FPGA_CON431	AM28	IO_L24N_CC_LC_7	IO_L9P_CC_LC_8	AL11	FPGA_CON367	23
23	FPGA_CON432	AP27	IO_L25P_CC_SM7_LC_7	IO_L8N_CC_LC_8	AV3	FPGA_CON368	23
23	FPGA_CON433	AR27	IO_L25N_CC_SM7_LC_7	IO_L8P_CC_LC_8	AV4	FPGA_CON369	23
23	FPGA_CON434	AV30	IO_L26P_SM6_7	IO_L7N_8	AR7	FPGA_CON370	23
23	FPGA_CON435	AU30	IO_L26N_SM6_7	IO_L7P_8	AR8	FPGA_CON371	23
23	FPGA_CON436	AR26	IO_L27P_SM5_7	IO_L6N_8	AN7	FPGA_CON372	23
23	FPGA_CON437	AT26	IO_L27N_SM5_7	IO_L6P_8	AP7	FPGA_CON373	23
23	FPGA_CON438	AW29	IO_L28P_7	IO_L5N_8	AN15	FPGA_CON374	23
23	FPGA_CON439	AV29	IO_L28N_VREF_7	IO_L5P_8	AM15	FPGA_CON375	23
23	FPGA_CON440	AV27	IO_L29P_SM4_7	IO_L4N_VREF_8	AK9	FPGA_CON376	23
23	FPGA_CON441	AW27	IO_L29N_SM4_7	IO_L4P_8	AL9	FPGA_CON377	23
23	FPGA_CON442	AT29	IO_L30P_SM3_7	IO_L3N_8	AN8	FPGA_CON378	23
23	FPGA_CON443	AR29	IO_L30N_SM3_7	IO_L3P_8	AN9	FPGA_CON379	23
23	FPGA_CON444	AU26	IO_L31P_SM2_7	IO_L2N_8	AJ9	FPGA_CON380	23
23	FPGA_CON445	AU27	IO_L31N_SM2_7	IO_L2P_8	AJ10	FPGA_CON381	23
23	FPGA_CON446	AT28	IO_L32P_SM1_7	IO_L1N_8	AU5	FPGA_CON382	23
23	FPGA_CON447	AR28	IO_L32N_SM1_7	IO_L1P_8	AV5	FPGA_CON383	23

VDD3V3	AK30	VCCO_7	VCCO_8	AW3	VDD3V3
VDD3V3	AL27	VCCO_7	VCCO_8	AW13	VDD3V3
VDD3V3	AN31	VCCO_7	VCCO_8	AV6	VDD3V3
VDD3V3	AP28	VCCO_7	VCCO_8	AU9	VDD3V3
VDD3V3	AR25	VCCO_7	VCCO_8	AT12	VDD3V3
VDD3V3	AT32	VCCO_7	VCCO_8	AP8	VDD3V3
VDD3V3	AU29	VCCO_7	VCCO_8	AN11	VDD3V3
VDD3V3	AV26	VCCO_7	VCCO_8	AM14	VDD3V3
VDD3V3	AW33	VCCO_7	VCCO_8	AK10	VDD3V3
			VCCO_8	AJ13	VDD3V3

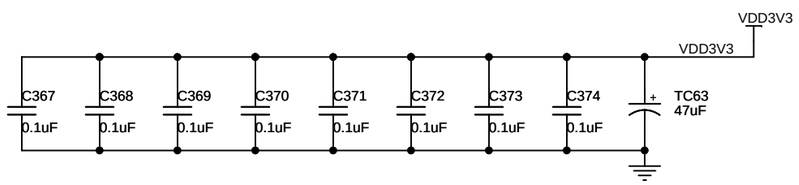
U51D
INS23832289

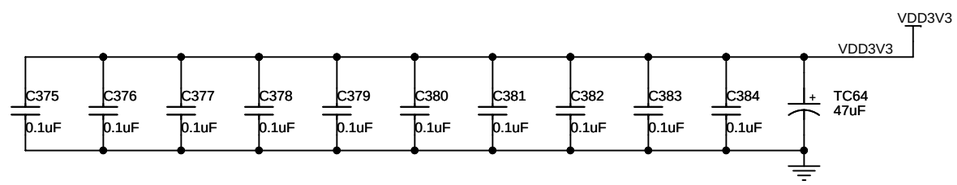
Bank 9 / Bank 10

14	EXP_IO_64	D34	IO_L1P_9	IO_L32N_10	T11	FPGA_CON64	23
14	EXP_IO_65	D35	IO_L1N_9	IO_L32P_10	U12	FPGA_CON65	23
14	EXP_IO_66	C37	IO_L2P_9	IO_L31N_10	R8	FPGA_CON66	23
14	EXP_IO_67	C38	IO_L2N_9	IO_L31P_10	R9	FPGA_CON67	23
14	EXP_IO_68	E34	IO_L3P_9	IO_L30N_10	P7	FPGA_CON68	23
14	EXP_IO_69	E34	IO_L3N_9	IO_L30P_10	N7	FPGA_CON69	23
14	EXP_IO_70	E35	IO_L4P_9	IO_L29N_10	M6	FPGA_CON70	23
14	EXP_IO_71	G35	IO_L4N_VREF_9	IO_L29P_10	L6	FPGA_CON71	23
14	EXP_IO_72	D36	IO_L5P_9	IO_L28N_VREF_10	N8	FPGA_CON72	23
14	EXP_IO_73	D37	IO_L5N_9	IO_L28P_10	P9	FPGA_CON73	23
14	EXP_IO_74	H33	IO_L6P_9	IO_L27N_10	M7	FPGA_CON74	23
14	EXP_IO_75	H34	IO_L6N_9	IO_L27P_10	M8	FPGA_CON75	23
14	EXP_IO_76	E36	IO_L7P_9	IO_L26N_10	U13	FPGA_CON76	23
14	EXP_IO_77	E36	IO_L7N_9	IO_L26P_10	T13	FPGA_CON77	23
14	EXP_IO_78	C39	IO_L8P_CC_LC_9	IO_L25N_CC_LC_10	R11	FPGA_CON78	23
14	EXP_IO_79	D39	IO_L8N_CC_LC_9	IO_L25P_CC_LC_10	P11	FPGA_CON79	23
14	EXP_IO_80	J32	IO_L9P_CC_LC_9	IO_L24N_CC_LC_10	G1	FPGA_CON80	23
14	EXP_IO_81	K32	IO_L9N_CC_LC_9	IO_L24P_CC_LC_10	F1	FPGA_CON81	23
14	EXP_IO_82	G36	IO_L10P_9	IO_L23N_VRP_10	K6	FPGA_CON82	23
14	EXP_IO_83	G37	IO_L10N_9	IO_L23P_VRN_10	J6	FPGA_CON83	23
14	EXP_IO_84	E37	IO_L11P_9	IO_L22N_10	G2	FPGA_CON84	23
14	EXP_IO_85	E38	IO_L11N_9	IO_L22P_10	G3	FPGA_CON85	23
14	EXP_IO_86	H35	IO_L12P_9	IO_L21N_10	J5	FPGA_CON86	23
14	EXP_IO_87	J35	IO_L12N_VREF_9	IO_L21P_10	H5	FPGA_CON87	23
14	EXP_IO_88	M30	IO_L13P_9	IO_L20N_VREF_10	L8	FPGA_CON88	23
14	EXP_IO_89	M31	IO_L13N_9	IO_L20P_10	K7	FPGA_CON89	23
14	EXP_IO_90	E39	IO_L14P_9	IO_L19N_10	R12	FPGA_CON90	23
14	EXP_IO_91	E39	IO_L14N_9	IO_L19P_10	P12	FPGA_CON91	23
14	EXP_IO_92	J34	IO_L15P_9	IO_L18N_10	E1	FPGA_CON92	23
14	EXP_IO_93	K34	IO_L15N_9	IO_L18P_10	E2	FPGA_CON93	23
14	EXP_IO_94	E38	IO_L16P_9	IO_L17N_10	T14	FPGA_CON94	23
14	EXP_IO_95	G38	IO_L16N_9	IO_L17P_10	R14	FPGA_CON95	23
14	EXP_IO_96	K33	IO_L17P_9	IO_L16N_10	D1	FPGA_CON96	23
14	EXP_IO_97	L33	IO_L17N_9	IO_L16P_10	D2	FPGA_CON97	23
14	EXP_IO_98	H37	IO_L18P_9	IO_L15N_10	E3	FPGA_CON98	23
14	EXP_IO_99	H38	IO_L18N_9	IO_L15P_10	E4	FPGA_CON99	23
14	EXP_IO_100	N30	IO_L19P_9	IO_L14N_10	N10	FPGA_CON100	23
14	EXP_IO_101	P29	IO_L19N_9	IO_L14P_10	M10	FPGA_CON101	23
14	EXP_IO_102	L34	IO_L20P_9	IO_L13N_10	T15	FPGA_CON102	23
14	EXP_IO_103	L35	IO_L20N_VREF_9	IO_L13P_10	R16	FPGA_CON103	23
14	EXP_IO_104	J36	IO_L21P_9	IO_L12N_VREF_10	F3	FPGA_CON104	23
14	EXP_IO_105	J37	IO_L21N_9	IO_L12P_10	F4	FPGA_CON105	23
14	EXP_IO_106	K36	IO_L22P_9	IO_L11N_10	N12	FPGA_CON106	23
14	EXP_IO_107	L36	IO_L22N_9	IO_L11P_10	M11	FPGA_CON107	23
14	EXP_IO_108	H39	IO_L23P_VRN_9	IO_L10N_10	G5	FPGA_CON108	23
14	EXP_IO_109	J39	IO_L23N_VRP_9	IO_L10P_10	F5	FPGA_CON109	23
14	EXP_IO_110	M33	IO_L24P_CC_LC_9	IO_L9N_CC_LC_10	G6	FPGA_CON110	23
14	EXP_IO_111	N32	IO_L24N_CC_LC_9	IO_L9P_CC_LC_10	G7	FPGA_CON111	23
14	EXP_IO_112	R28	IO_L25P_CC_LC_9	IO_L8N_CC_LC_10	J7	FPGA_CON112	23
14	EXP_IO_113	R29	IO_L25N_CC_LC_9	IO_L8P_CC_LC_10	H7	FPGA_CON113	23
14	EXP_IO_114	M35	IO_L26P_9	IO_L7N_10	F6	FPGA_CON114	23
14	EXP_IO_115	N35	IO_L26N_9	IO_L7P_10	F6	FPGA_CON115	23
14	EXP_IO_116	K37	IO_L27P_9	IO_L6N_10	C2	FPGA_CON116	23
14	EXP_IO_117	K38	IO_L27N_9	IO_L6P_10	C3	FPGA_CON117	23
14	EXP_IO_118	N33	IO_L28P_9	IO_L5N_10	D5	FPGA_CON118	23
14	EXP_IO_119	N34	IO_L28N_VREF_9	IO_L5P_10	D6	FPGA_CON119	23
14	EXP_IO_120	P31	IO_L29P_9	IO_L4N_VREF_10	D4	FPGA_CON120	23
14	EXP_IO_121	P32	IO_L29N_9	IO_L4P_10	C4	FPGA_CON121	23
14	EXP_IO_122	K39	IO_L30P_9	IO_L3N_10	C5	FPGA_CON122	23
14	EXP_IO_123	L39	IO_L30N_9	IO_L3P_10	B5	FPGA_CON123	23
14	EXP_IO_124	L38	IO_L31P_9	IO_L2N_10	B3	FPGA_CON124	23
14	EXP_IO_125	M38	IO_L31N_9	IO_L2P_10	A3	FPGA_CON125	23
14	EXP_IO_126	M36	IO_L32P_9	IO_L1N_10	A4	FPGA_CON126	23
14	EXP_IO_127	M37	IO_L32N_9	IO_L1P_10	A5	FPGA_CON127	23

VDD3V3	D38	VCCO_9	VCCO_10	T12	VDD3V3
VDD3V3	E35	VCCO_9	VCCO_10	R15	VDD3V3
VDD3V3	G39	VCCO_9	VCCO_10	P8	VDD3V3
VDD3V3	H36	VCCO_9	VCCO_10	N11	VDD3V3
VDD3V3	J33	VCCO_9	VCCO_10	L7	VDD3V3
VDD3V3	L37	VCCO_9	VCCO_10	H6	VDD3V3
VDD3V3	M34	VCCO_9	VCCO_10	F2	VDD3V3
VDD3V3	N31	VCCO_9	VCCO_10	E5	VDD3V3
VDD3V3	P28	VCCO_9	VCCO_10	C1	VDD3V3
			VCCO_10	B4	VDD3V3

U51E
INS23834214





SANGHWA FPGA PLATFORM

Title: FPGA0 BANK 7/8/9/10

Size	Document Number	Rev
A3	<Doc>	1.0

Date: Monday, August 21, 2006 Sheet 17 of 26

FPGA INTERCONNECTION

SSRAM INTERFACE

8 SMA_nOE — AG33

NAND FLASH

8 NDAREADY	AF33	IO_L1P_11	IO_L32N_12
8 NDARE	AC28	IO_L1N_11	IO_L32P_12
8 NDACE	AD29	IO_L2P_11	IO_L31N_12
8 NDACLE	AD27	IO_L2N_11	IO_L31P_12
8 NDAALE	AC27	IO_L3P_11	IO_L30N_12
8 NDAnWE	AE31	IO_L3N_11	IO_L30P_12
8 NDA_D7	AE32	IO_L4P_11	IO_L29N_12
8 NDA_D6	AD26	IO_L4N_VREF_11	IO_L29P_12
8 NDA_D5	AE26	IO_L5P_11	IO_L28N_VREF_12
8 NDA_D4	AE31	IO_L5N_11	IO_L28P_12
8 NDA_D3	AG32	IO_L6P_11	IO_L27N_12
8 NDA_D2	AH32	IO_L6N_11	IO_L27P_12
8 NDA_D1	AH33	IO_L7P_11	IO_L26N_12
8 NDA_D0	AJ34	IO_L7N_11	IO_L26P_12
	AH34	IO_L8P_CC_LC_11	IO_L25N_CC_LC_12
	AD25	IO_L8N_CC_LC_11	IO_L25P_CC_LC_12
	AE24	IO_L9P_CC_LC_11	IO_L24N_CC_LC_12
	AE28	IO_L9N_CC_LC_11	IO_L24P_CC_LC_12
14 EXP_IO_173	AF29	IO_L10P_11	IO_L23N_VRP_12
14 EXP_IO_172	AL34	IO_L10N_11	IO_L23P_VRN_12
14 EXP_IO_171	AK34	IO_L11P_11	IO_L22N_12
14 EXP_IO_170	AP39	IO_L11N_11	IO_L22P_12
14 EXP_IO_169	AN39	IO_L12P_11	IO_L21N_12
14 EXP_IO_168	AF28	IO_L12N_VREF_11	IO_L21P_12
14 EXP_IO_167	AF29	IO_L13P_11	IO_L20N_VREF_12
14 EXP_IO_166	AN37	IO_L13N_11	IO_L20P_12
14 EXP_IO_165	AN38	IO_L14P_11	IO_L19N_12
14 EXP_IO_164	AH30	IO_L14N_11	IO_L19P_12
14 EXP_IO_163	AG30	IO_L15P_11	IO_L18N_12
14 EXP_IO_162	AK33	IO_L15N_11	IO_L18P_12
14 EXP_IO_161	AJ32	IO_L16P_11	IO_L17N_12
14 EXP_IO_160	AR37	IO_L16N_11	IO_L17P_12
14 EXP_IO_159	AR38	IO_L17P_11	IO_L16N_12
14 EXP_IO_158	AM35	IO_L17N_11	IO_L16P_12
14 EXP_IO_157	AL35	IO_L18P_11	IO_L15N_12
14 EXP_IO_156	AP35	IO_L18N_11	IO_L15P_12
14 EXP_IO_155	AN35	IO_L19P_11	IO_L14N_12
14 EXP_IO_154	AT39	IO_L19N_11	IO_L14P_12
14 EXP_IO_153	AR39	IO_L20P_11	IO_L13N_12
14 EXP_IO_152	AG28	IO_L20N_VREF_11	IO_L13P_12
14 EXP_IO_151	AH29	IO_L21P_11	IO_L12N_VREF_12
14 EXP_IO_150	AP36	IO_L21N_11	IO_L12P_12
14 EXP_IO_149	AP37	IO_L22P_11	IO_L11N_12
14 EXP_IO_148	AN33	IO_L22N_11	IO_L11P_12
14 EXP_IO_147	AN34	IO_L23P_VRN_11	IO_L10N_12
14 EXP_IO_146	AU38	IO_L23N_VRP_11	IO_L10P_12
14 EXP_IO_145	AT38	IO_L24P_CC_LC_11	IO_L9N_CC_LC_12
14 EXP_IO_144	AU35	IO_L24N_CC_LC_11	IO_L9P_CC_LC_12
14 EXP_IO_143	AU36	IO_L25P_CC_LC_11	IO_L8N_CC_LC_12
14 EXP_IO_142	AM33	IO_L25N_CC_LC_11	IO_L8P_CC_LC_12
14 EXP_IO_141	AL33	IO_L26P_11	IO_L7N_12
14 EXP_IO_140	AT34	IO_L26N_11	IO_L7P_12
14 EXP_IO_139	AT35	IO_L27P_11	IO_L6N_12
14 EXP_IO_138	AT36	IO_L27N_11	IO_L6P_12
14 EXP_IO_137	AR36	IO_L28P_11	IO_L5N_12
14 EXP_IO_136	AW36	IO_L28N_VREF_11	IO_L5P_12
14 EXP_IO_135	AW37	IO_L29P_11	IO_L4N_VREF_12
14 EXP_IO_134	AV37	IO_L29N_11	IO_L4P_12
14 EXP_IO_133	AU37	IO_L30P_11	IO_L3N_12
14 EXP_IO_132	AW35	IO_L30N_11	IO_L3P_12
14 EXP_IO_131	AV35	IO_L31P_11	IO_L2N_12
14 EXP_IO_130	AR34	IO_L31N_11	IO_L2P_12
14 EXP_IO_129	AP34	IO_L32P_11	IO_L1N_12
14 EXP_IO_128		IO_L32N_11	IO_L1P_12

VDD3V3	AD28	VCCO_11	VCCO_12
VDD3V3	AE25	VCCO_11	VCCO_12
VDD3V3	AE32	VCCO_11	VCCO_12
VDD3V3	AG29	VCCO_11	VCCO_12
VDD3V3	AJ33	VCCO_11	VCCO_12
VDD3V3	AM34	VCCO_11	VCCO_12
VDD3V3	AP38	VCCO_11	VCCO_12
VDD3V3	AR35	VCCO_11	VCCO_12
VDD3V3	AU39	VCCO_11	VCCO_12
VDD3V3	AV36	VCCO_11	VCCO_12

Bank 11 **Bank 12**

U51F
INS23839244

AT3	FPGA_CON256	24	
AU3	FPGA_CON257	24	
AT5	FPGA_CON258	24	
AT6	FPGA_CON259	24	
AP4	FPGA_CON260	24	
AP5	FPGA_CON261	24	
AP6	FPGA_CON262	24	
AR6	FPGA_CON263	24	
AM6	FPGA_CON264	24	
AM7	FPGA_CON265	24	
AR4	FPGA_CON266	24	
AT4	FPGA_CON267	24	
AR2	FPGA_CON268	24	
AR3	FPGA_CON269	24	
AU1	FPGA_CON270	24	
AU2	FPGA_CON271	24	
AR1	FPGA_CON272	24	
AT1	FPGA_CON273	24	
AK8	FPGA_CON274	24	
AL8	FPGA_CON275	24	
AL5	FPGA_CON276	24	
AM5	FPGA_CON277	24	
AN4	FPGA_CON278	24	
AN5	FPGA_CON279	24	
AJ7	FPGA_CON280	24	
AK7	FPGA_CON281	24	
AH9	FPGA_CON282	24	
AH10	FPGA_CON283	24	
AN2	FPGA_CON284	24	
AN3	FPGA_CON285	24	
AK6	FPGA_CON286	24	
AL6	FPGA_CON287	24	
AK4	FPGA_CON288	24	
AL4	FPGA_CON289	24	
AP1	FPGA_CON290	24	
AP2	FPGA_CON291	24	
AM1	FPGA_CON292	24	
AM2	FPGA_CON293	24	
AL3	FPGA_CON294	24	
AM3	FPGA_CON295	24	
AE11	FPGA_CON296	24	
AE12	FPGA_CON297	24	
AG10	FPGA_CON298	24	
AF11	FPGA_CON299	24	
AK2	FPGA_CON300	24	
AK3	FPGA_CON301	24	
AJ5	FPGA_CON302	24	
AJ6	FPGA_CON303	24	
AH4	FPGA_CON304	24	
AJ4	FPGA_CON305	24	
AH7	FPGA_CON306	24	
AG8	FPGA_CON307	24	
AF8	FPGA_CON308	24	
AF9	FPGA_CON309	24	
AK1	FPGA_CON310	24	
AL1	FPGA_CON311	24	
AJ1	FPGA_CON312	24	
AJ2	FPGA_CON313	24	
AG6	FPGA_CON314	24	
AG7	FPGA_CON315	24	
AH2	FPGA_CON316	24	
AH3	FPGA_CON317	24	
AG5	FPGA_CON318	24	
AH5	FPGA_CON319	24	

AT2	VDD3V3		
AR5	VDD3V3		
AN1	VDD3V3		
AM4	VDD3V3		
AL7	VDD3V3		
AJ3	VDD3V3		
AH6	VDD3V3		
AG9	VDD3V3		
AF12	VDD3V3		

14 EXP_IO_0	R31	IO_L1P_13	IO_L32N_14
14 EXP_IO_1	R32	IO_L1N_13	IO_L32P_14
14 EXP_IO_2	P34	IO_L2P_13	IO_L31N_14
14 EXP_IO_3	P35	IO_L2N_13	IO_L31P_14
14 EXP_IO_4	T29	IO_L3P_13	IO_L30N_14
14 EXP_IO_5	U28	IO_L3N_13	IO_L30P_14
14 EXP_IO_6	P36	IO_L4P_13	IO_L29N_14
14 EXP_IO_7	P37	IO_L4N_VREF_13	IO_L29P_14
14 EXP_IO_8	N37	IO_L5P_13	IO_L28N_VREF_14
14 EXP_IO_9	N38	IO_L5N_13	IO_L28P_14
14 EXP_IO_10	N39	IO_L6P_13	IO_L27N_14
14 EXP_IO_11	P39	IO_L6N_13	IO_L27P_14
14 EXP_IO_12	R34	IO_L7P_13	IO_L26N_14
14 EXP_IO_13	T34	IO_L7N_13	IO_L26P_14
14 EXP_IO_14	T31	IO_L8P_CC_LC_13	IO_L25N_CC_LC_14
14 EXP_IO_15	U30	IO_L8N_CC_LC_13	IO_L25P_CC_LC_14
14 EXP_IO_16	R36	IO_L9P_CC_LC_13	IO_L24N_CC_LC_14
14 EXP_IO_17	T36	IO_L9N_CC_LC_13	IO_L24P_CC_LC_14
14 EXP_IO_18	T33	IO_L10P_13	IO_L23N_VRP_14
14 EXP_IO_19	U32	IO_L10N_13	IO_L23P_VRN_14
14 EXP_IO_20	R37	IO_L11P_13	IO_L22N_14
14 EXP_IO_21	R38	IO_L11N_13	IO_L22P_14
14 EXP_IO_22	R39	IO_L12P_13	IO_L21N_14
14 EXP_IO_23	T39	IO_L12N_VREF_13	IO_L21P_14
14 EXP_IO_24	V25	IO_L13P_13	IO_L20N_VREF_14
14 EXP_IO_25	U26	IO_L13N_13	IO_L20P_14
14 EXP_IO_26	V27	IO_L14P_13	IO_L19N_14
14 EXP_IO_27	U27	IO_L14N_13	IO_L19P_14
14 EXP_IO_28	T35	IO_L15P_13	IO_L18N_14
14 EXP_IO_29	U35	IO_L15N_13	IO_L18P_14
14 EXP_IO_30	U33	IO_L16P_13	IO_L17N_14
14 EXP_IO_31	V33	IO_L16N_13	IO_L17P_14
14 EXP_IO_32	T38	IO_L17P_13	IO_L16N_14
14 EXP_IO_33	U38	IO_L17N_13	IO_L16P_14
14 EXP_IO_34	V29	IO_L18P_13	IO_L15N_14
14 EXP_IO_35	V30	IO_L18N_13	IO_L15P_14
14 EXP_IO_36	U36	IO_L19P_13	IO_L14N_14
14 EXP_IO_37	U37	IO_L19N_13	IO_L14P_14
14 EXP_IO_38	V32	IO_L20P_13	IO_L13N_14
14 EXP_IO_39	W32	IO_L20N_VREF_13	IO_L13P_14
14 EXP_IO_40	W26	IO_L21P_13	IO_L12N_VREF_14
14 EXP_IO_41	W27	IO_L21N_13	IO_L12P_14
14 EXP_IO_42	V34	IO_L22P_13	IO_L11N_14
14 EXP_IO_43	V35	IO_L22N_13	IO_L11P_14
14 EXP_IO_44	V37	IO_L23P_VRN_13	IO_L10N_14
14 EXP_IO_45	V38	IO_L23N_VRP_13	IO_L10P_14
14 EXP_IO_46	V39	IO_L24P_CC_LC_13	IO_L9N_CC_LC_14
14 EXP_IO_47	W39	IO_L24N_CC_LC_13	IO_L9P_CC_LC_14
14 EXP_IO_48	W34	IO_L25P_CC_LC_13	IO_L8N_CC_LC_14
14 EXP_IO_49	W35	IO_L25N_CC_LC_13	IO_L8P_CC_LC_14
14 EXP_IO_50	W36	IO_L26P_13	IO_L7N_14
14 EXP_IO_51	W37	IO_L26N_13	IO_L7P_14
14 EXP_IO_52	Y37	IO_L27P_13	IO_L6N_14
14 EXP_IO_53	Y38	IO_L27N_13	IO_L6P_14
14 EXP_IO_54	Y39	IO_L28P_13	IO_L5N_14
14 EXP_IO_55	AA39	IO_L28N_VREF_13	IO_L5P_14
14 EXP_IO_56	AA36	IO_L29P_13	IO_L4N_VREF_14
14 EXP_IO_57	Y36	IO_L29N_13	IO_L4P_14
14 EXP_IO_58	Y33	IO_L30P_13	IO_L3N_14
14 EXP_IO_59	Y34	IO_L30N_13	IO_L3P_14
14 EXP_IO_60	AB36	IO_L31P_13	IO_L2N_14
14 EXP_IO_61	AB37	IO_L31N_13	IO_L2P_14
14 EXP_IO_62	AB38	IO_L32P_13	IO_L1N_14
14 EXP_IO_63	AA38	IO_L32N_13	IO_L1P_14

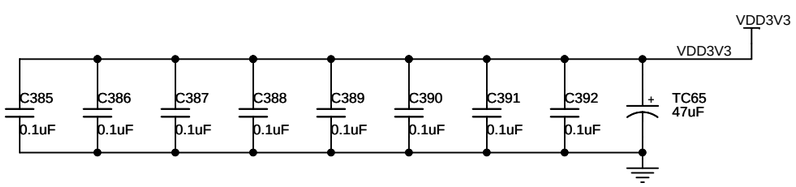
VDD3V3	AA37	VCCO_13	VCCO_14
VDD3V3	P38	VCCO_13	VCCO_14
VDD3V3	R35	VCCO_13	VCCO_14
VDD3V3	T32	VCCO_13	VCCO_14
VDD3V3	U29	VCCO_13	VCCO_14
VDD3V3	U39	VCCO_13	VCCO_14
VDD3V3	V26	VCCO_13	VCCO_14
VDD3V3	V36	VCCO_13	VCCO_14
VDD3V3	W33	VCCO_13	VCCO_14

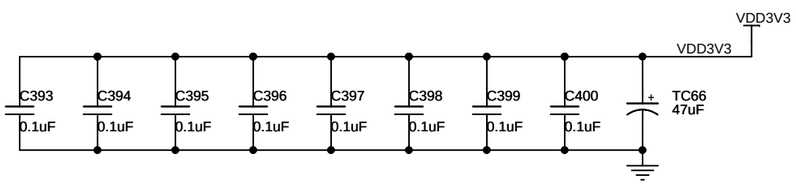
Bank 13 **Bank 14**

U51G
INS23841562

W12	FPGA_CON128	24	
Y13	FPGA_CON129	24	
Y11	FPGA_CON130	24	
AA11	FPGA_CON131	24	
Y9	FPGA_CON132	24	
AA10	FPGA_CON133	24	
W5	FPGA_CON134	24	
W6	FPGA_CON135	24	
W9	FPGA_CON136	24	
W10	FPGA_CON137	24	
W7	FPGA_CON138	24	
V7	FPGA_CON139	24	
U2	FPGA_CON140	24	
U3	FPGA_CON141	24	
U1	FPGA_CON142	24	
T1	FPGA_CON143	24	
V5	FPGA_CON144	24	
U5	FPGA_CON145	24	
V9	FPGA_CON146	24	
V10	FPGA_CON147	24	
U6	FPGA_CON148	24	
U7	FPGA_CON149	24	
T3	FPGA_CON150	24	
T4	FPGA_CON151	24	
R1	FPGA_CON152	24	
R2	FPGA_CON153	24	
T5	FPGA_CON154	24	
T6	FPGA_CON155	24	
R3	FPGA_CON156	24	
R4	FPGA_CON157	24	
T9	FPGA_CON158	24	
U10	FPGA_CON159	24	
P1	FPGA_CON160	24	
P2	FPGA_CON161	24	
U8	FPGA_CON162	24	
T8	FPGA_CON163	24	
V12	FPGA_CON164	24	
V13	FPGA_CON165	24	
N2	FPGA_CON166	24	
N3	FPGA_CON167	24	
P4	FPGA_CON168	24	
P5	FPGA_CON169	24	
R6	FPGA_CON170	24	
P6	FPGA_CON171	24	
M1	FPGA_CON172	24	
L1	FPGA_CON173	24	
N4	FPGA_CON174	24	
N5	FPGA_CON175	24	
M2	FPGA_CON176	24	
M3	FPGA_CON177	24	
L3	FPGA_CON178	24	
L4	FPGA_CON179	24	
K1	FPGA_CON180	24	
K2	FPGA_CON181	24	
M5	FPGA_CON182	24	
L5	FPGA_CON183	24	
J1	FPGA_CON184	24	
J2	FPGA_CON185	24	
H2	FPGA_CON186	24	
H3	FPGA_CON187	24	
K3	FPGA_CON188	24	
K4	FPGA_CON189	24	
J4	FPGA_CON190	24	
H4	FPGA_CON191	24	

Y10	VDD3V3		
W13	VDD3V3		
V6	VDD3V3		
U9	VDD3V3		
T2	VDD3V3		
R5	VDD3V3		
N1	VDD3V3		
M4	VDD3V3		
J3	VDD3V3		





Title	SANGHWA FPGA PLATFORM FPGA0 BANK 11/12/13/14		
Size A3	Document Number <Doc>		Rev 1.0
Date: Monday, August 21, 2006		Sheet 18 of 26	

VIRTEX-4 FPGA
POWER GROUND

GND	D13	GND	J28
GND	K13	GND	N28
GND	M13	GND	W28
GND	P13	GND	AJ28
GND	AD13	GND	AW28
GND	AF13	GND	B29
GND	AK13	GND	M29
GND	AP13	GND	AB29
GND	G14	GND	AM29
GND	L14	GND	E30
GND	N14	GND	R30
GND	U14	GND	AF30
GND	W14	GND	AR30
GND	AF14	GND	H31
GND	AG14	GND	V31
GND	AJ14	GND	AH31
GND	AU14	GND	AV31
GND	K15	GND	A32
GND	M15	GND	L32
GND	P15	GND	AA32
GND	V15	GND	AL32
GND	Y15	GND	D33
GND	AD15	GND	P33
GND	AF15	GND	AD33
GND	AK15	GND	AP33
GND	C16	GND	G34
GND	N16	GND	U34
GND	U16	GND	AG34
GND	W16	GND	AU34
GND	AC16	GND	K35
GND	AE16	GND	Y35
GND	AN16	GND	AK35
GND	F17	GND	C36
GND	T17	GND	N36
GND	V17	GND	AC36
GND	AF17	GND	AN36
GND	AT17	GND	F37
GND	J18	GND	T37
GND	W18	GND	AF37
GND	AC18	GND	AT37
GND	AJ18	GND	A38
GND	AW18	GND	J38
GND	B19	GND	W38
GND	M19	GND	AJ38
GND	V19	GND	AW38
GND	AB19	GND	B39
GND	AD19	GND	M39
GND	AM19	GND	AB39
GND	E20	GND	AM39
GND	R20	GND	AV39
GND	AE20	GND	B1
GND	AR20	GND	H1
GND	H21	GND	V1
GND	T21	GND	AH1
GND	V21	GND	AV1
GND	AB21	GND	A2
GND	AH21	GND	L2
GND	AV21	GND	AA2
GND	A22	GND	AL2
GND	L22	GND	AW2
GND	U22	GND	D3
GND	AA22	GND	P3
GND	AL22	GND	AD3
GND	D23	GND	AP3
GND	P23	GND	G4
GND	AB23	GND	U4
GND	AD23	GND	AG4
GND	AP23	GND	AU4
GND	G24	GND	K5
GND	R24	GND	Y5
GND	U24	GND	AK5
GND	AA24	GND	C6
GND	AC24	GND	N6
GND	AG24	GND	AC6
GND	AU24	GND	AN6
GND	K25	GND	F7
GND	P25	GND	T7
GND	T25	GND	AF7
GND	Y25	GND	AT7
GND	AB25	GND	J8
GND	AF25	GND	W8
GND	AH25	GND	AJ8
GND	AK25	GND	AW8
GND	C26	GND	B9
GND	L26	GND	M9
GND	N26	GND	AB9
GND	R26	GND	AM9
GND	AA26	GND	E10
GND	AC26	GND	R10
GND	AG26	GND	AF10
GND	AJ26	GND	AR10
GND	AN26	GND	H11
GND	F27	GND	V11
GND	K27	GND	AH11
GND	P27	GND	AV11
GND	T27	GND	A12
GND	AF27	GND	L12
GND	AH27	GND	AA12
GND	AK27	GND	AG12
GND	AT27	GND	AL12

U51K
INS23847039

SSRAM INTERFACE

8	SMA_A2	Y27	IO_L1P_15	IO_L32N_16	AF3	FPGA_CON192	25
8	SMA_A3	AA28	IO_L1N_15	IO_L32P_16	AG3	FPGA_CON193	25
8	SMA_A4	W29	IO_L2P_15	IO_L31N_16	AF8	FPGA_CON194	25
8	SMA_A5	W30	IO_L2N_15	IO_L31P_16	AF9	FPGA_CON195	25
8	SMA_A6	AA34	IO_L3P_15	IO_L30N_16	AG1	FPGA_CON196	25
8	SMA_A7	AA35	IO_L3N_15	IO_L30P_16	AG2	FPGA_CON197	25
8	SMA_A8	Y29	IO_L4P_15	IO_L29N_16	AF5	FPGA_CON198	25
8	SMA_A9	AA30	IO_L4N_VREF_15	IO_L29P_16	AF6	FPGA_CON199	25
8	SMA_A10	AC38	IO_L5P_15	IO_L28N_VREF_16	AD6	FPGA_CON200	25
8	SMA_A11	AC39	IO_L5N_15	IO_L28P_16	AE6	FPGA_CON201	25
8	SMA_A12	AA31	IO_L6P_15	IO_L27N_16	AE4	FPGA_CON202	25
8	SMA_A13	Y31	IO_L6N_15	IO_L27P_16	AE4	FPGA_CON203	25
8	SMA_A14	AC35	IO_L7P_15	IO_L26N_16	AE1	FPGA_CON204	25
8	SMA_A15	AB35	IO_L7N_15	IO_L26P_16	AE1	FPGA_CON205	25
8	SMA_A16	AB33	IO_L8P_CC_LC_15	IO_L25N_CC_LC_16	AD11	FPGA_CON206	25
8	SMA_A17	AA33	IO_L8N_CC_LC_15	IO_L25P_CC_LC_16	AC12	FPGA_CON207	25
8	SMA_A18	AC33	IO_L9P_CC_LC_15	IO_L24N_CC_LC_16	AE2	FPGA_CON208	25
8	SMA_A19	AC34	IO_L9N_CC_LC_15	IO_L24P_CC_LC_16	AE3	FPGA_CON209	25
8	SMA_A20	AD37	IO_L10P_15	IO_L23N_VRP_16	AC7	FPGA_CON210	25
8	SMA_nADSC	AC37	IO_L10N_15	IO_L23P_VRN_16	AD7	FPGA_CON211	25
8	SMA_nADSP	AC32	IO_L11P_15	IO_L22N_16	AD9	FPGA_CON212	25
8	SMA_nADV	AB31	IO_L11N_15	IO_L22P_16	AC10	FPGA_CON213	25
8	SMA_nBW1	AE39	IO_L12P_15	IO_L21N_16	AC14	FPGA_CON214	25
8	SMA_nBW2	AD39	IO_L12N_VREF_15	IO_L21P_16	AB15	FPGA_CON215	25
8	SMA_nBW3	AE38	IO_L13P_15	IO_L20N_VREF_16	AC13	FPGA_CON216	25
8	SMA_nBW4	AE39	IO_L13N_15	IO_L20P_16	AB13	FPGA_CON217	25
8	SMA_nBWE	AD35	IO_L14P_15	IO_L19N_16	AD4	FPGA_CON218	25
8	SMA_nCE	AD36	IO_L14N_15	IO_L19P_16	AD5	FPGA_CON219	25
8	SMA_CLK	AC30	IO_L15P_15	IO_L18N_16	AD1	FPGA_CON220	25
8	SMA_nCS1	AB30	IO_L15N_15	IO_L18P_16	AD2	FPGA_CON221	25
8	SMA_nGW	AE37	IO_L16P_15	IO_L17N_16	AB8	FPGA_CON222	25
8	SMA_nLBO	AE38	IO_L16N_15	IO_L17P_16	AC8	FPGA_CON223	25
8	SMA_D31	AB27	IO_L17P_15	IO_L16N_16	AC4	FPGA_CON224	25
8	SMA_D30	AB28	IO_L17N_15	IO_L16P_16	AC5	FPGA_CON225	25
8	SMA_D29	AE34	IO_L18P_15	IO_L15N_16	AB10	FPGA_CON226	25
8	SMA_D28	AD34	IO_L18N_15	IO_L15P_16	AB11	FPGA_CON227	25
8	SMA_D27	AD31	IO_L19P_15	IO_L14N_16	AA8	FPGA_CON228	25
8	SMA_D26	AD32	IO_L19N_15	IO_L14P_16	AB7	FPGA_CON229	25
8	SMA_D25	AE36	IO_L20P_15	IO_L13N_16	AC2	FPGA_CON230	25
8	SMA_D24	AE36	IO_L20N_VREF_15	IO_L13P_16	AC3	FPGA_CON231	25
8	SMA_D23	AJ39	IO_L21P_15	IO_L12N_VREF_16	AB1	FPGA_CON232	25
8	SMA_D22	AH39	IO_L21N_15	IO_L12P_16	AB2	FPGA_CON233	25
8	SMA_D21	AG37	IO_L22P_15	IO_L11N_16	AB5	FPGA_CON234	25
8	SMA_D20	AG38	IO_L22N_15	IO_L11P_16	AB6	FPGA_CON235	25
8	SMA_D19	AH37	IO_L23P_VRN_15	IO_L10N_16	AA5	FPGA_CON236	25
8	SMA_D18	AH38	IO_L23N_VRP_15	IO_L10P_16	AA6	FPGA_CON237	25
8	SMA_D17	AE34	IO_L24P_CC_LC_15	IO_L9N_CC_LC_16	AA13	FPGA_CON238	25
8	SMA_D16	AE35	IO_L24N_CC_LC_15	IO_L9P_CC_LC_16	AA14	FPGA_CON239	25
8	SMA_D15	AJ36	IO_L25P_CC_LC_15	IO_L8N_CC_LC_16	AA1	FPGA_CON240	25
8	SMA_D14	AJ37	IO_L25N_CC_LC_15	IO_L8P_CC_LC_16	Y1	FPGA_CON241	25
8	SMA_D13	AG35	IO_L26P_15	IO_L7N_16	AB3	FPGA_CON242	25
8	SMA_D12	AG36	IO_L26N_15	IO_L7P_16	AA3	FPGA_CON243	25
8	SMA_D11	AJ35	IO_L27P_15	IO_L6N_16	Y2	FPGA_CON244	25
8	SMA_D10	AH35	IO_L27N_15	IO_L6P_16	Y3	FPGA_CON245	25
8	SMA_D9	AK38	IO_L28P_15	IO_L5N_16	AA4	FPGA_CON246	25
8	SMA_D8	AK39	IO_L28N_VREF_15	IO_L5P_16	Y4	FPGA_CON247	25
8	SMA_D7	AM37	IO_L29P_15	IO_L4N_VREF_16	Y6	FPGA_CON248	25
8	SMA_D6	AM38	IO_L29N_15	IO_L4P_16	Y7	FPGA_CON249	25
8	SMA_D5	AL38	IO_L30P_15	IO_L3N_16	W1	FPGA_CON250	25
8	SMA_D4	AL39	IO_L30N_15	IO_L3P_16	W2	FPGA_CON251	25
8	SMA_D3	AM36	IO_L31P_15	IO_L2N_16	V2	FPGA_CON252	25
8	SMA_D2	AL36	IO_L31N_15	IO_L2P_16	V3	FPGA_CON253	25
8	SMA_D1	AK36	IO_L32P_15	IO_L1N_16	W4	FPGA_CON254	25
8	SMA_D0	AK37	IO_L32N_15	IO_L1P_16	V4	FPGA_CON255	25

Bank 15 **Bank 16**

VDD3V3	AA27	VCCO_15	VCCO_16	W3	VDD3V3
VDD3V3	AB34	VCCO_15	VCCO_16	AF2	VDD3V3
VDD3V3	AC31	VCCO_15	VCCO_16	AF5	VDD3V3
VDD3V3	AD38	VCCO_15	VCCO_16	AD8	VDD3V3
VDD3V3	AE35	VCCO_15	VCCO_16	AC11	VDD3V3
VDD3V3	AG39	VCCO_15	VCCO_16	AC1	VDD3V3
VDD3V3	AH36	VCCO_15	VCCO_16	AB4	VDD3V3
VDD3V3	AL37	VCCO_15	VCCO_16	AB14	VDD3V3
VDD3V3	Y30	VCCO_15	VCCO_16	AA7	VDD3V3

U51H
INS28868288

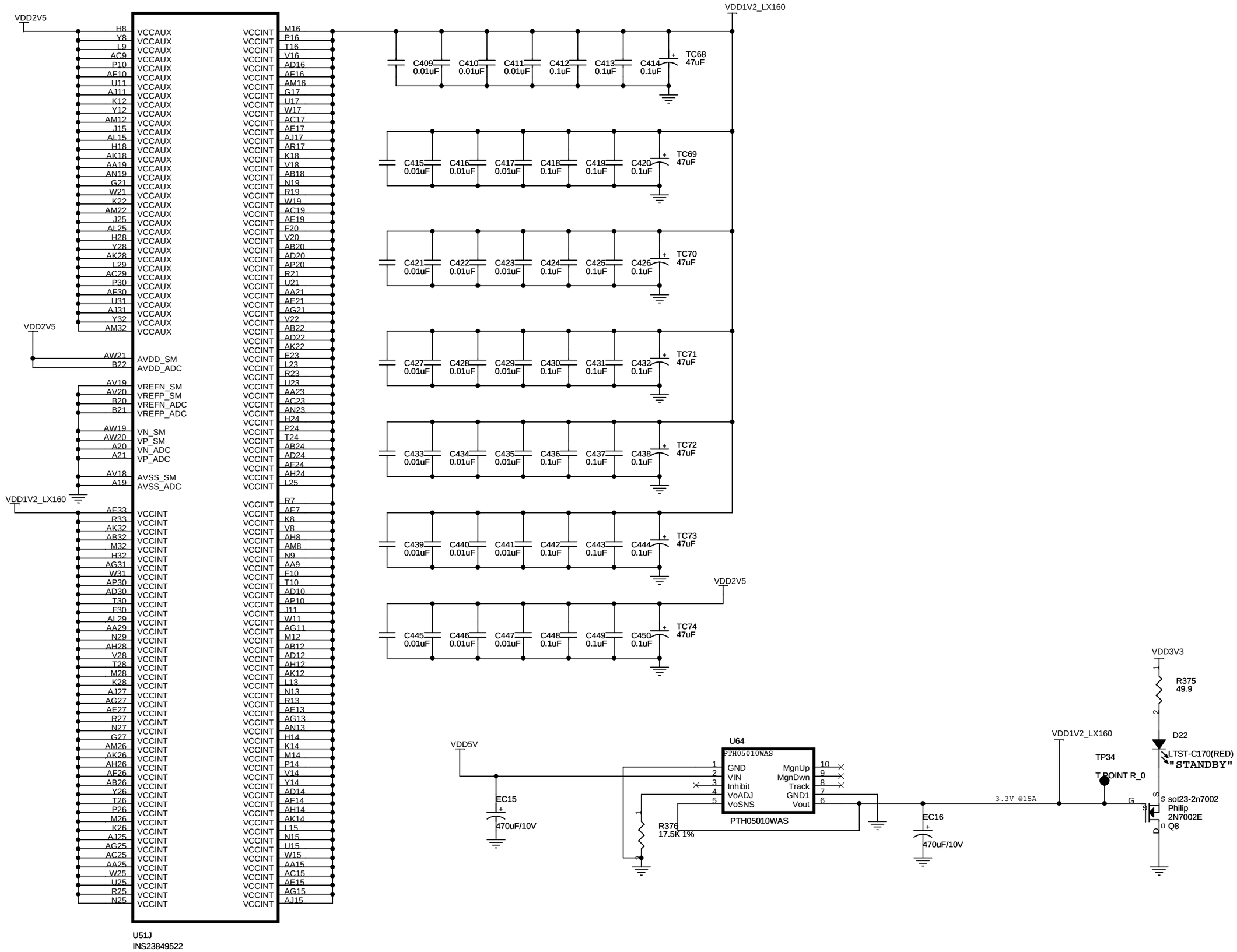
VDD3V3

C401	C402	C403	C404	C405	C406	C407	C408	TC67
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	47uF

Title: SANGHWA FPGA PLATFORM
FPGA0 BANK 15/16/GND

Size	Document Number	Rev
A3	<Doc>	1.0

Date: Monday, August 21, 2006 Sheet 19 of 26



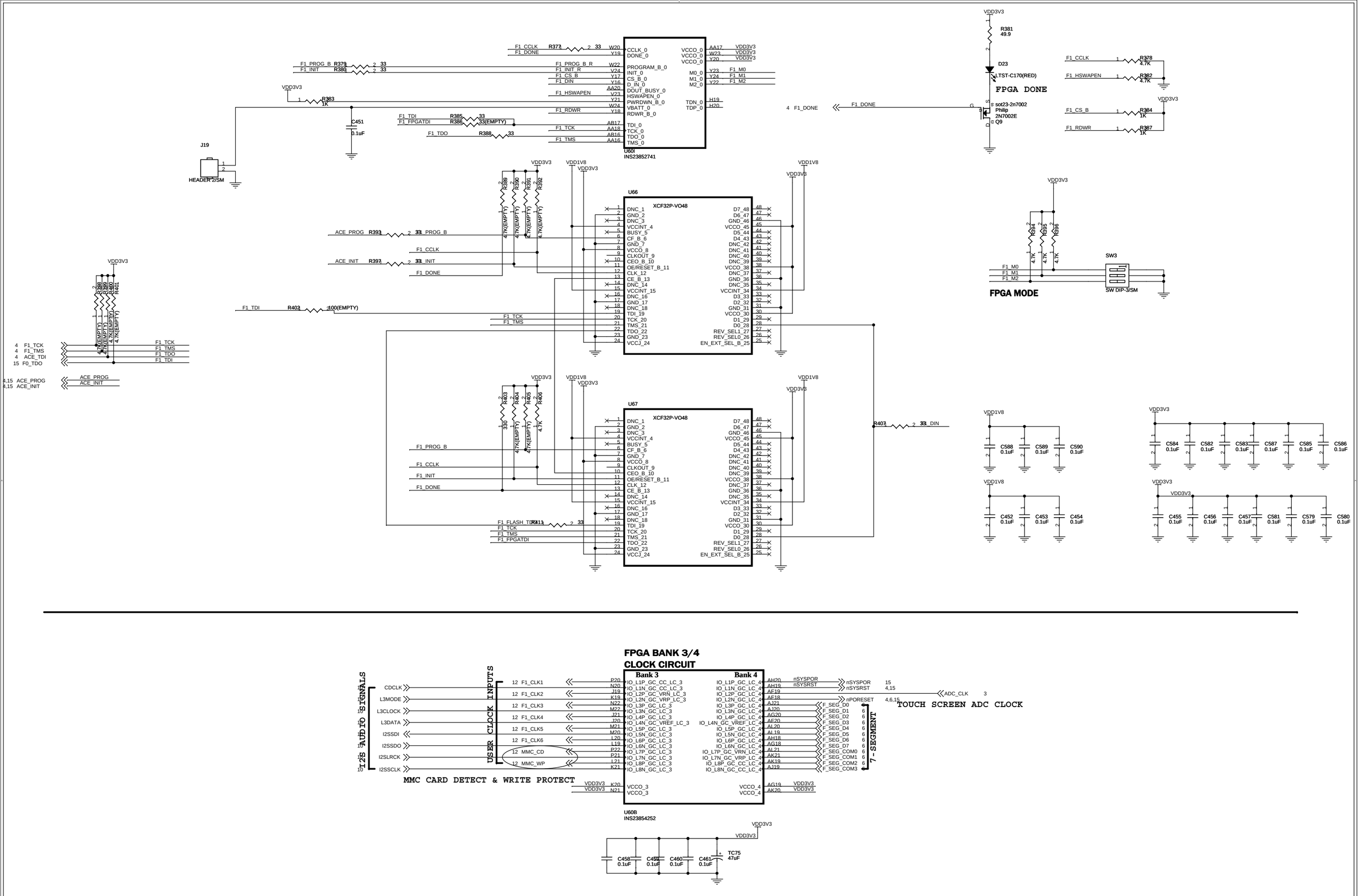
SANGHWA FPGA PLATFORM

Title

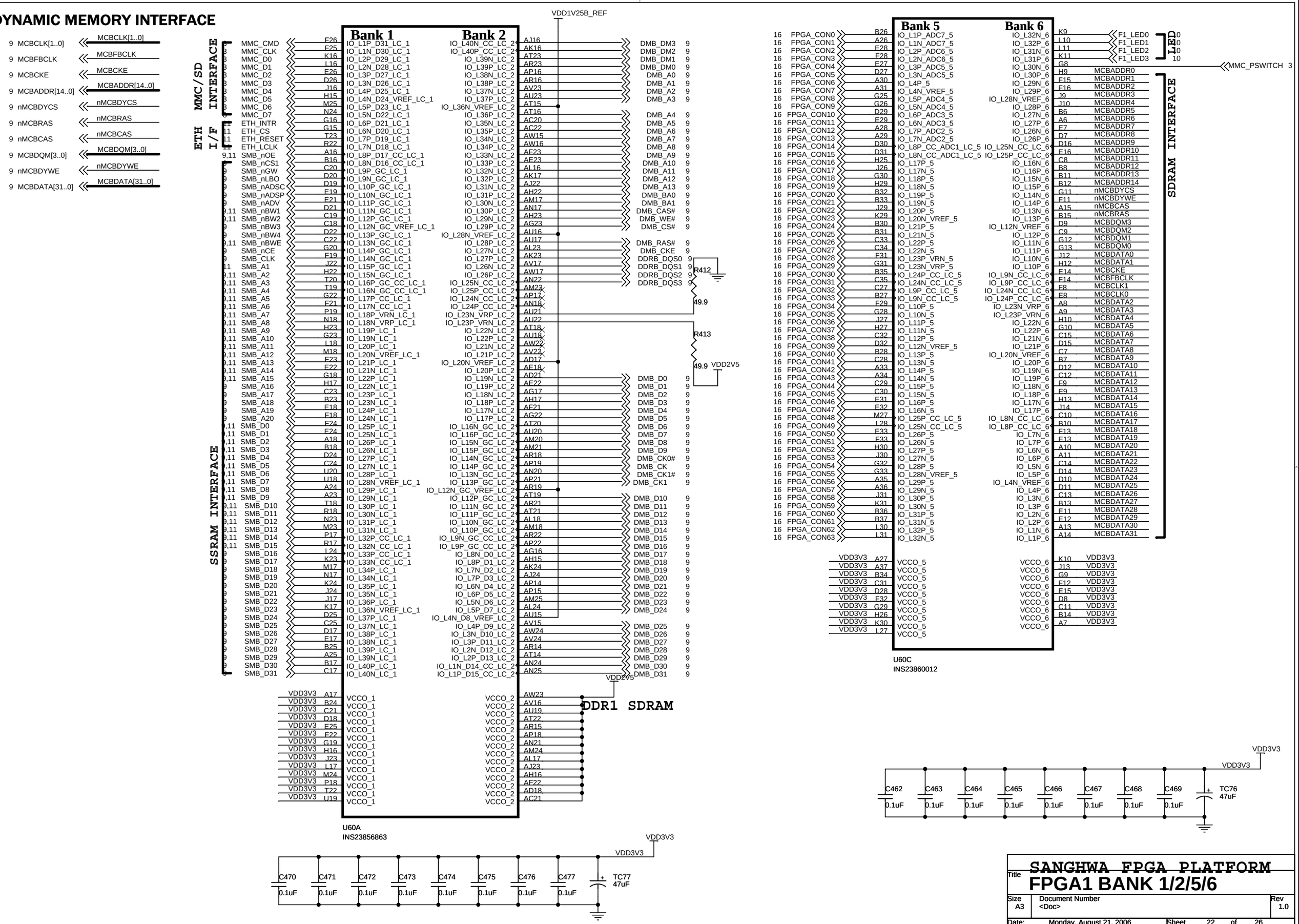
FPGA0 POWER VCCO

Size	Document Number	Rev
A3	<Doc>	1.0

Date: Monday, August 21, 2006 Sheet 20 of 26


U60I
INS23852741
U66
XCF32P-VO48
U67
XCF32P-VO48
FPGA DONE
FPGA MODE
SW3
SW DIP-3/SM
J19
HEADER 2/SM
FPGA BANK 3/4
CLOCK CIRCUIT
Bank 3
Bank 4
U60B
INS23854252
USER CLOCK INPUTS
I2S AUDIO SIGNALS
MMC CARD DETECT & WRITE PROTECT
7-SEGMENT
TOUCH SCREEN ADC CLOCK
SANGHWA FPGA PLATFORM
FPGA1 CONFIG/CLOCK
Size A2
Document Number <Doc>
Rev 1.0
Date: Monday, August 21, 2006
Sheet 21 of 26

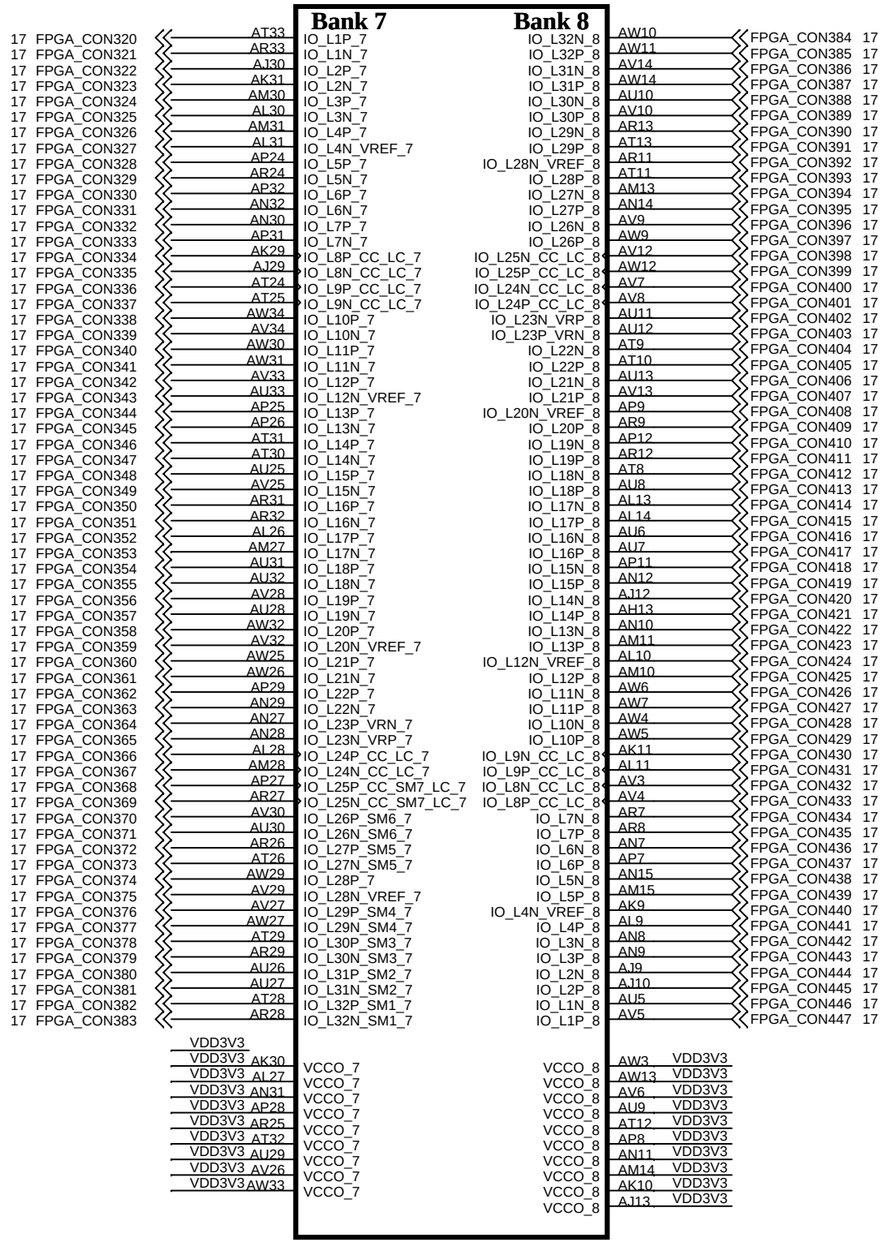
DYNAMIC MEMORY INTERFACE



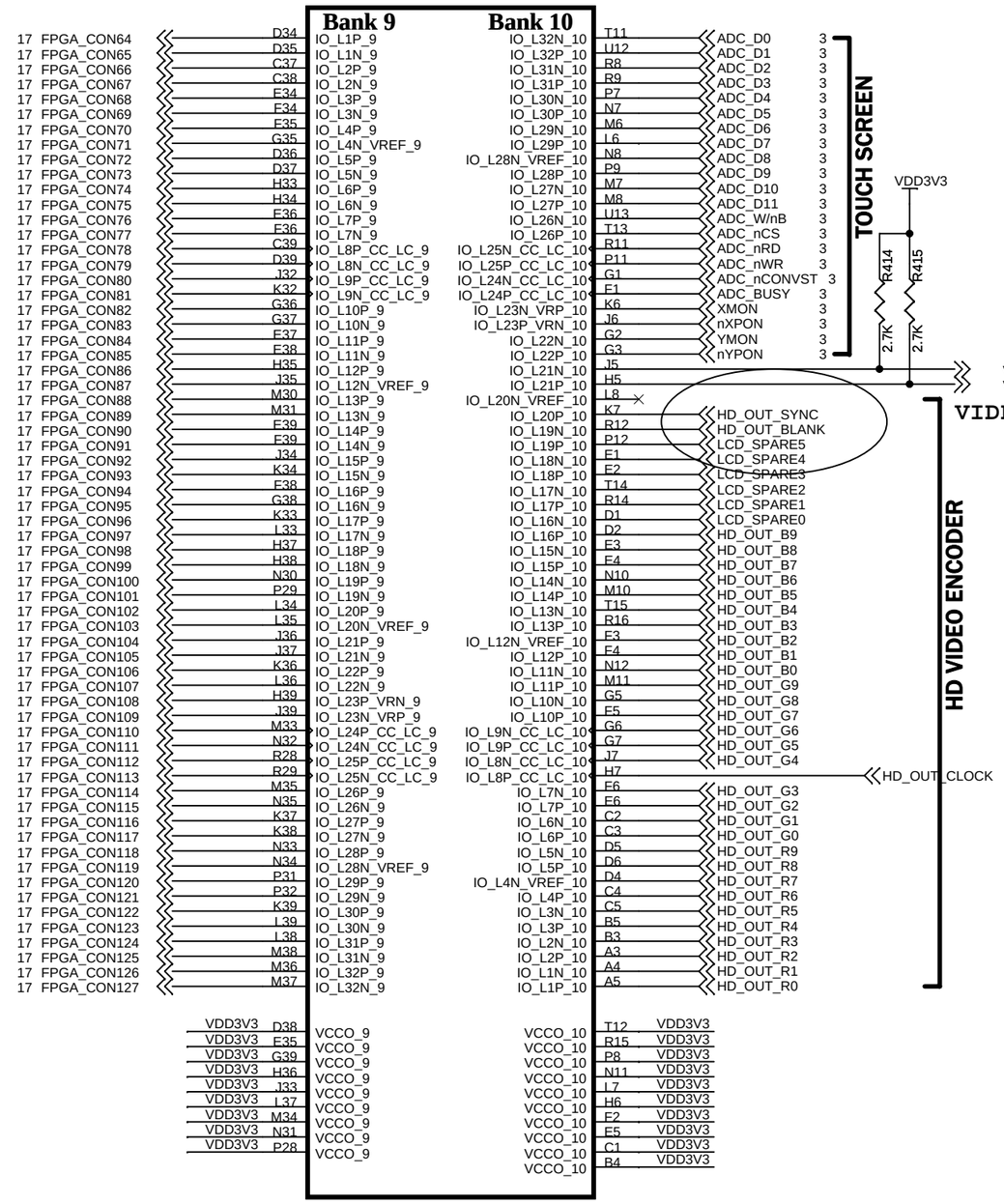
Title: SANGHWA FPGA PLATFORM
FPGA1 BANK 1/2/5/6

Size	Document Number	Rev
A3	<Doc>	1.0

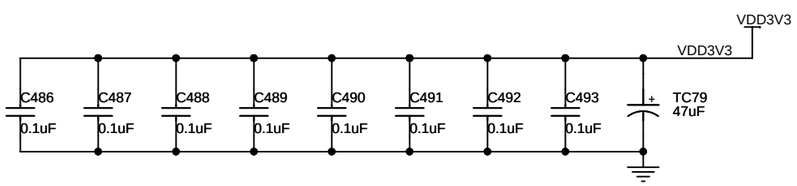
Date: Monday, August 21, 2006 Sheet 22 of 26

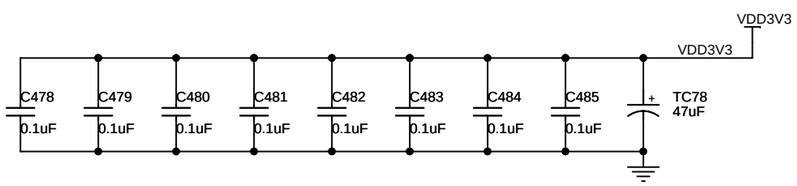


U60D
INS23864101

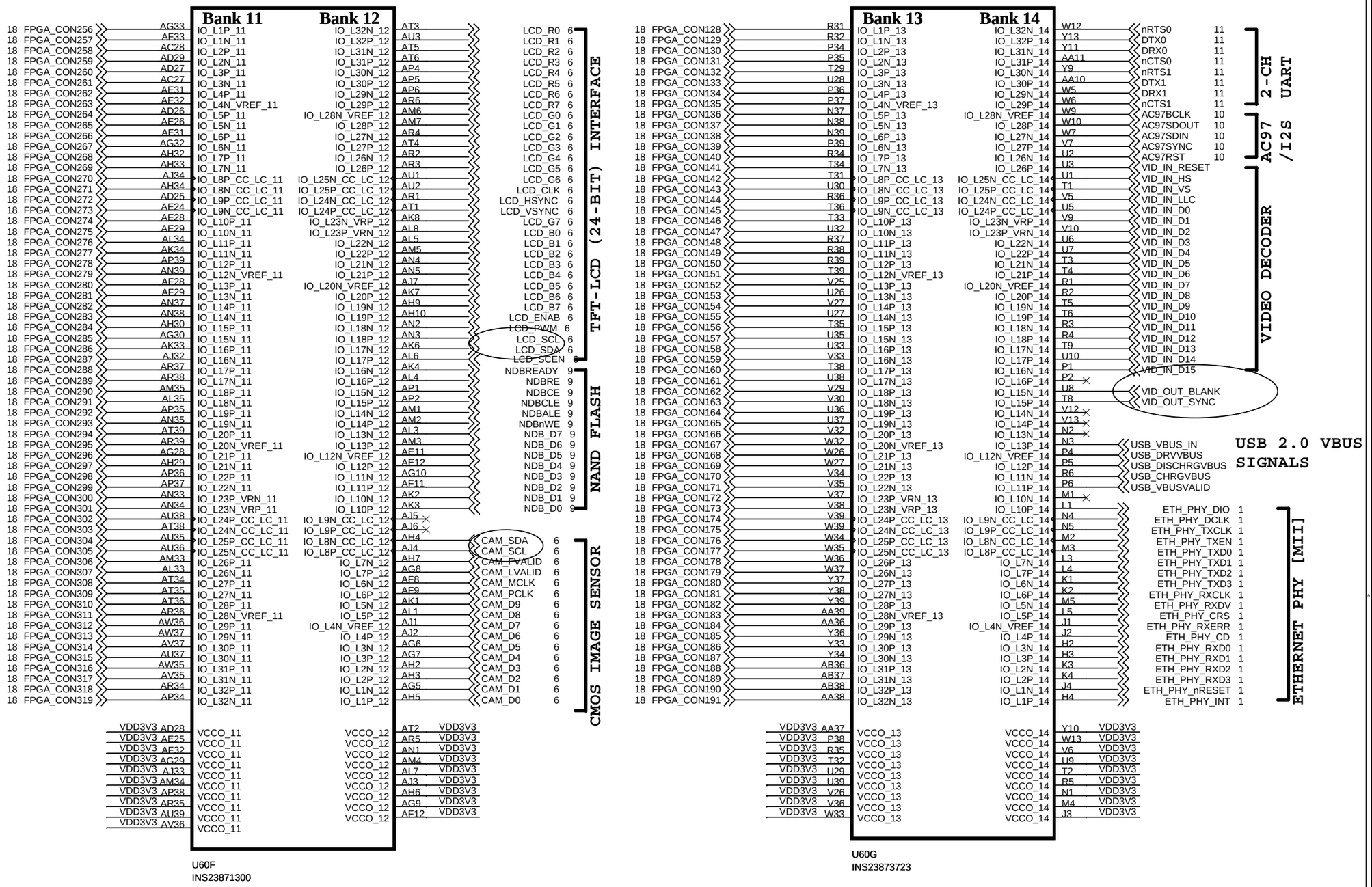


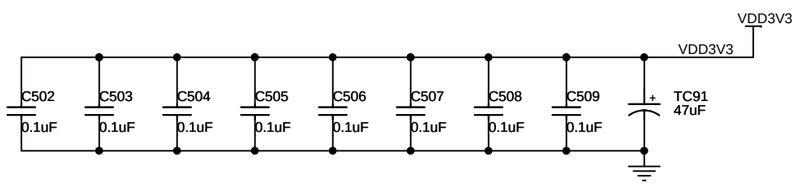
U60E
INS23867347

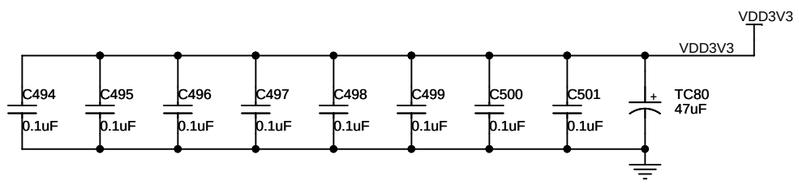




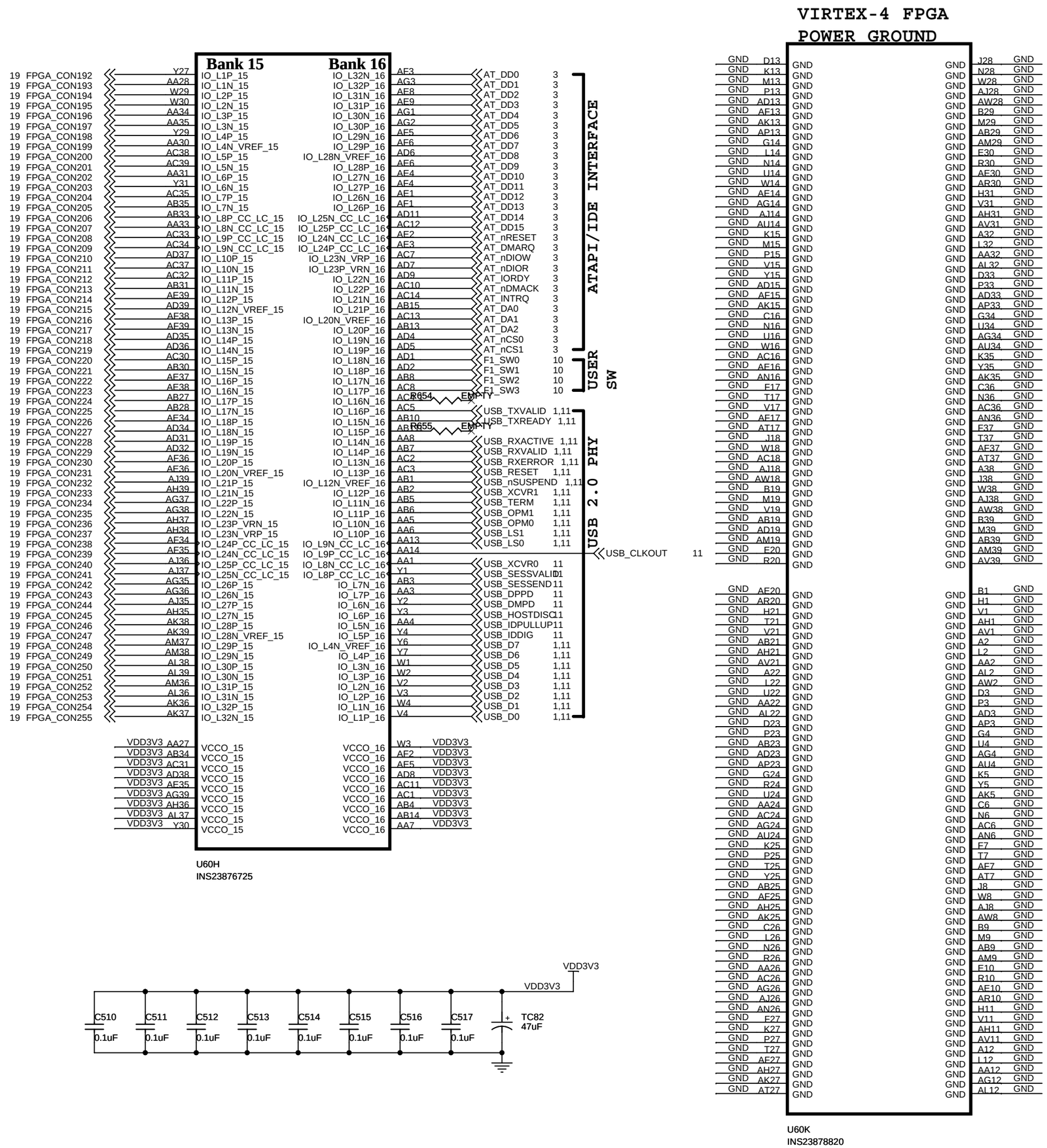
Title	SANGHWA FPGA PLATFORM FPGA1 BANK 7/8/9/10	
Size A3	Document Number <Doc>	Rev 1.0
Date: Monday, August 21, 2006	Sheet 23 of 26	



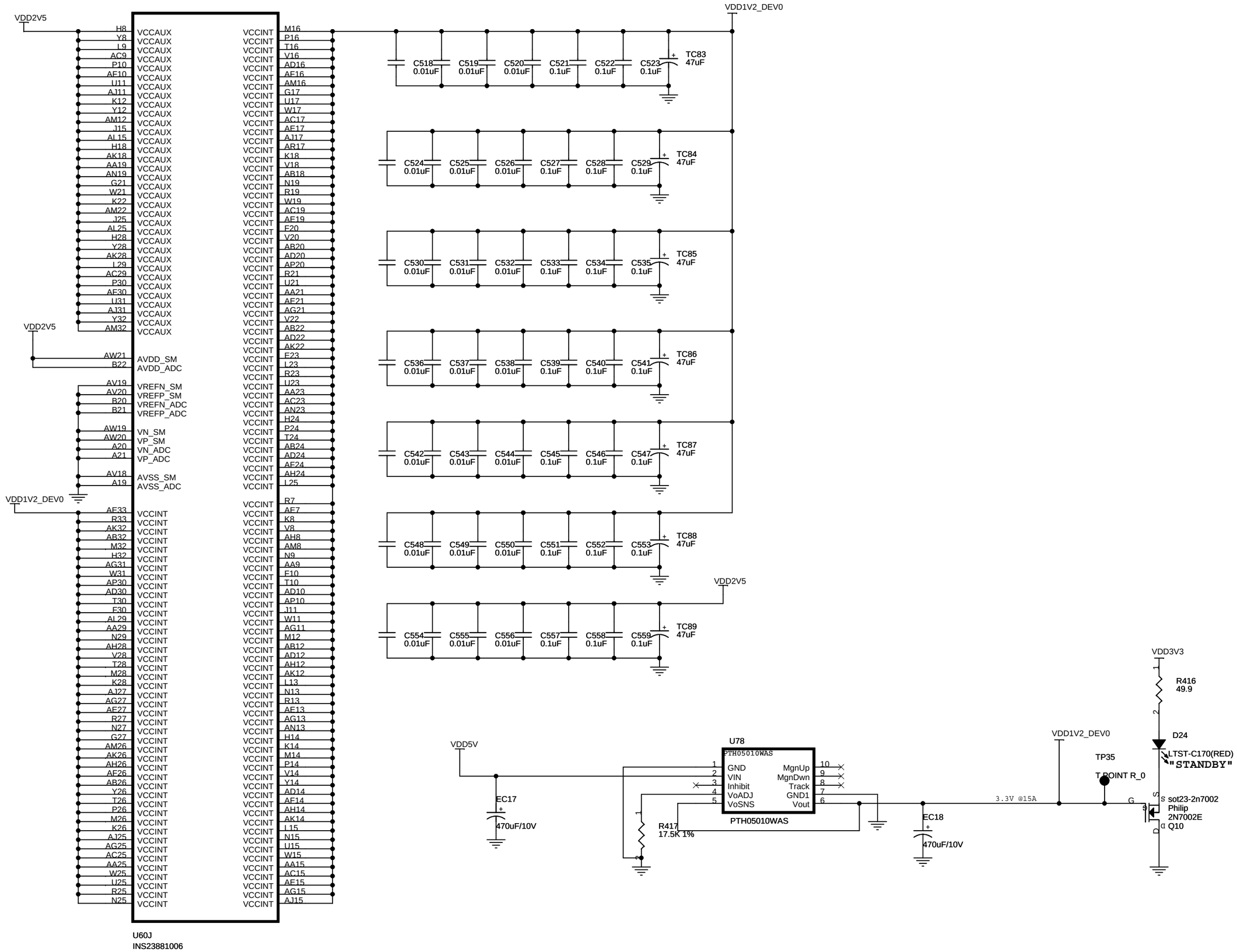




Title	SANGHWA FPGA PLATFORM FPGA1 BANK 11/12/13/14
Size A3	Document Number <Doc>
Rev	1.0
Date: Monday, August 21, 2006	Sheet 24 of 26



Title	SANGHWA FPGA PLATFORM FPGA1 BANK 15/16/GND
Size A3	Document Number <Doc>
Rev 1.0	
Date: Monday, August 21, 2006	Sheet 25 of 26



Title	SANGHWA FPGA PLATFORM FPGA1 POWER VCCO	
Size A3	Document Number <Doc>	Rev 1.0
Date: Monday, August 21, 2006	Sheet 26 of 26	