SANGHWA FPGA PLATFORM

PAGE #	DESCRIPTION
P00	TITLE PAGE (THIS)
P01	SD/MMC/TOUCH
P02	SYSTEM ACE (FPGA CONFIGURATION)
P03	NONE
P04	VIDEO
P05	MEMORY BLOCK
P06	SW/AC97
P07	ETH/USB/UART
P08	CLOCK/PLL/MULTIPLEXOR
P09	SYSTEM POWER
P10	FPGA TEST MICTOR
P11	F0 CONFIG/CLOCK
P12	F0 BANK 1/2/5/6
P13	F0 BANK 7/8/9/10
P14	F0 BANK 11/12/13/14
P15	F0 BANK 15/16/GND
P16	F0 POWER VCCO
P17	F1 CONFIG/CLOCK
P18	F1 BANK 1/2/5/7
P19	F1 BANK 7/8/9/11
P20	F1 BANK 11/12/13/15
P21	F1 BANK 15/16/GND
P22	F1 POWER VCCO

2006-7-20
DESIGNED BY DDSMURF

SANGHWA FPGA PLATFORM

Title	SANGHWA FPGA PLATFORM	
Size A3	Document Number <Doc>	Rev 1.0
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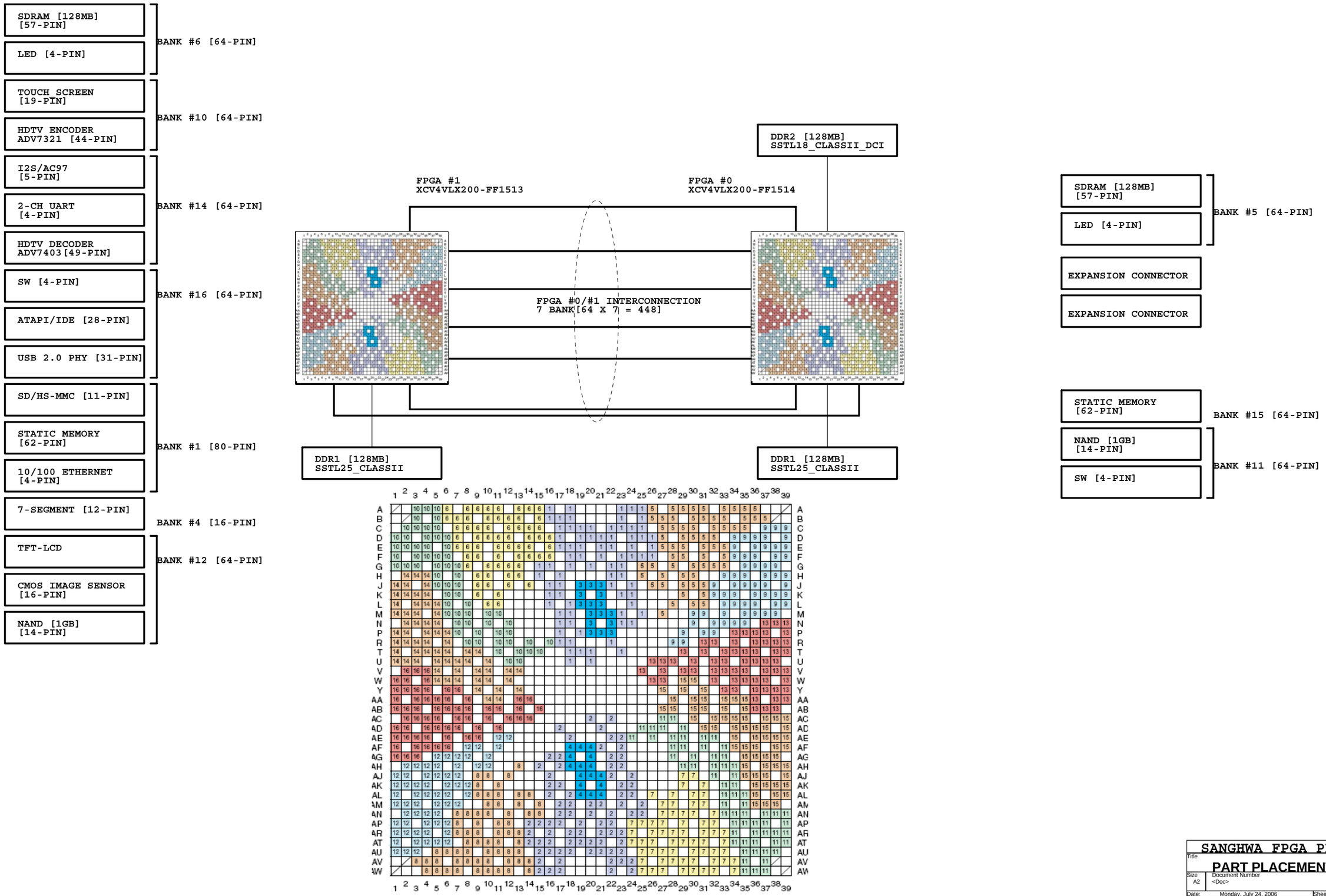
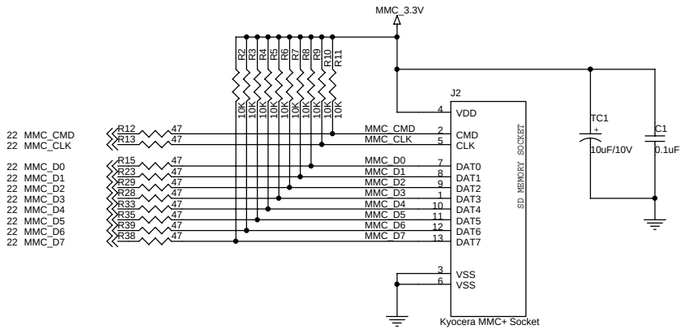
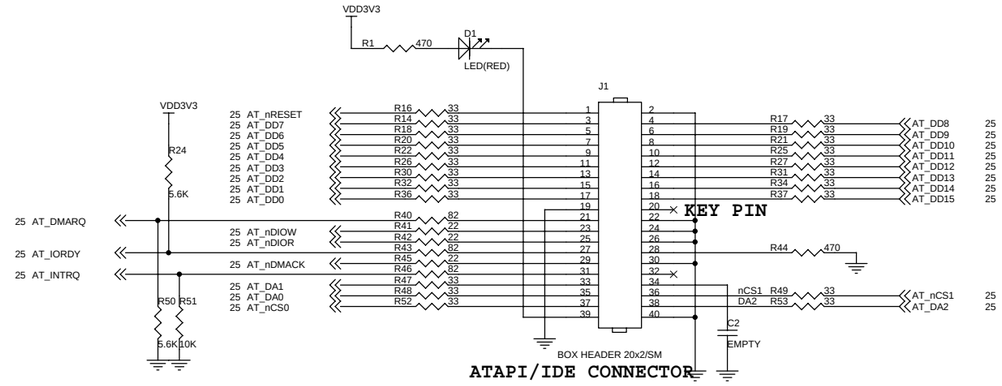
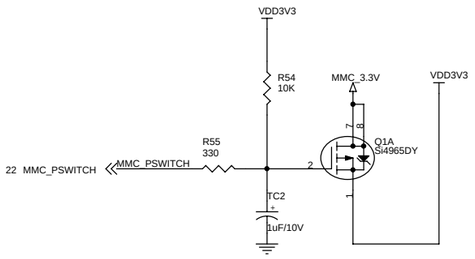


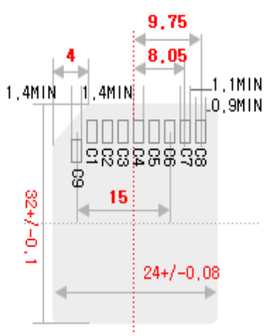
Title	SANGHWA FPGA PLATFORM PART PLACEMENT
Size A2	Document Number <Doc>
Rev	1.0
Date:	Monday, July 24, 2006
Sheet	2 of 26



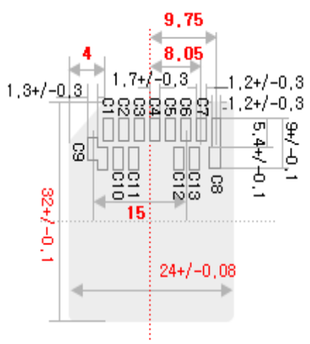




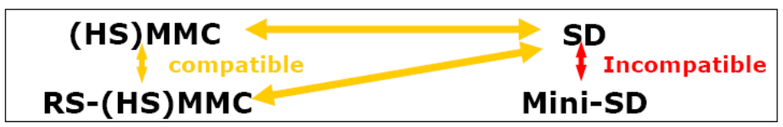
SD/HS-MMC SOCKET

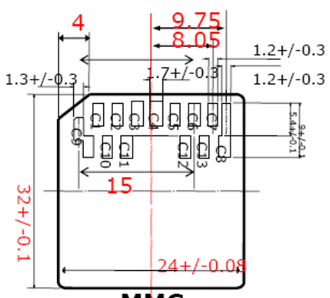


SD Card

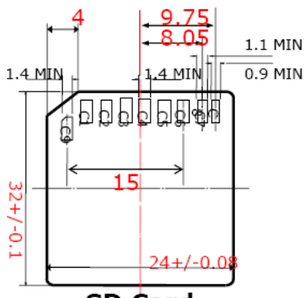


HS-MMC

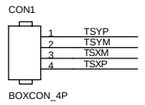




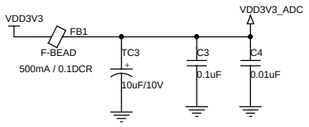
MMC

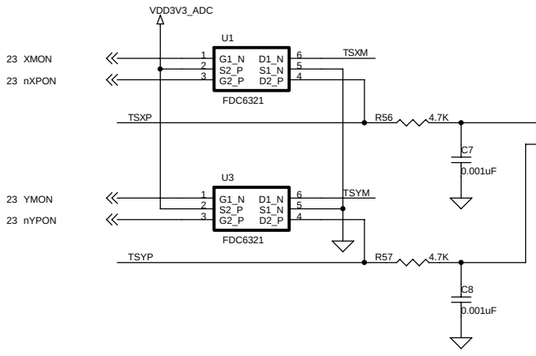


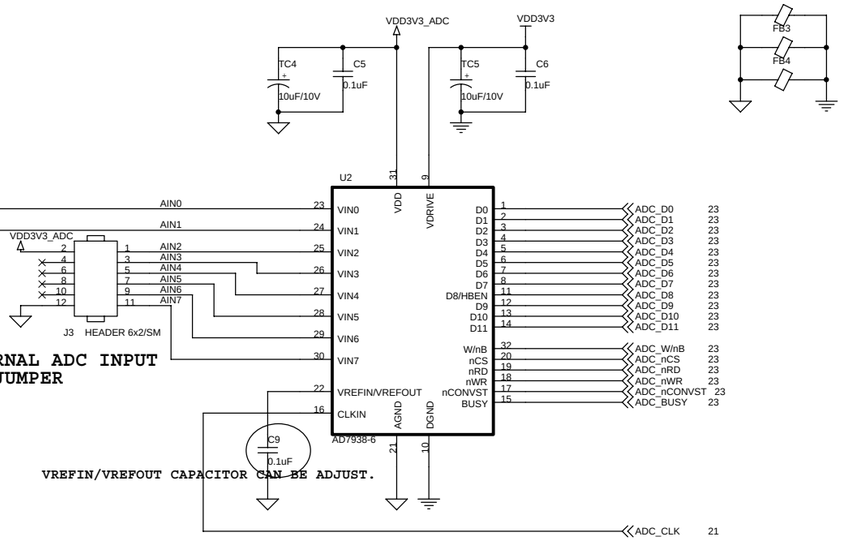
SD Card



TOUCHSCREEN CONN.
MITSHMI
M60-04-30-134P







EXTERNAL ADC INPUT
AND JUMPER

VREFIN/VREFOUT CAPACITOR CAN BE ADJUST.

SANGHWA FPGA PLATFORM

Title: SD/MMC/IDE/TOUCH SCREEN

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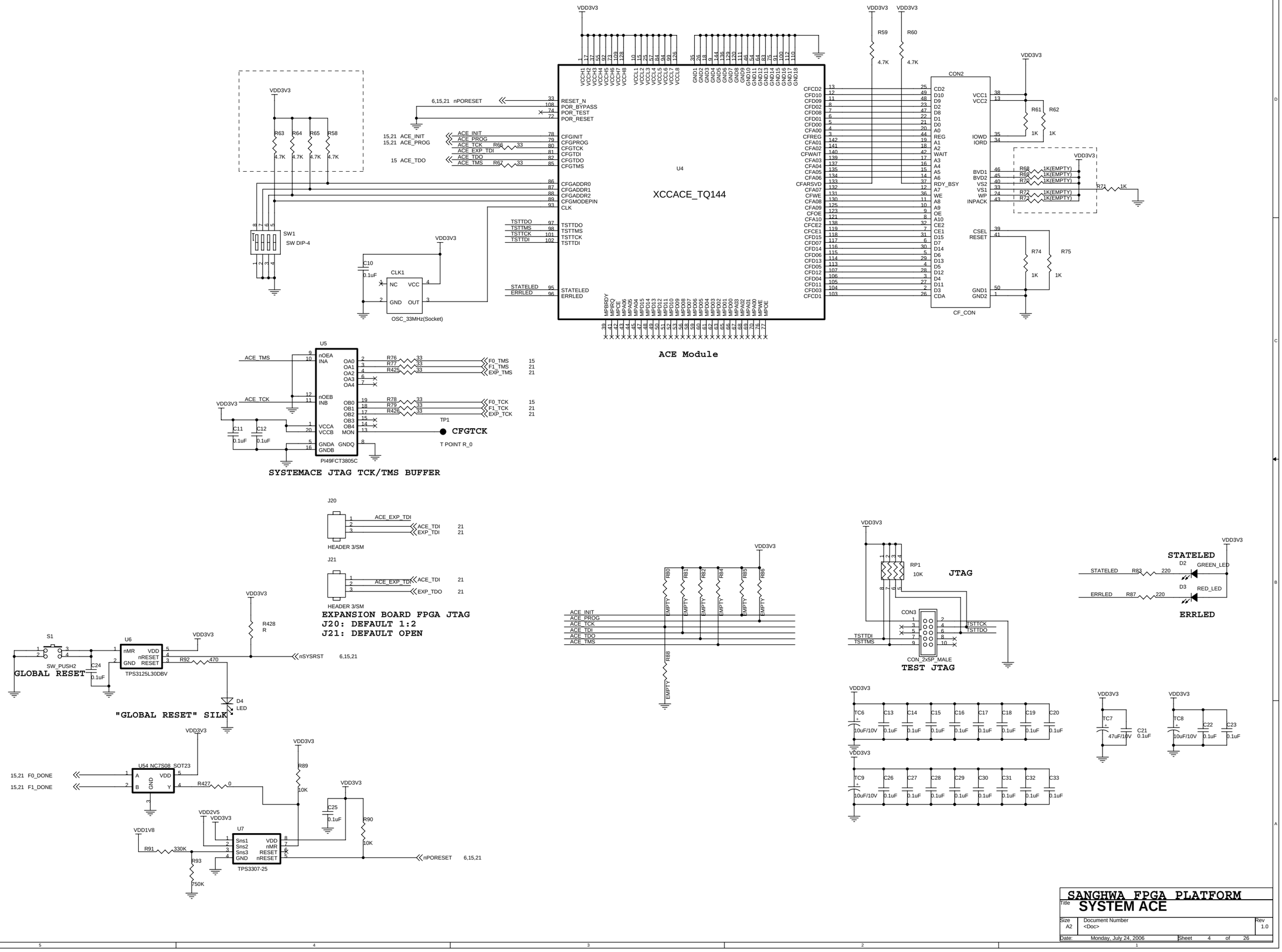
XCCACE_TQ144
U4
ACE Module
CON2
CF_CON
SW1
SW DIP-4
OSC_33MHz(Socket)
CLK1
U5
PI49FCT3805C
SYSTEMACE JTAG TCK/TMS BUFFER
J20
HEADER 3/SM
J21
HEADER 3/SM
EXPANSION BOARD FPGA JTAG
J20: DEFAULT 1:2
J21: DEFAULT OPEN
S1
SW_PUSH2
GLOBAL RESET
U6
TPS3125L30DBV
"GLOBAL RESET" SILK
U54 NC7S08 SOT23
U7
TPS3307-25
JTAG
CON3
CON_2x5P_MALE
TEST JTAG
STATELED
ERRLED
SANGHWA FPGA PLATFORM
SYSTEM ACE
Size A2
Document Number <Doc>
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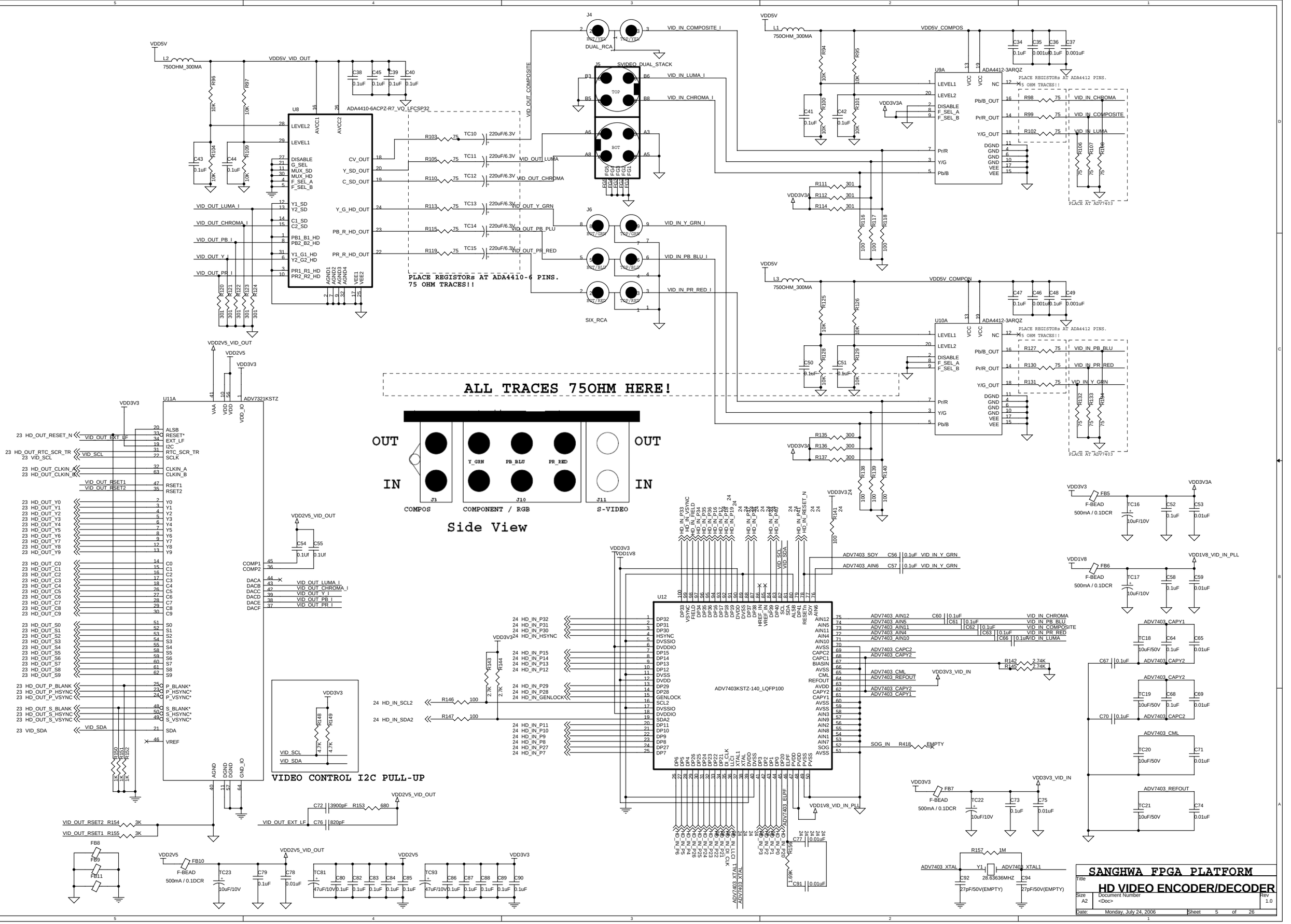
ALL TRACES 75OHM HERE!
Side View
IN
OUT
COMPOS
COMPONENT / RGB
S-VIDEO
Y_GRN
PB_BLU
PR_RED
J3
J10
J11
U8
ADA4410-6ACPZ-R7_VQ_LFCSP32
PLACE REGISTORs AT ADA4410-6 PINS.
75 OHM TRACES!!
U9A
ADA4412-3ARQZ
U10A
ADA4412-3ARQZ
PLACE REGISTORs AT ADA4412 PINS.
75 OHM TRACES!!
PLACE AT ADV7403
U11A
ADV7321KSTZ
U12
ADV7403KSTZ-140_LQFP100
VIDEO CONTROL I2C PULL-UP
SANGHWA FPGA PLATFORM
HD VIDEO ENCODER/DECODER
Size A2
Document Number <Doc>
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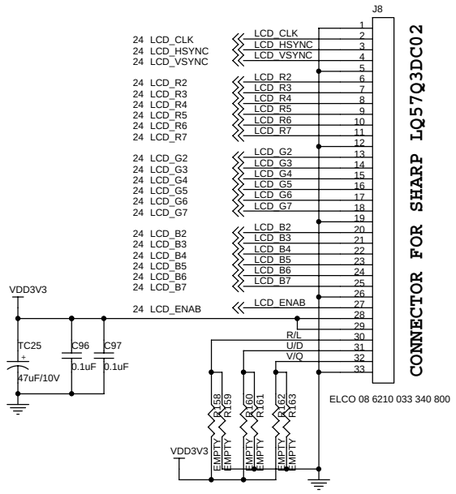
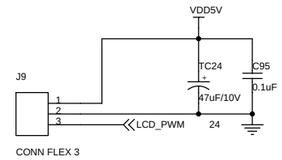
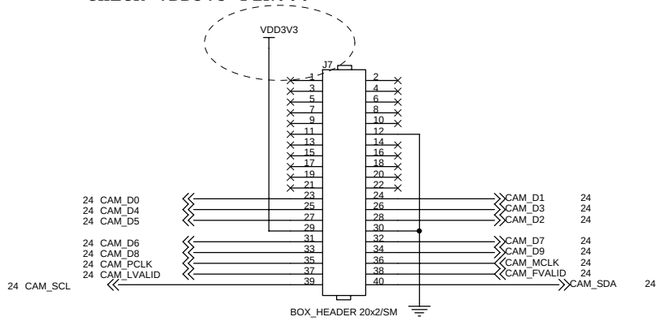




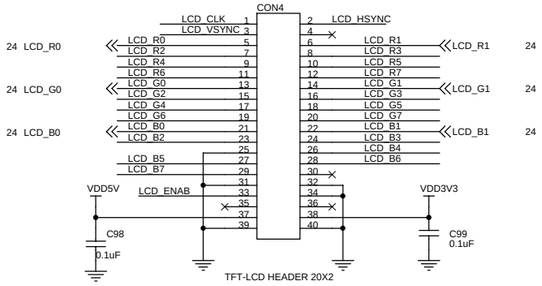
LCD BACK-LIGHT

CHECK VDD3V3 PIN!!!

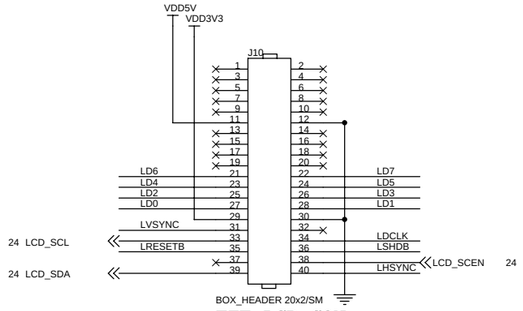


CMOS IMAGE SENSOR SOCKET

TERASIC, INC. (TRDB_DC2 BOARD)

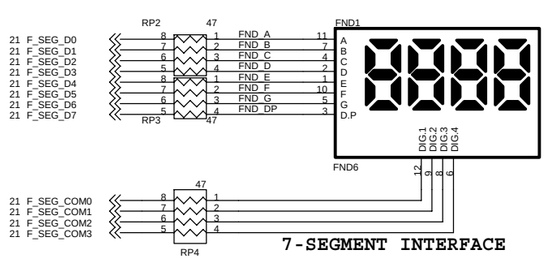


TFT-LCD CON

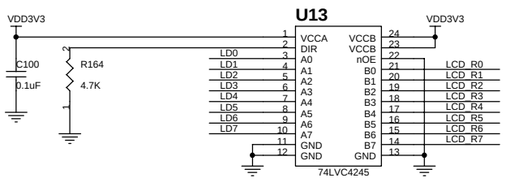


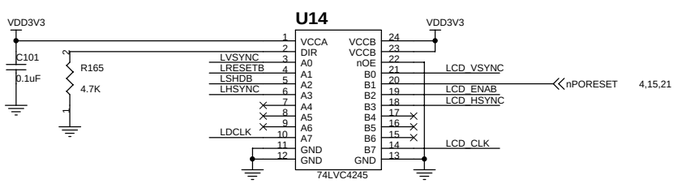
TFT-LCD CON

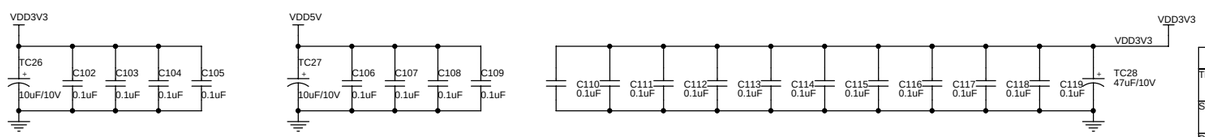
TERASIC, INC. (TRDB_LCM BOARD)



7-SEGMENT INTERFACE







SANGHWA FPGA PLATFORM

Title: CIS/TFT-LCD

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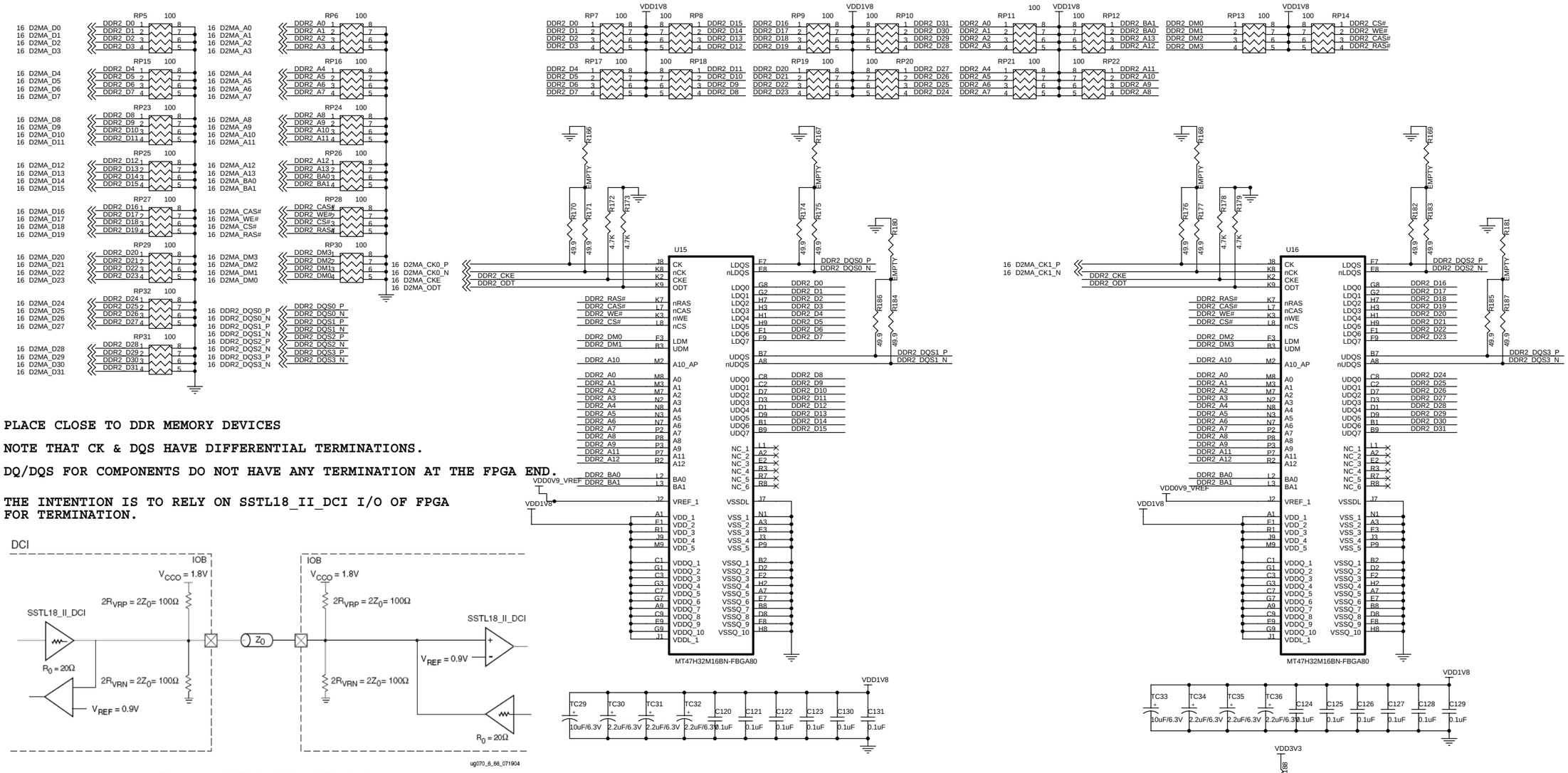


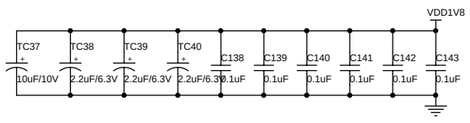
PLACE CLOSE TO DDR MEMORY DEVICES

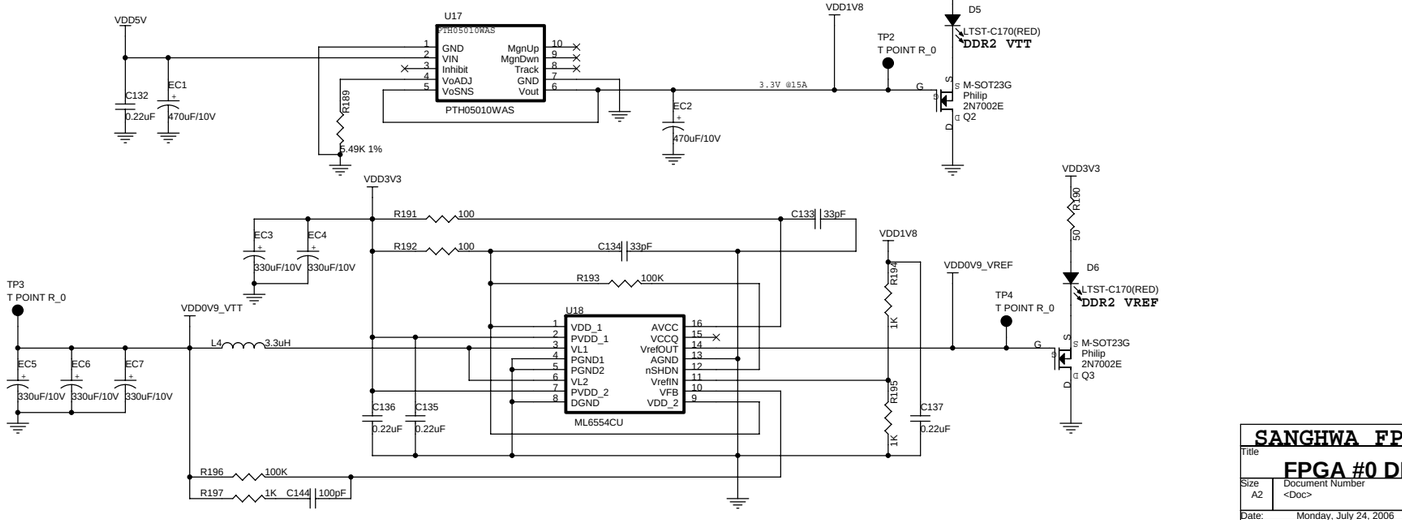
NOTE THAT CK & DQS HAVE DIFFERENTIAL TERMINATIONS.

DQ/DQS FOR COMPONENTS DO NOT HAVE ANY TERMINATION AT THE FPGA END.

THE INTENTION IS TO RELY ON SSTL18_II_DCI I/O OF FPGA FOR TERMINATION.

Figure 6-68: **SSTL (1.8V) Class II Termination**





SANGHWA FPGA PLATFORM			
Title **FPGA #0 DDR2 SDRAM**			
Size A2	Document Number <Doc>		Rev 1.0
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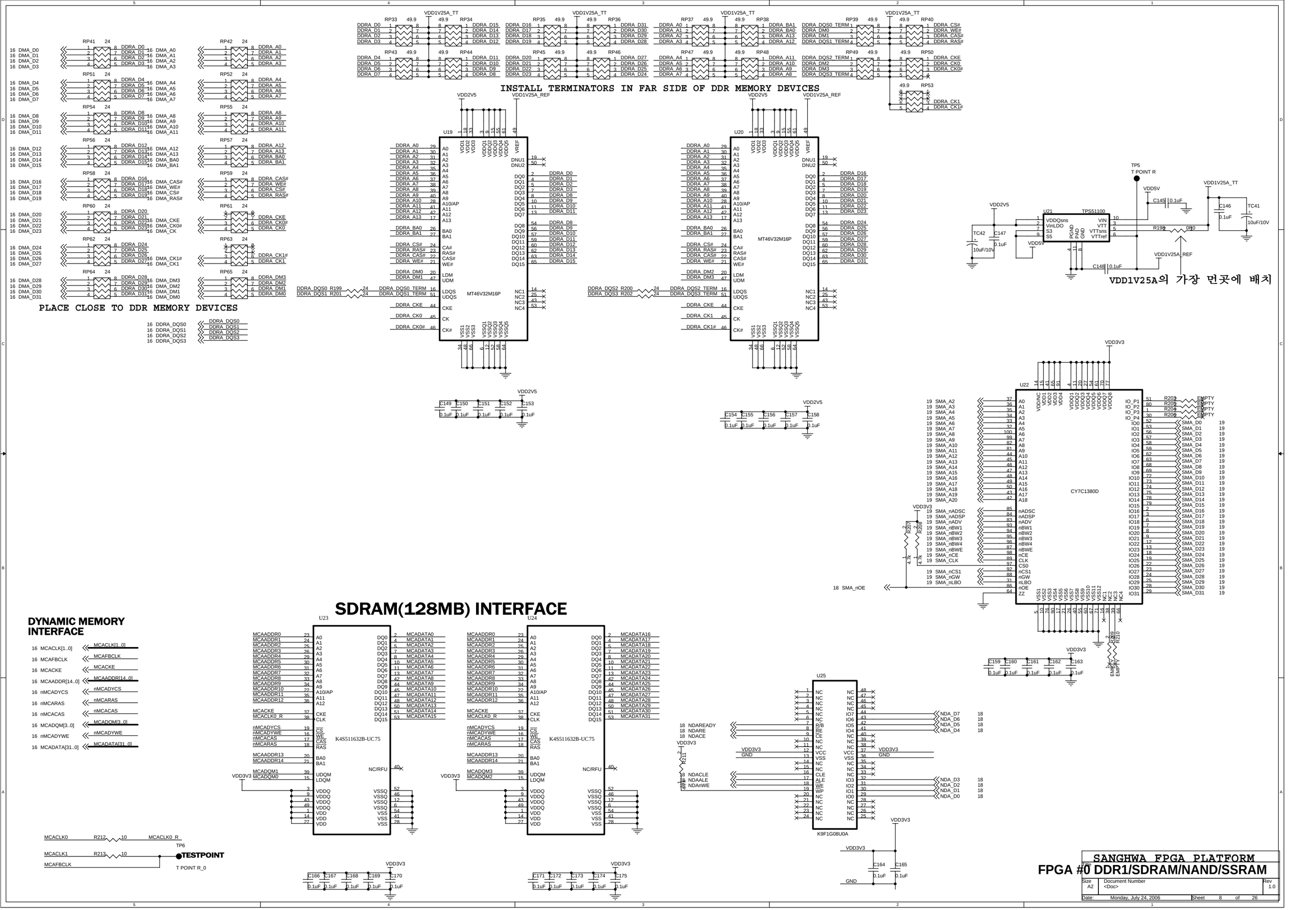
INSTALL TERMINATORS IN FAR SIDE OF DDR MEMORY DEVICES
PLACE CLOSE TO DDR MEMORY DEVICES
VDD1V25A의 가장 먼곳에 배치
DYNAMIC MEMORY INTERFACE
SDRAM(128MB) INTERFACE
U19 MT46V32M16P
U20 MT46V32M16P
U21 TPS51100
U22 CY7C1380D
U23 K4S511632B-UC75
U24 K4S511632B-UC75
U25 K9F1G08U0A
TESTPOINT
SANGHWA FPGA PLATFORM
FPGA #0 DDR1/SDRAM/NAND/SSRAM
Size A2
Document Number <Doc>
Rev 1.0
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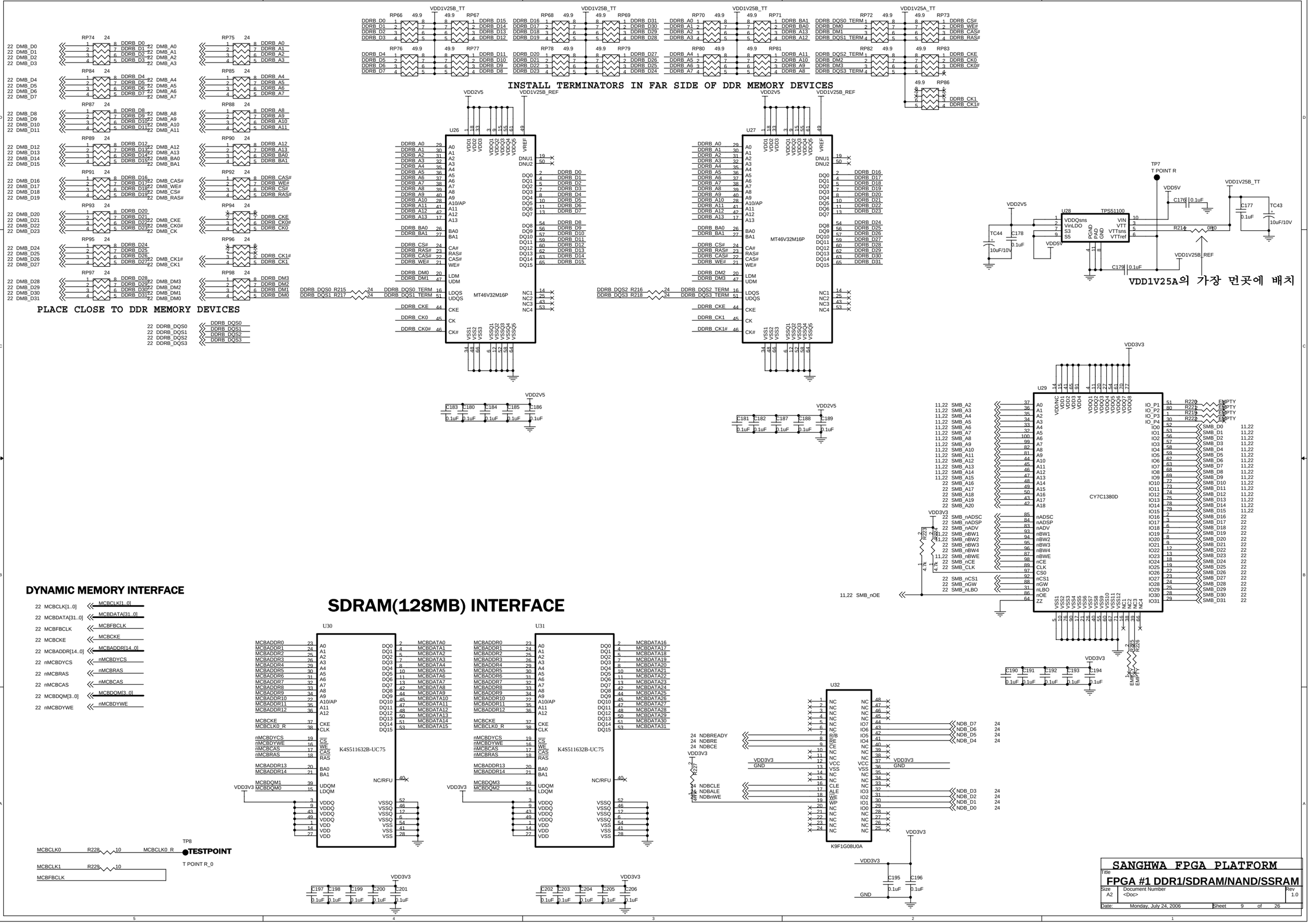
INSTALL TERMINATORS IN FAR SIDE OF DDR MEMORY DEVICES
PLACE CLOSE TO DDR MEMORY DEVICES
VDD1V25A의 가장 먼곳에 배치
DYNAMIC MEMORY INTERFACE
SDRAM(128MB) INTERFACE
U26
U27
MT46V32M16P
U28
TPS51100
U29
CY7C1380D
U30
U31
K4S511632B-UC75
U32
K9F1G08U0A
TP7
T POINT R
TP8
TESTPOINT
T POINT R_0
SANGHWA FPGA PLATFORM
FPGA #1 DDR1/SDRAM/NAND/SSRAM
Size A2
Document Number <Doc>
Rev 1.0
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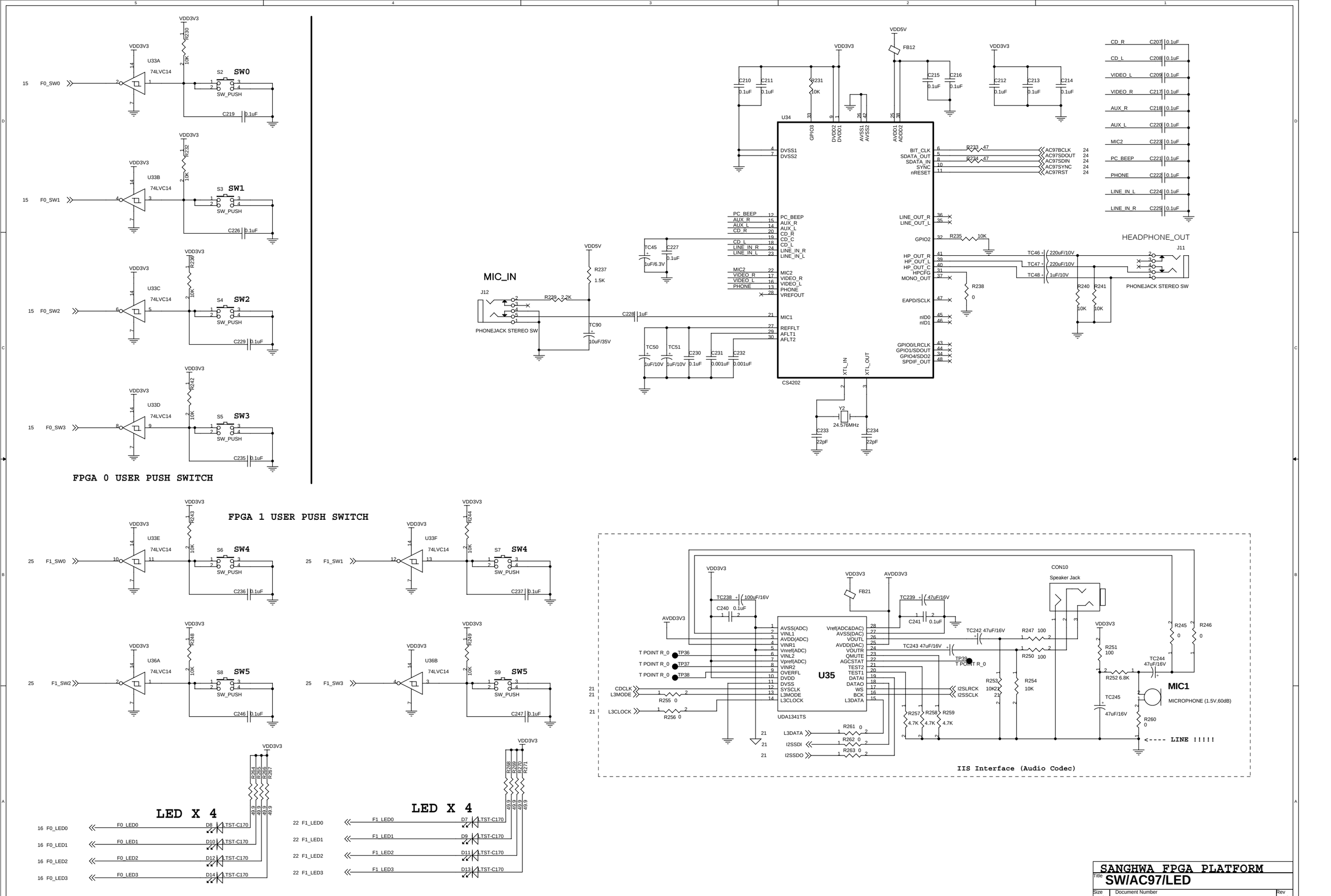
FPGA 0 USER PUSH SWITCH
FPGA 1 USER PUSH SWITCH
SW0
SW1
SW2
SW3
SW4
SW5
SW_PUSH
74LVC14
F0_SW0
F0_SW1
F0_SW2
F0_SW3
F1_SW0
F1_SW1
F1_SW2
F1_SW3
LED X 4
F0_LED0
F0_LED1
F0_LED2
F0_LED3
F1_LED0
F1_LED1
F1_LED2
F1_LED3
LTST-C170
MIC_IN
PHONEJACK STEREO SW
HEADPHONE_OUT
CS4202
U34
VDD3V3
VDD5V
FB12
Y2
24.576MHz
U35
UDA1341TS
CON10
Speaker Jack
MIC1
MICROPHONE (1.5V,60dB)
<---- LINE !!!!!
IIS Interface (Audio Codec)
SANGHWA FPGA PLATFORM
SW/AC97/LED
Size A2
Document Number <Doc>
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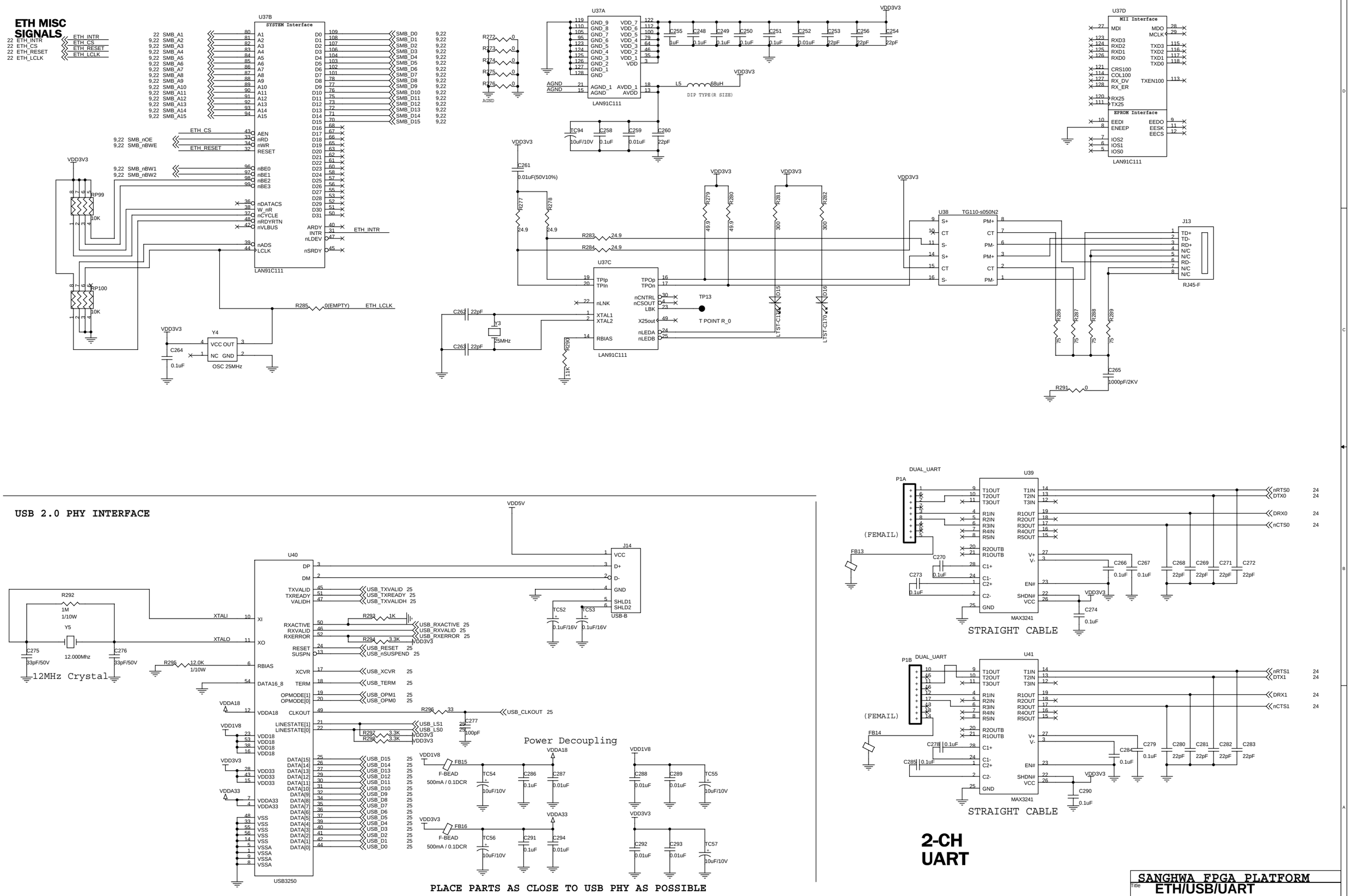
ETH MISC SIGNALS
22 ETH_INTR
22 ETH_CS
22 ETH_RESET
22 ETH_LCLK
U37B
SYSTEM Interface
LAN91C111
U37A
LAN91C111
U37D
MII Interface
EPROM Interface
LAN91C111
U37C
LAN91C111
U38
TG110-s050N2
J13
RJ45-F
Y4
OSC 25MHz
Y3
25MHz
TP13
T POINT R_0
VDD3V3
USB 2.0 PHY INTERFACE
U40
USB3250
J14
USB-B
12MHz Crystal
Power Decoupling
PLACE PARTS AS CLOSE TO USB PHY AS POSSIBLE
DUAL_UART
P1A
U39
MAX3241
STRAIGHT CABLE
P1B
U41
MAX3241
STRAIGHT CABLE
2-CH UART
SANGHWA FPGA PLATFORM
ETH/USB/UART
Size A2
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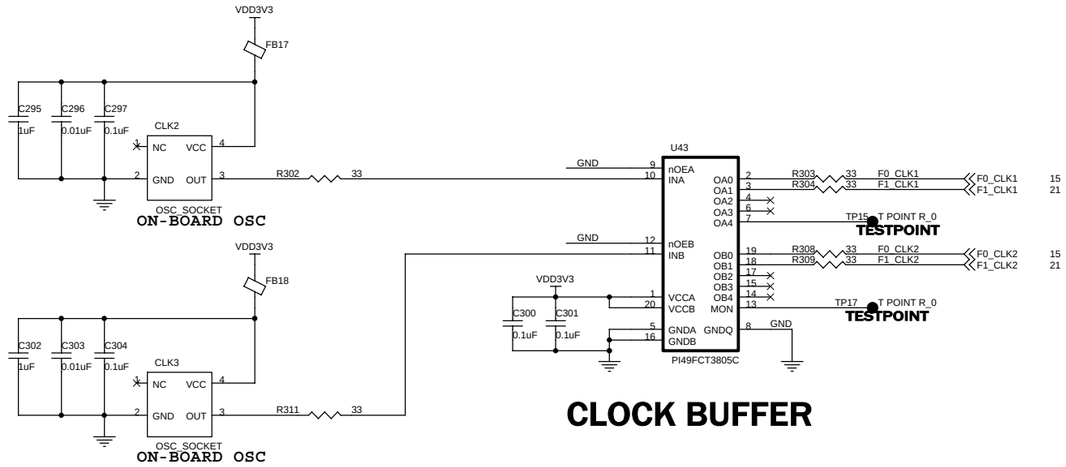
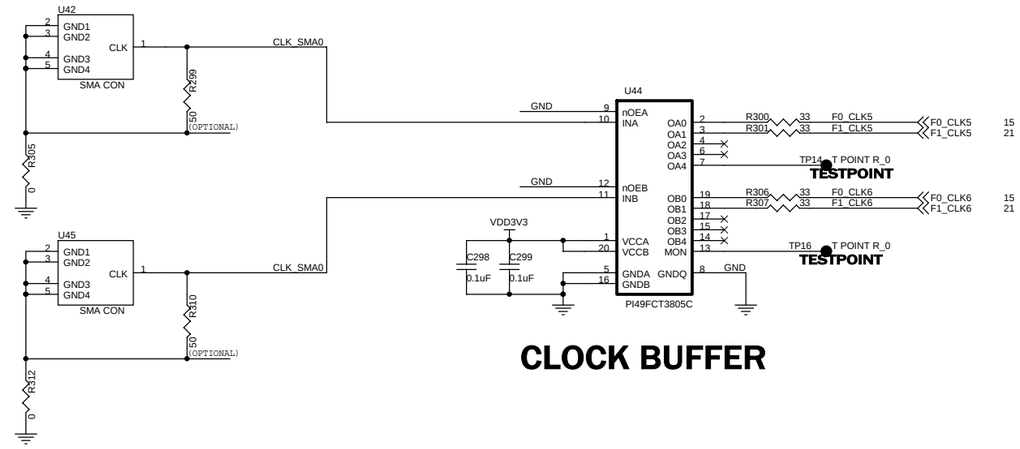


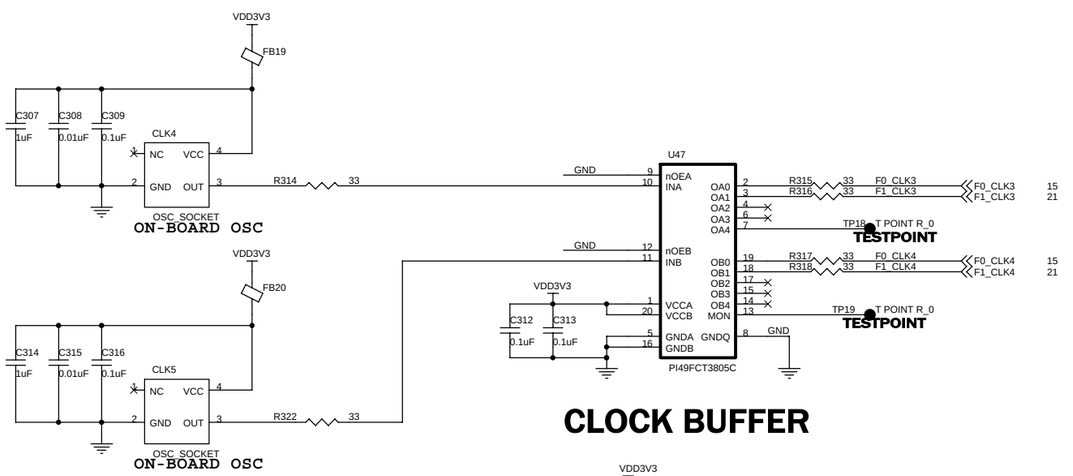
CLOCK BUFFER



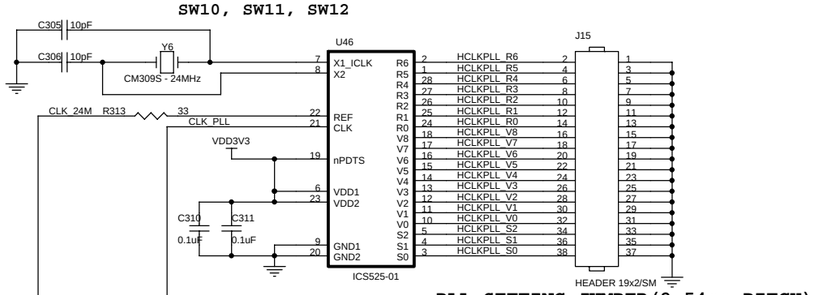
CLOCK BUFFER

2006-3-4 부품 제거

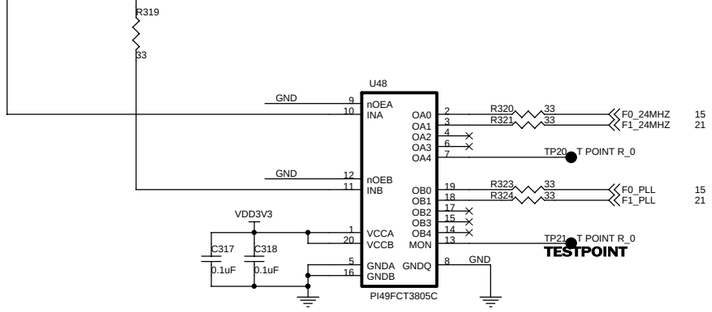
SW10, SW11, SW12

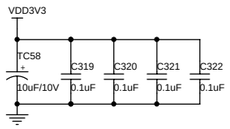


CLOCK BUFFER



PLL SETTING JUMPER(2.54mm PITCH)





SANGHWA FPGA PLATFORM

Title **CLOCK/PLL/MULTIPLEXOR**

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A2	<Doc>	1.0

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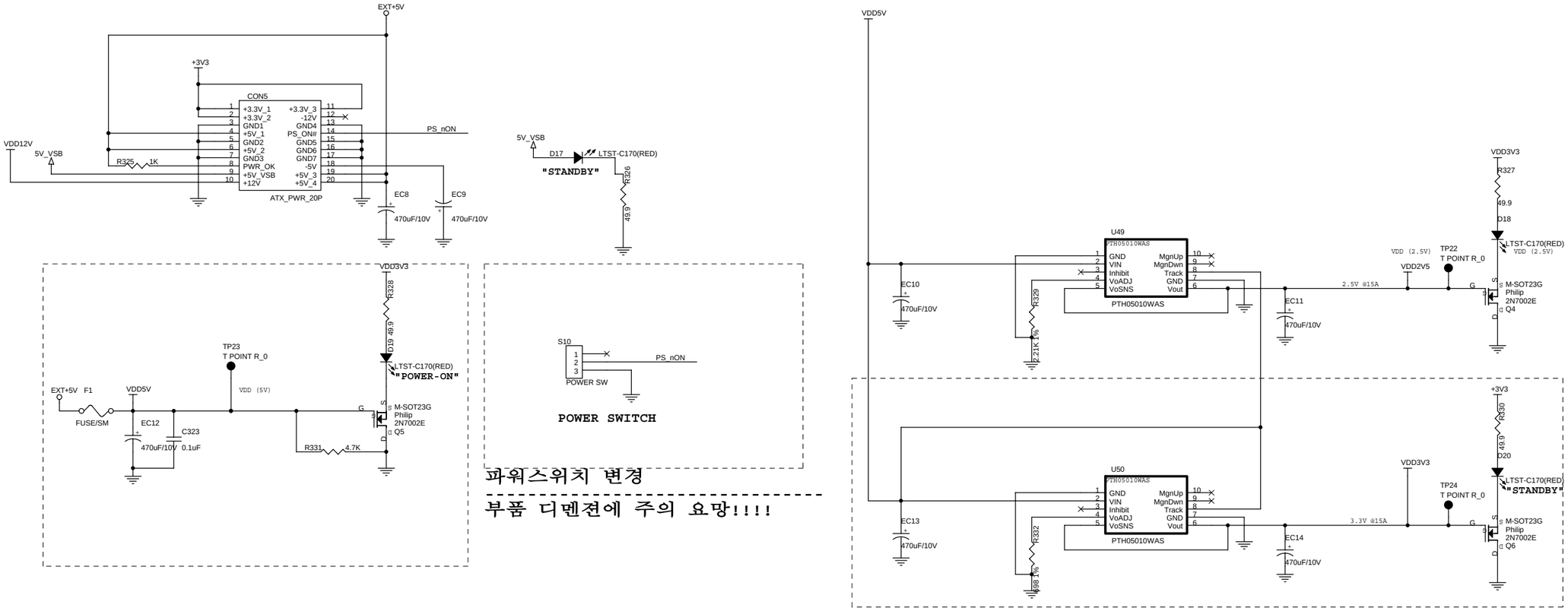
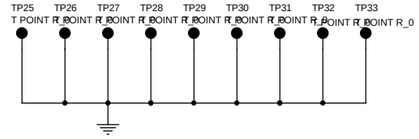


파워스위치 변경

부품 디멘젼에 주의 요망!!!!

GND Point



Title	SANGHWA FPGA PLATFORM SYSTEM POWER	
Size A2	Document Number <Doc>	Rev 1.0
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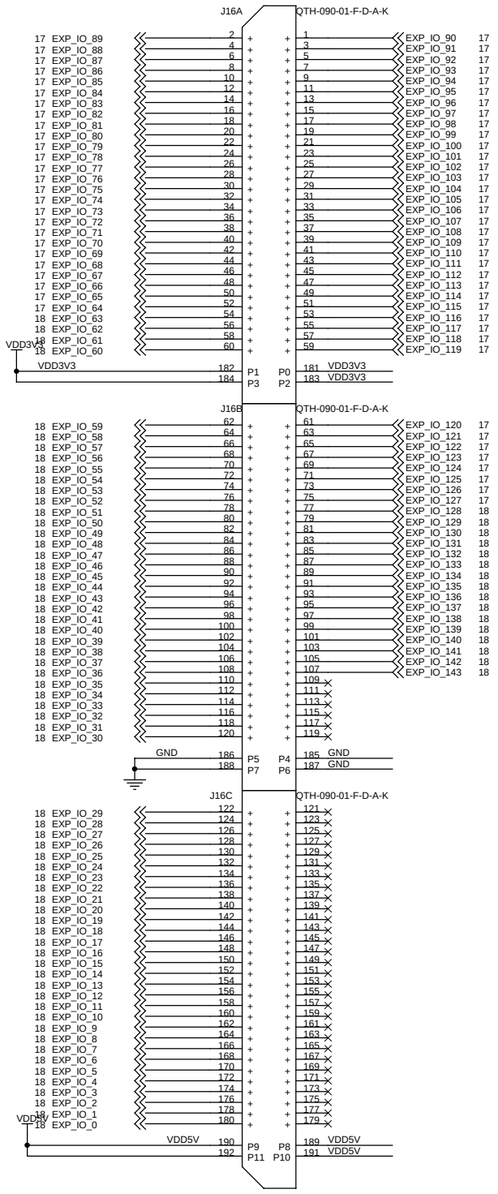
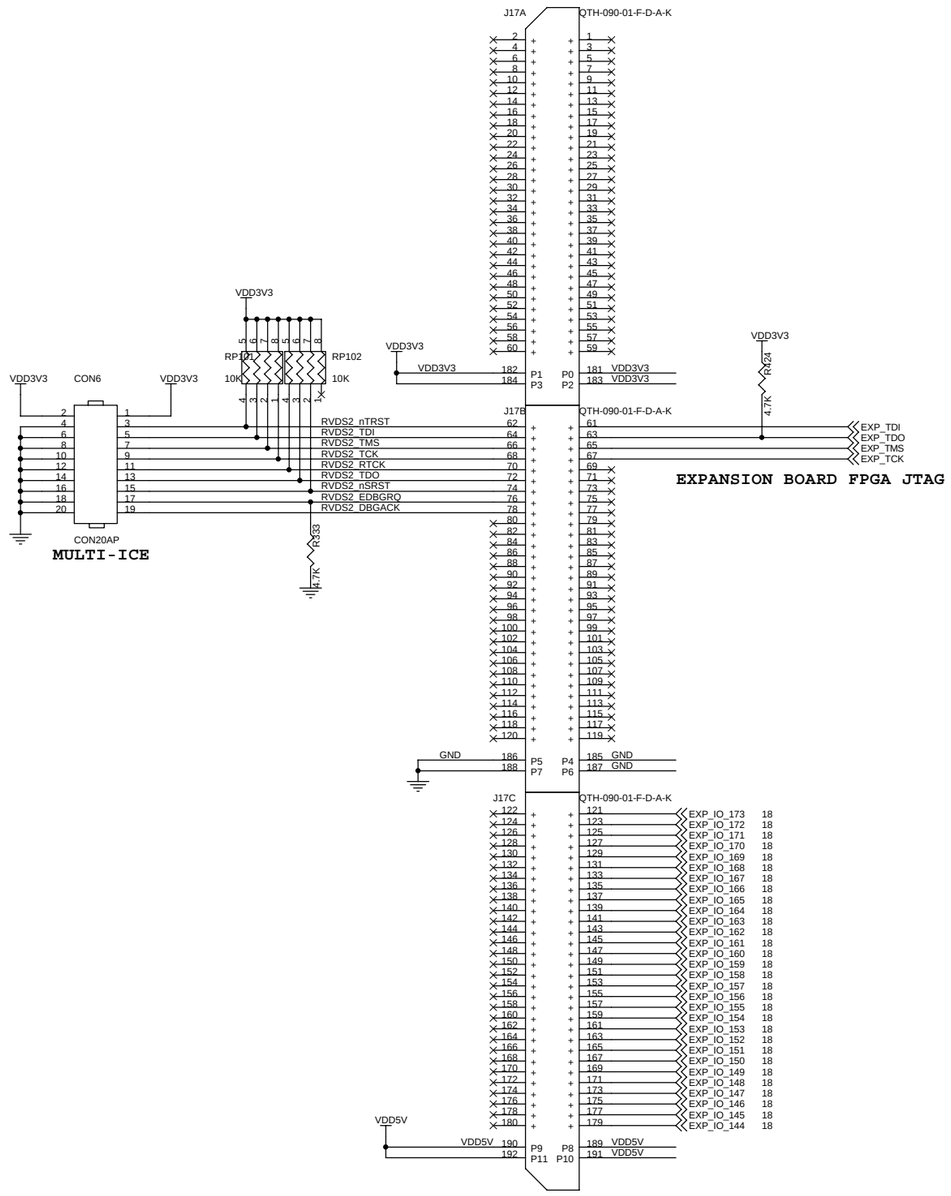
EXPANSION SLOT FOR FPGA #0



EXP2



EXP1

SANGHWA FPGA PLATFORM		
Title: FPGA #0 EXPANSION CONNECTOR		
Size: A2	Document Number: <Doc>	Rev: 1.0
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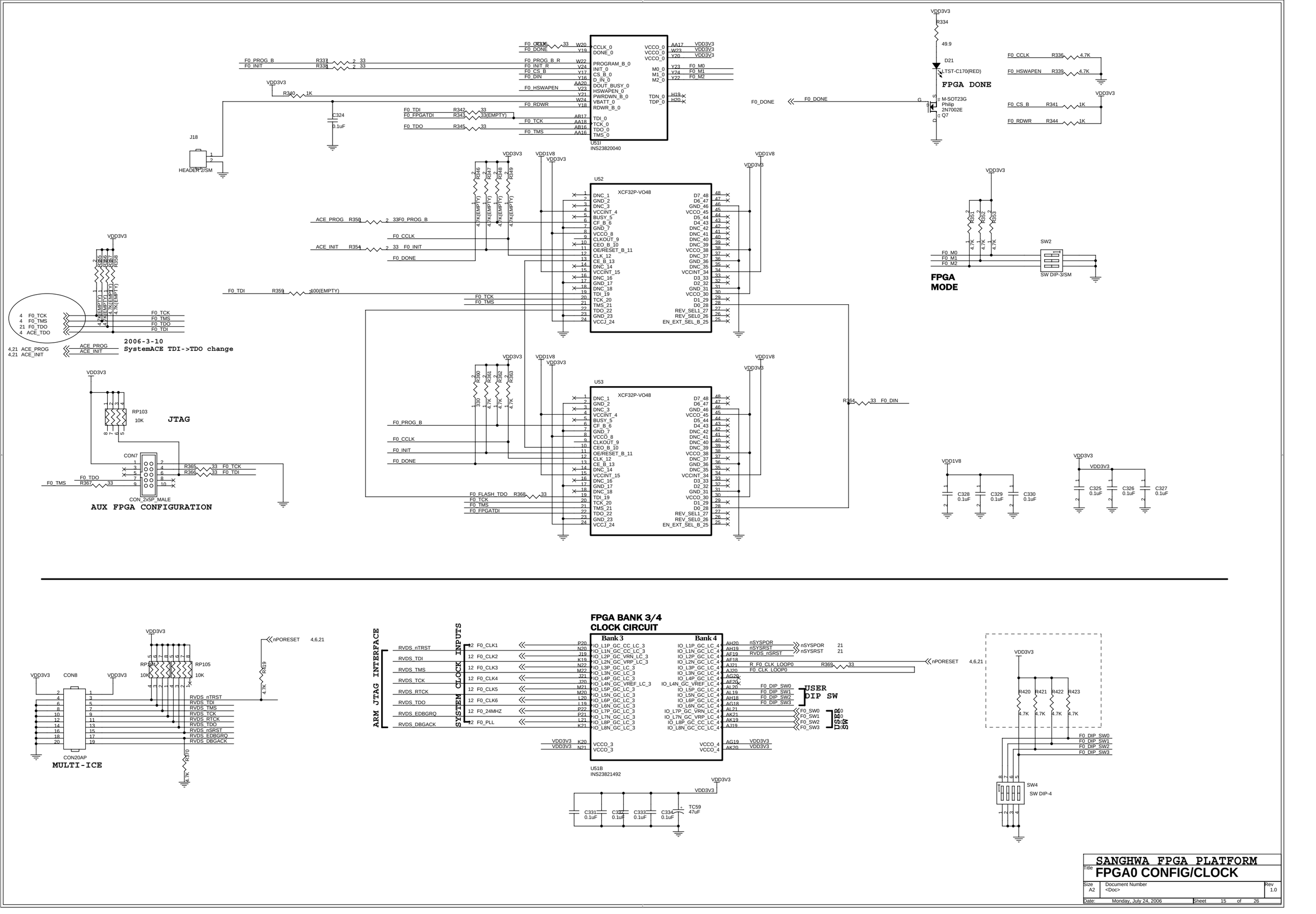
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U52
XCF32P-VO48
U53
XCF32P-VO48
FPGA DONE
FPGA MODE
JTAG
AUX FPGA CONFIGURATION
2006-3-10
SystemACE TDI->TDO change
MULTI-ICE
FPGA BANK 3/4
CLOCK CIRCUIT
Bank 3
Bank 4
ARM JTAG INTERFACE
SYSTEM CLOCK INPUTS
USER DIP SW
U51B
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SANGHWA FPGA PLATFORM
FPGA0 CONFIG/CLOCK
Size A2
Document Number <Doc>
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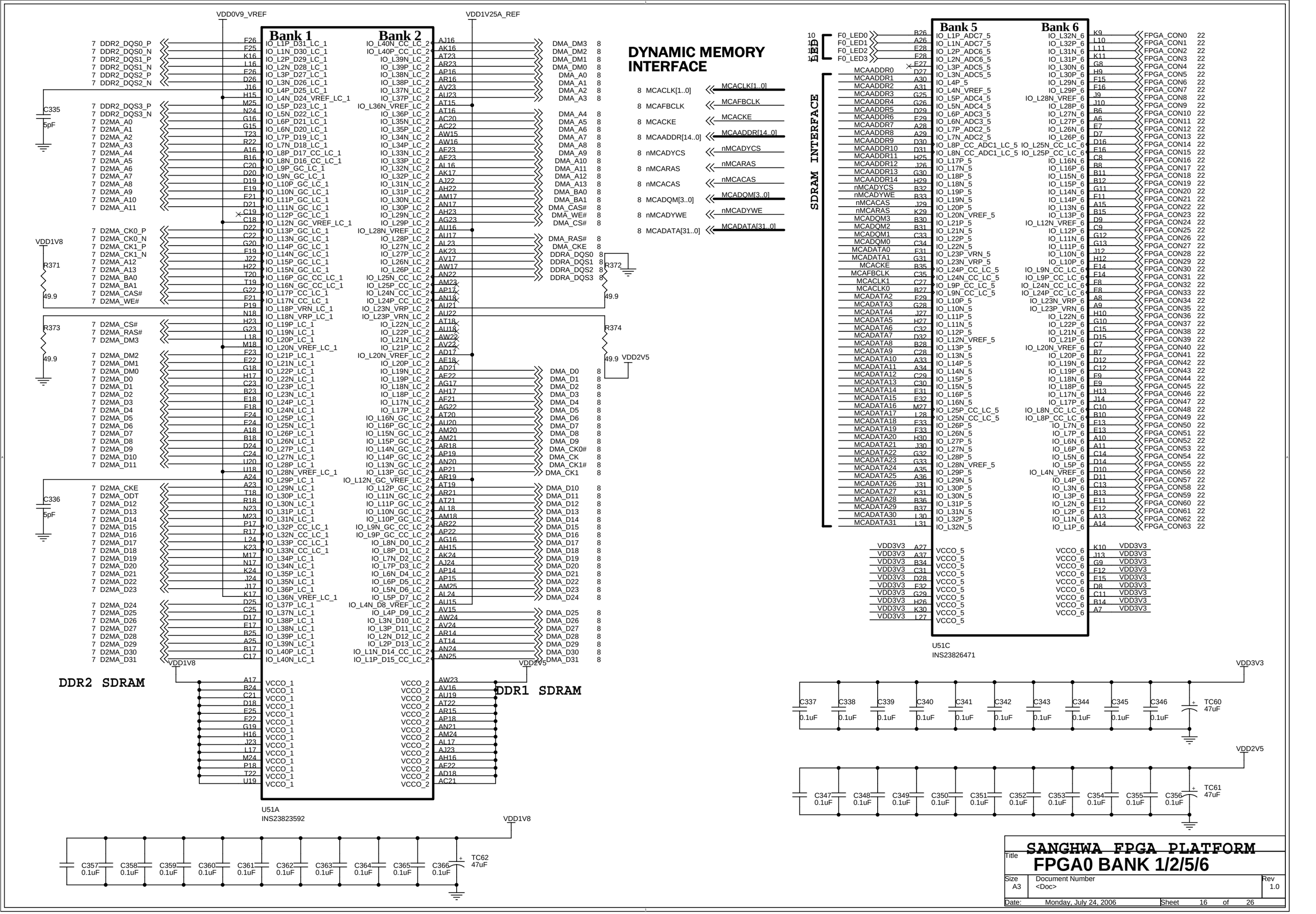
DYNAMIC MEMORY INTERFACE
Bank 1
Bank 2
DDR2 SDRAM
DDR1 SDRAM
U51A
INS23823592
Bank 5
Bank 6
U51C
INS23826471
SDRAM INTERFACE
LED
VDD0V9_VREF
VDD1V25A_REF
VDD1V8
VDD2V5
VDD3V3
C335 5pF
C336 5pF
R371 49.9
R372 49.9
R373 49.9
R374 49.9
TC62 47uF
TC60 47uF
TC61 47uF
SANGHWA FPGA PLATFORM
FPGA0 BANK 1/2/5/6
Title
Size A3
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FPGA INTERCONNECTION

Bank 7 / Bank 8

		Bank 7	Bank 8			
23	FPGA_CON384	AT33	IO_L1P_7	IO_L32N_8	AW10	FPGA_CON320 23
23	FPGA_CON385	AR33	IO_L1N_7	IO_L32P_8	AW11	FPGA_CON321 23
23	FPGA_CON386	AJ30	IO_L2P_7	IO_L31N_8	AV14	FPGA_CON322 23
23	FPGA_CON387	AK31	IO_L2N_7	IO_L31P_8	AW14	FPGA_CON323 23
23	FPGA_CON388	AM30	IO_L3P_7	IO_L30N_8	AU10	FPGA_CON324 23
23	FPGA_CON389	AL30	IO_L3N_7	IO_L30P_8	AV10	FPGA_CON325 23
23	FPGA_CON390	AM31	IO_L4P_7	IO_L29N_8	AR13	FPGA_CON326 23
23	FPGA_CON391	AL31	IO_L4N_VREF_7	IO_L29P_8	AT13	FPGA_CON327 23
23	FPGA_CON392	AP24	IO_L5P_7	IO_L28N_VREF_8	AR11	FPGA_CON328 23
23	FPGA_CON393	AR24	IO_L5N_7	IO_L28P_8	AT11	FPGA_CON329 23
23	FPGA_CON394	AP32	IO_L6P_7	IO_L27N_8	AM13	FPGA_CON330 23
23	FPGA_CON395	AN32	IO_L6N_7	IO_L27P_8	AN14	FPGA_CON331 23
23	FPGA_CON396	AN30	IO_L7P_7	IO_L26N_8	AV9	FPGA_CON332 23
23	FPGA_CON397	AP31	IO_L7N_7	IO_L26P_8	AW9	FPGA_CON333 23
23	FPGA_CON398	AK29	IO_L8P_CC_LC_7	IO_L25N_CC_LC_8	AV12	FPGA_CON334 23
23	FPGA_CON399	AJ29	IO_L8N_CC_LC_7	IO_L25P_CC_LC_8	AW12	FPGA_CON335 23
23	FPGA_CON400	AT24	IO_L9P_CC_LC_7	IO_L24N_CC_LC_8	AV7	FPGA_CON336 23
23	FPGA_CON401	AT25	IO_L9N_CC_LC_7	IO_L24P_CC_LC_8	AV8	FPGA_CON337 23
23	FPGA_CON402	AW34	IO_L10P_7	IO_L23N_VRP_8	AU11	FPGA_CON338 23
23	FPGA_CON403	AV34	IO_L10N_7	IO_L23P_VRN_8	AU12	FPGA_CON339 23
23	FPGA_CON404	AW30	IO_L11P_7	IO_L22N_8	AT9	FPGA_CON340 23
23	FPGA_CON405	AW31	IO_L11N_7	IO_L22P_8	AT10	FPGA_CON341 23
23	FPGA_CON406	AV33	IO_L12P_7	IO_L21N_8	AU13	FPGA_CON342 23
23	FPGA_CON407	AU33	IO_L12N_VREF_7	IO_L21P_8	AV13	FPGA_CON343 23
23	FPGA_CON408	AP25	IO_L13P_7	IO_L20N_VREF_8	AP9	FPGA_CON344 23
23	FPGA_CON409	AP26	IO_L13N_7	IO_L20P_8	AR9	FPGA_CON345 23
23	FPGA_CON410	AT31	IO_L14P_7	IO_L19N_8	AP12	FPGA_CON346 23
23	FPGA_CON411	AT30	IO_L14N_7	IO_L19P_8	AR12	FPGA_CON347 23
23	FPGA_CON412	AU25	IO_L15P_7	IO_L18N_8	AT8	FPGA_CON348 23
23	FPGA_CON413	AV25	IO_L15N_7	IO_L18P_8	AU8	FPGA_CON349 23
23	FPGA_CON414	AR31	IO_L16P_7	IO_L17N_8	AL13	FPGA_CON350 23
23	FPGA_CON415	AR32	IO_L16N_7	IO_L17P_8	AL14	FPGA_CON351 23
23	FPGA_CON416	AL26	IO_L17P_7	IO_L16N_8	AU6	FPGA_CON352 23
23	FPGA_CON417	AM27	IO_L17N_7	IO_L16P_8	AU7	FPGA_CON353 23
23	FPGA_CON418	AU31	IO_L18P_7	IO_L15N_8	AP11	FPGA_CON354 23
23	FPGA_CON419	AU32	IO_L18N_7	IO_L15P_8	AN12	FPGA_CON355 23
23	FPGA_CON420	AV28	IO_L19P_7	IO_L14N_8	AJ12	FPGA_CON356 23
23	FPGA_CON421	AU28	IO_L19N_7	IO_L14P_8	AH13	FPGA_CON357 23
23	FPGA_CON422	AW32	IO_L20P_7	IO_L13N_8	AN10	FPGA_CON358 23
23	FPGA_CON423	AV32	IO_L20N_VREF_7	IO_L13P_8	AM11	FPGA_CON359 23
23	FPGA_CON424	AW25	IO_L21P_7	IO_L12N_VREF_8	AL10	FPGA_CON360 23
23	FPGA_CON425	AW26	IO_L21N_7	IO_L12P_8	AM10	FPGA_CON361 23
23	FPGA_CON426	AP29	IO_L22P_7	IO_L11N_8	AW6	FPGA_CON362 23
23	FPGA_CON427	AN29	IO_L22N_7	IO_L11P_8	AW7	FPGA_CON363 23
23	FPGA_CON428	AN27	IO_L23P_VRN_7	IO_L10N_8	AW4	FPGA_CON364 23
23	FPGA_CON429	AN28	IO_L23N_VRP_7	IO_L10P_8	AW5	FPGA_CON365 23
23	FPGA_CON430	AL28	IO_L24P_CC_LC_7	IO_L9N_CC_LC_8	AK11	FPGA_CON366 23
23	FPGA_CON431	AM28	IO_L24N_CC_LC_7	IO_L9P_CC_LC_8	AL11	FPGA_CON367 23
23	FPGA_CON432	AP27	IO_L25P_CC_SM7_LC_7	IO_L8N_CC_LC_8	AV3	FPGA_CON368 23
23	FPGA_CON433	AR27	IO_L25N_CC_SM7_LC_7	IO_L8P_CC_LC_8	AV4	FPGA_CON369 23
23	FPGA_CON434	AV30	IO_L26P_SM6_7	IO_L7N_8	AR7	FPGA_CON370 23
23	FPGA_CON435	AU30	IO_L26N_SM6_7	IO_L7P_8	AR8	FPGA_CON371 23
23	FPGA_CON436	AR26	IO_L27P_SM5_7	IO_L6N_8	AN7	FPGA_CON372 23
23	FPGA_CON437	AT26	IO_L27N_SM5_7	IO_L6P_8	AP7	FPGA_CON373 23
23	FPGA_CON438	AW29	IO_L28P_7	IO_L5N_8	AN15	FPGA_CON374 23
23	FPGA_CON439	AV29	IO_L28N_VREF_7	IO_L5P_8	AM15	FPGA_CON375 23
23	FPGA_CON440	AV27	IO_L29P_SM4_7	IO_L4N_VREF_8	AK9	FPGA_CON376 23
23	FPGA_CON441	AW27	IO_L29N_SM4_7	IO_L4P_8	AL9	FPGA_CON377 23
23	FPGA_CON442	AT29	IO_L30P_SM3_7	IO_L3N_8	AN8	FPGA_CON378 23
23	FPGA_CON443	AR29	IO_L30N_SM3_7	IO_L3P_8	AN9	FPGA_CON379 23
23	FPGA_CON444	AU26	IO_L31P_SM2_7	IO_L2N_8	AJ9	FPGA_CON380 23
23	FPGA_CON445	AU27	IO_L31N_SM2_7	IO_L2P_8	AJ10	FPGA_CON381 23
23	FPGA_CON446	AT28	IO_L32P_SM1_7	IO_L1N_8	AU5	FPGA_CON382 23
23	FPGA_CON447	AR28	IO_L32N_SM1_7	IO_L1P_8	AV5	FPGA_CON383 23

VDD3V3	AK30	VCCO_7	VCCO_8	AW3	VDD3V3
VDD3V3	AL27	VCCO_7	VCCO_8	AW13	VDD3V3
VDD3V3	AN31	VCCO_7	VCCO_8	AV6	VDD3V3
VDD3V3	AP28	VCCO_7	VCCO_8	AU9	VDD3V3
VDD3V3	AR25	VCCO_7	VCCO_8	AT12	VDD3V3
VDD3V3	AT32	VCCO_7	VCCO_8	AP8	VDD3V3
VDD3V3	AU29	VCCO_7	VCCO_8	AN11	VDD3V3
VDD3V3	AV26	VCCO_7	VCCO_8	AM14	VDD3V3
VDD3V3	AW33	VCCO_7	VCCO_8	AK10	VDD3V3
			VCCO_8	AJ13	VDD3V3

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Bank 9 / Bank 10

		Bank 9	Bank 10			
14	EXP_IO_64	D34	IO_L1P_9	IO_L32N_10	T11	FPGA_CON64 23
14	EXP_IO_65	D35	IO_L1N_9	IO_L32P_10	U12	FPGA_CON65 23
14	EXP_IO_66	C37	IO_L2P_9	IO_L31N_10	R8	FPGA_CON66 23
14	EXP_IO_67	C38	IO_L2N_9	IO_L31P_10	R9	FPGA_CON67 23
14	EXP_IO_68	E34	IO_L3P_9	IO_L30N_10	P7	FPGA_CON68 23
14	EXP_IO_69	F34	IO_L3N_9	IO_L30P_10	N7	FPGA_CON69 23
14	EXP_IO_70	F35	IO_L4P_9	IO_L29N_10	M6	FPGA_CON70 23
14	EXP_IO_71	G35	IO_L4N_VREF_9	IO_L29P_10	L6	FPGA_CON71 23
14	EXP_IO_72	D36	IO_L5P_9	IO_L28N_VREF_10	N8	FPGA_CON72 23
14	EXP_IO_73	D37	IO_L5N_9	IO_L28P_10	P9	FPGA_CON73 23
14	EXP_IO_74	H33	IO_L6P_9	IO_L27N_10	M7	FPGA_CON74 23
14	EXP_IO_75	H34	IO_L6N_9	IO_L27P_10	M8	FPGA_CON75 23
14	EXP_IO_76	E36	IO_L7P_9	IO_L26N_10	U13	FPGA_CON76 23
14	EXP_IO_77	F36	IO_L7N_9	IO_L26P_10	T13	FPGA_CON77 23
14	EXP_IO_78	C39	IO_L8P_CC_LC_9	IO_L25N_CC_LC_10	R11	FPGA_CON78 23
14	EXP_IO_79	D39	IO_L8N_CC_LC_9	IO_L25P_CC_LC_10	P11	FPGA_CON79 23
14	EXP_IO_80	J32	IO_L9P_CC_LC_9	IO_L24N_CC_LC_10	G1	FPGA_CON80 23
14	EXP_IO_81	K32	IO_L9N_CC_LC_9	IO_L24P_CC_LC_10	F1	FPGA_CON81 23
14	EXP_IO_82	G36	IO_L10P_9	IO_L23N_VRP_10	K6	FPGA_CON82 23
14	EXP_IO_83	G37	IO_L10N_9	IO_L23P_VRN_10	J6	FPGA_CON83 23
14	EXP_IO_84	E37	IO_L11P_9	IO_L22N_10	G2	FPGA_CON84 23
14	EXP_IO_85	E38	IO_L11N_9	IO_L22P_10	G3	FPGA_CON85 23
14	EXP_IO_86	H35	IO_L12P_9	IO_L21N_10	J5	FPGA_CON86 23
14	EXP_IO_87	J35	IO_L12N_VREF_9	IO_L21P_10	H5	FPGA_CON87 23
14	EXP_IO_88	M30	IO_L13P_9	IO_L20N_VREF_10	L8	FPGA_CON88 23
14	EXP_IO_89	M31	IO_L13N_9	IO_L20P_10	K7	FPGA_CON89 23
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14	EXP_IO_92	J34	IO_L15P_9	IO_L18N_10	F1	FPGA_CON92 23
14	EXP_IO_93	K34	IO_L15N_9	IO_L18P_10	F2	FPGA_CON93 23
14	EXP_IO_94	F38	IO_L16P_9	IO_L17N_10	T14	FPGA_CON94 23
14	EXP_IO_95	G38	IO_L16N_9	IO_L17P_10	R14	FPGA_CON95 23
14	EXP_IO_96	K33	IO_L17P_9	IO_L16N_10	D1	FPGA_CON96 23
14	EXP_IO_97	L33	IO_L17N_9	IO_L16P_10	D2	FPGA_CON97 23
14	EXP_IO_98	H37	IO_L18P_9	IO_L15N_10	E3	FPGA_CON98 23
14	EXP_IO_99	H38	IO_L18N_9	IO_L15P_10	E4	FPGA_CON99 23
14	EXP_IO_100	N30	IO_L19P_9	IO_L14N_10	N10	FPGA_CON100 23
14	EXP_IO_101	P29	IO_L19N_9	IO_L14P_10	M10	FPGA_CON101 23
14	EXP_IO_102	L34	IO_L20P_9	IO_L13N_10	T15	FPGA_CON102 23
14	EXP_IO_103	L35	IO_L20N_VREF_9	IO_L13P_10	R16	FPGA_CON103 23
14	EXP_IO_104	J36	IO_L21P_9	IO_L12N_VREF_10	F3	FPGA_CON104 23
14	EXP_IO_105	J37	IO_L21N_9	IO_L12P_10	F4	FPGA_CON105 23
14	EXP_IO_106	K36	IO_L22P_9	IO_L11N_10	N12	FPGA_CON106 23
14	EXP_IO_107	L36	IO_L22N_9	IO_L11P_10	M11	FPGA_CON107 23
14	EXP_IO_108	H39	IO_L23P_VRN_9	IO_L10N_10	G5	FPGA_CON108 23
14	EXP_IO_109	J39	IO_L23N_VRP_9	IO_L10P_10	F5	FPGA_CON109 23
14	EXP_IO_110	M33	IO_L24P_CC_LC_9	IO_L9N_CC_LC_10	G6	FPGA_CON110 23
14	EXP_IO_111	N32	IO_L24N_CC_LC_9	IO_L9P_CC_LC_10	G7	FPGA_CON111 23
14	EXP_IO_112	R28	IO_L25P_CC_LC_9	IO_L8N_CC_LC_10	J7	FPGA_CON112 23
14	EXP_IO_113	R29	IO_L25N_CC_LC_9	IO_L8P_CC_LC_10	H7	FPGA_CON113 23
14	EXP_IO_114	M35	IO_L26P_9	IO_L7N_10	F6	FPGA_CON114 23
14	EXP_IO_115	N35	IO_L26N_9	IO_L7P_10	E6	FPGA_CON115 23
14	EXP_IO_116	K37	IO_L27P_9	IO_L6N_10	C2	FPGA_CON116 23
14	EXP_IO_117	K38	IO_L27N_9	IO_L6P_10	C3	FPGA_CON117 23
14	EXP_IO_118	N33	IO_L28P_9	IO_L5N_10	D5	FPGA_CON118 23
14	EXP_IO_119	N34	IO_L28N_VREF_9	IO_L5P_10	D6	FPGA_CON119 23
14	EXP_IO_120	P31	IO_L29P_9	IO_L4N_VREF_10	D4	FPGA_CON120 23
14	EXP_IO_121	P32	IO_L29N_9	IO_L4P_10	C4	FPGA_CON121 23
14	EXP_IO_122	K39	IO_L30P_9	IO_L3N_10	C5	FPGA_CON122 23
14	EXP_IO_123	L39	IO_L30N_9	IO_L3P_10	B5	FPGA_CON123 23
14	EXP_IO_124	L38	IO_L31P_9	IO_L2N_10	B3	FPGA_CON124 23
14	EXP_IO_125	M38	IO_L31N_9	IO_L2P_10	A3	FPGA_CON125 23
14	EXP_IO_126	M36	IO_L32P_9	IO_L1N_10	A4	FPGA_CON126 23
14	EXP_IO_127	M37	IO_L32N_9	IO_L1P_10	A5	FPGA_CON127 23

VDD3V3	D38	VCCO_9	VCCO_10	T12	VDD3V3
VDD3V3	E35	VCCO_9	VCCO_10	R15	VDD3V3
VDD3V3	G39	VCCO_9	VCCO_10	P8	VDD3V3
VDD3V3	H36	VCCO_9	VCCO_10	N11	VDD3V3
VDD3V3	J33	VCCO_9	VCCO_10	L7	VDD3V3
VDD3V3	L37	VCCO_9	VCCO_10	H6	VDD3V3
VDD3V3	M34	VCCO_9	VCCO_10	E2	VDD3V3
VDD3V3	N31	VCCO_9	VCCO_10	E5	VDD3V3
VDD3V3	P28	VCCO_9	VCCO_10	C1	VDD3V3
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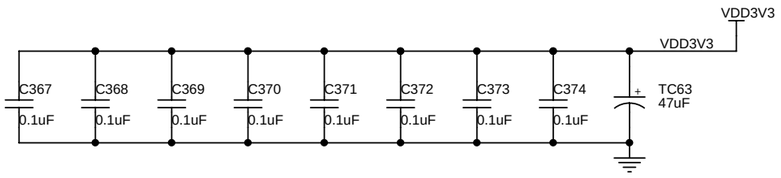

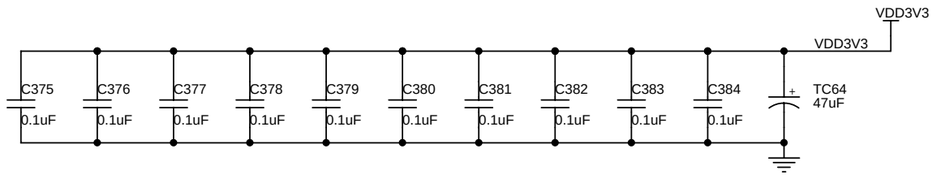

Title	SANGHWA FPGA PLATFORM FPGA0 BANK 7/8/9/10		
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FPGA INTERCONNECTION

SSRAM INTERFACE

8 SMA_nOE

NAND FLASH

8 NDAREADY
8 NDARE
8 NDACE
8 NDACLE
8 NDAALE
8 NDAnWE
8 NDA_D7
8 NDA_D6
8 NDA_D5
8 NDA_D4
8 NDA_D3
8 NDA_D2
8 NDA_D1
8 NDA_D0

14 EXP_IO_173
14 EXP_IO_172
14 EXP_IO_171
14 EXP_IO_170
14 EXP_IO_169
14 EXP_IO_168
14 EXP_IO_167
14 EXP_IO_166
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14 EXP_IO_161
14 EXP_IO_160
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14 EXP_IO_134
14 EXP_IO_133
14 EXP_IO_132
14 EXP_IO_131
14 EXP_IO_130
14 EXP_IO_129
14 EXP_IO_128

Bank 11 / Bank 12

	Bank 11	Bank 12		
AG33	IO_L1P_11	IO_L32N_12	AT3	FPGA_CON256 24
AF33	IO_L1N_11	IO_L32P_12	AU3	FPGA_CON257 24
AC28	IO_L2P_11	IO_L31N_12	AT5	FPGA_CON258 24
AD29	IO_L2N_11	IO_L31P_12	AT6	FPGA_CON259 24
AD27	IO_L3P_11	IO_L30N_12	AP4	FPGA_CON260 24
AC27	IO_L3N_11	IO_L30P_12	AP5	FPGA_CON261 24
AE31	IO_L4P_11	IO_L29N_12	AP6	FPGA_CON262 24
AE32	IO_L4N_VREF_11	IO_L29P_12	AR6	FPGA_CON263 24
AD26	IO_L5P_11	IO_L28N_VREF_12	AM6	FPGA_CON264 24
AE26	IO_L5N_11	IO_L28P_12	AM7	FPGA_CON265 24
AE31	IO_L6P_11	IO_L27N_12	AR4	FPGA_CON266 24
AG32	IO_L6N_11	IO_L27P_12	AT4	FPGA_CON267 24
AH32	IO_L7P_11	IO_L26N_12	AR2	FPGA_CON268 24
AH33	IO_L7N_11	IO_L26P_12	AR3	FPGA_CON269 24
AJ34	IO_L8P_CC_LC_11	IO_L25N_CC_LC_12	AU1	FPGA_CON270 24
AH34	IO_L8N_CC_LC_11	IO_L25P_CC_LC_12	AU2	FPGA_CON271 24
AD25	IO_L9P_CC_LC_11	IO_L24N_CC_LC_12	AR1	FPGA_CON272 24
AE24	IO_L9N_CC_LC_11	IO_L24P_CC_LC_12	AT1	FPGA_CON273 24
AE28	IO_L10P_11	IO_L23N_VRP_12	AK8	FPGA_CON274 24
AE29	IO_L10N_11	IO_L23P_VRN_12	AL8	FPGA_CON275 24
AL34	IO_L11P_11	IO_L22N_12	AL5	FPGA_CON276 24
AK34	IO_L11N_11	IO_L22P_12	AM5	FPGA_CON277 24
AP39	IO_L12P_11	IO_L21N_12	AN4	FPGA_CON278 24
AN39	IO_L12N_VREF_11	IO_L21P_12	AN5	FPGA_CON279 24
AE28	IO_L13P_11	IO_L20N_VREF_12	AJ7	FPGA_CON280 24
AE29	IO_L13N_11	IO_L20P_12	AK7	FPGA_CON281 24
AN37	IO_L14P_11	IO_L19N_12	AH9	FPGA_CON282 24
AN38	IO_L14N_11	IO_L19P_12	AH10	FPGA_CON283 24
AH30	IO_L15P_11	IO_L18N_12	AN2	FPGA_CON284 24
AG30	IO_L15N_11	IO_L18P_12	AN3	FPGA_CON285 24
AK33	IO_L16P_11	IO_L17N_12	AK6	FPGA_CON286 24
AJ32	IO_L16N_11	IO_L17P_12	AL6	FPGA_CON287 24
AR37	IO_L17P_11	IO_L16N_12	AK4	FPGA_CON288 24
AR38	IO_L17N_11	IO_L16P_12	AL4	FPGA_CON289 24
AM35	IO_L18P_11	IO_L15N_12	AP1	FPGA_CON290 24
AL35	IO_L18N_11	IO_L15P_12	AP2	FPGA_CON291 24
AP35	IO_L19P_11	IO_L14N_12	AM1	FPGA_CON292 24
AN35	IO_L19N_11	IO_L14P_12	AM2	FPGA_CON293 24
AT39	IO_L20P_11	IO_L13N_12	AL3	FPGA_CON294 24
AR39	IO_L20N_VREF_11	IO_L13P_12	AM3	FPGA_CON295 24
AG28	IO_L21P_11	IO_L12N_VREF_12	AE11	FPGA_CON296 24
AH29	IO_L21N_11	IO_L12P_12	AE12	FPGA_CON297 24
AP36	IO_L22P_11	IO_L11N_12	AG10	FPGA_CON298 24
AP37	IO_L22N_11	IO_L11P_12	AE11	FPGA_CON299 24
AN33	IO_L23P_VRN_11	IO_L10N_12	AK2	FPGA_CON300 24
AN34	IO_L23N_VRP_11	IO_L10P_12	AK3	FPGA_CON301 24
AU38	IO_L24P_CC_LC_11	IO_L9N_CC_LC_12	AJ5	FPGA_CON302 24
AT38	IO_L24N_CC_LC_11	IO_L9P_CC_LC_12	AJ6	FPGA_CON303 24
AU35	IO_L25P_CC_LC_11	IO_L8N_CC_LC_12	AH4	FPGA_CON304 24
AU36	IO_L25N_CC_LC_11	IO_L8P_CC_LC_12	AJ4	FPGA_CON305 24
AM33	IO_L26P_11	IO_L7N_12	AH7	FPGA_CON306 24
AL33	IO_L26N_11	IO_L7P_12	AG8	FPGA_CON307 24
AT34	IO_L27P_11	IO_L6N_12	AF8	FPGA_CON308 24
AT35	IO_L27N_11	IO_L6P_12	AF9	FPGA_CON309 24
AT36	IO_L28P_11	IO_L5N_12	AK1	FPGA_CON310 24
AR36	IO_L28N_VREF_11	IO_L5P_12	AL1	FPGA_CON311 24
AW36	IO_L29P_11	IO_L4N_VREF_12	AJ1	FPGA_CON312 24
AW37	IO_L29N_11	IO_L4P_12	AJ2	FPGA_CON313 24
AV37	IO_L30P_11	IO_L3N_12	AG6	FPGA_CON314 24
AU37	IO_L30N_11	IO_L3P_12	AG7	FPGA_CON315 24
AW35	IO_L31P_11	IO_L2N_12	AH2	FPGA_CON316 24
AV35	IO_L31N_11	IO_L2P_12	AH3	FPGA_CON317 24
AR34	IO_L32P_11	IO_L1N_12	AG5	FPGA_CON318 24
AP34	IO_L32N_11	IO_L1P_12	AH5	FPGA_CON319 24

VDD3V3 AD28	VCCO_11	VCCO_12	AT2	VDD3V3
VDD3V3 AE25	VCCO_11	VCCO_12	AR5	VDD3V3
VDD3V3 AE32	VCCO_11	VCCO_12	AN1	VDD3V3
VDD3V3 AG29	VCCO_11	VCCO_12	AM4	VDD3V3
VDD3V3 AJ33	VCCO_11	VCCO_12	AL7	VDD3V3
VDD3V3 AM34	VCCO_11	VCCO_12	AJ3	VDD3V3
VDD3V3 AP38	VCCO_11	VCCO_12	AH6	VDD3V3
VDD3V3 AR35	VCCO_11	VCCO_12	AG9	VDD3V3
VDD3V3 AU39	VCCO_11	VCCO_12	AF12	VDD3V3
VDD3V3 AV36	VCCO_11			

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14 EXP_IO_62
14 EXP_IO_63

Bank 13 / Bank 14

	Bank 13	Bank 14		
R31	IO_L1P_13	IO_L32N_14	W12	FPGA_CON128 24
R32	IO_L1N_13	IO_L32P_14	Y13	FPGA_CON129 24
P34	IO_L2P_13	IO_L31N_14	Y11	FPGA_CON130 24
P35	IO_L2N_13	IO_L31P_14	AA11	FPGA_CON131 24
T29	IO_L3P_13	IO_L30N_14	Y9	FPGA_CON132 24
U28	IO_L3N_13	IO_L30P_14	AA10	FPGA_CON133 24
P36	IO_L4P_13	IO_L29N_14	W5	FPGA_CON134 24
P37	IO_L4N_VREF_13	IO_L29P_14	W6	FPGA_CON135 24
N37	IO_L5P_13	IO_L28N_VREF_14	W9	FPGA_CON136 24
N38	IO_L5N_13	IO_L28P_14	W10	FPGA_CON137 24
N39	IO_L6P_13	IO_L27N_14	W7	FPGA_CON138 24
P39	IO_L6N_13	IO_L27P_14	V7	FPGA_CON139 24
R34	IO_L7P_13	IO_L26N_14	U2	FPGA_CON140 24
T34	IO_L7N_13	IO_L26P_14	U3	FPGA_CON141 24
T31	IO_L8P_CC_LC_13	IO_L25N_CC_LC_14	U1	FPGA_CON142 24
U30	IO_L8N_CC_LC_13	IO_L25P_CC_LC_14	T1	FPGA_CON143 24
R36	IO_L9P_CC_LC_13	IO_L24N_CC_LC_14	V5	FPGA_CON144 24
T36	IO_L9N_CC_LC_13	IO_L24P_CC_LC_14	U5	FPGA_CON145 24
T33	IO_L10P_13	IO_L23N_VRP_14	V9	FPGA_CON146 24
U32	IO_L10N_13	IO_L23P_VRN_14	V10	FPGA_CON147 24
R37	IO_L11P_13	IO_L22N_14	U6	FPGA_CON148 24
R38	IO_L11N_13	IO_L22P_14	U7	FPGA_CON149 24
R39	IO_L12P_13	IO_L21N_14	T3	FPGA_CON150 24
T39	IO_L12N_VREF_13	IO_L21P_14	T4	FPGA_CON151 24
V25	IO_L13P_13	IO_L20N_VREF_14	R1	FPGA_CON152 24
U26	IO_L13N_13	IO_L20P_14	R2	FPGA_CON153 24
V27	IO_L14P_13	IO_L19N_14	T5	FPGA_CON154 24
U27	IO_L14N_13	IO_L19P_14	T6	FPGA_CON155 24
T35	IO_L15P_13	IO_L18N_14	R3	FPGA_CON156 24
U35	IO_L15N_13	IO_L18P_14	R4	FPGA_CON157 24
U33	IO_L16P_13	IO_L17N_14	T9	FPGA_CON158 24
V33	IO_L16N_13	IO_L17P_14	U10	FPGA_CON159 24
T38	IO_L17P_13	IO_L16N_14	P1	FPGA_CON160 24
U38	IO_L17N_13	IO_L16P_14	P2	FPGA_CON161 24
V29	IO_L18P_13	IO_L15N_14	U8	FPGA_CON162 24
V30	IO_L18N_13	IO_L15P_14	T8	FPGA_CON163 24
U36	IO_L19P_13	IO_L14N_14	V12	FPGA_CON164 24
U37	IO_L19N_13	IO_L14P_14	V13	FPGA_CON165 24
V32	IO_L20P_13	IO_L13N_14	N2	FPGA_CON166 24
W32	IO_L20N_VREF_13	IO_L13P_14	N3	FPGA_CON167 24
W26	IO_L21P_13	IO_L12N_VREF_14	P4	FPGA_CON168 24
W27	IO_L21N_13	IO_L12P_14	P5	FPGA_CON169 24
V34	IO_L22P_13	IO_L11N_14	R6	FPGA_CON170 24
V35	IO_L22N_13	IO_L11P_14	P6	FPGA_CON171 24
V37	IO_L23P_VRN_13	IO_L10N_14	M1	FPGA_CON172 24
V38	IO_L23N_VRP_13	IO_L10P_14	L1	FPGA_CON173 24
V39	IO_L24P_CC_LC_13	IO_L9N_CC_LC_14	N4	FPGA_CON174 24
W39	IO_L24N_CC_LC_13	IO_L9P_CC_LC_14	N5	FPGA_CON175 24
W34	IO_L25P_CC_LC_13	IO_L8N_CC_LC_14	M2	FPGA_CON176 24
W35	IO_L25N_CC_LC_13	IO_L8P_CC_LC_14	M3	FPGA_CON177 24
W36	IO_L26P_13	IO_L7N_14	L3	FPGA_CON178 24
W37	IO_L26N_13	IO_L7P_14	L4	FPGA_CON179 24
Y37	IO_L27P_13	IO_L6N_14	K1	FPGA_CON180 24
Y38	IO_L27N_13	IO_L6P_14	K2	FPGA_CON181 24
Y39	IO_L28P_13	IO_L5N_14	M5	FPGA_CON182 24
AA39	IO_L28N_VREF_13	IO_L5P_14	L5	FPGA_CON183 24
AA36	IO_L29P_13	IO_L4N_VREF_14	J1	FPGA_CON184 24
Y36	IO_L29N_13	IO_L4P_14	J2	FPGA_CON185 24
Y33	IO_L30P_13	IO_L3N_14	H2	FPGA_CON186 24
Y34	IO_L30N_13	IO_L3P_14	H3	FPGA_CON187 24
AB36	IO_L31P_13	IO_L2N_14	K3	FPGA_CON188 24
AB37	IO_L31N_13	IO_L2P_14	K4	FPGA_CON189 24
AB38	IO_L32P_13	IO_L1N_14	J4	FPGA_CON190 24
AA38	IO_L32N_13	IO_L1P_14	H4	FPGA_CON191 24

VDD3V3 AA37	VCCO_13	VCCO_14	Y10	VDD3V3
VDD3V3 P38	VCCO_13	VCCO_14	W13	VDD3V3
VDD3V3 R35	VCCO_13	VCCO_14	V6	VDD3V3
VDD3V3 T32	VCCO_13	VCCO_14	U9	VDD3V3
VDD3V3 U29	VCCO_13	VCCO_14	T2	VDD3V3
VDD3V3 U39	VCCO_13	VCCO_14	R5	VDD3V3
VDD3V3 V26	VCCO_13	VCCO_14	N1	VDD3V3
VDD3V3 V36	VCCO_13	VCCO_14	M4	VDD3V3
VDD3V3 W33	VCCO_13	VCCO_14	J3	VDD3V3

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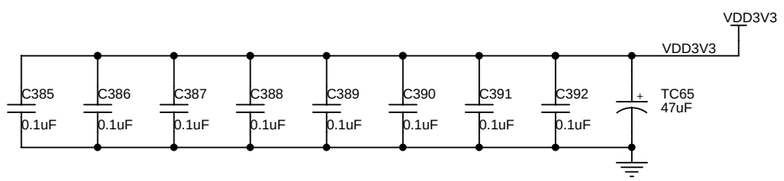

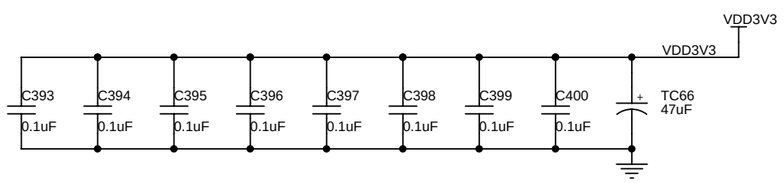

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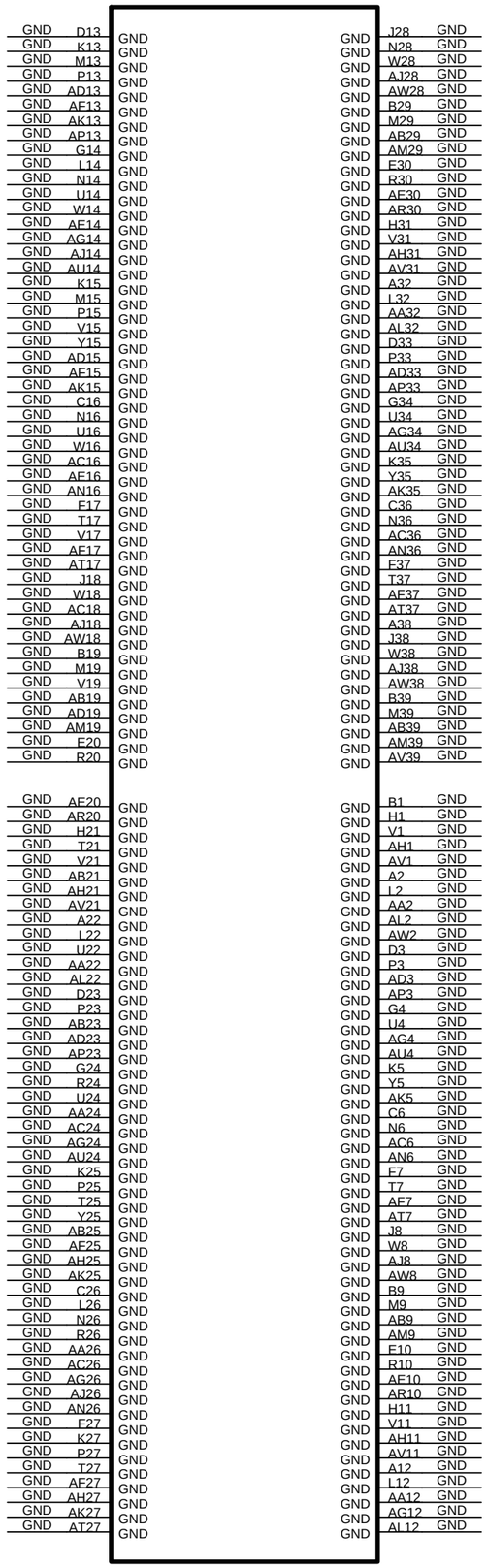
VIRTEX-4 FPGA POWER GROUND



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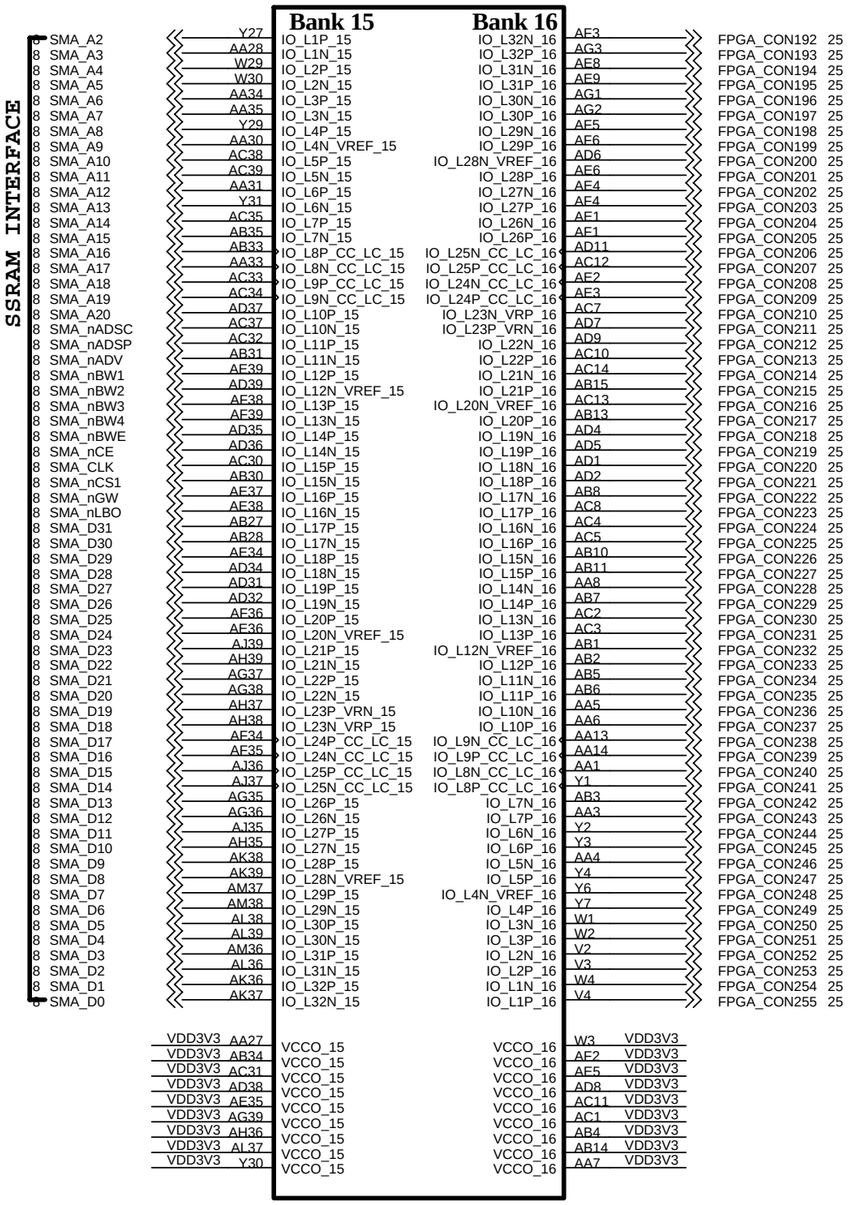
SSRAM INTERFACE



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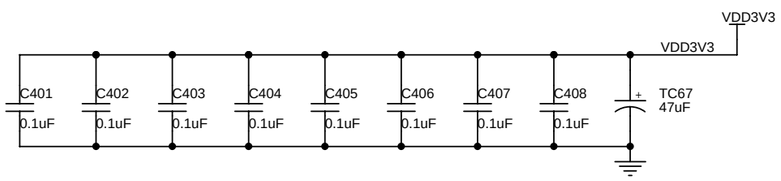

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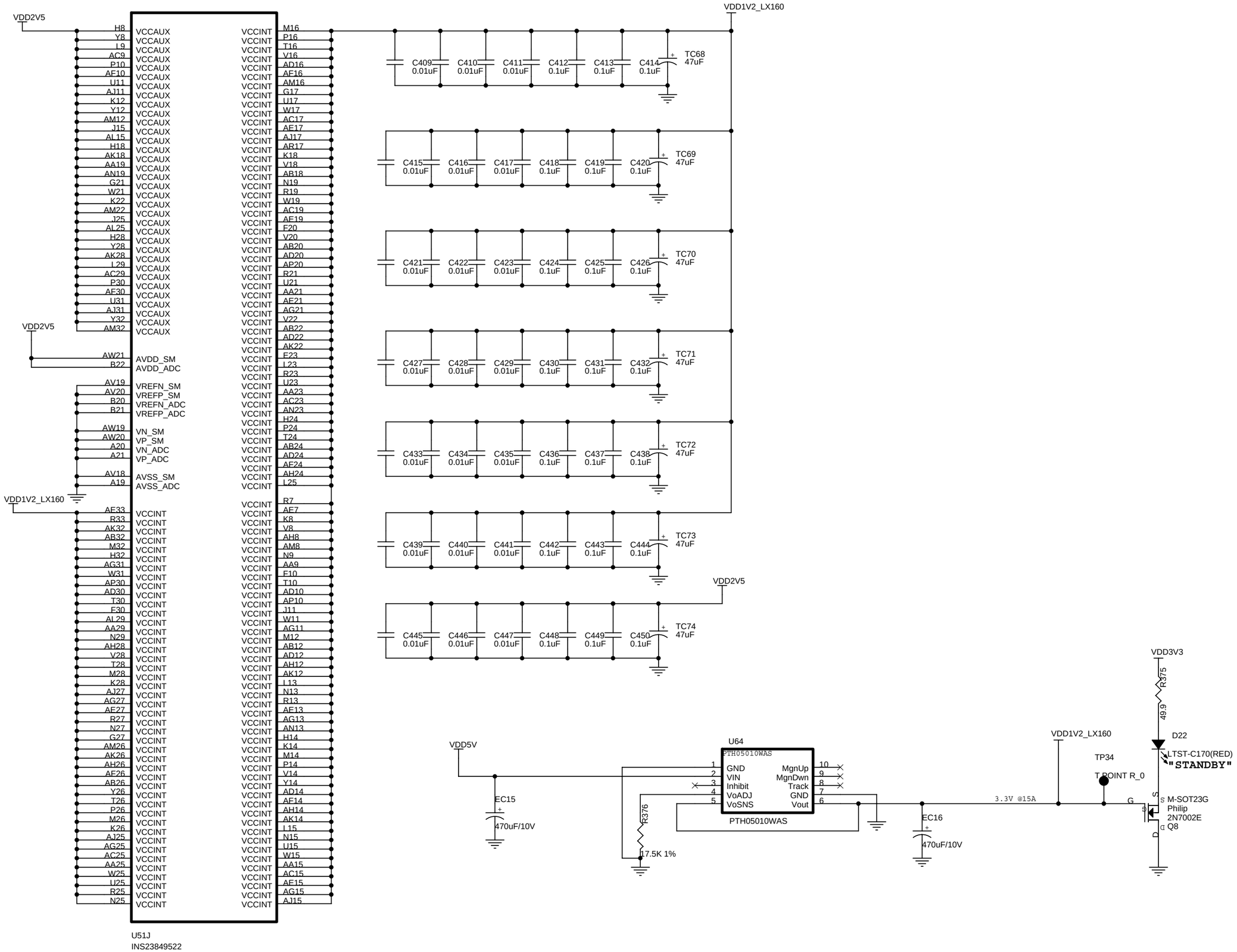

SANGHWA FPGA PLATFORM

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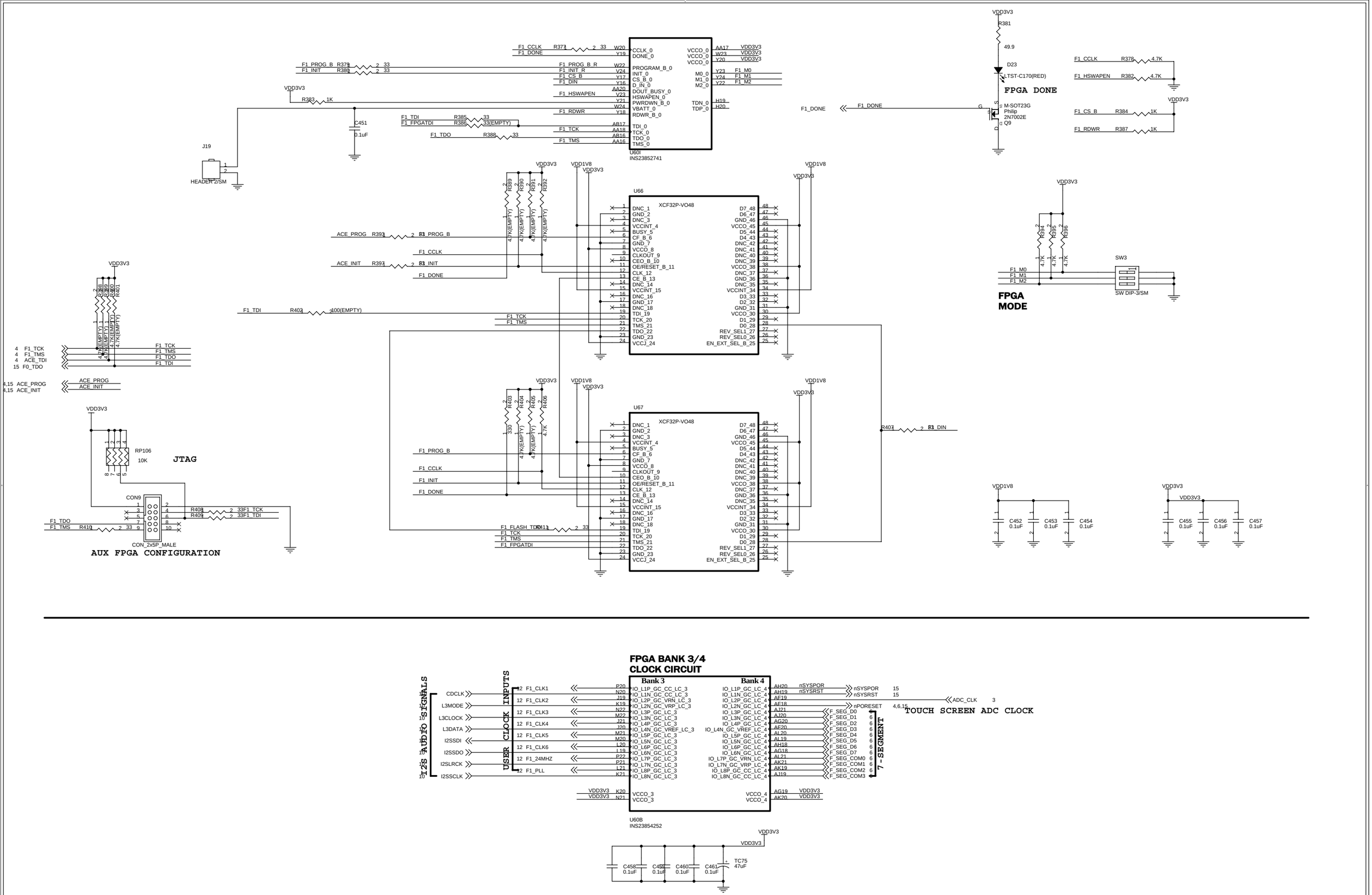
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FPGA MODE
SW3
SW DIP-3/SM
J19
HEADER 2/SM
JTAG
RP106
10K
CON9
CON_2x5P_MALE
AUX FPGA CONFIGURATION
FPGA BANK 3/4
CLOCK CIRCUIT
Bank 3
Bank 4
U60B
INS23854252
USER CLOCK INPUTS
AUDIO SIGNALS
7-SEGMENT
TOUCH SCREEN ADC CLOCK
SANGHWA FPGA PLATFORM
FPGA1 CONFIG/CLOCK
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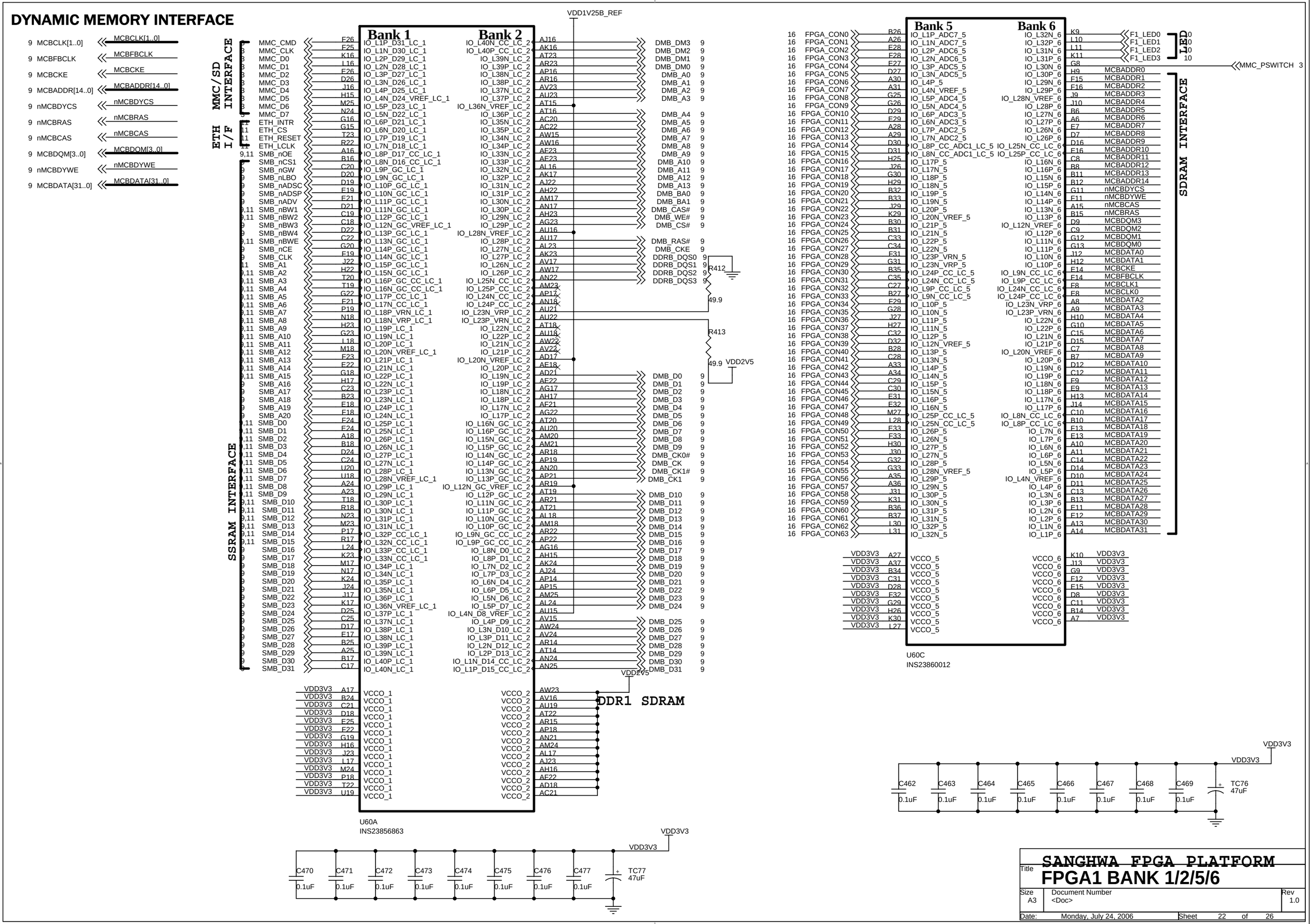
DYNAMIC MEMORY INTERFACE



Title	SANGHWA FPGA PLATFORM FPGA1 BANK 1/2/5/6
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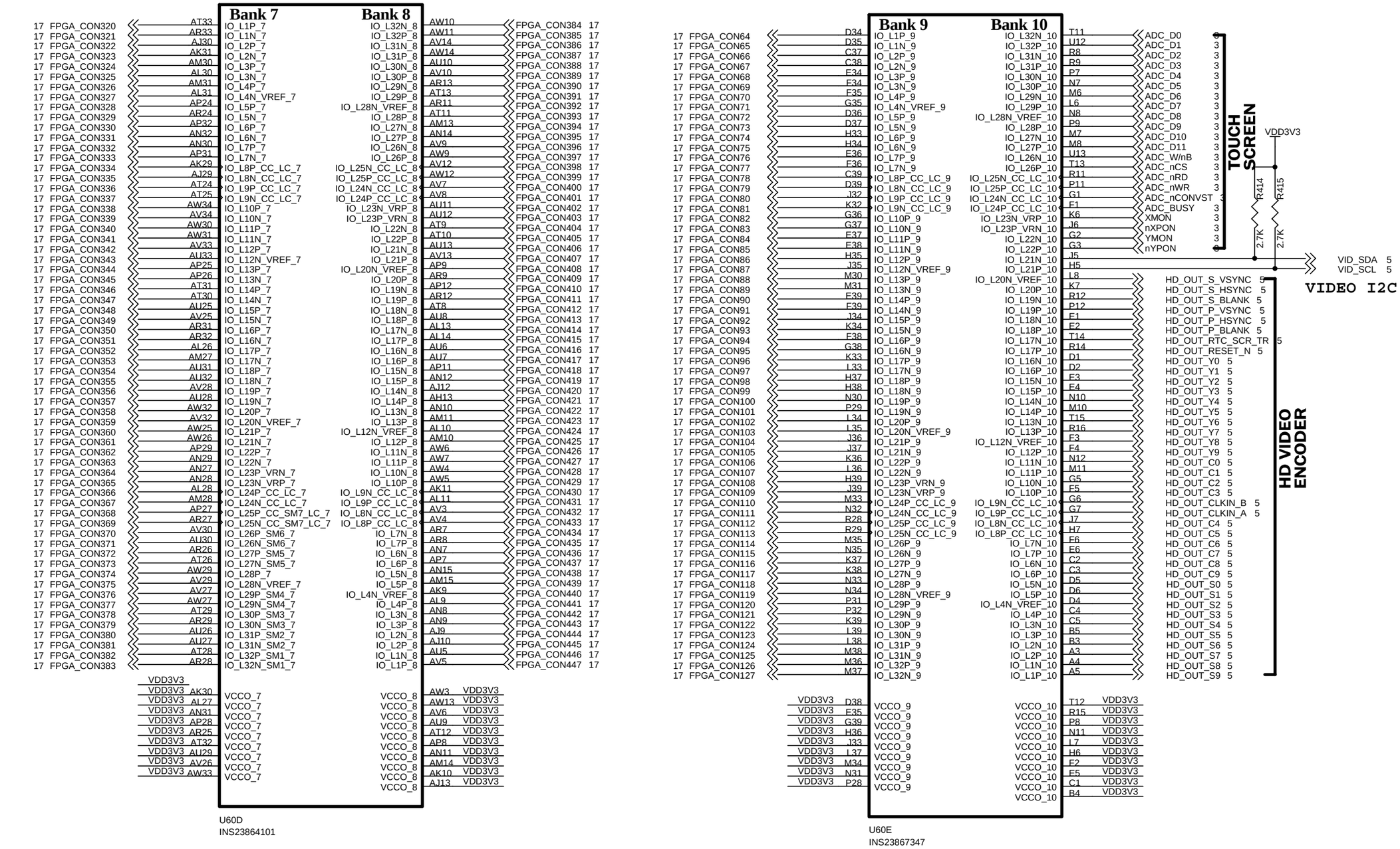

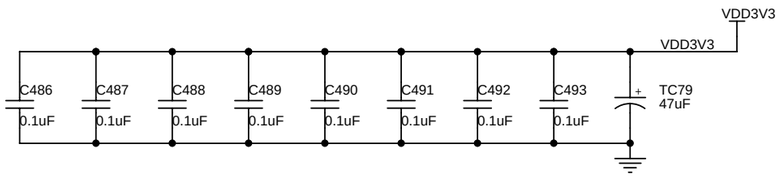

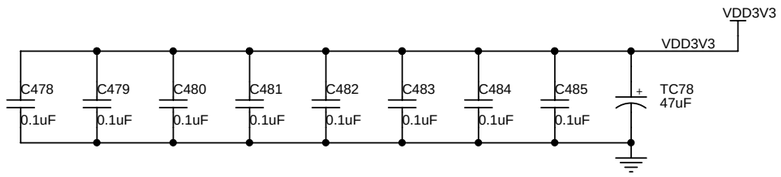

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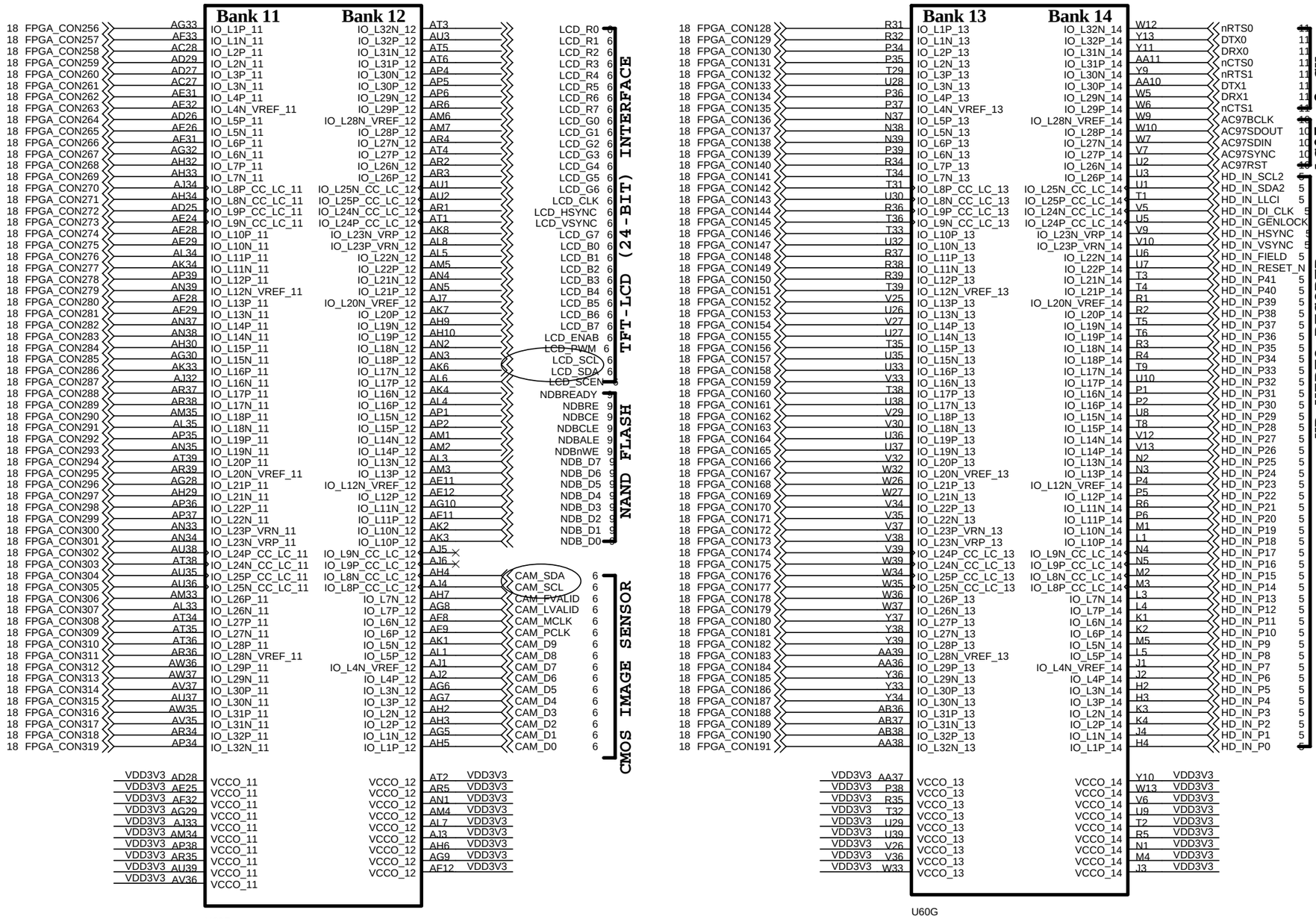

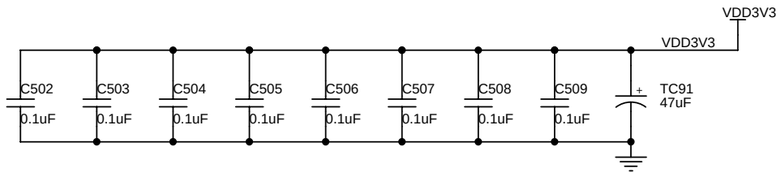

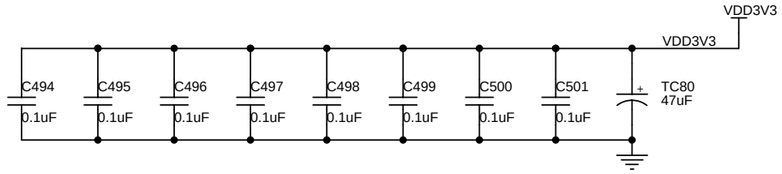

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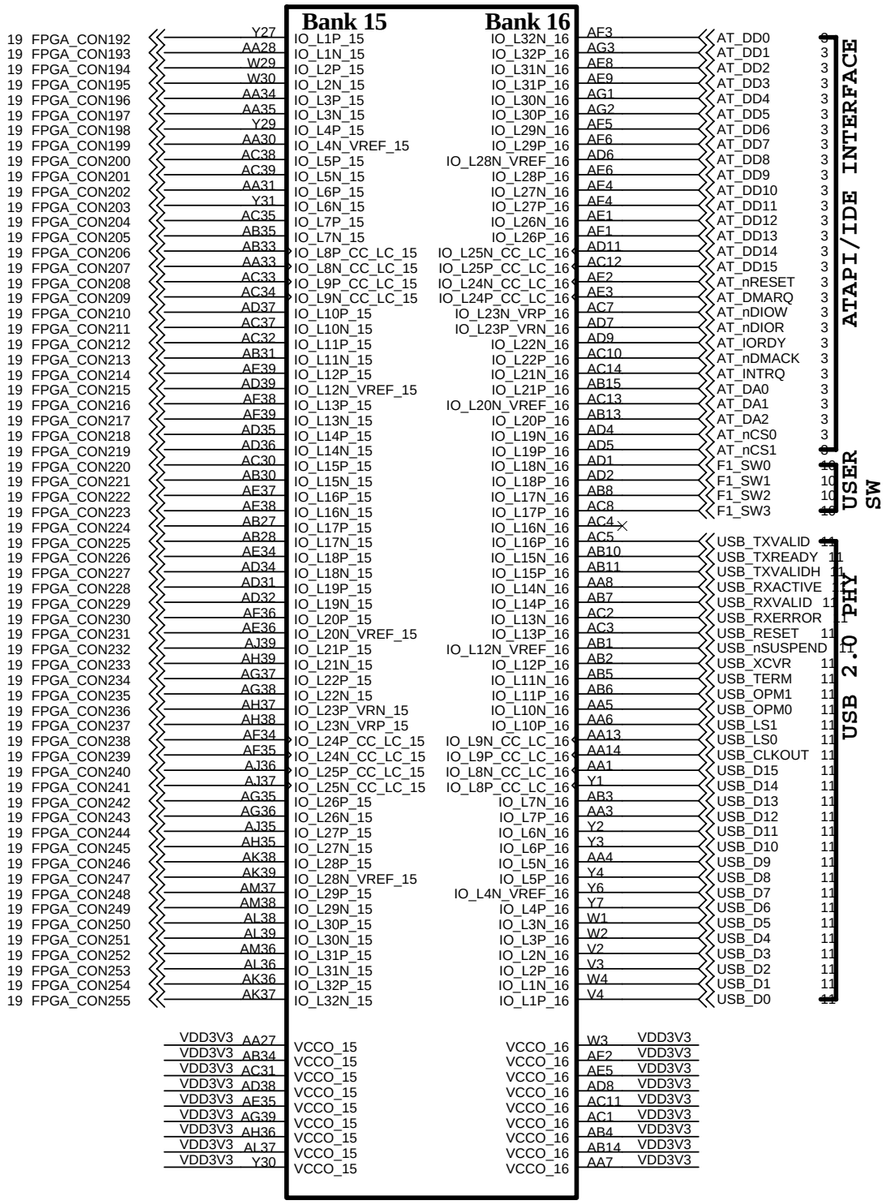

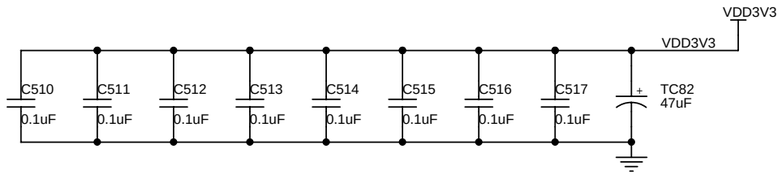

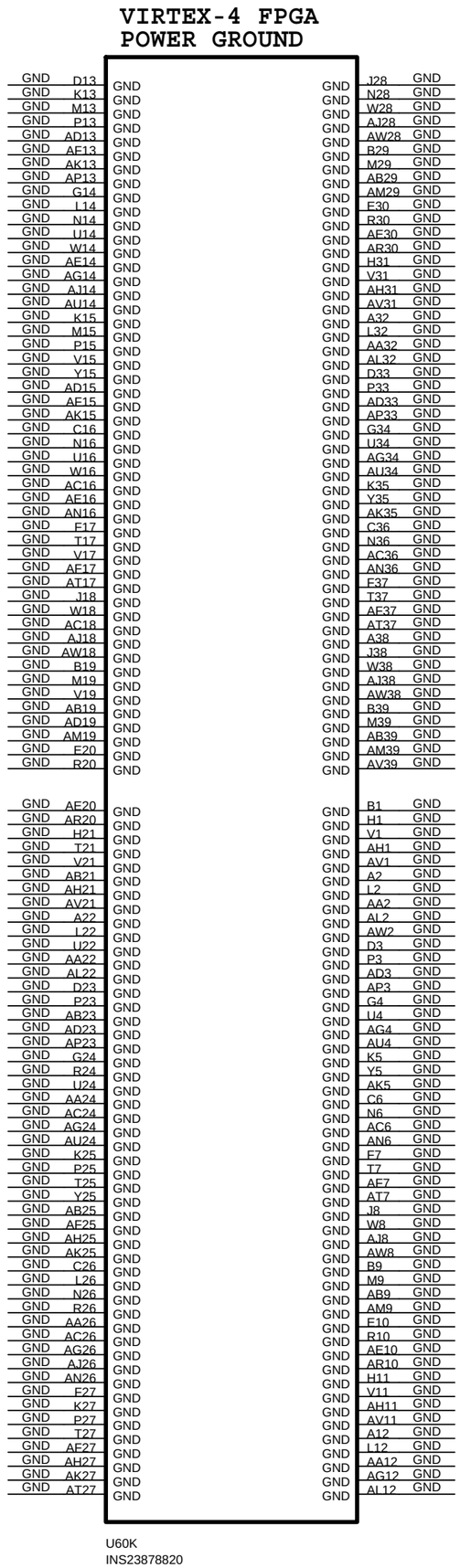

SANGHWA FPGA PLATFORM

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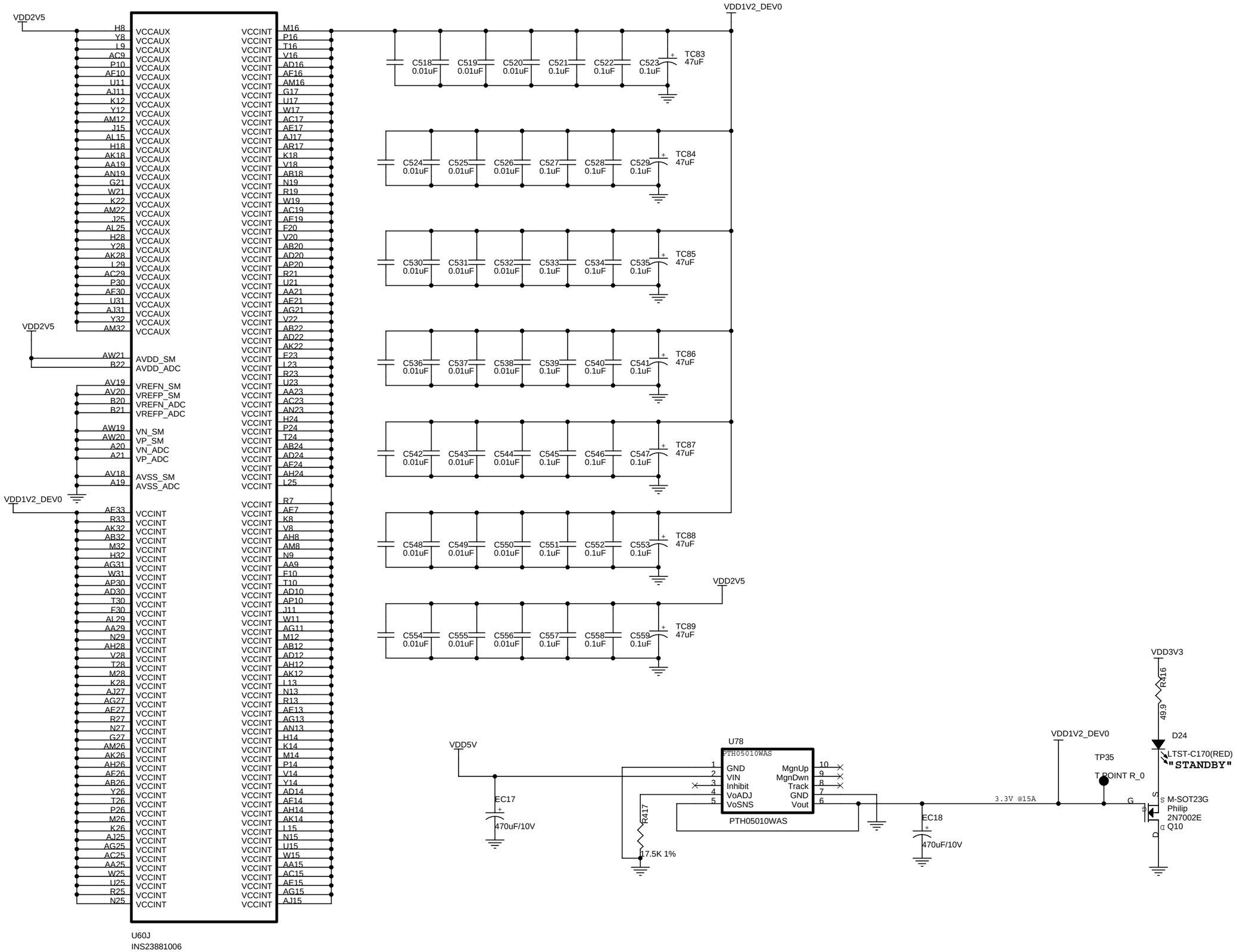

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