GRADUATE COURSE EXAM
ADVANCED COMPUTER ARCHITECTURE
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QUESTIONS

1. (10 points) We want to accelerate a single thread program with multi-threading on a multi-core CPU. Suppose we plan to use 8 threads which is the maximal number of simultaneous threads supported by the multi-core CPU. If we want to achieve a speedup of 5, what percentage of the program workload should we accelerate with these 8 threads?

2. (10 points) Suppose a single thread program spends 10% of its execution time on data I/O which is sequential and 90% of its execution time on numerical computation which is parallelizable. If we use a GPU to accelerate the computational part with 100 GPU threads, but a GPU thread runs 50% slower than that of a CPU thread and data I/O time will be doubled when using GPU, what is the speedup we can get? If we can launch infinite number of threads on GPU, what is the maximal speedup we can get?

3. (10 points) It is claimed that the ideal speedup of a pipelined CPU over an unpipelined one is the number of pipeline stages. Please provide an explanation of this statement.

4. (10 points) Data forwarding is a technique to deal with the data hazard in pipelined CPU. In the 5-stage pipelined MIPS CPU, data forwarding can eliminate the stall cycle between dependant arithmetic-logic and store instructions but can not eliminate the stall between the load instruction and its succeeding instruction that requires the loaded value. Please give an explanation on this.

5. (10 points) In the 5-stage pipelined MIPS CPU, ideal CPI is expected to be 1. However, a stall cycle is needed for branch instructions to determine branch outcome and branch target address. If this stall can't be eliminated, what is the average CPI for branch instructions? If the hardware fetches the succeeding instruction after the branch (always predict branch is not taken), and cancel it when the branch is taken, what is the average CPI for branchs when the frequency of taken branchs is 60%?

6. (10 points) The 5-stage pipelined MIPS CPU has 1 clock cycle stall for load instruction and its succeeding dependant instruction, and 1 clock cycle stall for branch instruction. A naive compiler takes no effort to hide these stalls while an optimized compiler can hide half of the load stall and 20% of the branch stall by instruction rescheduling. Considering the following instruction mix, assuming that all load instruction has a succeeding instruction that requires the loaded value, what is the speedup of the optimized compiler over the naive one?

Instruction type	Frequency	CPI not considering optimization
ALU ops	0.43	1
Loads	0.21	2
Stores	0.12	1
Branchs	0.24	2

7. (10 points) The 5-stage pipelined MIPS CPU has 1 clock cycle stall for load instruction and its succeeding dependant instruction, and 1 clock cycle stall for branch instruction. In addition to these stalls, CPU has to stall for memory accesses if not hit in cache. If the cache hit rate is 90%, hit time is 1 cycle, and miss penalty is 60 cycles, what is the average CPI considering the following instruction mix? If the hit rate is improved to 99% by some hardware and software techniques at a cost of 10% lower CPU frequency, will the overall performance improve?

Instruction type	Frequency	CPI not considering memory stalls
ALU ops	0.5	1
Loads	0.2	2
Stores	0.1	1
Branchs	0.2	2

8. (10 points) The following diagram is the structure of the Tomasulo's algorithm with reorder buffer (ROB). What is the advantage of using this structure?

9. (10 points) The following diagram shows a TLB miss procedure. Please briefly describe the actions of the arrows with labels from 1 to 6.

10. (10 points) The following diagram is a directory-based cache coherence structure in a multiprocessor machine. If processor 2 is going to read some new data belonging to a memory block with processor 1 as the home node while is currently owned by processor 0 and is dirty, what actions should be done to complete this read request?