Design Journal

Week 6-7

24/10/2024 SUBGROUP B z5592274

Overview

Both teams have been working on completing a final product for acceptance testing, being in the “assembly phase” of the project.The 3D design is complete, and we are all looking to get our circuits synthesised onto veroboards. The Gannt chart below outlines our roles coming up to this milestone.

DESN1000: EE&T

PROJECT TITLE	DESN1000: EE&T	GROUP NAME	
PROJECT MANAGER	Subgroup A: Casey, Subgroup B: Aaron	DATE	9/9/24

					RESEARCH			IMPLEMENTATION			FINAL ASSEMBLY			TESTING AND REPORT		
SUBGROUP	TASK TITLE	TASK OWNER	START DATE	DUE DATE	WEEK 1	WEEK 2	WEEK 3	WEEK 4	WEEK 5	WEEK 6	WEEK 7	WEEK 8	WEEK 9	WEEK 10	WEEK 11	WEEK 12
SG-A/B	DESN1000: EE&T															
SG-B	Phototransistor and Bandpass	Aaron	16/09/24	10/24/24	N/A	Research	Research	Phototransistor	Band Pass	Prototype Sensor	SG-B Assembly	Acceptance SG-B	Full Assembly	Final Testing	Reflection/Report	PARTY
SG-B	Amplification and AC to DC	Jonas	16/09/24	10/24/24	N/A	Research	Research	Op Amps	AC to DC	Prototype Sensor	SG-B Assembly	Acceptance SG-B	Full Assembly	Final Testing	Reflection/Report	PARTY
SG-B	Arduino Calculations	Matthew	16/09/24	10/24/24	N/A	Research	Research	Input Voltage	Output Voltage	Prototype Signal	SG-B Assembly	Acceptance SG-B	Full Assembly	Final Testing	Reflection/Report	PARTY
SG-B	LED and Exterminate	Freesia	16/09/24	10/24/24	N/A	Research	Research	LED Config	Conversion	Prototype Signal	SG-B Assembly	Acceptance SG-B	Report	Final Testing	Reflection/Report	PARTY
SG-A	Motors and H-Bridge	Casey	16/09/25	10/24/24	N/A	Research	Research	H-Bridge	Motor Turning	Prototype Motor	SG-A Assembly	Acceptance SG-A	Report	Final Testing	Reflection/Report	PARTY
SG-A	Body Design	Sean	16/09/26	10/24/24	N/A	Research	Research	Gears and Motion	Main Body	Prototype Body	SG-A Assembly	Acceptance SG-A	Full Assembly	Final Testing	Reflection/Report	PARTY
SG-A	Exterminate	Jimmy	16/09/27	10/24/24	N/A	Research	Research	Voltage Detection	Speaker	Prototype Sounds	SG-A Assembly	Acceptance SG-A	Full Assembly	Final Testing	Reflection/Report	PARTY
SG-A	Left DESN	Chloe			N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

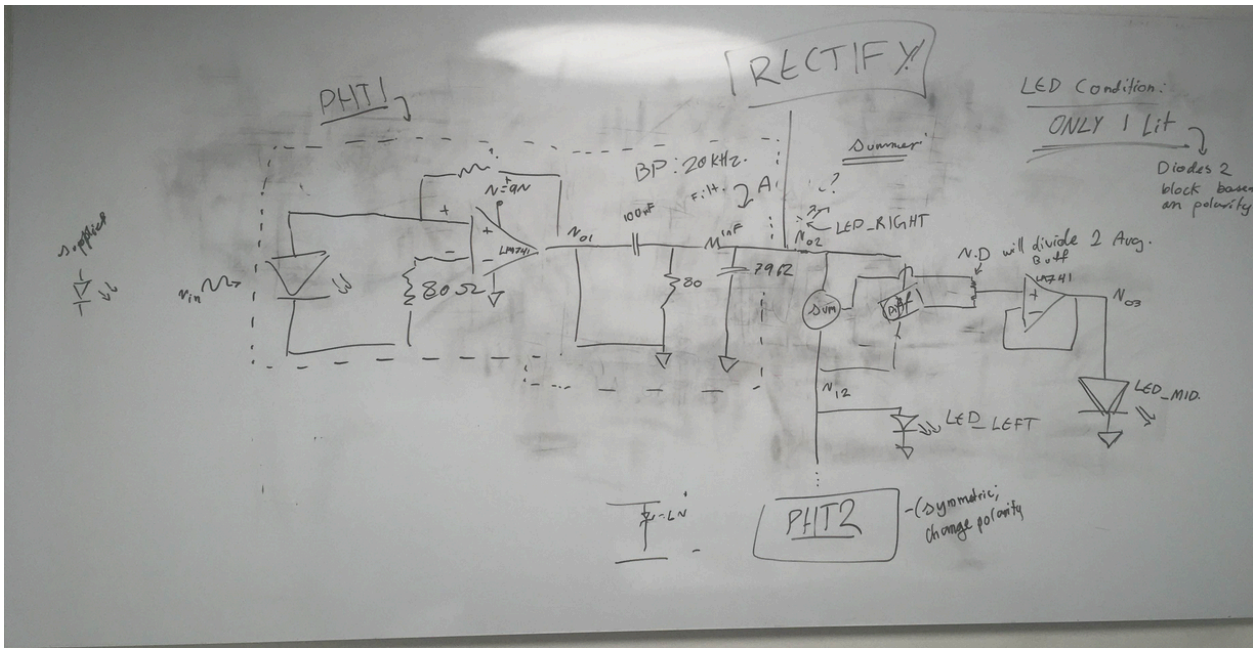
Personal Tasks

Due to my background in hobbyist electronics, I have taken on a simulator and synthesis role within the group. I do the ‘pickup’ through my understanding of theory if anything doesn’t work or connect. I have been using EasyEDA and LTSpice for many of my simulations and schematics. I am also responsible for the LED’s.

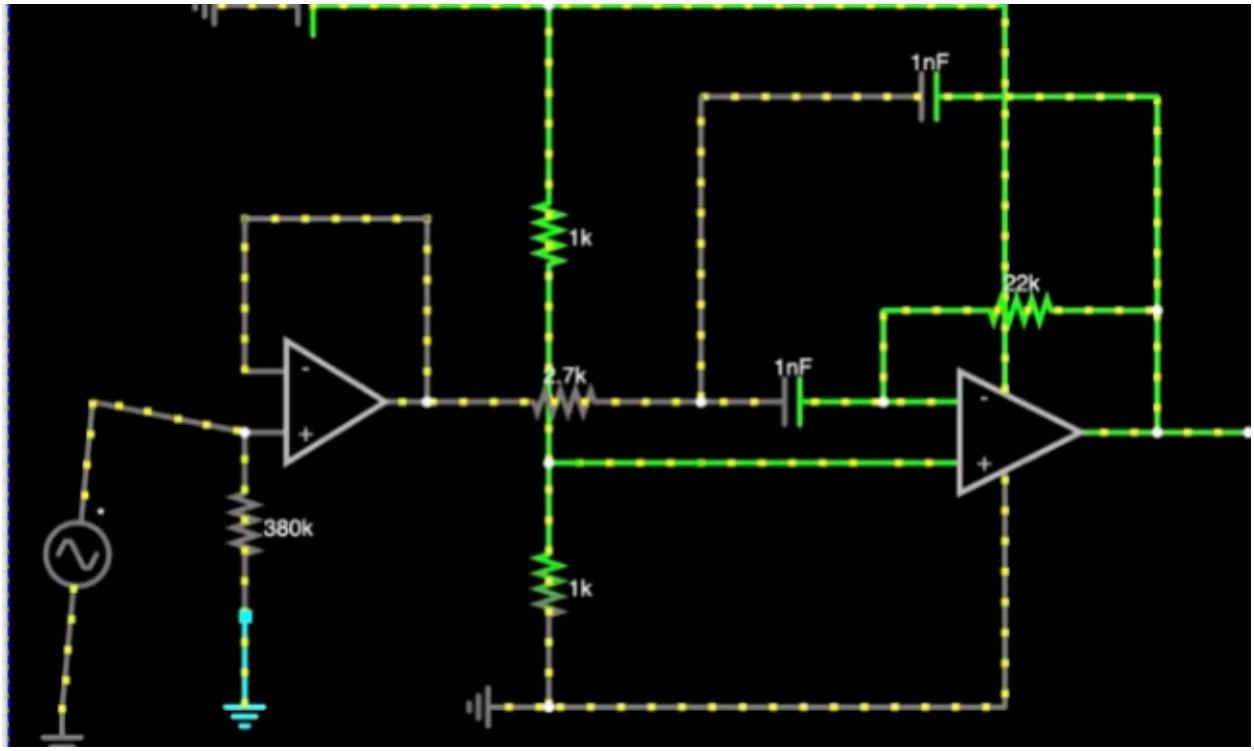
Over the last two weeks I have:

- Been determining a reliable method of AoA (angle of arrival) calculation, working alongside Matthew Shih’s circuit. I have modelled it and simulated it in EasyEDA
    - His circuit can be made much smaller upon inspection, and I believe it will benefit from a voltage averager (as seen in the rough draft below,) where LED’s are strictly on or off, determined by BJT’s going into the base. Below is the rough

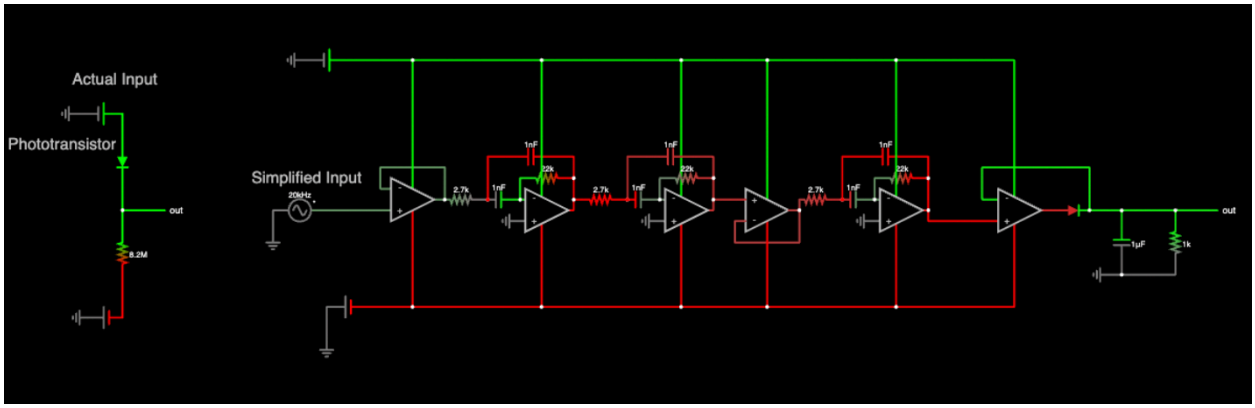
idea for what will likely be implemented.



- Modelled Aaron See's schematic and am looking at methods to prevent saturation of the op-amp's. Below was his approach:
  Filter:



  Input Sensor Diagram:



- Compiled all information and datasheets for each individual component into a USB for easy access to ensure power ratings and other key information is followed.
- Soon to solder all of the key (non-volatile) circuits to veroboards.

Challenges

- **Component Organisation**
  - People in my team, and people who are not will take a part and forget to return it. I need to go to JayCar to get more photodiodes tomorrow so that they can be soldered on.
  - Electret microphone wire is missing. This is a problem, however with our IR range we can still complete acceptance testing without it.
- **Synthesis**
  - Some teammates are still not fully done with their circuits, so I have to fill in and help out as we are facing a major deadline.
  - By some twist of fate every teammate in our group uses different simulation softwares, so I'm localising them all into EasyEDA.
- **Resources**
  - We are using near the maximum amount of op-amps by implementing the comparator, which is concerning as it could take away from the amplification stage.

Coming up

Acceptance testing on Monday. I suspect there will be weekend "overtime" working on the rectifiers. However, each subgroup has agreed to create a soft deadline where we present our work to one another over the weekend, including our presentations, as preparation. I think that wrapping everything up will be tough, but doable.