

Logic Synthesis With Design Compiler

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OUTLINE

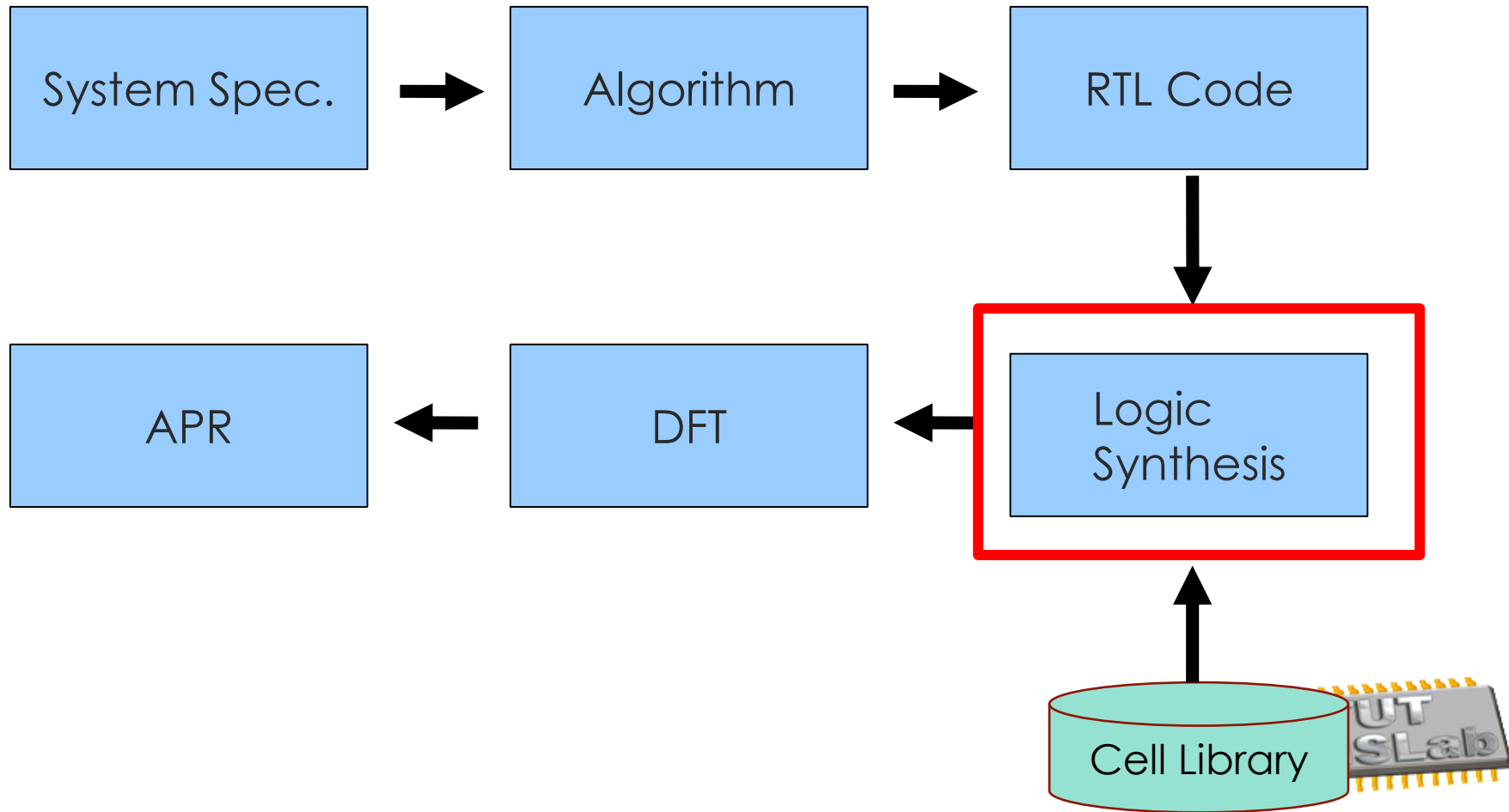
- Introduction
- Synthesis Object
- Synthesis GUI-Design Vision
- Setting Design Constraints
- Setting Design Environment
- Reports and Save file



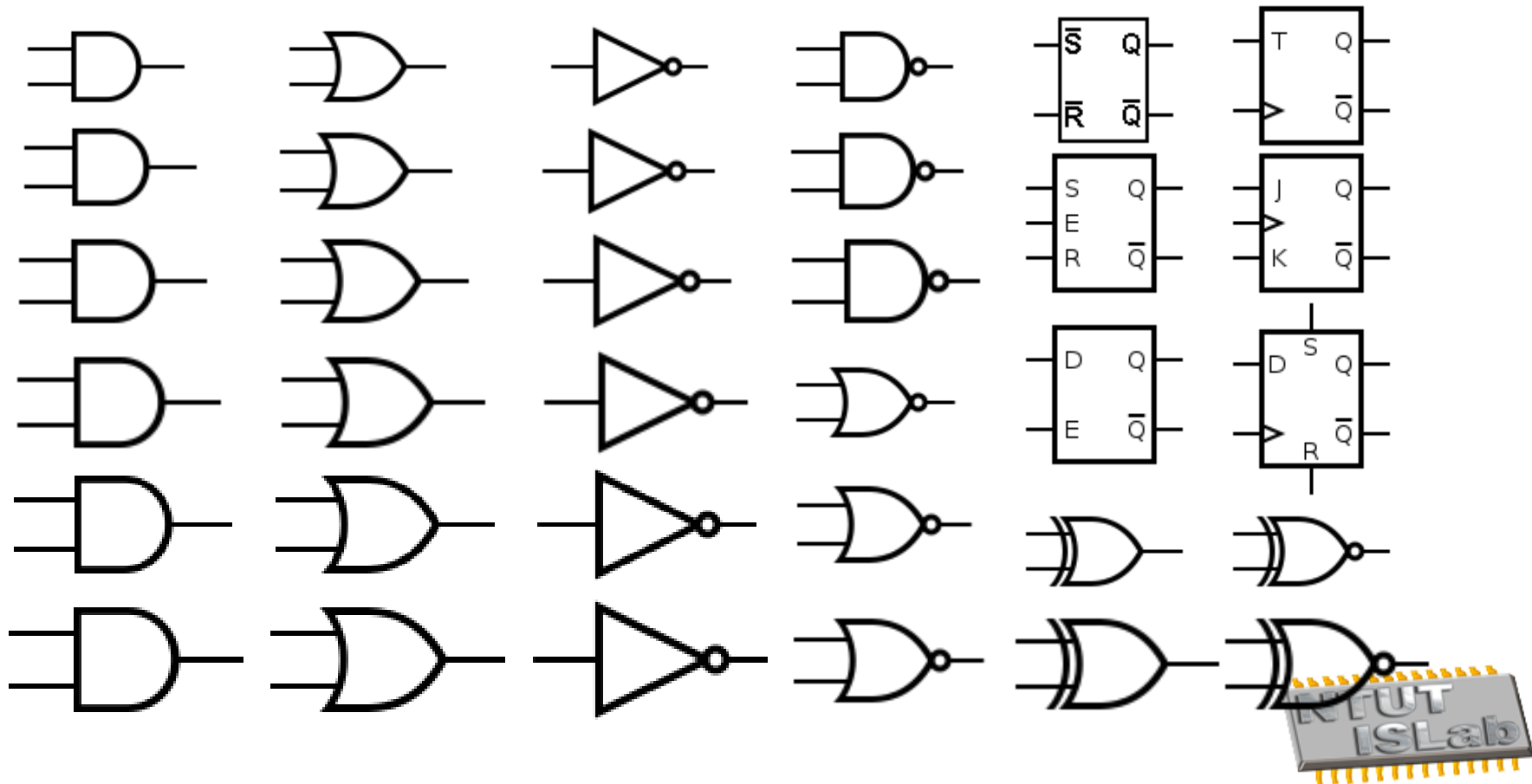
INTRODUCTION



Cell-Based Design flow



Cell Library (Logic Gate v.s. Lego)



Logic Synthesis

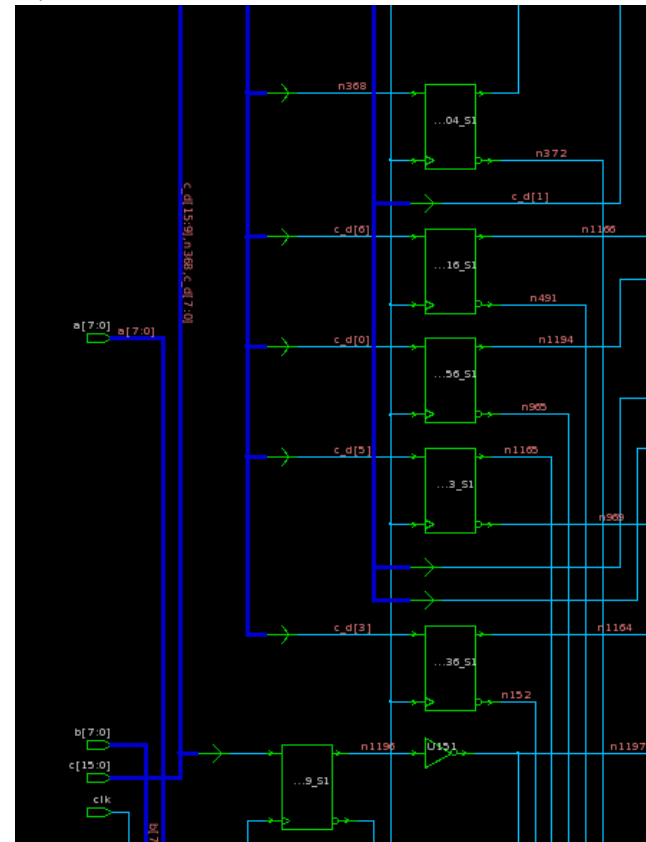
Behavior code

```
module top(clk,out,a,b,c);
output [15:0] out;
input [7:0] a,b;
input [15:0] c;
input clk;
reg [15:0] mul_out;
reg [15:0] out;
reg [15:0] c_d;

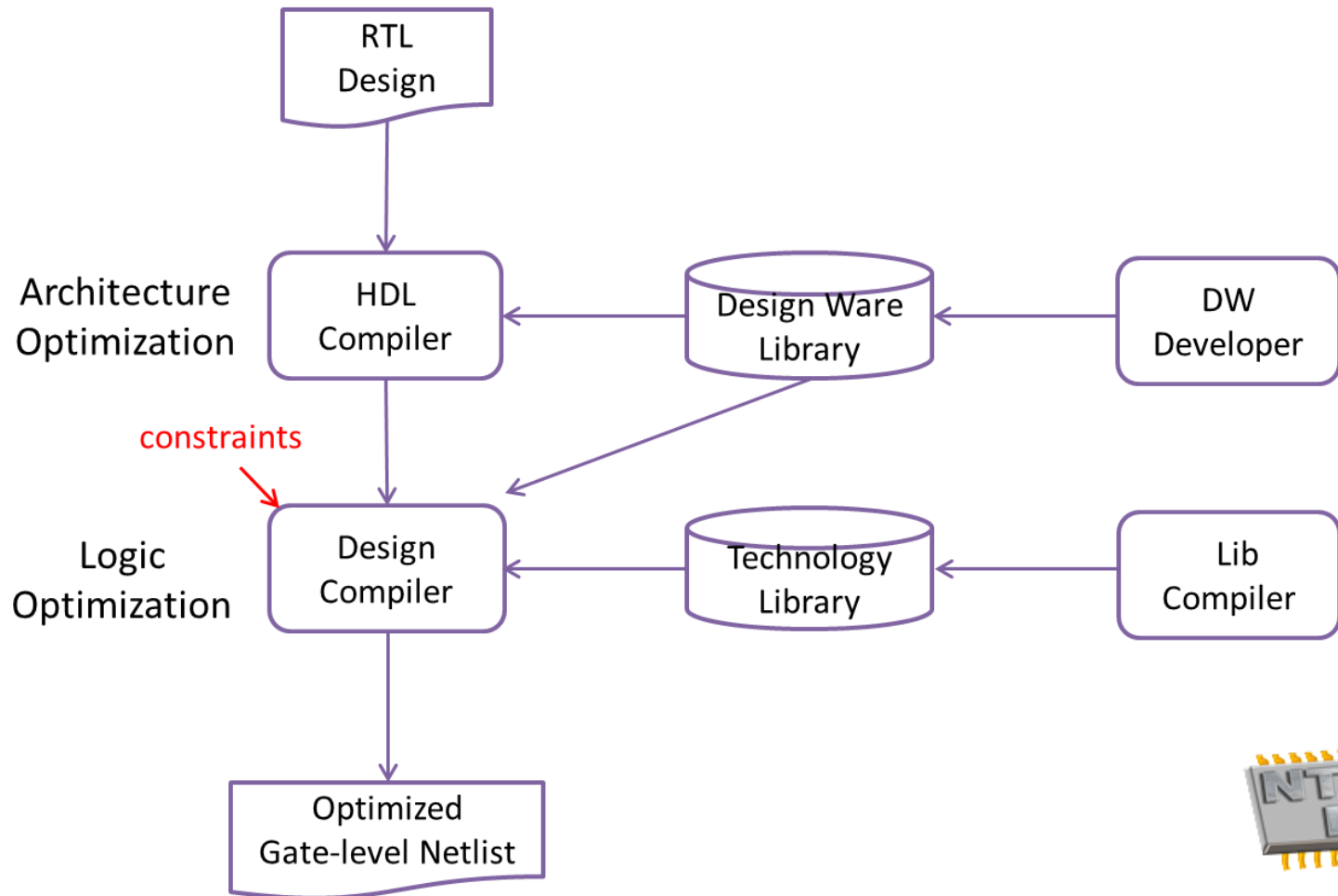
always @(posedge clk) mul_out=a*b;
always @(posedge clk) c_d=c;
always @(posedge clk) out=mul_out/c_d;

endmodule
```

Gate level code

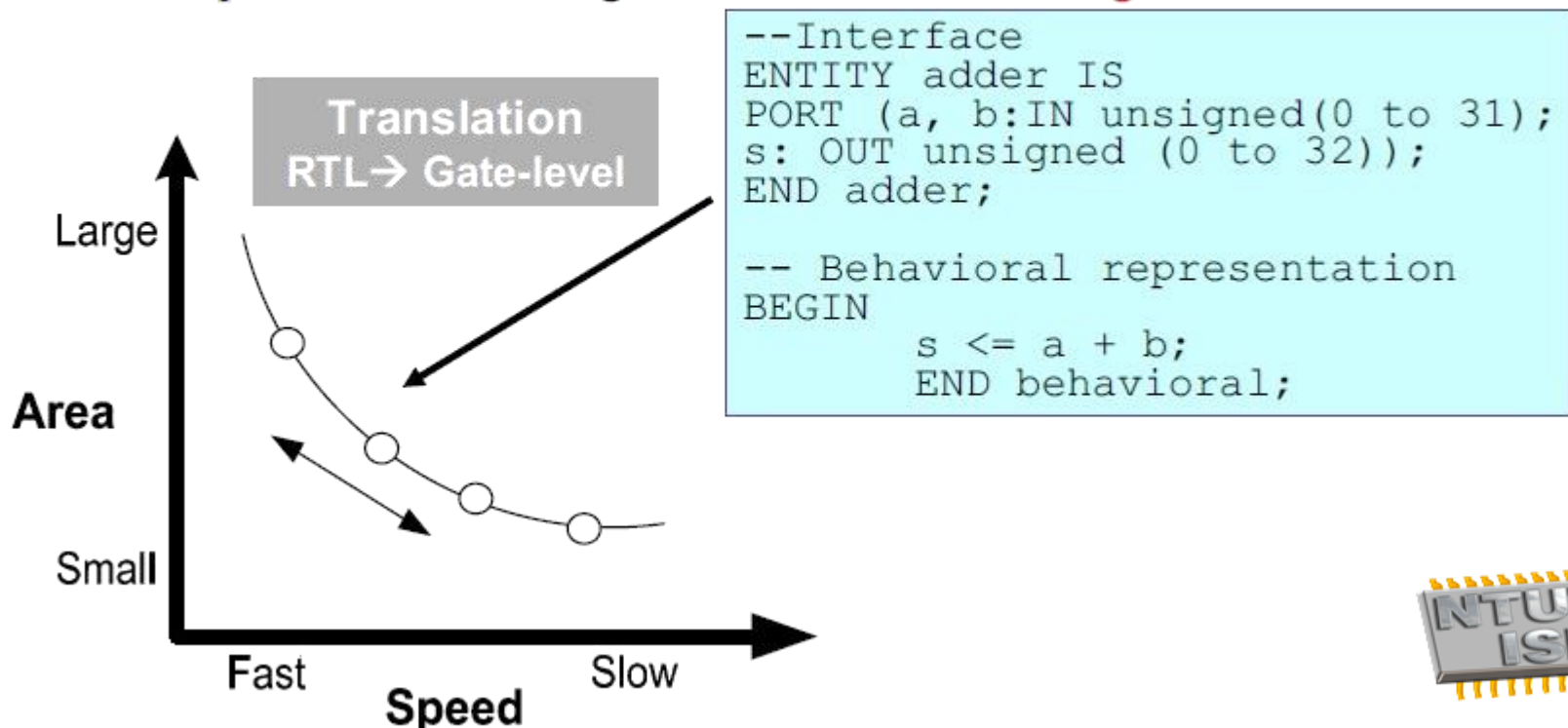


Logic Synthesis Overview



Synthesis is Constraint Driven

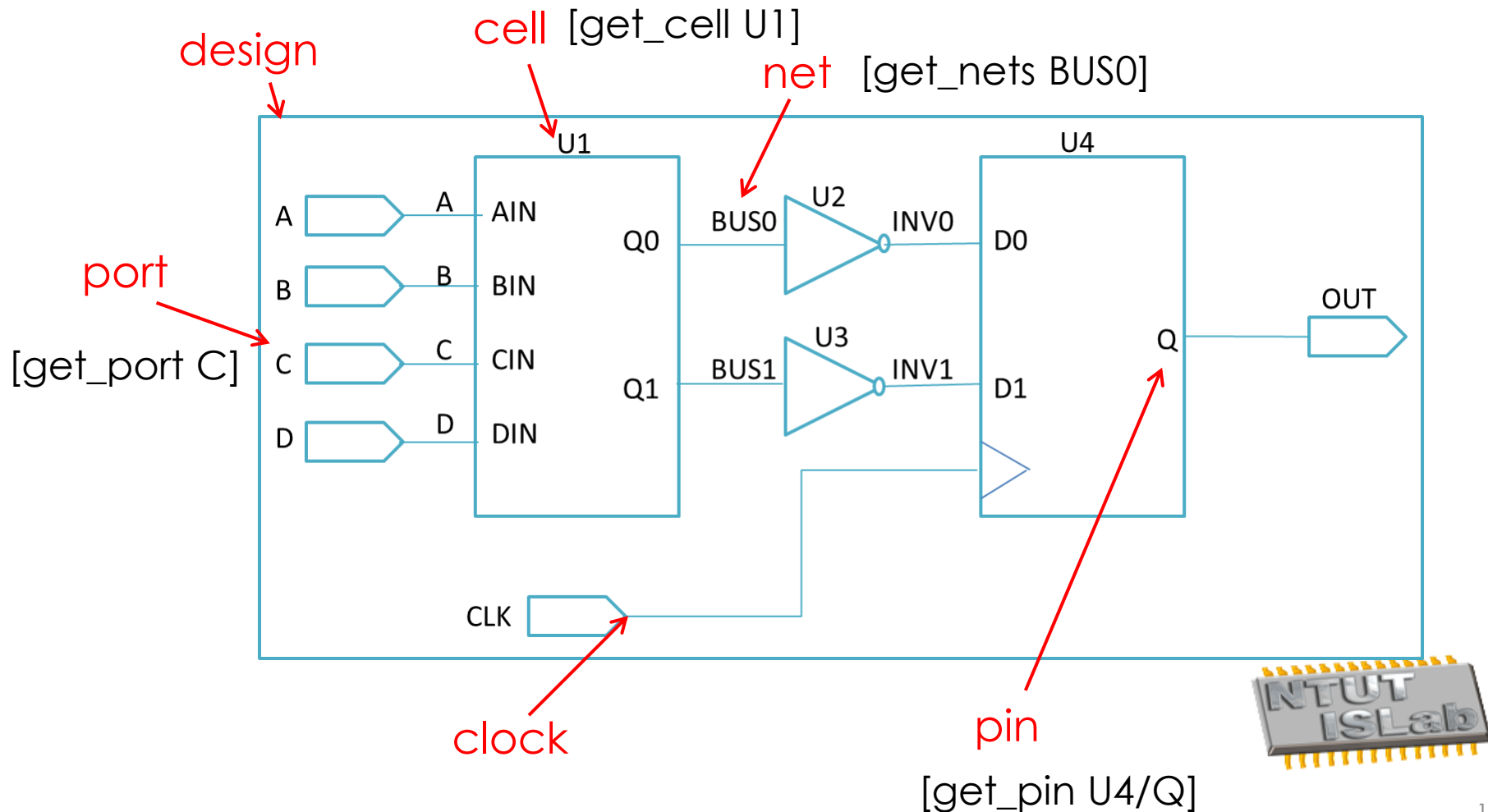
- Logic Synthesizer first translates RTL design to an intermediate gate-level design, then optimize according to the **area** and **timing** constraint.



SYNTHESIS OBJECT



Design Objects (1/2)



Design Objects (2/2)

- Design : A circuit that performs one or more logical functions.
- Cell : An instantiation of a design within another design.
- Port : The input or output of a design.
- Pin : The input or output of a cell.
- Net : The wire that connects ports to pins and/or pins to other each other.
- Clock : Waveform applied to a port or pin identified as a clock source.



SYNTHESIS GUI-DESIGN VISION



Environment Setup (1/3)

- Set the environmental files

Open Terminal

Key in Key in “ls -a .cs*”

“cp

/home/standard/Environment_Setup_File/cshrc .cshrc”

```
[t00418099@islax2 ~]$ ls -a .cs*
```

.cshrc

Key in “source .cshrc”



Environment Setup (2/3)

```
t107368062@islabx5:~/Desktop
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
[ t107368062@islabx5 ~/Desktop]$ ls -a .cs*
.cshrc
[ t107368062@islabx5 ~/Desktop]$ cp /home/standard/Environment_Setup_File/cshrc .
.cshrc
[ t107368062@islabx5 ~/Desktop]$ source .cshrc
-- Now source Cadence NC-Verilog --
-- Now source Synopsys Design Compiler --
Platform = amd64
-- Now source Synopsys Formality --
-- Now source Mentor MBISTArchitect ^ 空格
-- Now source Synopsys TetraMAX --
-- Now source Cadence INNOVUS --
-- Now source Mentor Calibre --
-- Now source Synopsys PrimeTime --
Platform = amd64
-- Now source Synopsys Nanosim --
-- Now source Synopsys Verdi --
Platform = LINUX
#####
# 32BIT is the default mode #
# If you want to run 64BIT mode, #
# please set the LD_LIBRARY_PATH and SHLIB_PATH #
# to path of 64BIT by yourself. #
#####
[ t107368062@islabx5 ~/Desktop]$
```

ls -a .cs* (*後面有空格)

cp /home/standard/Environment_Setup_File/cshrc .cshrc

^ 空格

^ 空格

source .cshrc

^ 空格

代表終端機(Terminal)，成功開啟



Environment Setup (3/3)

Create a New Folder for Synthesis

Ex:

1. `mkdir Synthesis` (terminal command)
2. `cd Synthesis` (terminal command)

Copy File for Environment Setting

△ 代表空格

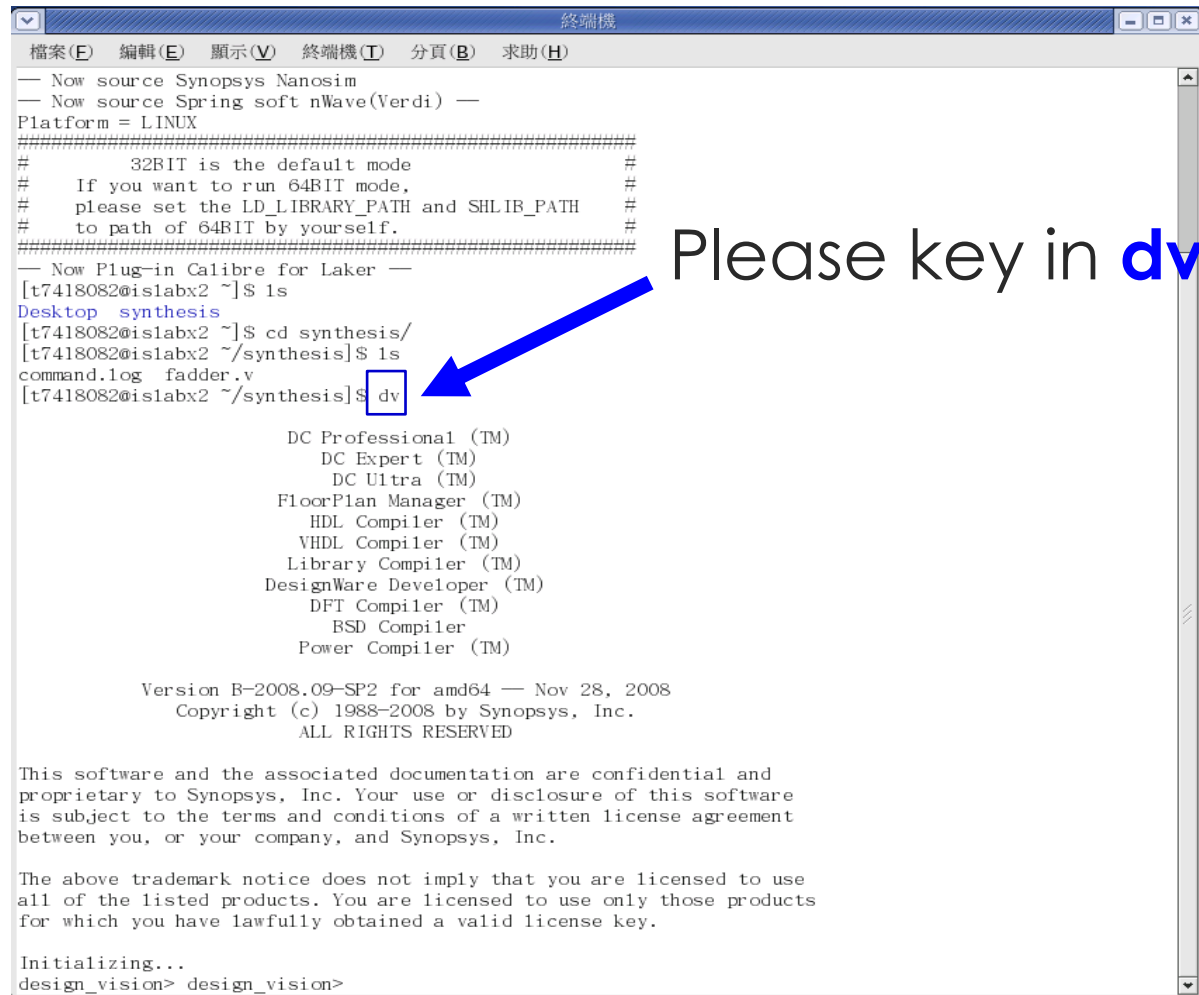
```
cp△  
/home/standard/Environment_Setup_File/synthesis_setup_for_18/synopsys_dc.s  
etup△.synopsys_dc.setup
```

Copy File for Synthesis

```
cp△/home/standard/vlsi_2022/synthesis/*△
```



Open Design Vision



```
终端機
檔案(E) 編輯(E) 顯示(V) 终端機(T) 分页(B) 求助(H)
— Now source Synopsys Nanosim
— Now source Spring soft nWave(Verdi) —
Platform = LINUX
#####
#       32BIT is the default mode           #
#       If you want to run 64BIT mode,      #
#       please set the LD_LIBRARY_PATH and  #
#       SHLIB_PATH to path of 64BIT by     #
#       yourself.                           #
#####
— Now Plug-in Calibre for Laker —
[t7418082@islabx2 ~]$ ls
Desktop  synthesis
[t7418082@islabx2 ~]$ cd synthesis/
[t7418082@islabx2 ~/synthesis]$ ls
command.log  fadder.v
[t7418082@islabx2 ~/synthesis]$ dv

    DC Professional (TM)
    DC Expert (TM)
    DC Ultra (TM)
    FloorPlan Manager (TM)
    HDL Compiler (TM)
    VHDL Compiler (TM)
    Library Compiler (TM)
    DesignWare Developer (TM)
    DFT Compiler (TM)
    BSD Compiler
    Power Compiler (TM)

Version B-2008.09-SP2 for amd64 — Nov 28, 2008
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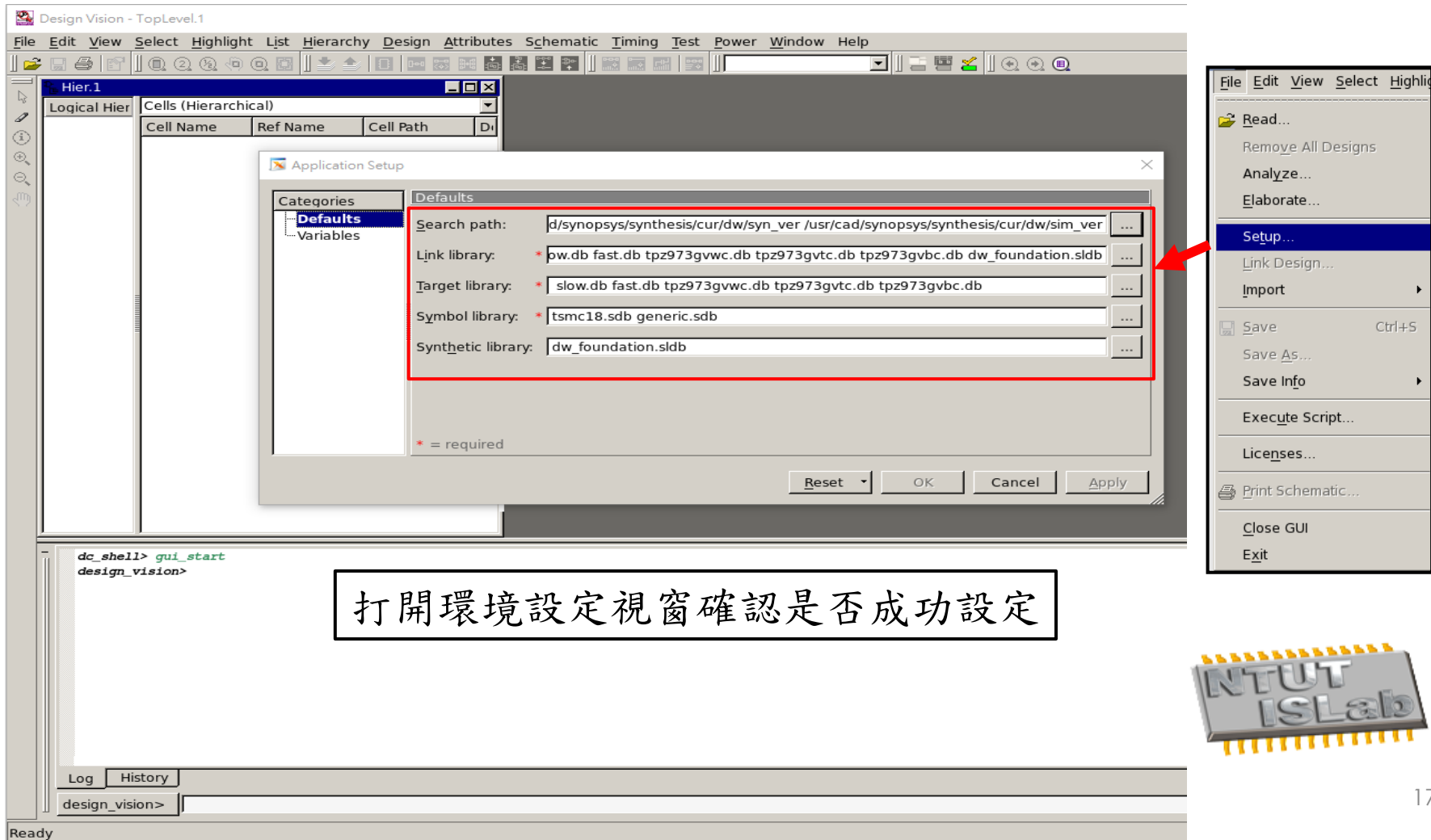
The above trademark notice does not imply that you are licensed to use
all of the listed products. You are licensed to use only those products
for which you have lawfully obtained a valid license key.

Initializing...
design_vision> design_vision>
```

Please key in **dv**



Environment Setup Check



Design Vision - TopLevel.1

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help

Hier.1

Logical Hier

Cells (Hierarchical)

Cell Name	Ref Name	Cell Path	Di
-----------	----------	-----------	----

Application Setup

Categories

- Defaults
- Variables

Defaults

Search path: d:\synopsys\synthesis\cur\dw\syn_ver /usr/cad/synopsys\synthesis\cur\dw\sim_ver ...

Link library: * pw.db fast.db tpz973gvwc.db tpz973gvtc.db tpz973gvbc.db dw_foundation.sldb ...

Target library: * slow.db fast.db tpz973gvwc.db tpz973gvtc.db tpz973gvbc.db ...

Symbol library: * tsmc18.sdb generic.sdb ...

Synthetic library: dw_foundation.sldb ...

* = required

Reset OK Cancel Apply

File Edit View Select Highlight

- Read...
- Remove All Designs
- Analyze...
- Elaborate...
- Setup...
- Link Design...
- Import
- Save Ctrl+S
- Save As...
- Save Info
- Execute Script...
- Licenses...
- Print Schematic...
- Close GUI
- Exit

dc_shell> gui_start
design_vision>

Log History

design_vision>

Ready

打開環境設定視窗確認是否成功設定

NTUT ISLab

Analysis the Design(1/2)

The screenshot shows the Design Vision - TopLevel.1 interface. The 'File' menu is open, and the 'Analyze...' option is highlighted. The 'Analyze Designs' dialog box is open, showing the file path 'C:\Users\user\Documents\2020_cic_synthesis\2020_summer_test\synthesis\CS.v' in the 'File names in analysis order:' field. The 'Format:' dropdown is set to 'Auto', and the 'Work library' is set to 'CS'. The 'Create new library if it does not exist' checkbox is checked. The 'OK' button is highlighted.

1. File

2. Analyze...

3. Add your design

4. Select work lib

Choose CS.v

Format: Auto

Work library: CS

☒ Create new library if it does not exist

OK Cancel

Log History

design_vision>

Analyze HDL files.

NTUT ISLab

Analysis the Design(2/2)

```
design_vision> sh mkdir CS
design_vision> define_design_lib CS -path ./CS
design_vision> analyze -library CS -format verilog {/home/t107368062/Desktop/2020_cic_synthesis/2020_summer_test/synthesis/CS.v}
Running PRESTO HDLC
Compiling source file /home/t107368062/Desktop/2020_cic_synthesis/2020_summer_test/synthesis/CS.v
Presto compilation completed successfully.
Loading db file '/home/cell_lib/CBDK_TSMC018_Arm_v4.0/CIC/SynopsysDC/db/slow.db'
Loading db file '/home/cell_lib/CBDK_TSMC018_Arm_v4.0/CIC/SynopsysDC/db/fast.db'
Loading db file '/home/cell_lib/CBDK_TSMC018_Arm_v4.0/CIC/SynopsysDC/db/tpz973gvwc.db'
Loading db file '/home/cell_lib/CBDK_TSMC018_Arm_v4.0/CIC/SynopsysDC/db/tpz973gvtc.db'
Loading db file '/home/cell_lib/CBDK_TSMC018_Arm_v4.0/CIC/SynopsysDC/db/tpz973gvbc.db'
Loading db file '/usr/cad/synopsys/synthesis/cur/libraries/syn/dw_foundation.sldb'
design_vision>
```

Log History

design_vision>



Elaborate the Design

The screenshot shows the Design Vision software interface. The 'File' menu is open, and the 'Elaborate...' option is highlighted. A red arrow points from the 'Elaborate...' menu item to the 'Elaborate Designs' dialog box. The dialog box has two dropdown menus: 'Library' set to 'CS' and 'Design' set to 'CS(verilog)'. Both dropdown menus are highlighted with a red box. The 'Parameters' table is empty. The 'Reanalyze out-of-date libraries' checkbox is unchecked. The 'OK' and 'Cancel' buttons are at the bottom.

1 File

2 Elaborate...

3 Select work lib

4 Select your design

Library: CS

Design: CS(verilog)

Parameters:

Name	Value
------	-------

☐ Reanalyze out-of-date libraries

OK Cancel



Symbol View

1 Select model or cell

2 Create Symbol View

Symbol View

```
in routine CS line 54 in file
'/home/t107368062/Desktop/2020_cic_synthesis/2020_summer_test/synthesis/CS.v'.
=====
| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |
=====
| Xt_reg       | Flip-flop | 12 | Y | N | Y | N | N | N | N |
=====
Presto compilation completed successfully.
Elaborated 1 design.
Current design is now 'CS'.
design_vision>
Current design is 'CS'.
Loading db file '/usr/cad/synopsys/synthesis/cur/libraries/syn/generic.sdb'
```

Log History

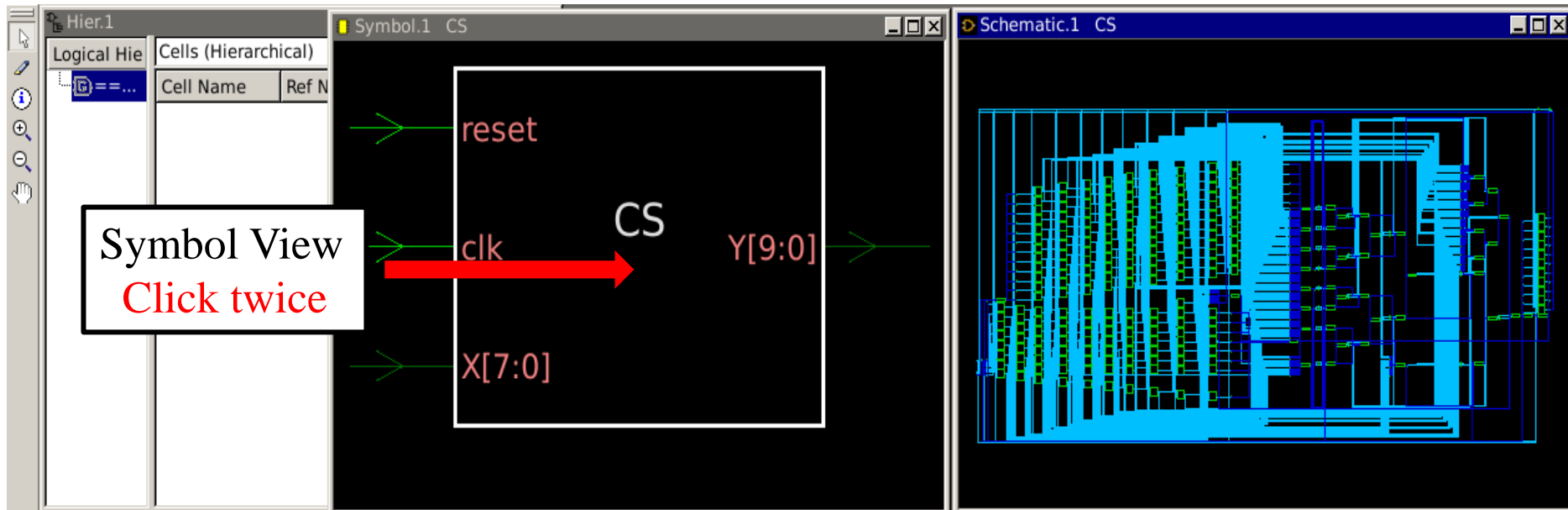
design_vision>

Ready

Design CS

NTUT ISLab

Schematic View



Schematic View



SETTING DESIGN CONSTRAINTS



Define Clock specification

- We need to accurately specify the clock including the clock routing details in the early design stage in order to achieve timing convergence.
- What should be defined?
 - ✓ Period
 - ✓ Area
 - ✓ Waveform
 - ✓ Max fanout
 - ✓ Uncertainty
 - skew
 - ✓ Latency
 - Source latency
 - Network latency
 - ✓ Transition
 - Input transition
 - Clock transition



Specify Clock

Command: `create_clock -name clk -period 20 -waveform {0 10} [get_ports clk]`
`set_dont_touch_network [get_clocks clk]`
`set_fix_hold [get_clocks clk]`

The screenshot shows the 'Specify Clock' dialog box in a CAD tool. The dialog box is titled 'Specify Clock' and has several fields and options. The steps are numbered 1 through 6:

- 1 Select clock port**: A red arrow points to the 'clk' port in the schematic view.
- 2**: A red arrow points to the 'Attributes' menu in the top toolbar.
- 3 Enter clk name**: A red box highlights the 'Clock name' field, which contains 'clk'.
- 4 Enter period**: A red box highlights the 'Period' field, which contains '20'.
- 5 Enter waveform**: A red box highlights the 'Edge' and 'Value' table, which contains the following data:

Edge	Value
Rising	0
Falling	10
- 6**: A red box highlights the 'Don't touch network' and 'Fix hold' checkboxes, both of which are checked.

The schematic view shows a clock signal 'clk' connected to a block 'X[7:0]'. The 'Attributes' menu is open, showing the 'Specify Clock...' option.



Report Clock

- Design → Report_Clocks

Attributes:

d - dont_touch_network
f - fix_hold
p - propagated_clock
G - generated_clock
g - lib_generated_clock

Clock	Period	Waveform	Attrs	Sources
clk	20.00	{0 10}	d f	{clk}

Current design is 'CS'.

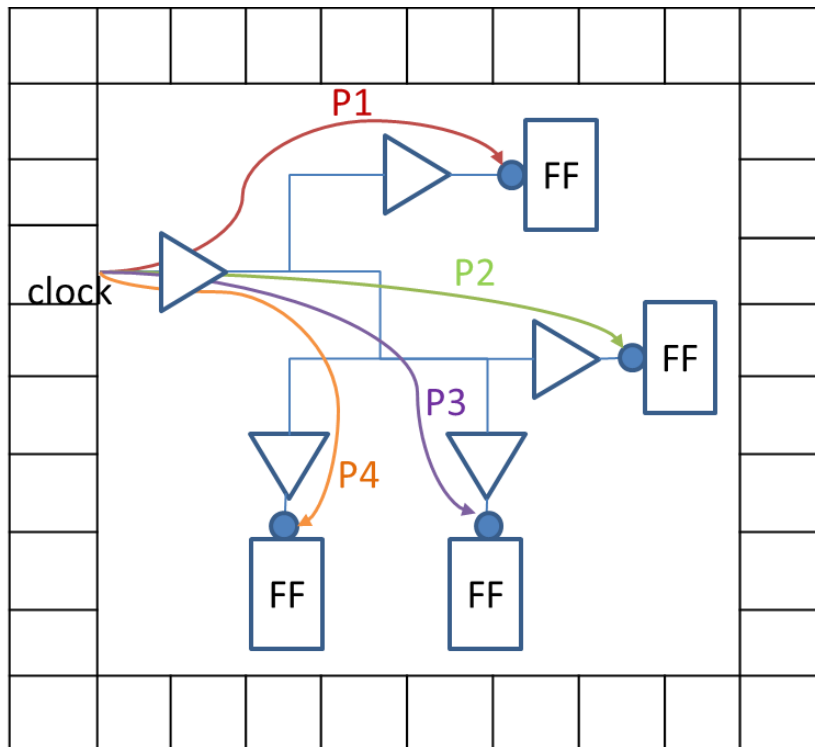
***** End Of Report *****



Clock skew

- The maximum difference between the arrival of clock signals at sequential cells in one clock domain or between domains.

Command: `set_clock_uncertainty 0.8 [get_clocks clock]`



Arrival(P1)=0.5ns

Arrival(P2)=1ns

Arrival(P3)=1.2ns

Arrival(P4)=1.3ns

Uncertainty = $1.3 - 0.5$
= 0.8ns **clock skew!!**

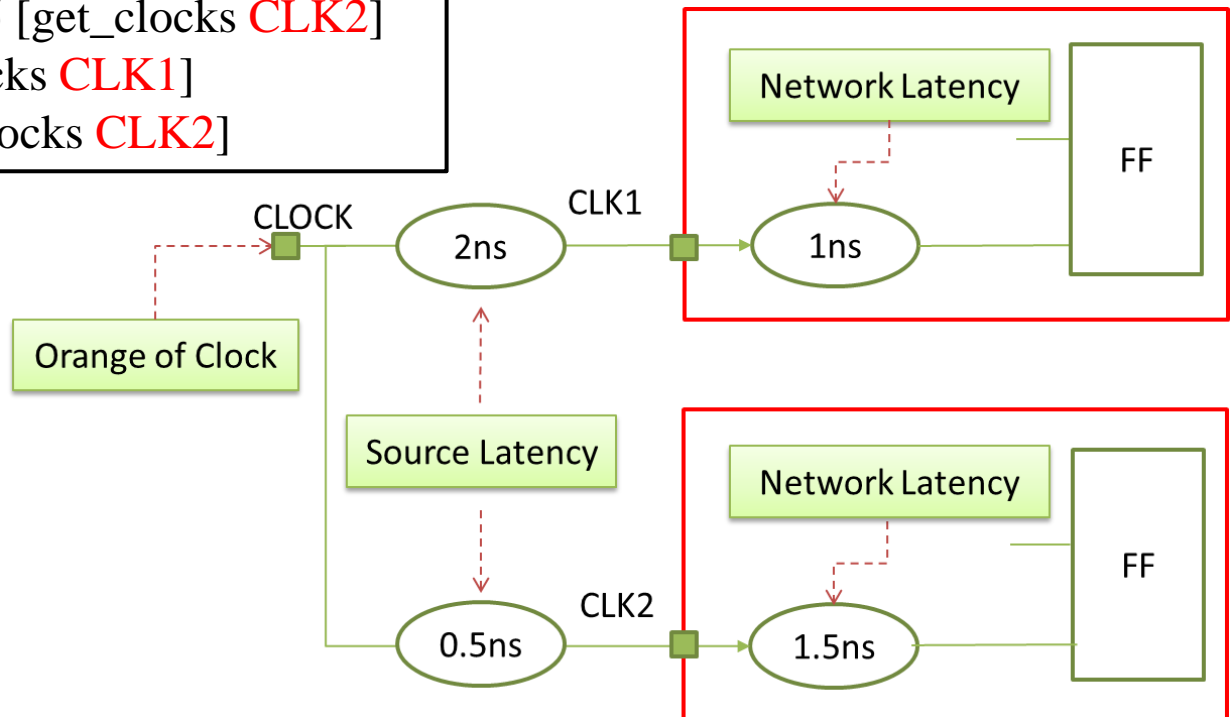


Model Source Latency

- Source latency is the propagation time from the actual clock origin to the clock definition point in the design.

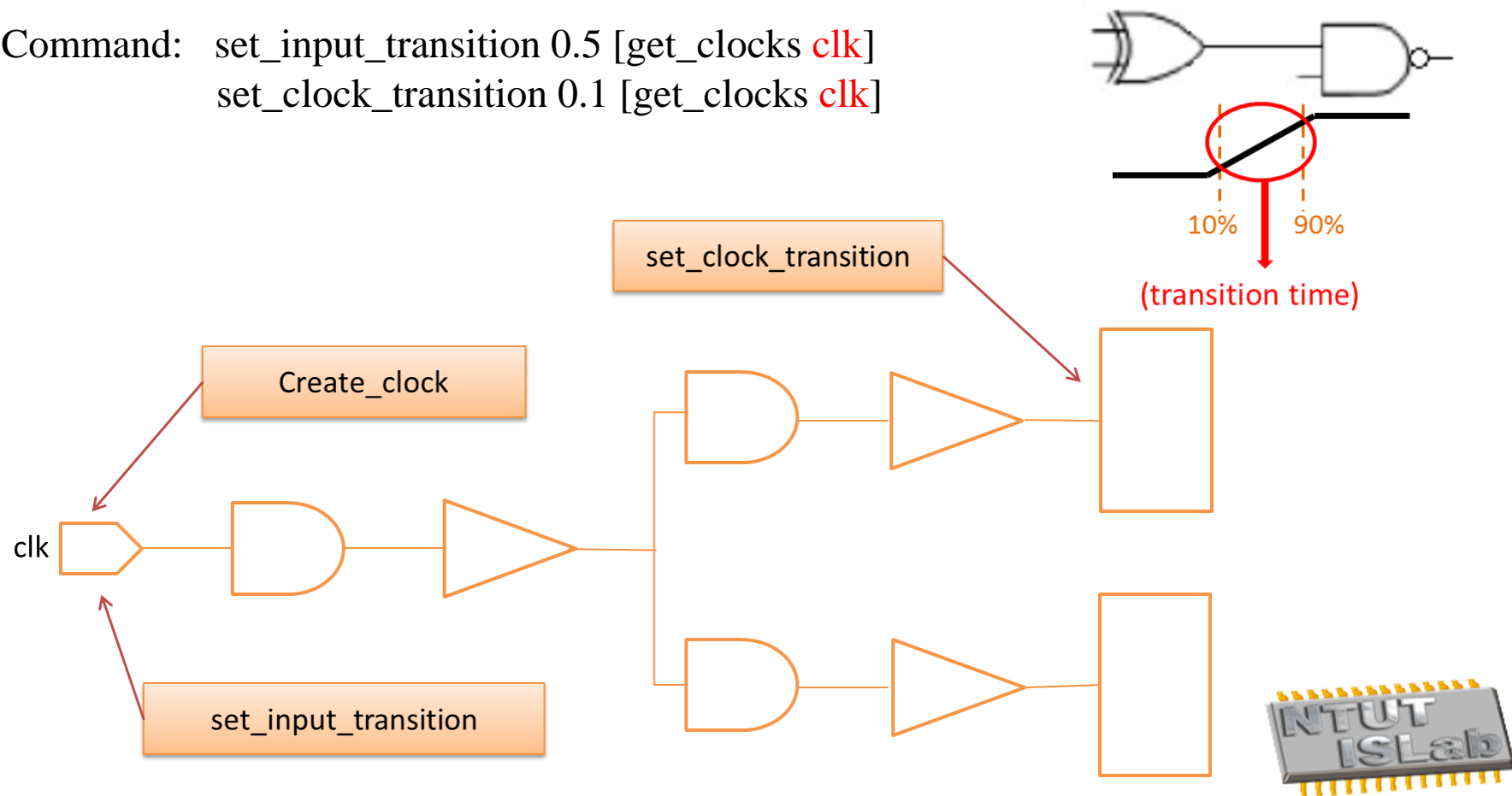
Command:

```
set_clock_latency -source 2 [get_clocks CLK1]  
set_clock_latency -source 0.5 [get_clocks CLK2]  
set_clock_latency 1 [get_clocks CLK1]  
set_clock_latency 1.5 [get_clocks CLK2]
```



Clock Transition Time

Command: `set_input_transition 0.5 [get_clocks clk]`
`set_clock_transition 0.1 [get_clocks clk]`

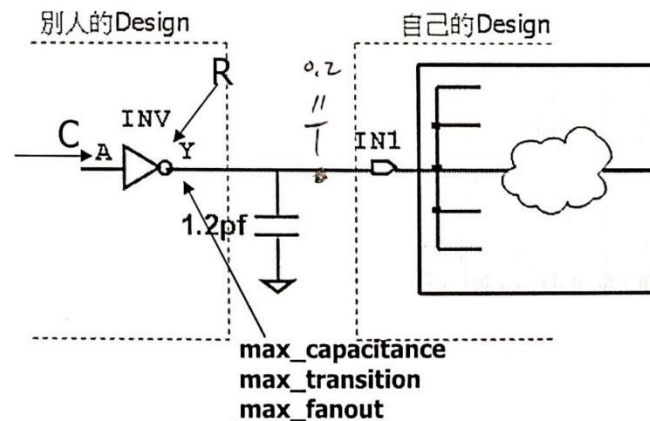


Design Rule Constraints

- ◆ Vendors impose design rules that restrict how many cells are connected to one another based on capacitance, transition and fanout
- ◆ You may apply more conservative design rules to:
 - Anticipate the interface environment your block will see
 - Prevent the design from operating cells close to their limits, where performance degrades rapidly

DRC Syntax:

```
set_max_capacitance 0.1 [get_ports IN1]
set_max_transition 0.2 [get_ports IN1]
set_max_fanout 10 [get_ports IN1]
```

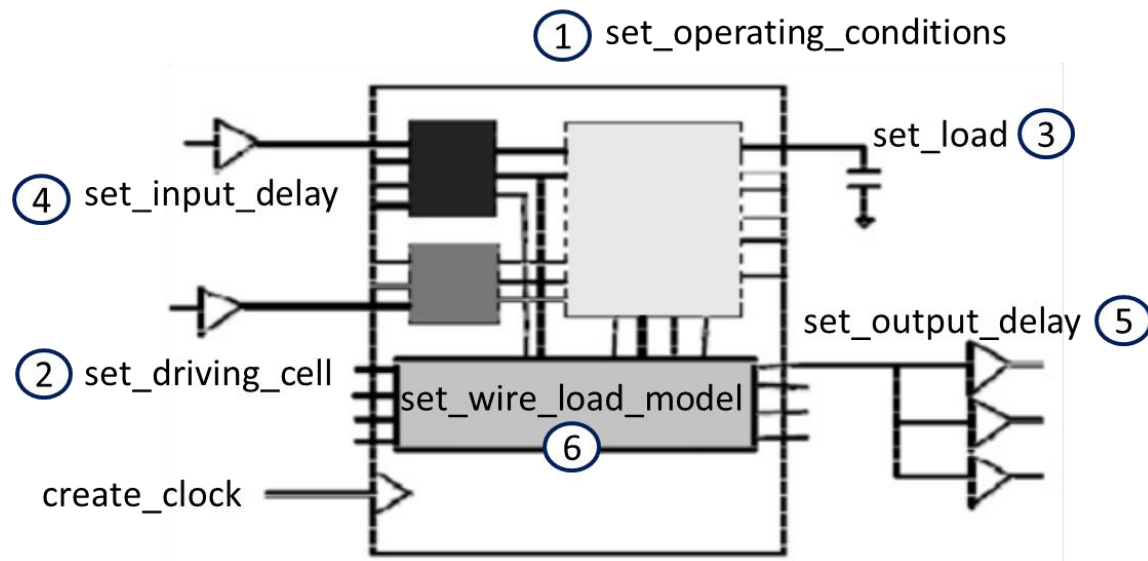


SETTING DESIGN ENVIRONMENT

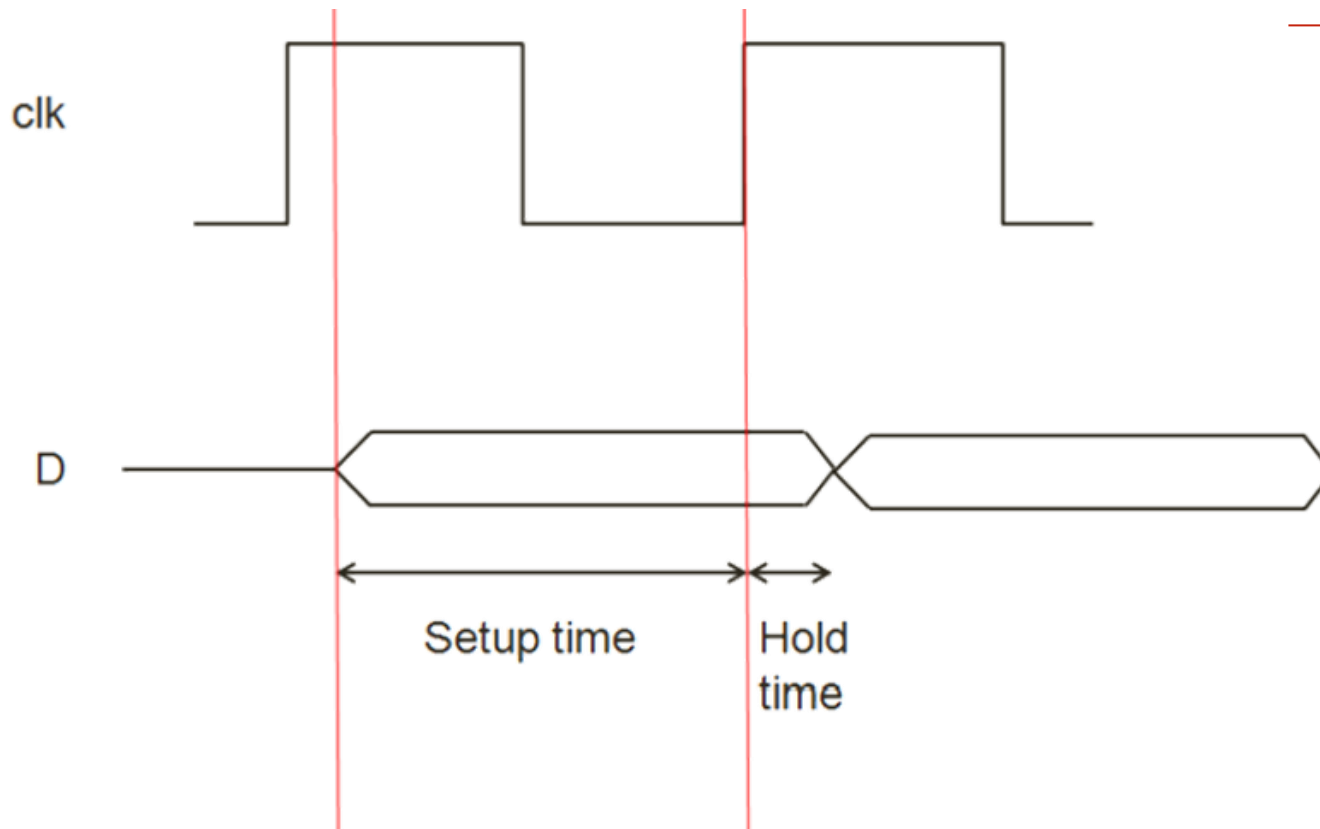
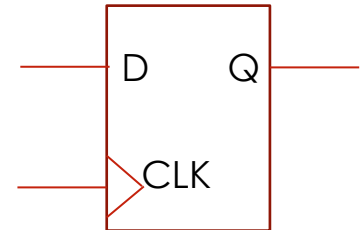


Real World Environmen

- Beware the defaults are not realistic conditions
 - ✓ Input drive is not infinite
 - ✓ Capacitive loading is usually not zero
 - ✓ Consider process, voltage, temperature (PVT) variation



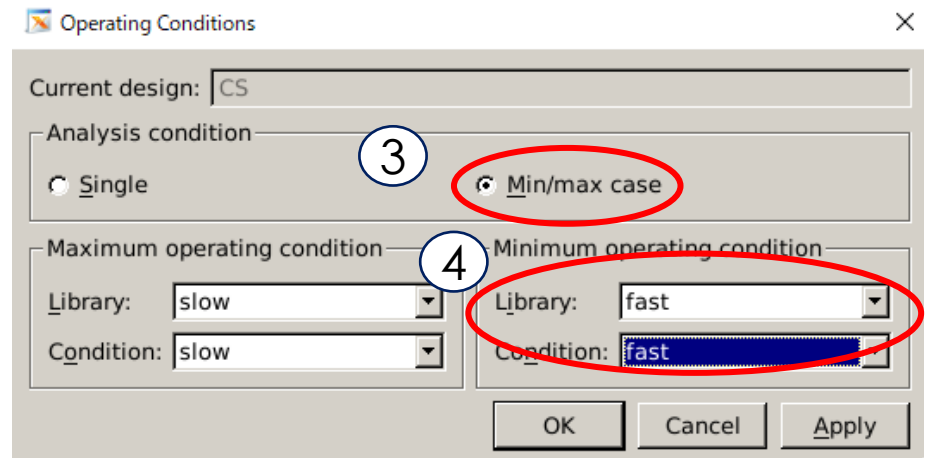
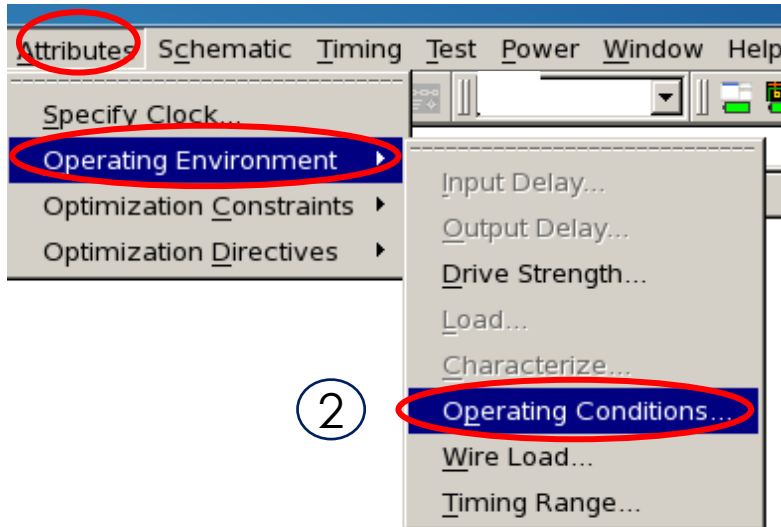
Setup Time & Hold Time



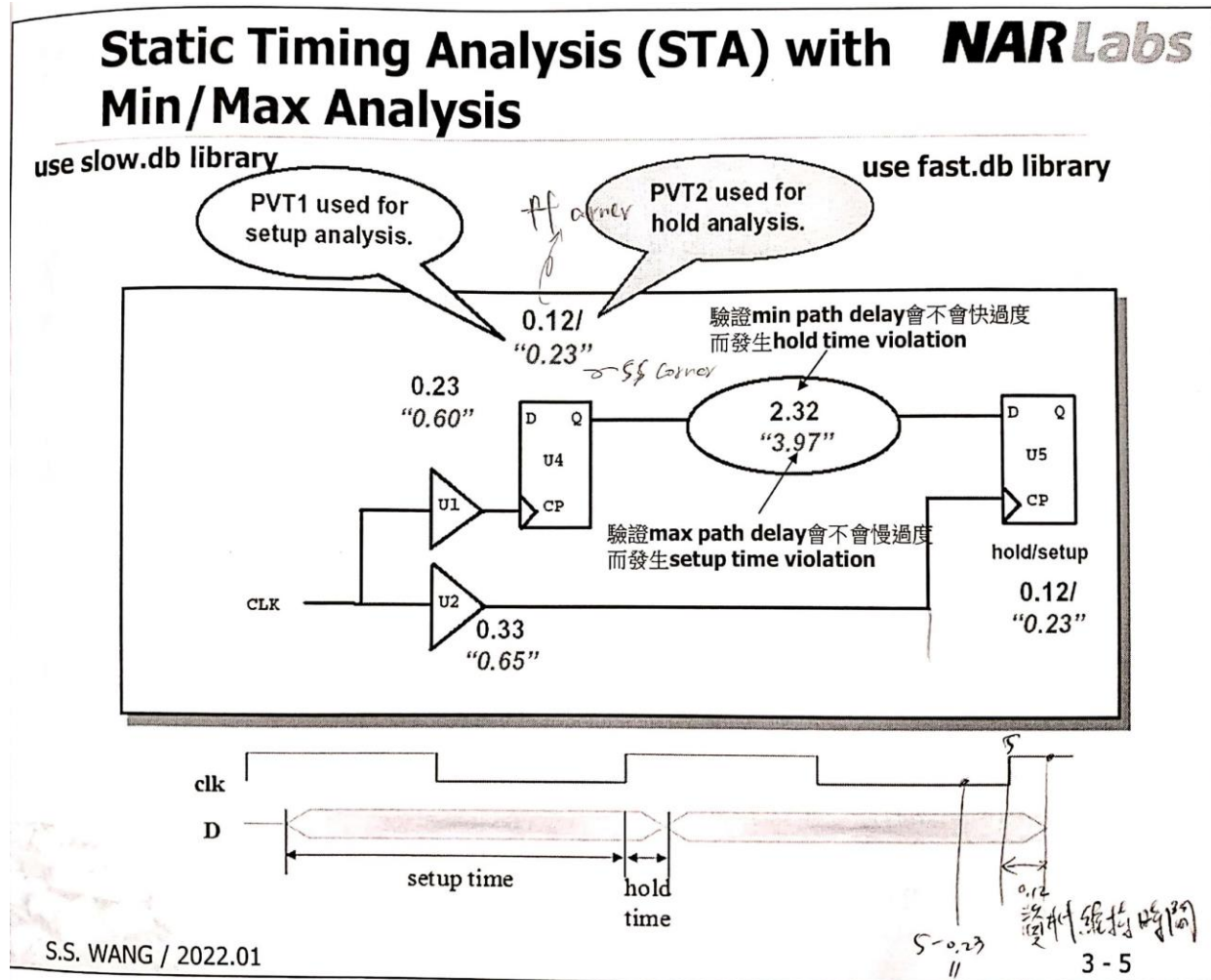
Setting Operating Condition

Command: `set_operating_conditions -min_library fast -min fast -max_library slow -max slow`

①



Setting Operating Condition



Setting driving Cell and output load

1. Setting input driving strength for clk port

```
-> set_driving_cell -library slow -lib_cell BUFX4 -pin { Y }  
    [get_ports clk]
```

2. Setting input driving strength for all input port except clk

```
-> set_driving_cell -library slow -lib_cell DFFX1 -pin { Q }  
    [remove_from_collection [all_inputs] [get_ports clk]]
```

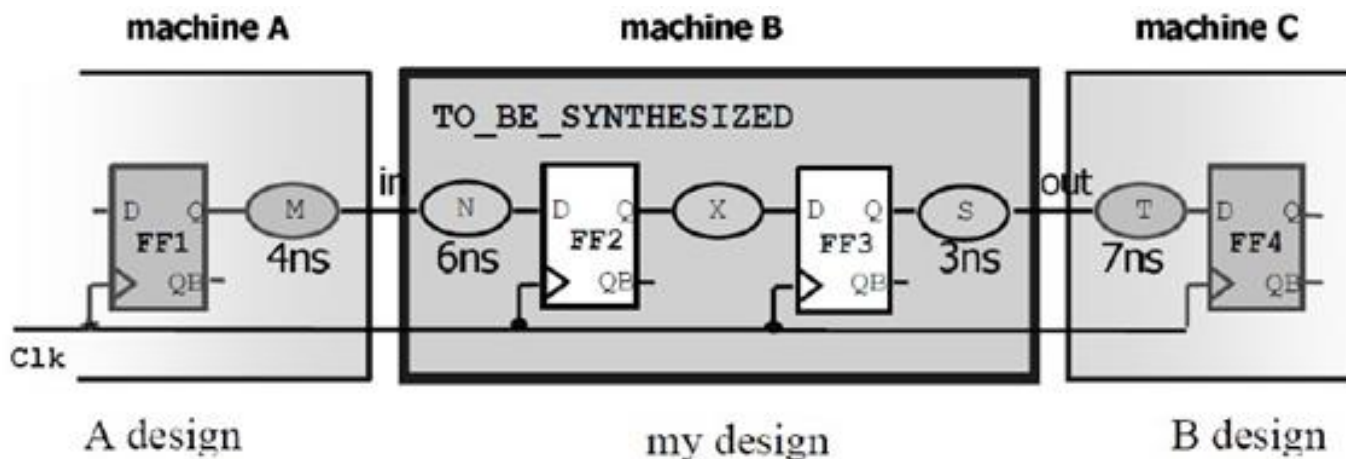
3. Setting output load 0.001913

```
-> set_load 0.001913 [all_outputs]
```



Input Delay and Output Delay

- Clock cycle $\geq (\text{DFF}_{\text{clk}} - \text{Q delay}) + X + \text{DFF}_{\text{setup}}$
- Input Delay = $(\text{DFF}_{\text{clk}} - \text{Q delay}) + M$
- Output delay = $T + \text{DFF}_{\text{setup}}$

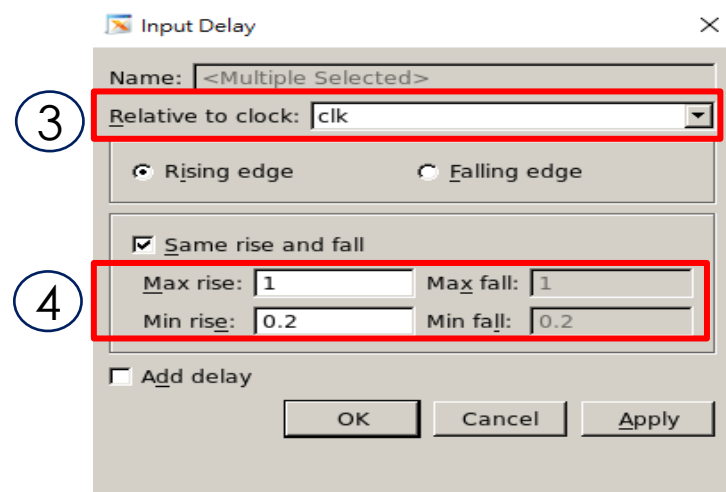
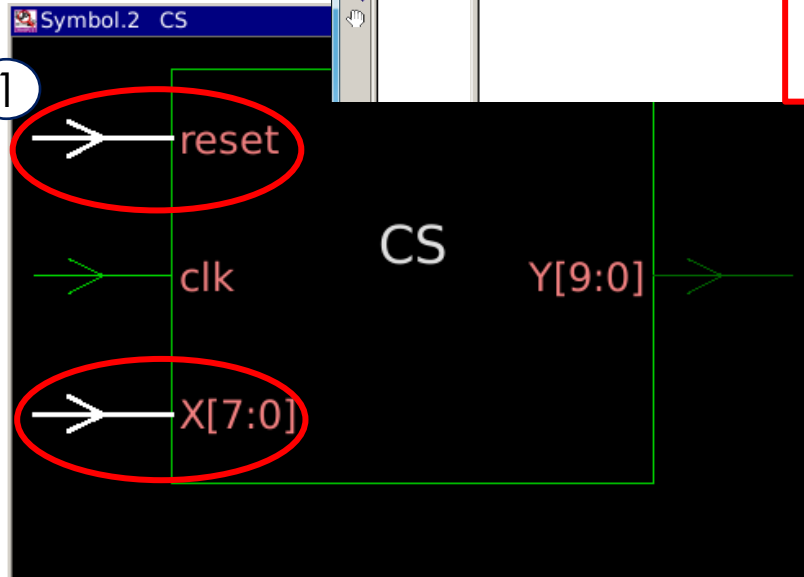
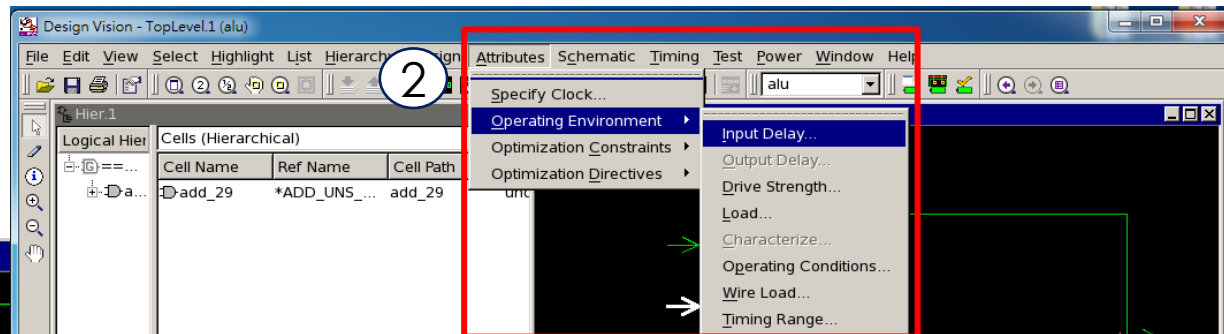


```
design_vision>set_input_delay -clock#clk -max 4 [get_ports in]
design_vision>set_output_delay -clock#clk -max 7 [get_ports out]
```



Setting Input Delay

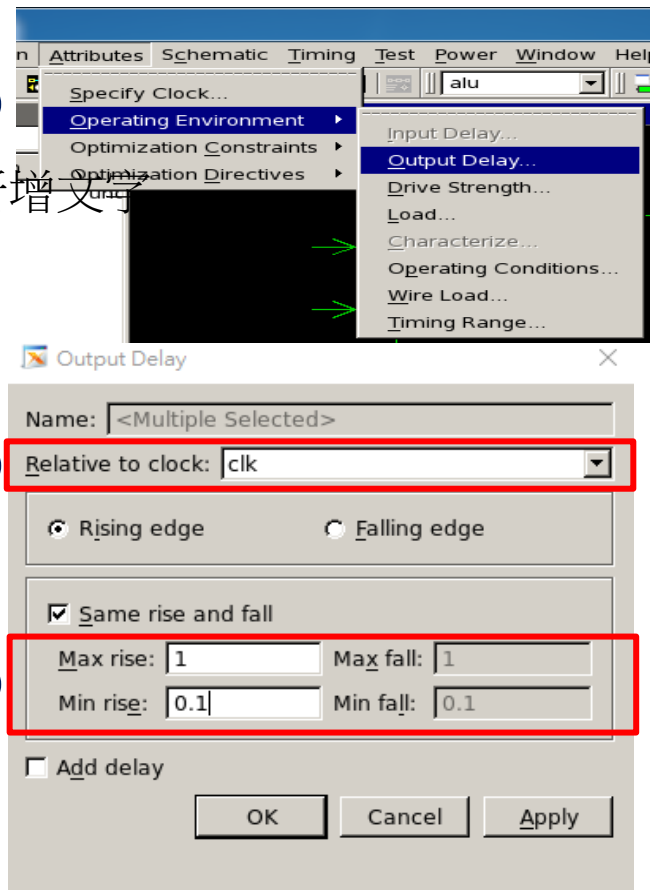
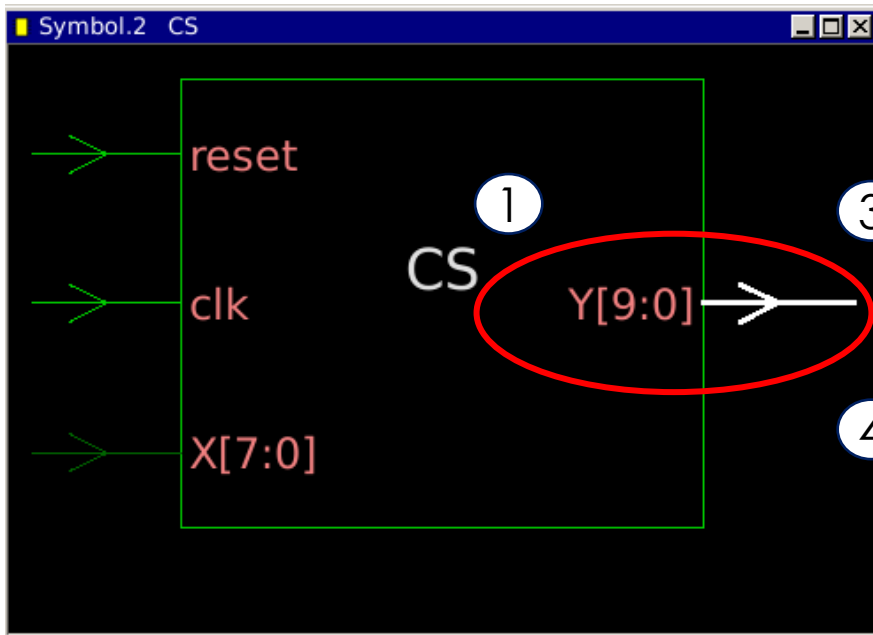
```
set_input_delay -clock clk -max 1 [remove_from_collection [all_inputs] [get_clocks clk]]  
set_input_delay -clock clk -min 0.2 [remove_from_collection [all_inputs] [get_clocks clk]]
```



Setting Output Delay

Command: `set_output_delay -clock clk -max 1 [all_outputs]`
`set_output_delay -clock clk -min 0.1 [all_outputs]`

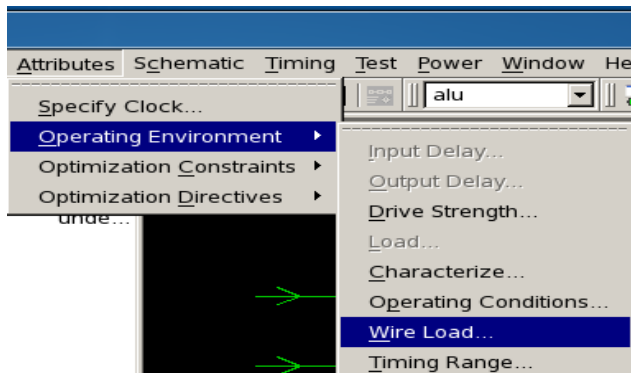
按一下以新增文字



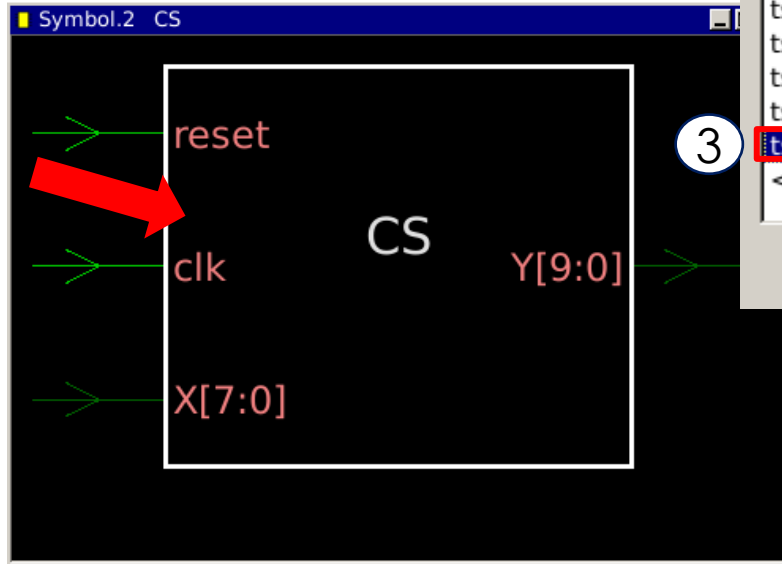
Setting Wire Load Model for Net Delay

Command: `set_wire_load_model -name tsmc18_wl10 -library slow`

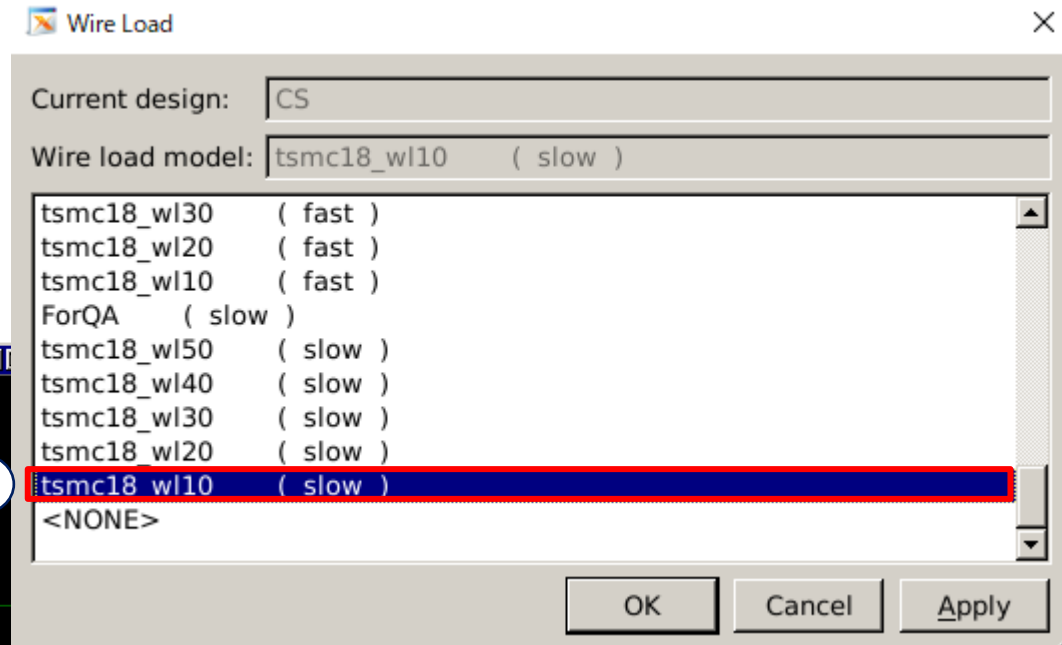
2



1



3



Check & unquify Design

- You have to check design after setting.

Command:

->check_design -multiple_designs

->uniquify



REPORTS AND SAVE FILE



Reports Before Compiler

The screenshot shows the Design Vision software interface. The 'Design' menu is open, and 'Report Ports...' is selected. The 'Report Ports' dialog box is open, showing the 'Report for' section with 'Ports' set to 'Selection'. The 'Report options' section has 'Significant digits' set to 4. The 'Output options' section has 'To report viewer' checked. The 'Report.2 - Port' window is open, showing a table of port data. A red box highlights the output loading values for Y[0] through Y[9], all of which are 0.001913. A red arrow points from the 'Report Ports...' menu item to the 'Report.2 - Port' window.

Design Vision - TopLevel.1 (CS)

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help

Hier.1 Cells (Hierarchical) Symbol.3 CS

Design Attributes Schematic

Compile Design...
Compile Ultra...
Check Design...
Report Design...
Report Design Hierarchy...
Report Design Resources...
Report Constraints...
Report Reference...
Report Ports...
Report Cells...
Report Nets...
Report Clocks...
Report Area...
Report Compile Options...
Report Power...
Reset Current Design

reset
clk
X[7:0]

Report.2 - Port

X[1]	in	0.0000	0
X[2]	in	0.0000	0
X[3]	in	0.0000	0
X[4]	in	0.0000	0
X[5]	in	0.0000	0
X[6]	in	0.0000	0
X[7]	in	0.0000	0
clk	in	0.0000	0
reset	in	0.0000	0
Y[0]	out	0.0019	0.0000 -- -- --
Y[1]	out	0.0019	0.0000 -- -- --
Y[2]	out	0.0019	0.0000 -- -- --
Y[3]	out	0.0019	0.0000 -- -- --
Y[4]	out	0.0019	0.0000 -- -- --
Y[5]	out	0.0019	0.0000 -- -- --
Y[6]	out	0.0019	0.0000 -- -- --
Y[7]	out	0.0019	0.0000 -- -- --
Y[8]	out	0.0019	0.0000 -- -- --
Y[9]	out	0.0019	0.0000 -- -- --

***** End Of Report *****

Report Ports

Report for:

Ports: Selection

Report options

☐ No line split ☐ Verbose

☐ Show only input port drive

Significant digits: 4

Output options

☒ To report viewer

☐ To file: Report.txt Browse...

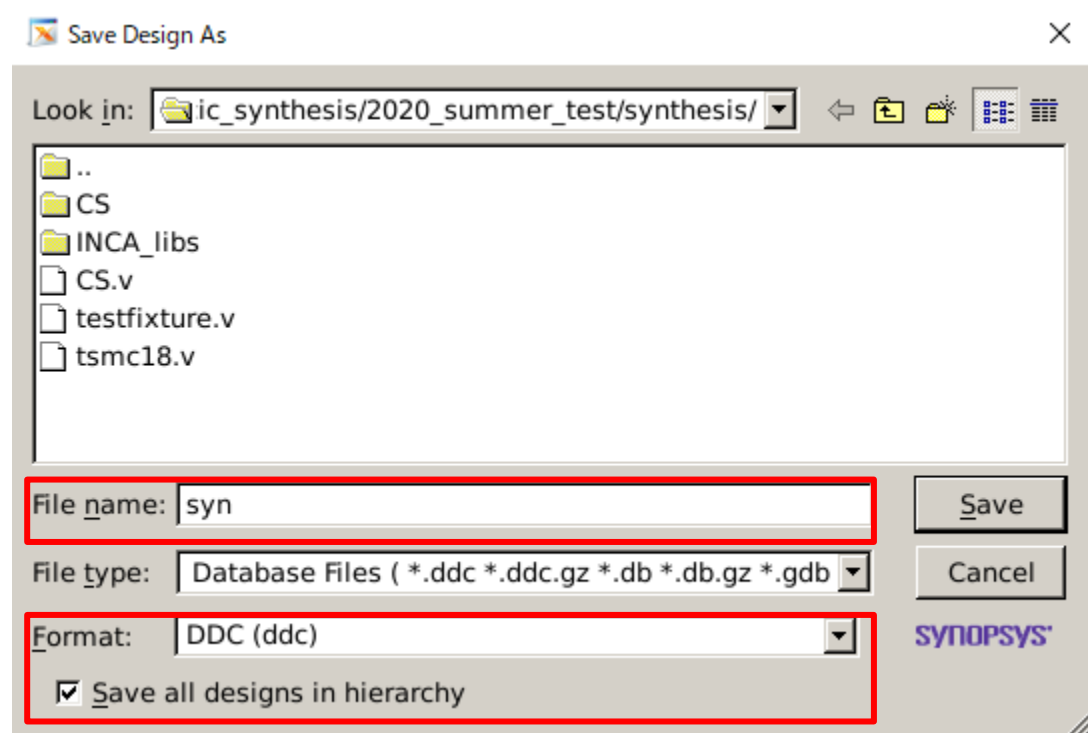
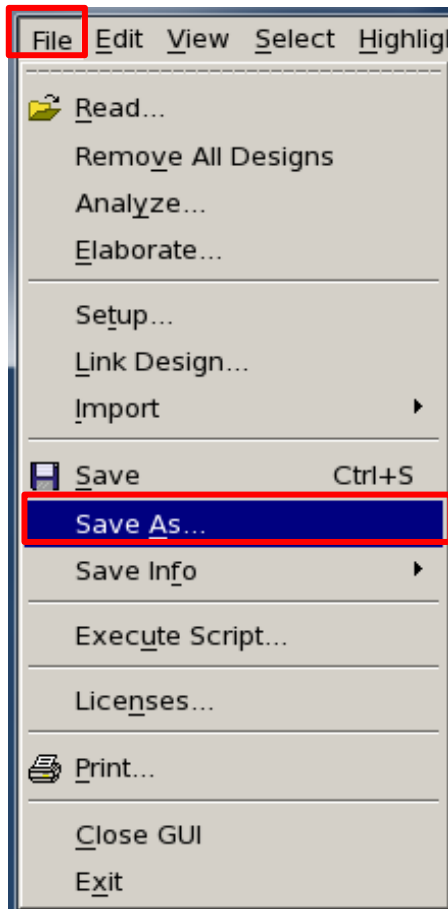
☒ Append to file

OK Cancel Apply

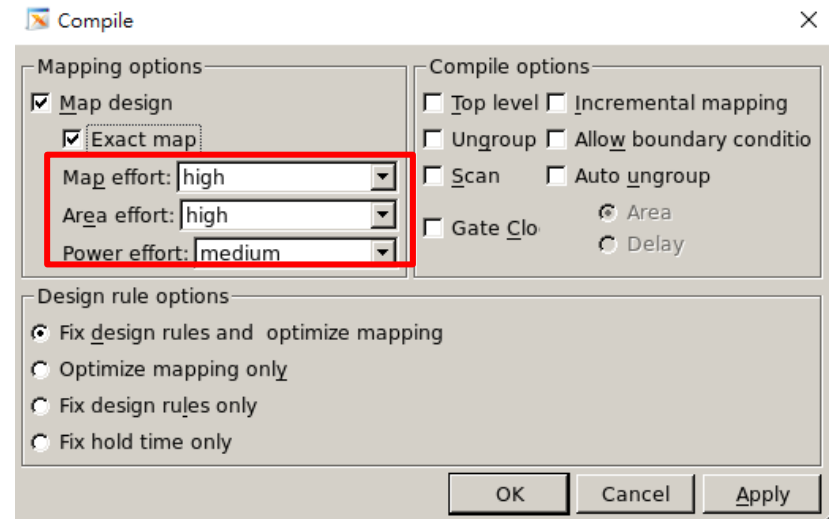
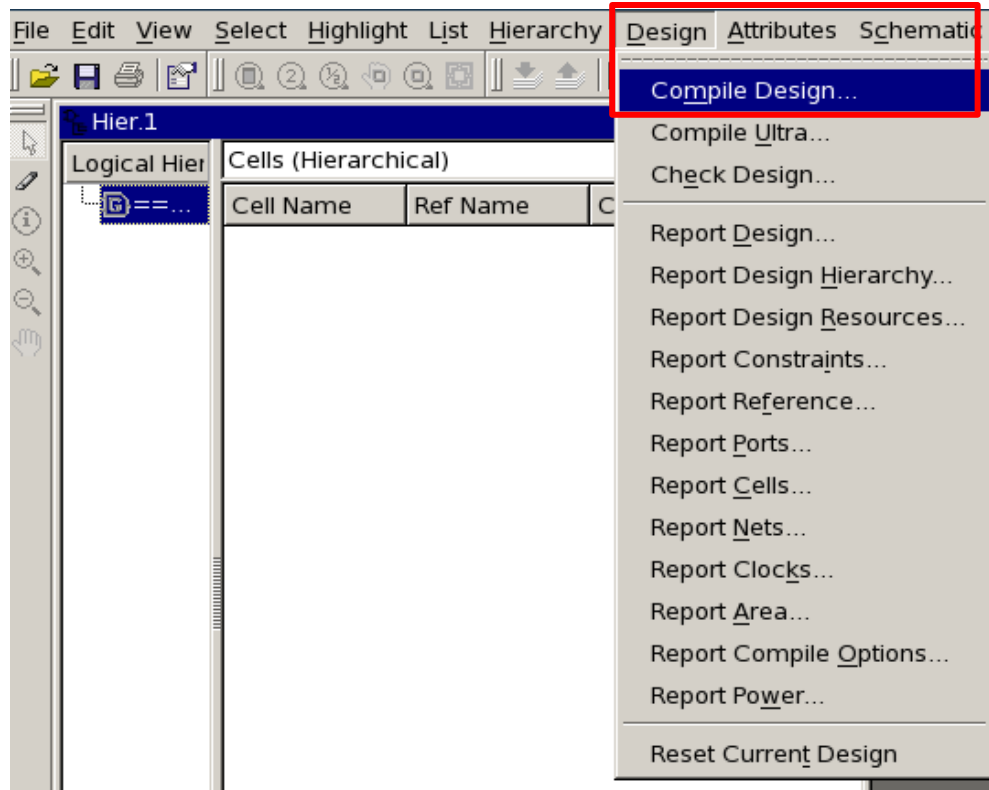
NTUT ISLab

Make sure the output loading is 0.001913 in Report Ports.

Save Design as .DDC File

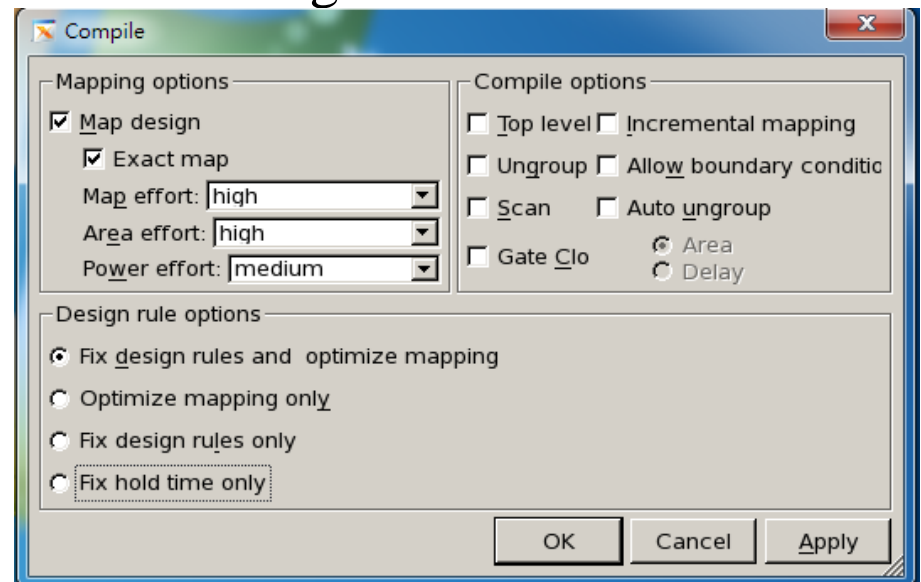


Compile Design



Mapping Effort

- Three effort levels, low, medium, high, determine relative amount of CPU time spent during mapping phase of compile.
 - Low - quicker synthesis, does not do all algorithms.
 - Medium – default, good, for many design.
 - High – it does critical path re-synthesis, but it will use more CPU time; in some cases the action of compile will not terminate.



Explore The Schematic View

The screenshot shows the Design Vision software interface. The main window is titled "Design Vision - TopLevel.1 (CS)". The menu bar includes File, Edit, View, Select, Highlight, List, Hierarchy, Design, Attributes, Schematic, Timing, Test, Power, Window, and Help. The toolbar contains various icons for file operations, navigation, and design actions. The "Hierarchy" menu is open, showing options like Group..., Ungroup..., Uniquify, and New Logical Hierarchy View. The "Schematic" menu is also visible. The "Logical Hierarchy" view is active, showing a list of cells in a hierarchical structure. The "Cells (Hierarchical)" table is displayed, listing cell names, reference names, and cell paths. The "Symbol.4 CS" window shows a schematic diagram of a component labeled "CS". The schematic has inputs for "reset", "clk", and "X[7:0]", and an output for "Y[9:0]". A red circle highlights the "CS" symbol, with a red arrow pointing to it and the text "Click twice". The "Schematic.3 CS" window shows a detailed schematic of the component, with a red arrow pointing from the "CS" symbol in the "Symbol.4 CS" window to it.

Cell Name	Ref Name	Cell Path	Di
sub_18	CS_DW01_s...	sub_18	u...
sub_17	CS_DW01_s...	sub_17	u...
sub_16	CS_DW01_s...	sub_16	u...
sub_15	CS_DW01_s...	sub_15	u...
sub_14	CS_DW01_s...	sub_14	u...
sub_13	CS_DW01_s...	sub_13	u...
sub_12	CS_DW01_s...	sub_12	u...
sub_11	CS_DW01_s...	sub_11	u...
sub_10	CS_DW01_s...	sub_10	u...
add_23	CS_DW01_a...	add_23	u...
add_0_ro...	CS_DW01_a...	add_0_root...	u...

Select CS and save again



Report Area & Timing

Timing Test Power Report 1 - Timing

New Path Analyz New Path Inspec Timing Analysis Path Slack... Slack Histogram Slack Histogram Endpoint Slack... Net Capacitance Capacitance of Path Profile View Check Timing... Report Timing Parameters Report Timing Re Report Clock Sk Report Clock Tre Report Path Grou Report Wire Load

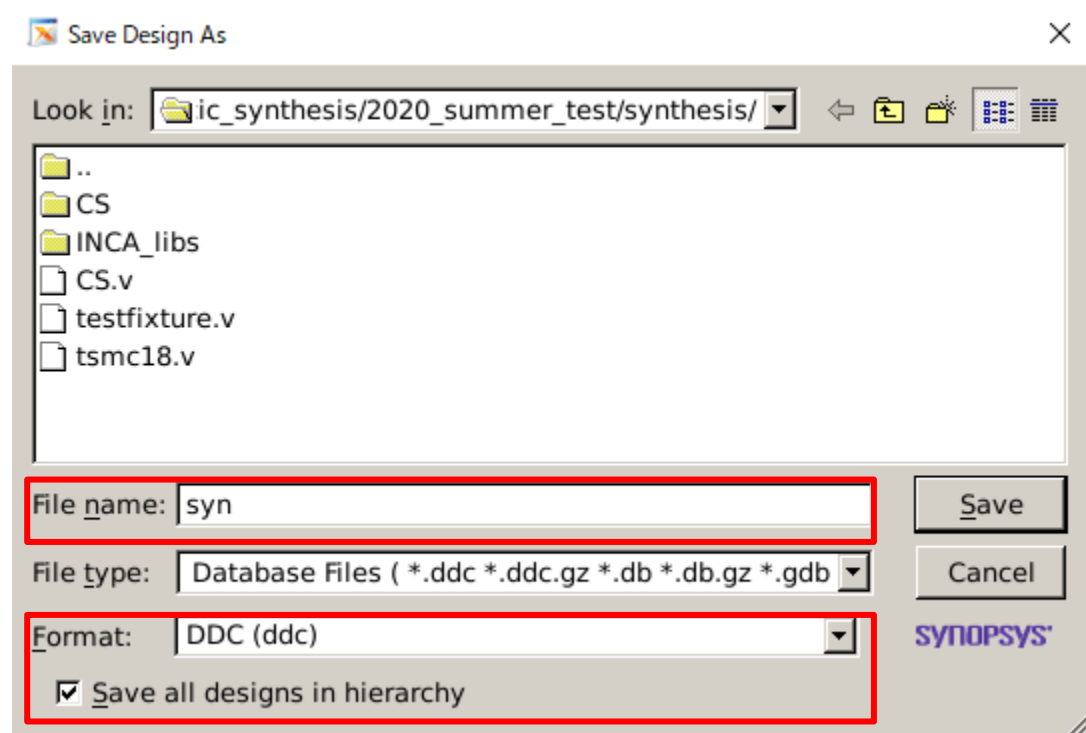
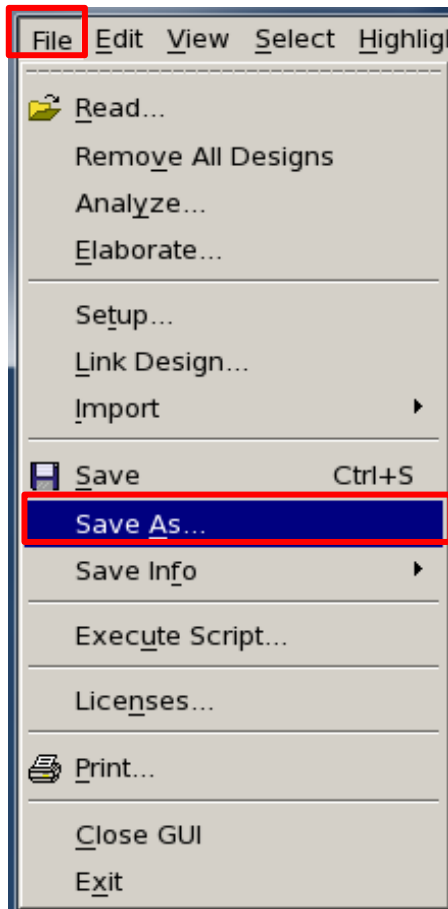
add_23/U126/Y (OAI21X4)	0.1450	18.4203 f
add_23/U108/Y (AOI21X1)	0.3071	18.7275 r
add_23/U131/Y (OAI21X2)	0.1483	18.8757 f
add_23/U152/Y (XOR2X1)	0.3190	19.1947 r
add_23/SUM[11] (CS_DW01_add_14)	0.0000	19.1947 r
Y[8] (out)	0.0000	19.1947 r
data arrival time		19.1947
clock clk (rise edge)	20.0000	20.0000
clock network delay (ideal)	1.0000	21.0000
clock uncertainty	-0.8000	20.2000
output external delay	-1.0000	19.2000
data required time		19.2000
data required time		19.2000
data arrival time		-19.1947
slack (MET)		0.0053

***** End Of Report *****

Reports Area (μm^2) : Total Area
 Gate Count Gate Count: Total cell area / 10



Save Design as .DDC File



Write SDF File for Pre-Sim

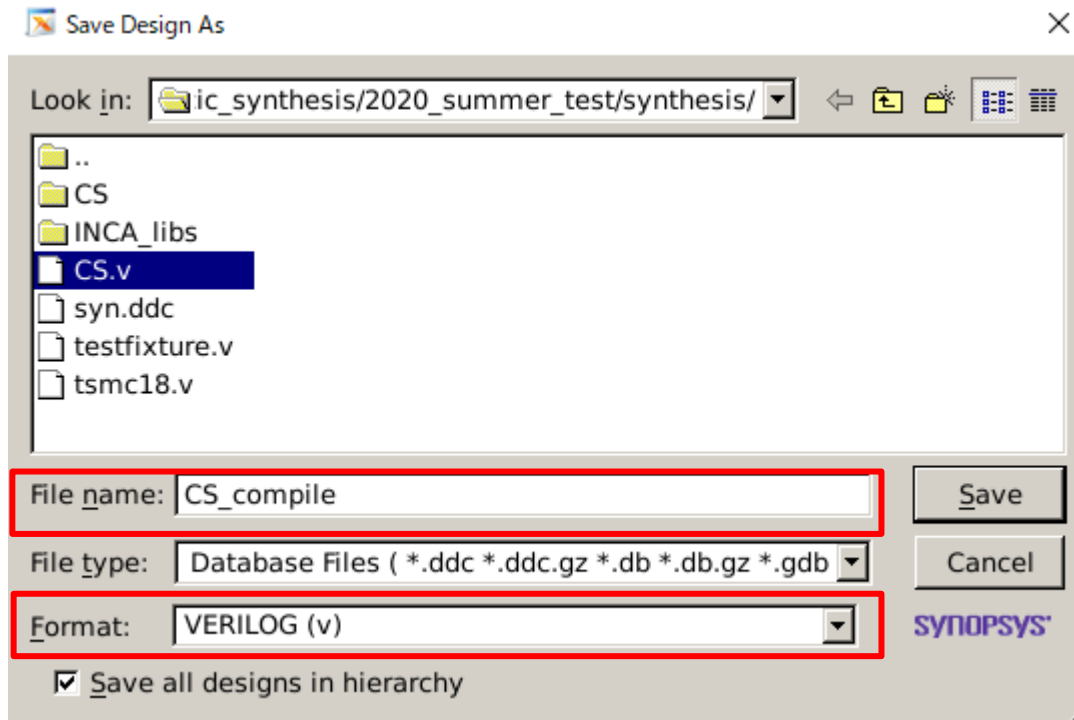
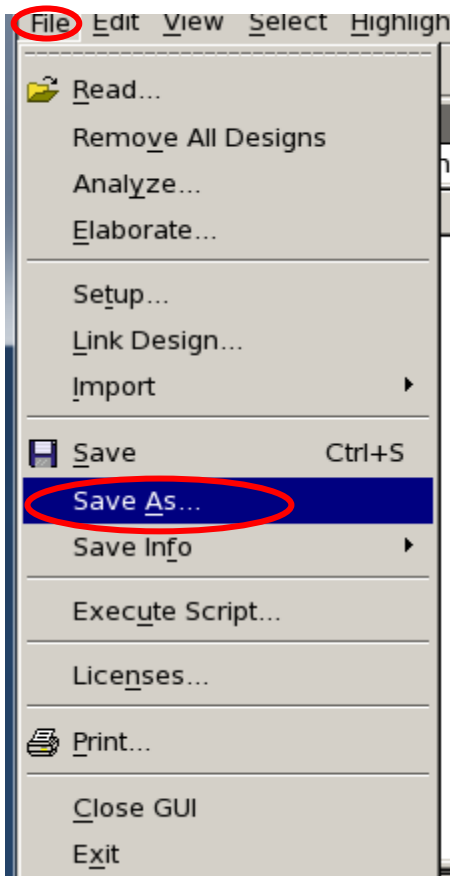
- The file includes information of delay of Gate-Level circuit.

Command:

```
-> write_sdf -version 1.0 -context verilog chip_syn.sdf  
-> write_sdc -version 1.7 CHIP.sdc
```



Save Design as .V File : Netlist



Pre-Layout Simulation

- 以剛剛產生出的Netlist檔進行 Gate-Level Simulation也常稱作Pre-Sim用以驗證確認我們合成出來的邏輯電路是否符合System Spec.所要求的功能。

```
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
Timing checks:          4050      224
Interconnect:           3029      -
Delayed tcheck signals:  600      20
Simulation timescale:    1ps
Writing initial simulation snapshot: worklib.test.v
Loading snapshot worklib.test.v ..... Done
*Verdi3* Loading libsscore_ius122.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
-----
All data have been generated successfully!
-----PASS-----
Simulation complete via $finish(1) at time 1055 NS + 0
./testfixture.v:114      $finish;
ncsim> exit
```

Command (Terminal , not Design Compiler):
ncverilog testfixture.v CS_compile.v -v tsmc18.v +access+r



Thank
you!

LAB2 PROCEDURE

- Environment setup
- Environment setup check
- Analysis the design, Elaborate the design
- Constraints(Reference command)
- Compile design
- Reports and Save file
- Gate-Level simulation

Environment Setup (for control.v)

Create a New Folder for Synthesis

Ex:

1. `mkdir Synthesis` (terminal command)
2. `cd Synthesis` (terminal command)

Copy File for Environment Setting

△ 代表空格

```
cp△  
/home/standard/Environment_Setup_File/synthesis_setup_for_18/synopsys_dc.s  
etup△.synopsys_dc.setup
```

Copy File for Synthesis

```
cp△/home/standard/vlsi_2022/synthesis/*△
```



除了以上cp指令，Lab1寫完的control相關檔案也要複製到Synthesis的資料夾中

Reference command_1

- Command:

```
create_clock -name clk -period 20 -waveform {0 10} [get_ports clk]
```

```
set_dont_touch_network [get_clocks clk]
```

```
set_fix_hold [get_clocks clk]
```

```
set_clock_uncertainty 0.8 [get_clocks clk]
```

```
set_clock_latency -source 0 [get_clocks clk]
```

```
set_clock_latency 1 [get_clocks clk]
```

```
set_input_transition 0.5 [all_inputs]
```

```
set_clock_transition 0.5 [all_clocks]
```

```
set_max_area 0
```

```
set_max_fanout 6 [all_inputs]
```

```
set_max_transition 0.3 [all_inputs]
```



Reference command_2

- Command:

```
set_driving_cell -library slow -lib_cell BUFX4 -pin {Y} [get_ports clk]
set_driving_cell -library slow -lib_cell DFFX1 -pin {Q} [remove_from_collection [all_inputs] [get_ports clk]]
set_load 0.001913 [all_outputs]

set_input_delay -clock clk -max 1 [remove_from_collection [all_inputs] [get_clocks clk]]
set_input_delay -clock clk -min 0.2 [remove_from_collection [all_inputs] [get_clocks clk]]

set_output_delay -clock clk -max 1 [all_outputs]
set_output_delay -clock clk -min 0.1 [all_outputs]

set_wire_load_model -name tsmc18_wl10 -library slow

check_design -multiple_designs
uniquify
```



Gate-Level simulation

```
Always blocks:      1      1
Initial blocks:     5      5
Pseudo assignments: 4      4
Timing checks:     112     19
Interconnect:       100     -
Delayed tcheck signals: 37     2
Simulation timescale: 1ps

Writing initial simulation snapshot: worklib.controller_test: v
Loading snapshot worklib.controller_test: v ..... Done
*Verdi* Loading libsscore_ius152.so
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi_Q-2020.03, Linux, 02/09/2020
(C) 1996 - 2020 by Synopsys, Inc.
*Verdi* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may
crash the programs that are using this file.
*Verdi* : Create FSDB file 'controller.fsdb'
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.

*** REACHED END OF TEST VECTORS ***

There were 0 errors detected!

Simulation complete via $finish(1) at time 1278 NS + 0
./control_test.v:73      $finish; // This prevents simulation beyond end of test
patterns
ncsim> exit
```

Command (Terminal , not Design Compiler):

ncverilog control_test_syn.v control_syn.v -v tsmc18.v +access+r +define+SDF

合成完的NETLIST檔

