

# Auto Placement & Routing with Innovus

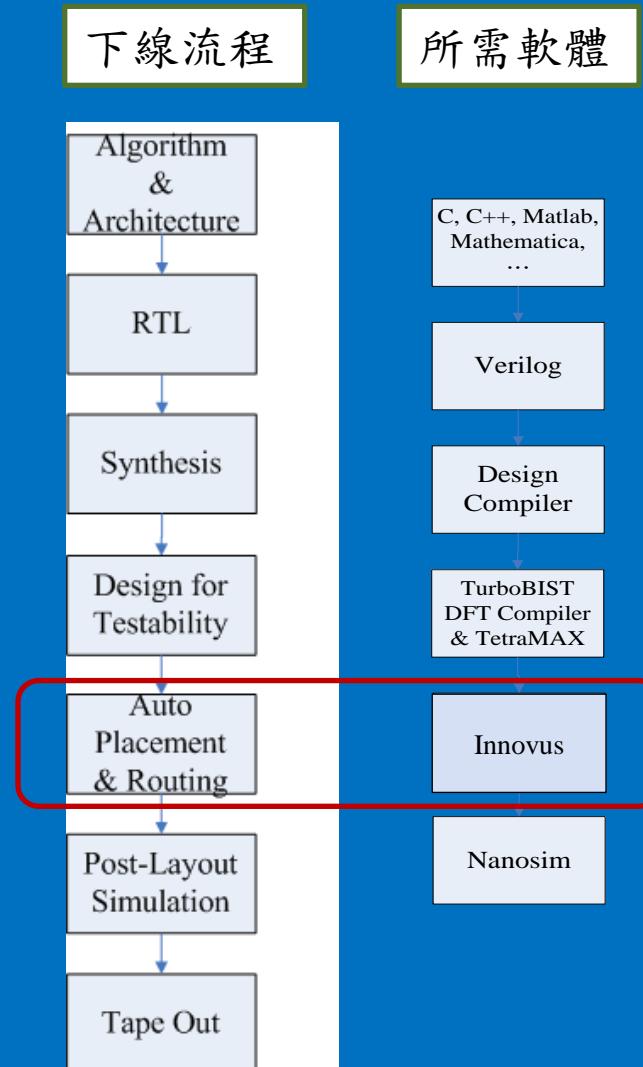
**Advisor : Yu-Cheng Fan**  
**Presenter : Ping-Chun Chen**



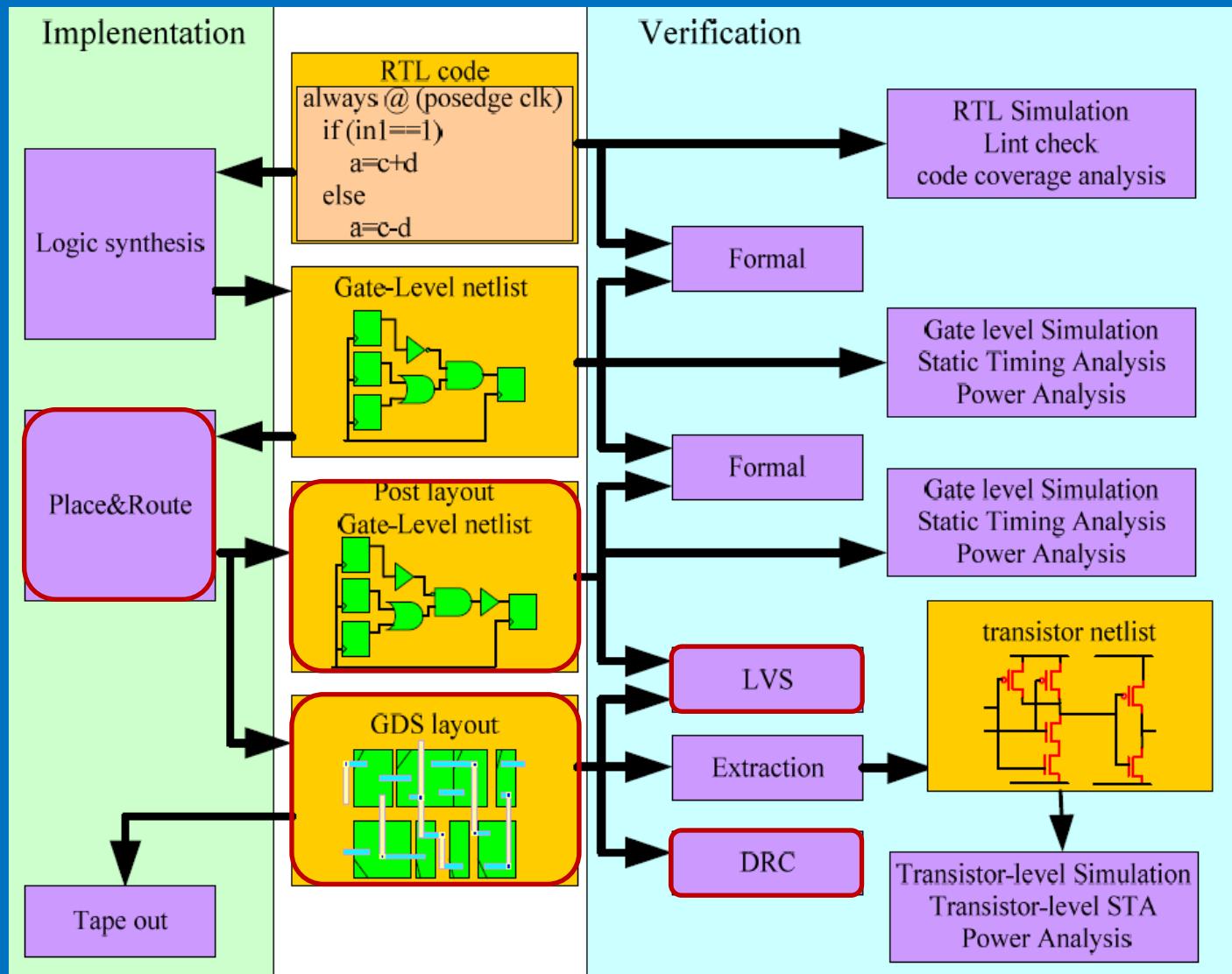


# Introduction

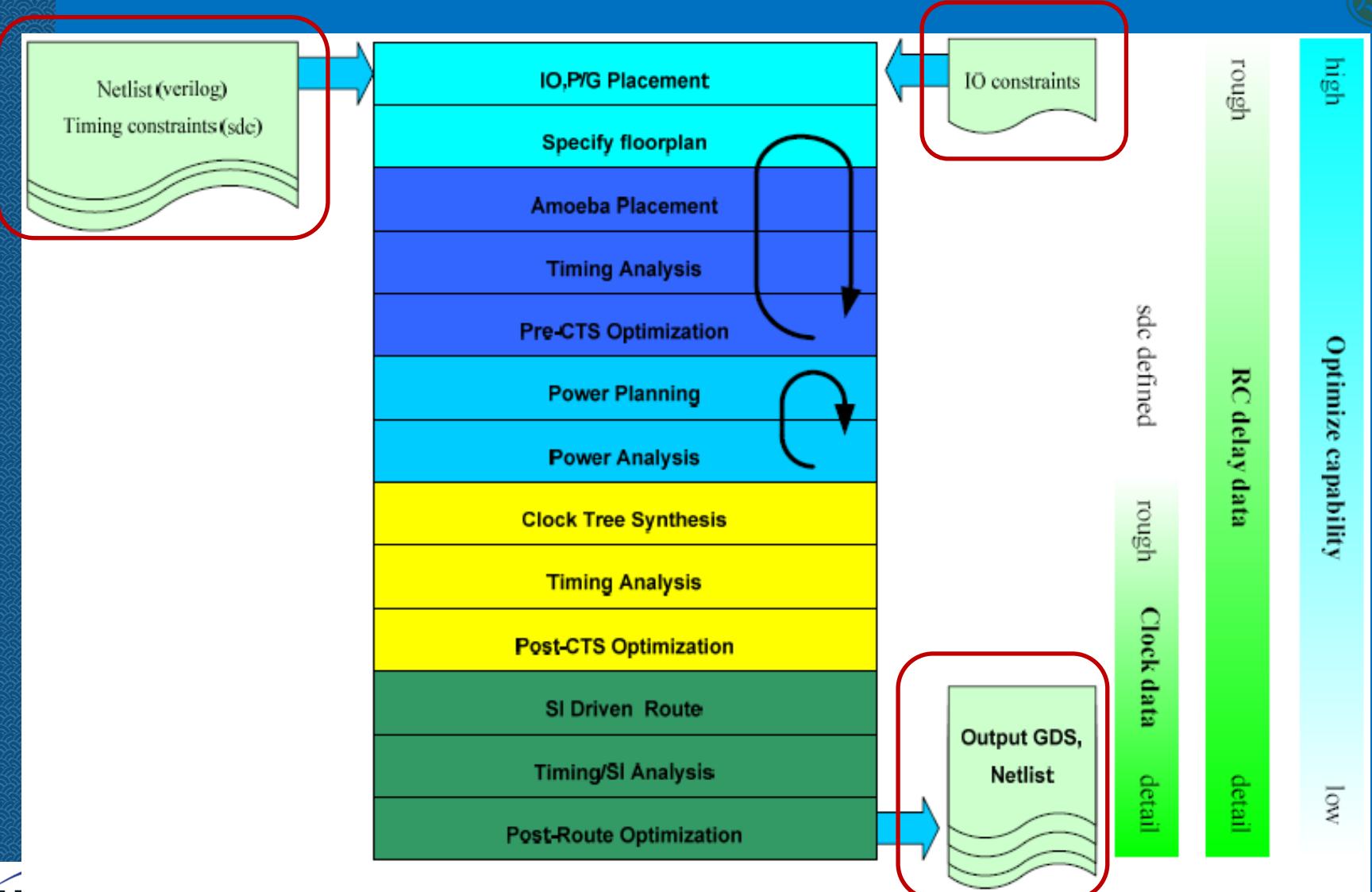
## ◆ Cell-Based Physical Design—INNOVUS



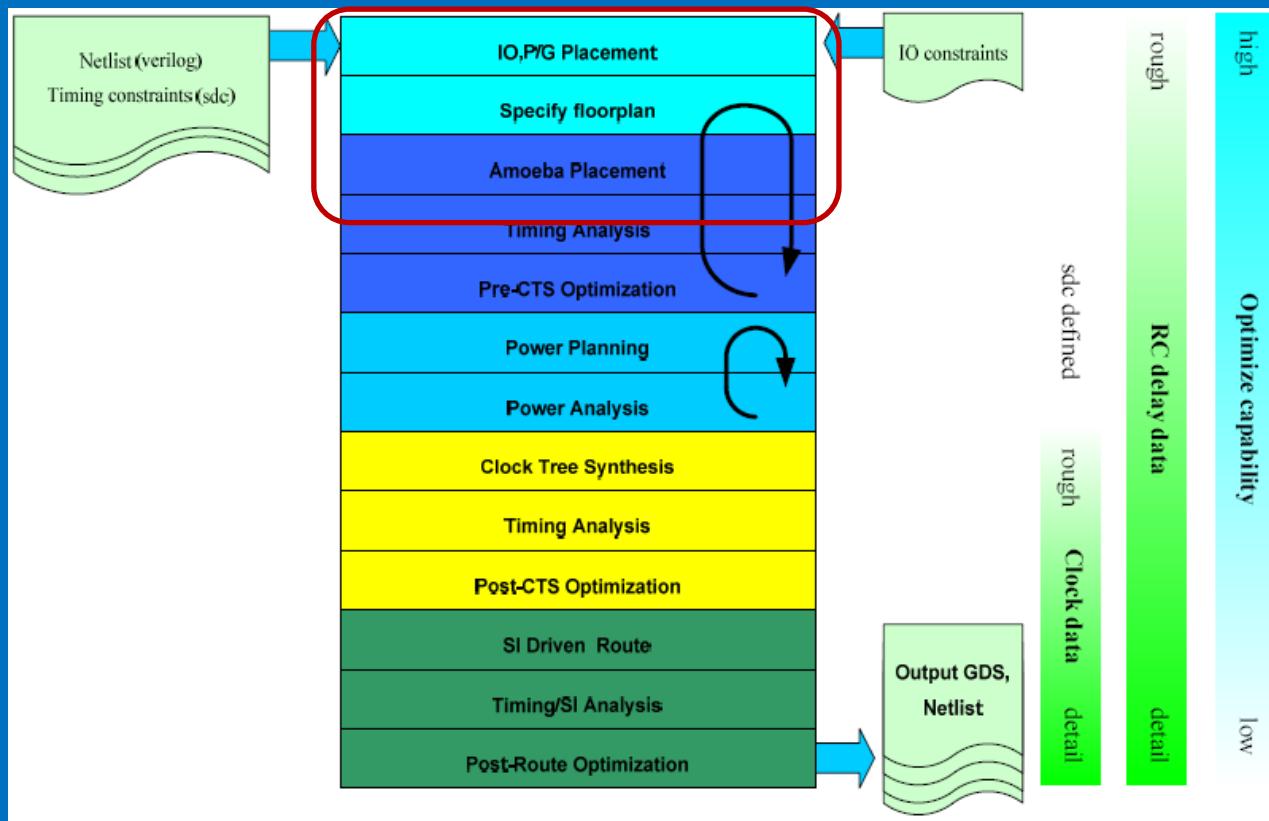
# Cell-Based Design Flow



# Innovus P&R flow -- Import



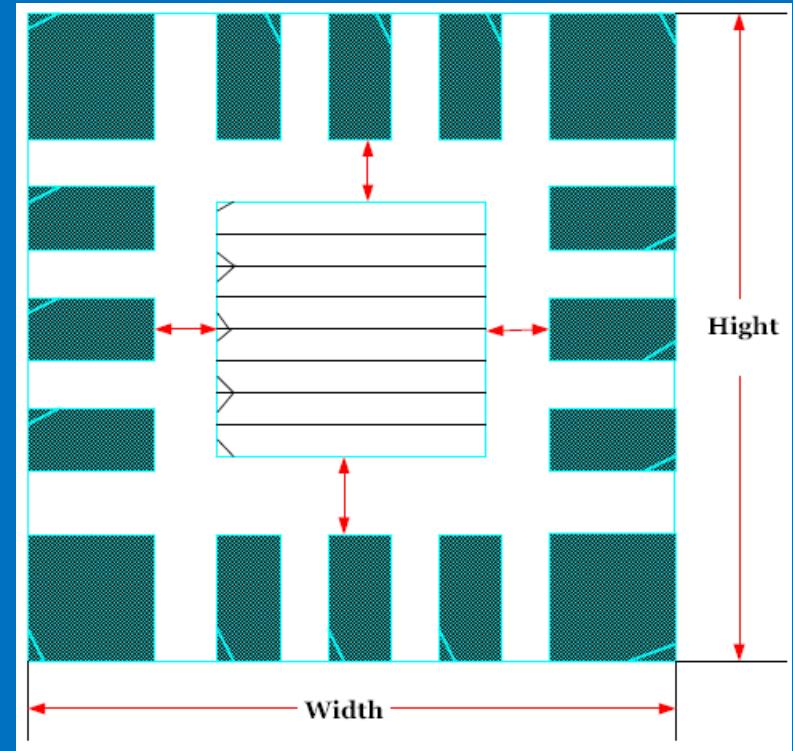
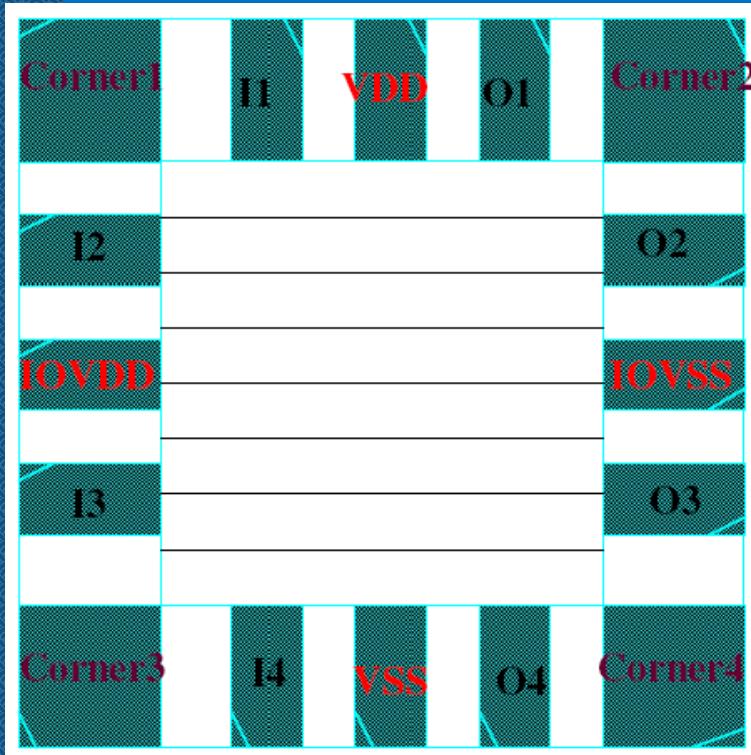
# FloorPlan & Placement



# IO, P/G Placement & specify Floorplan



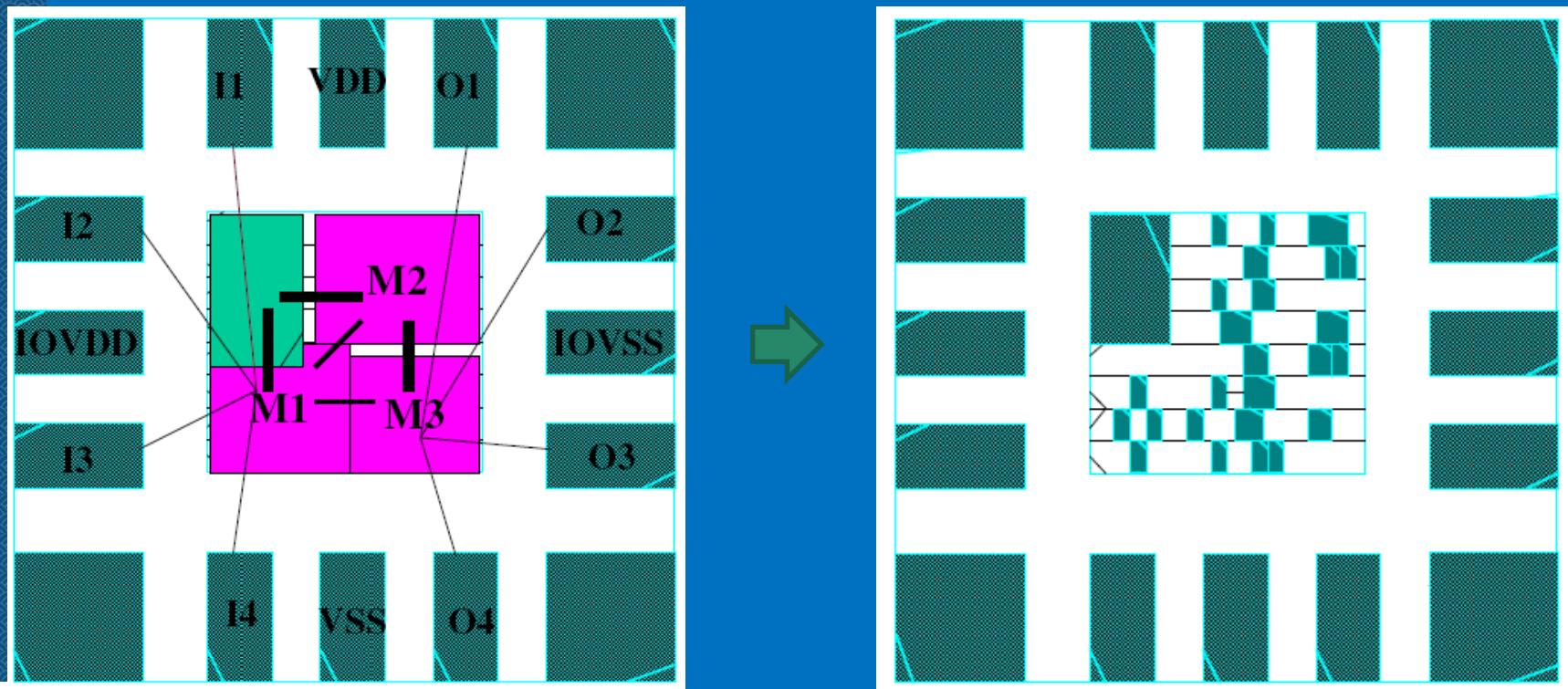
- ◆ 利用 IO Constraints 來實現晶片 IO 位置的擺放
- ◆ 決定晶片 core 與 Power ring 的大小



# Floorplan & Placement



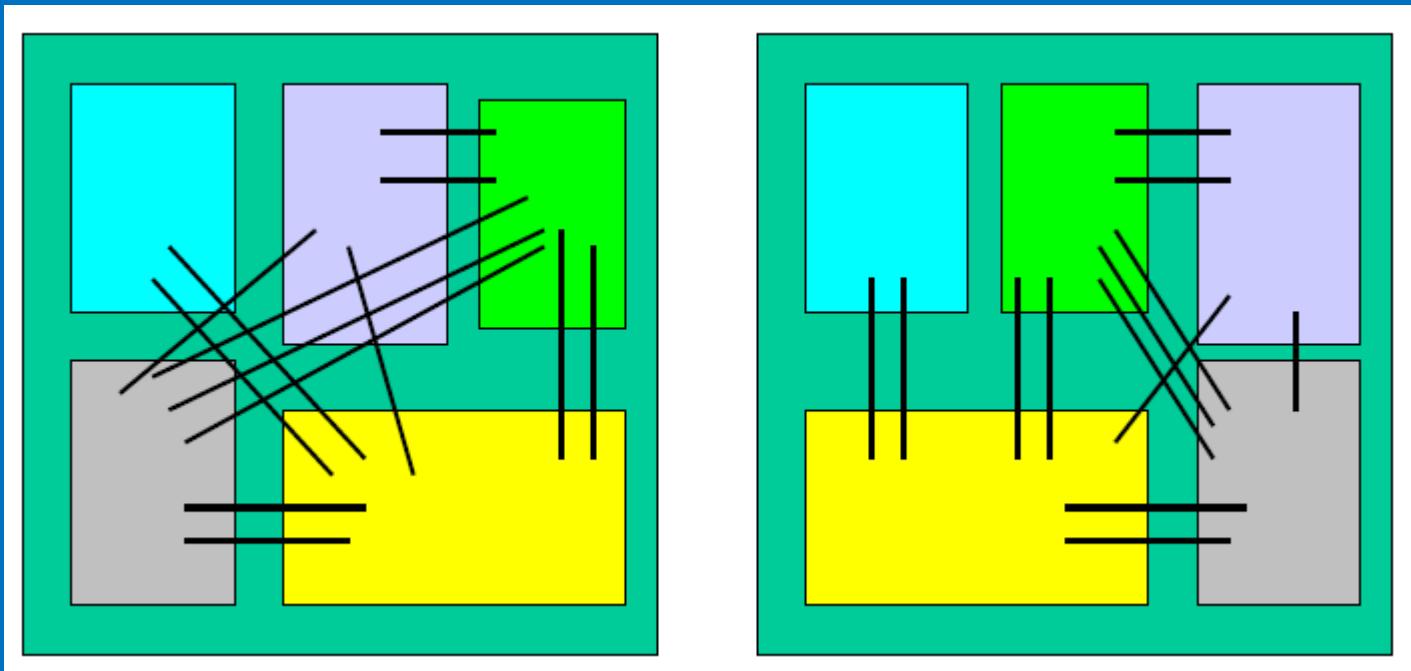
- ◆ User由設計的概念決定module, hard IP, Soft IP, Ram等元件如何擺放才可以符合晶片所需
- ◆ 依照Floorplan的結果將cell擺進core裡面



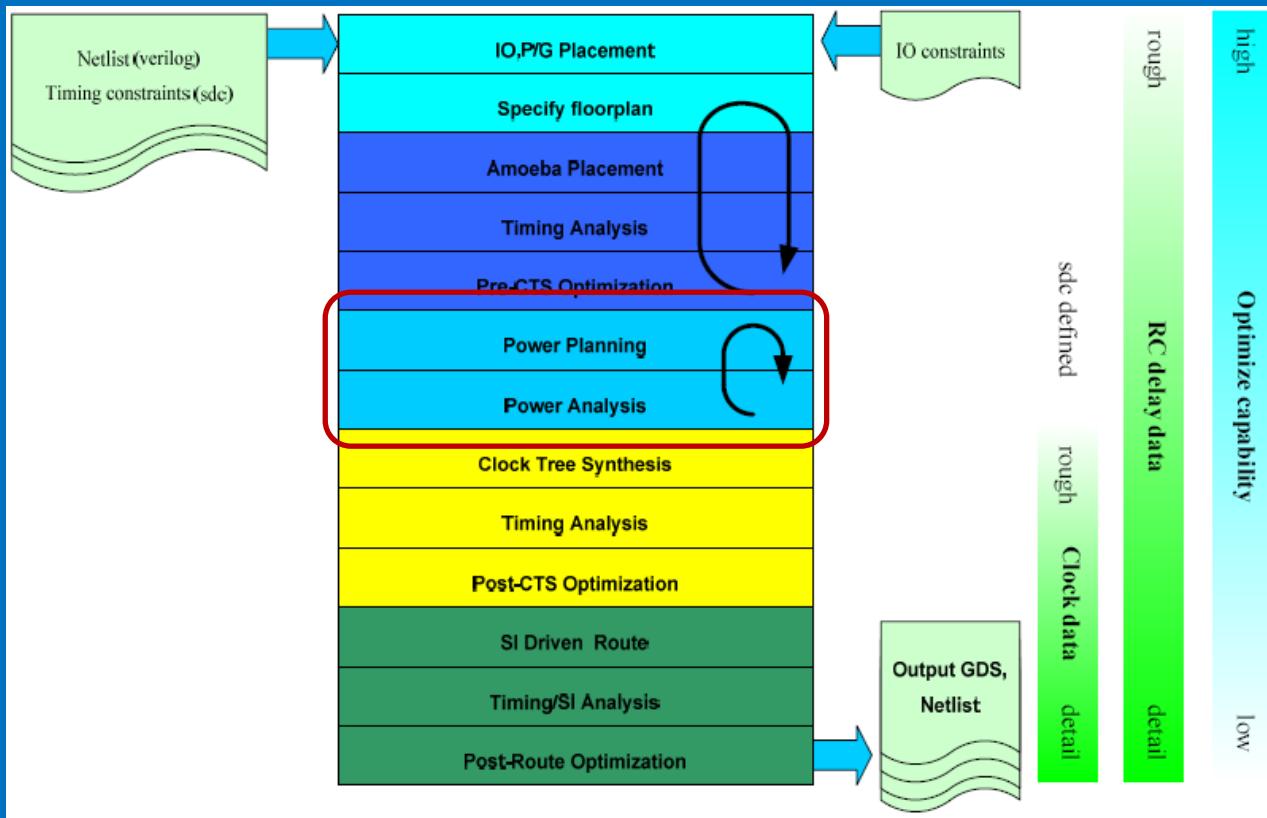
# Floorplan & Placement



- ◆ Develop early physical layout to ensure design objective can be archived
  - Minimum area for low cost
  - Minimum congestion for design routable
  - Estimate parasitic for delay calculation
  - Analysis power for reliability



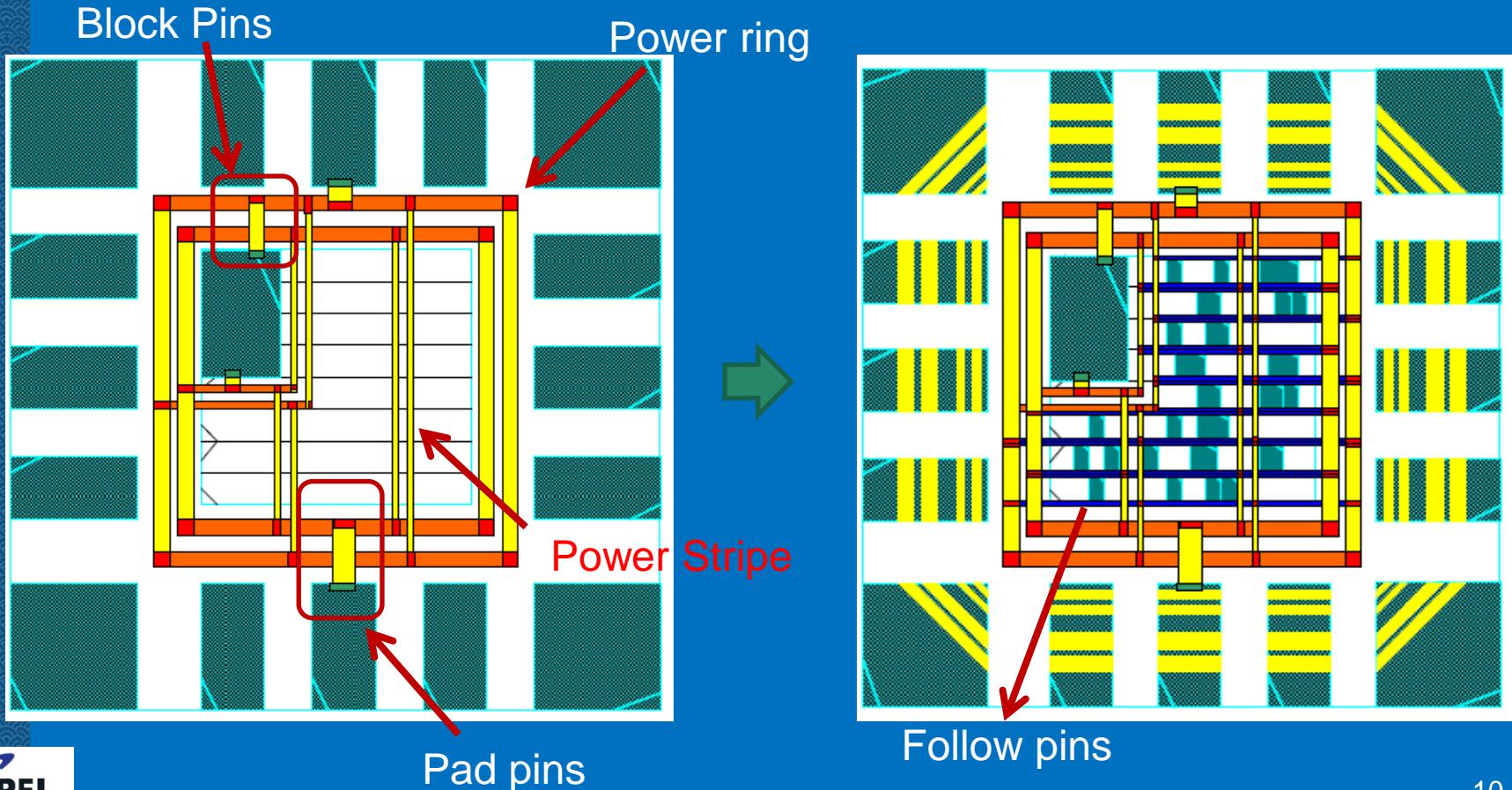
# Power Planning



# Power Planning & Power Route



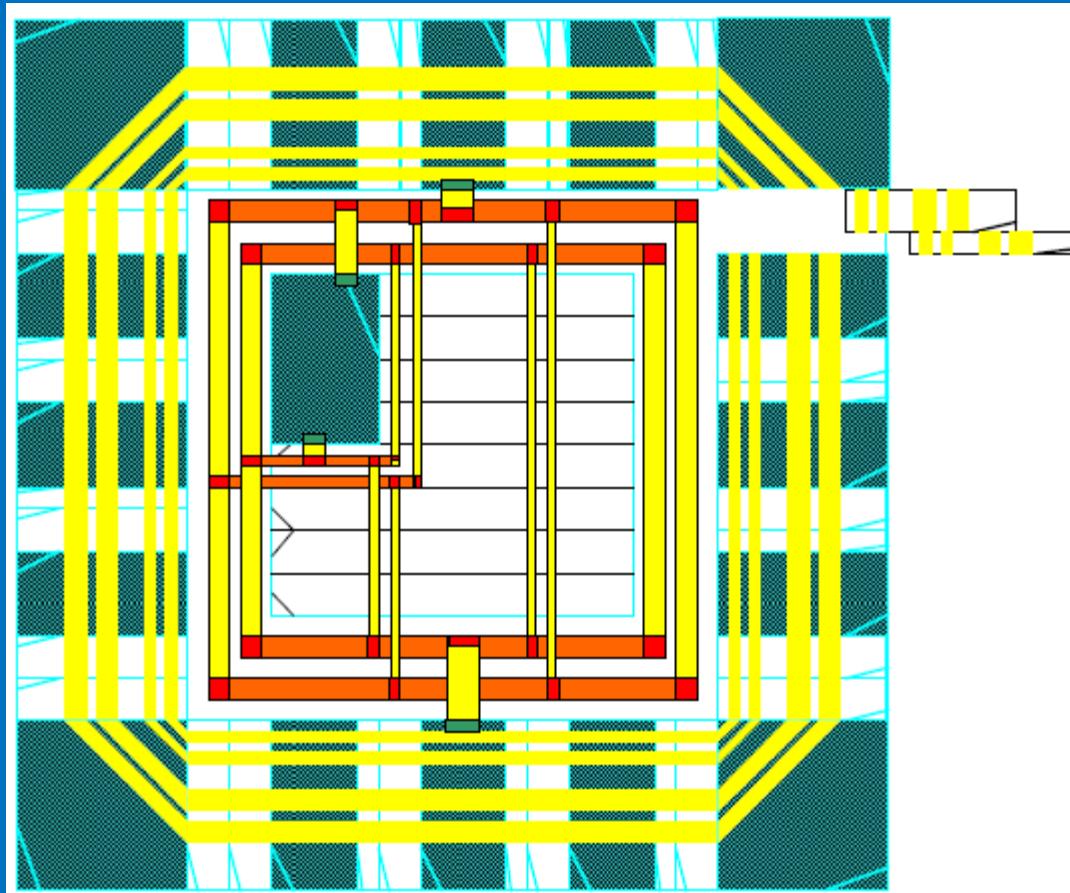
- ◆ 架設Power ring, Pad pins, Power Stripe, Block Pins, Follow Pins



# Power Planning – Add IO Filler



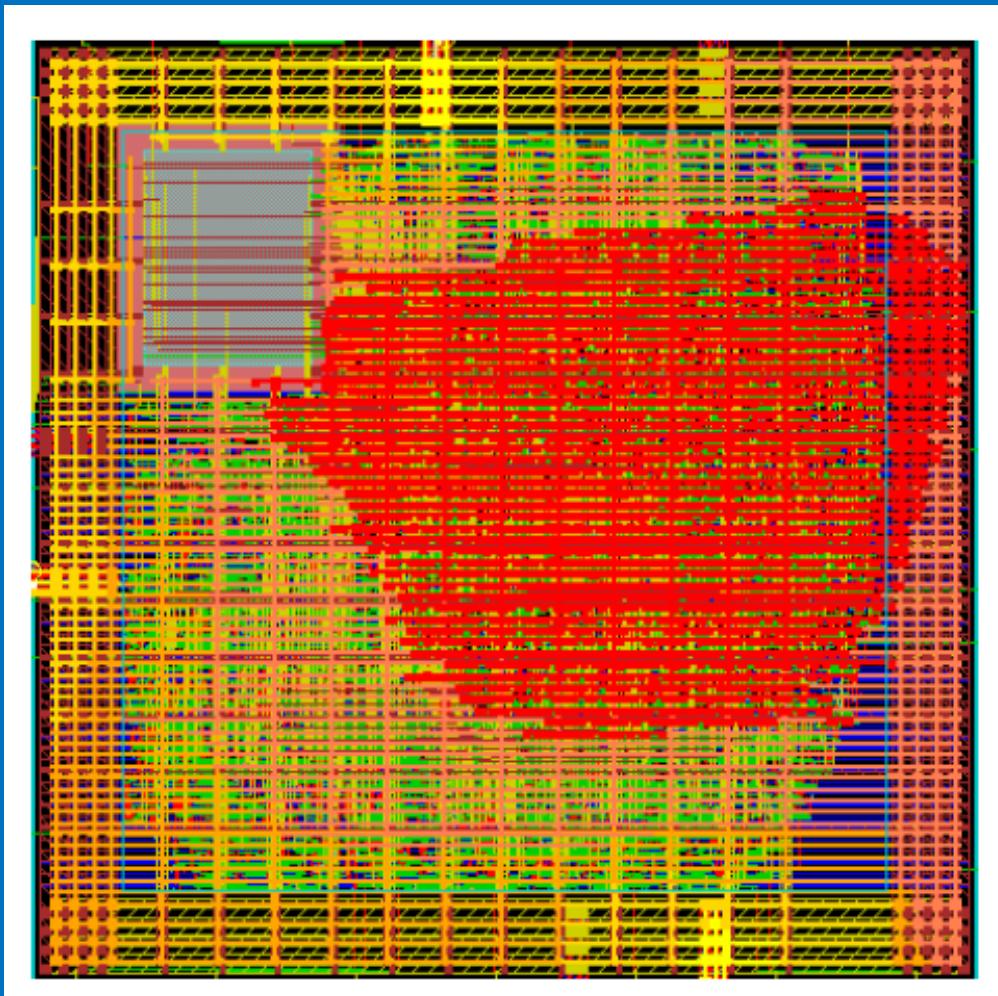
- ◆ 加入IO Filler將Pad連接起來
- ◆ IO Filler無任何Logic Function，僅為了連接IO PAD的電源



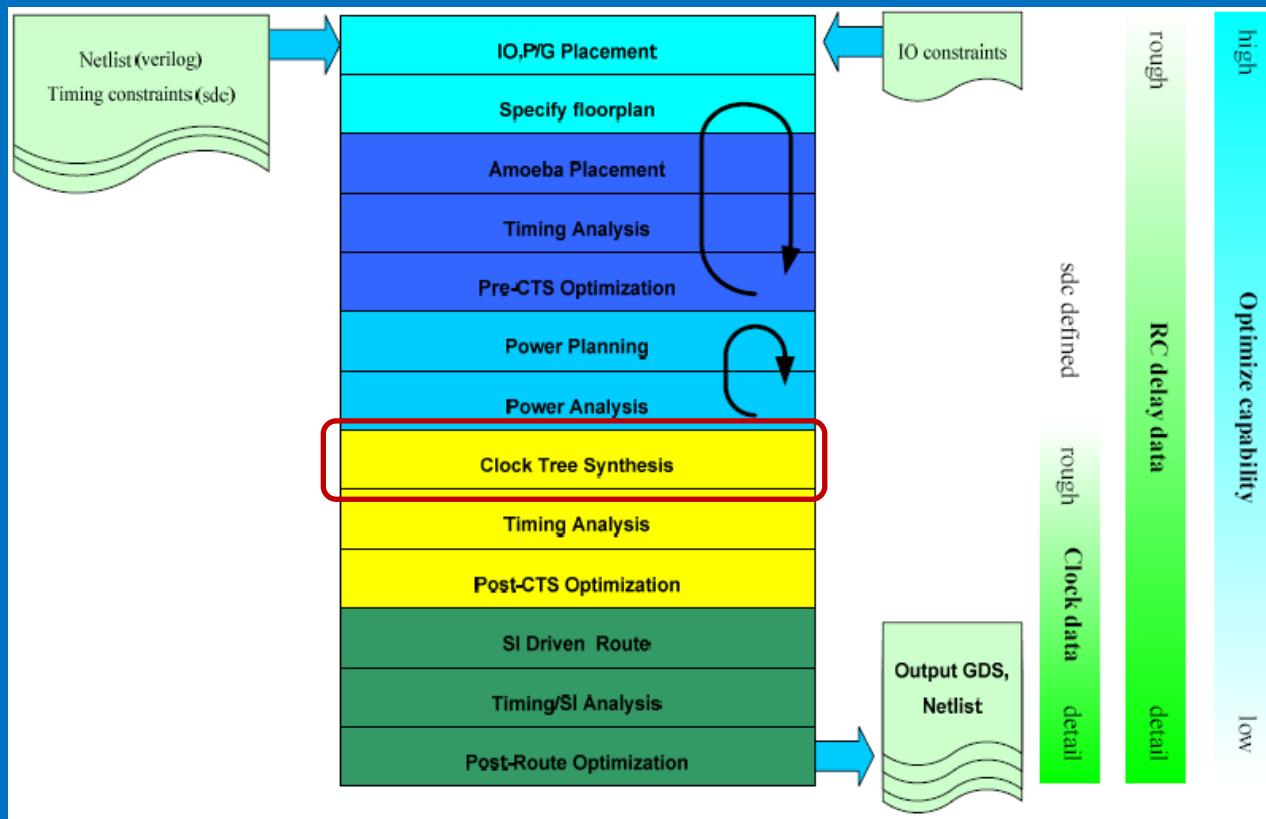


# Power Analysis

- ◆ 分析晶片內部的Power



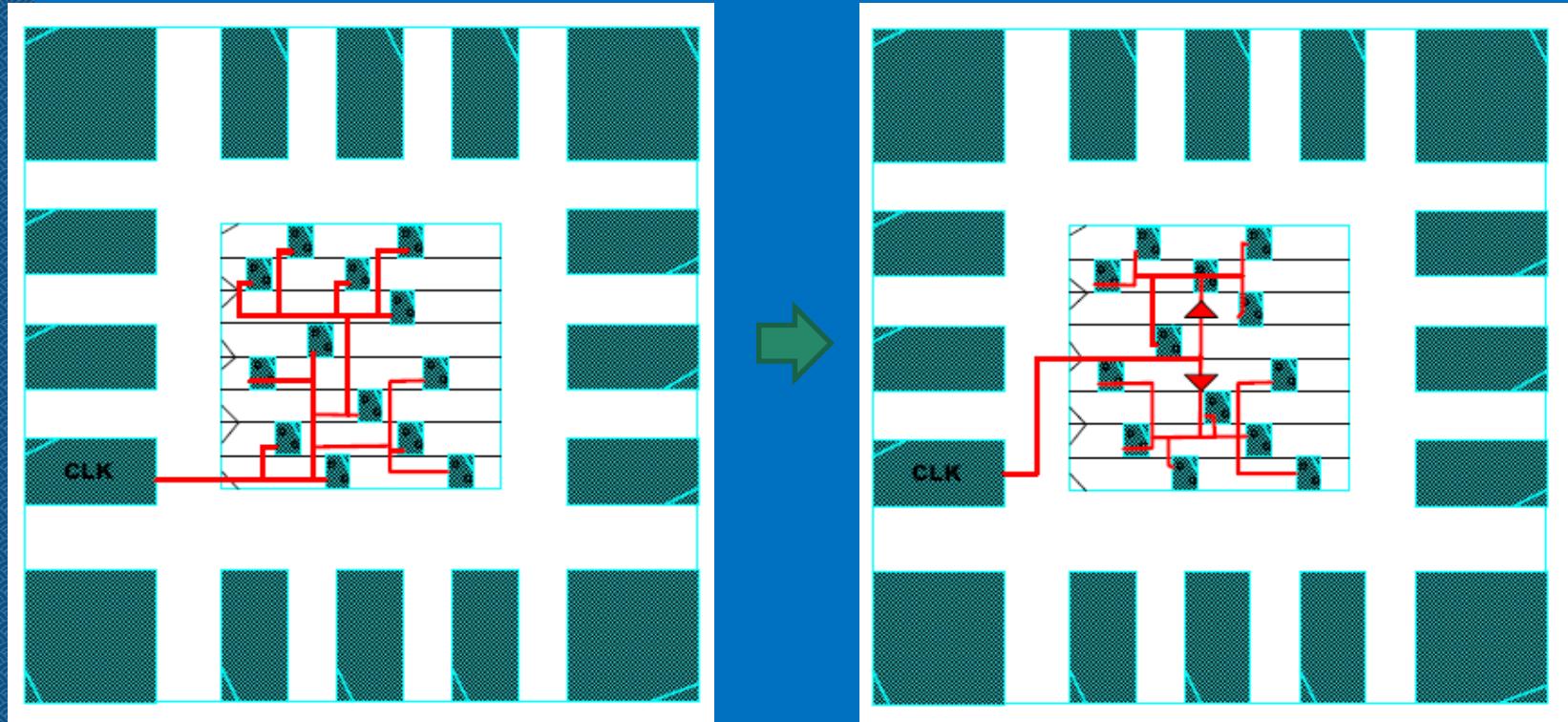
# Clock Tree Synthesis



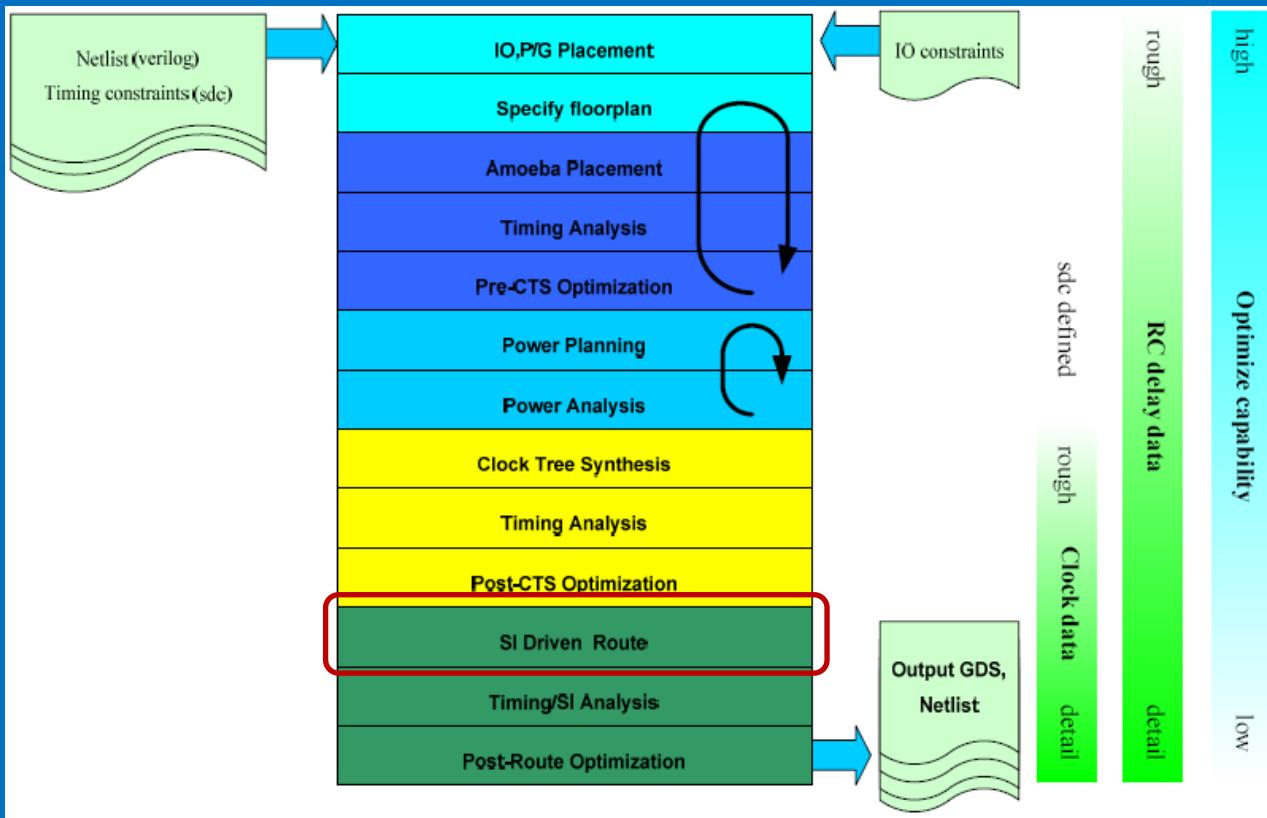
# Clock Tree Synthesis



- ◆ 由於Clock訊號必須推動大量的Flip-Flop，所以為了解決負載過重的問題，做CTS的時候會加入Buffer來解決loading的問題



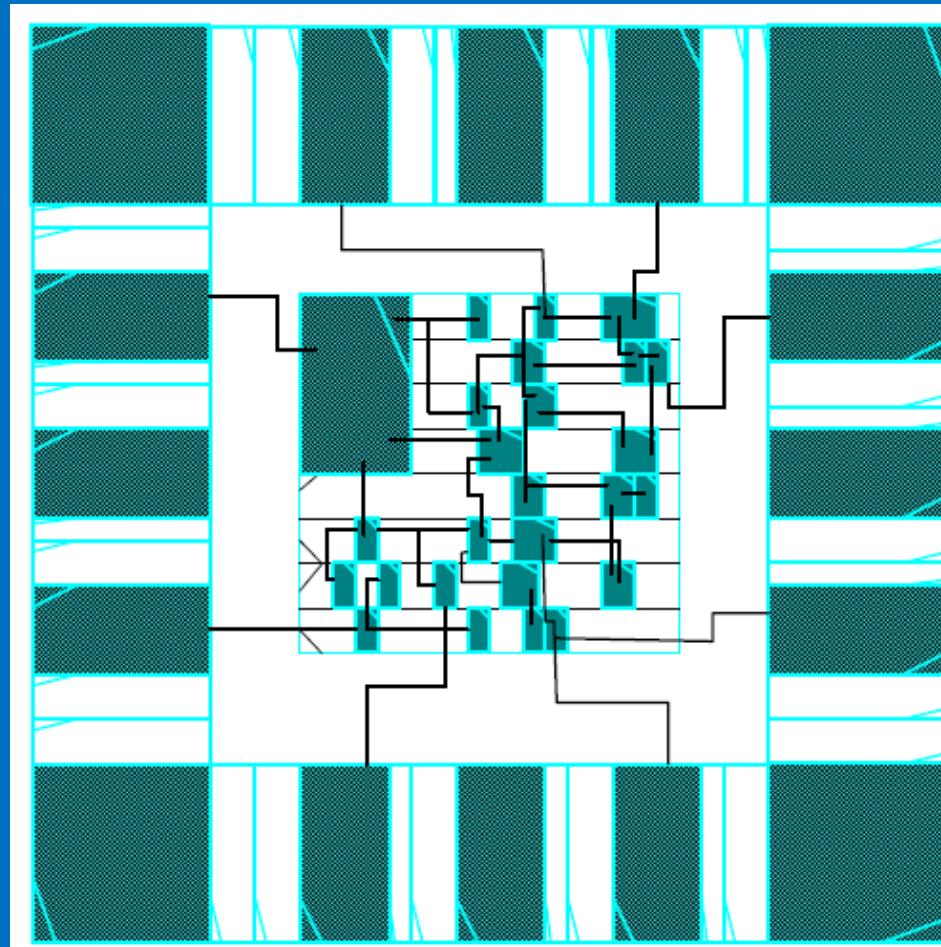
# Routing



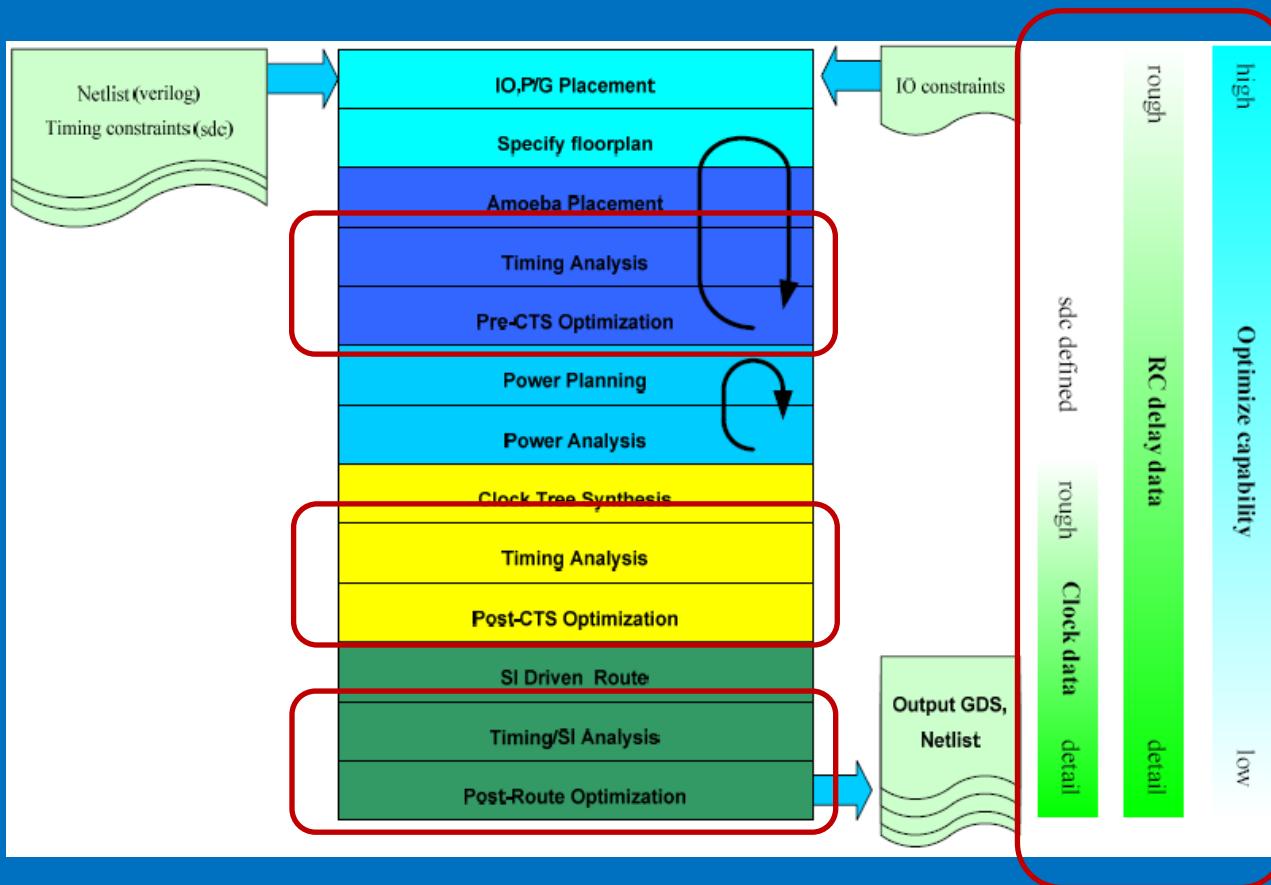
# Routing



- ◆ 根據timing的需求，將晶片內部的cell去做繞線



# Timing Analysis and Optimization

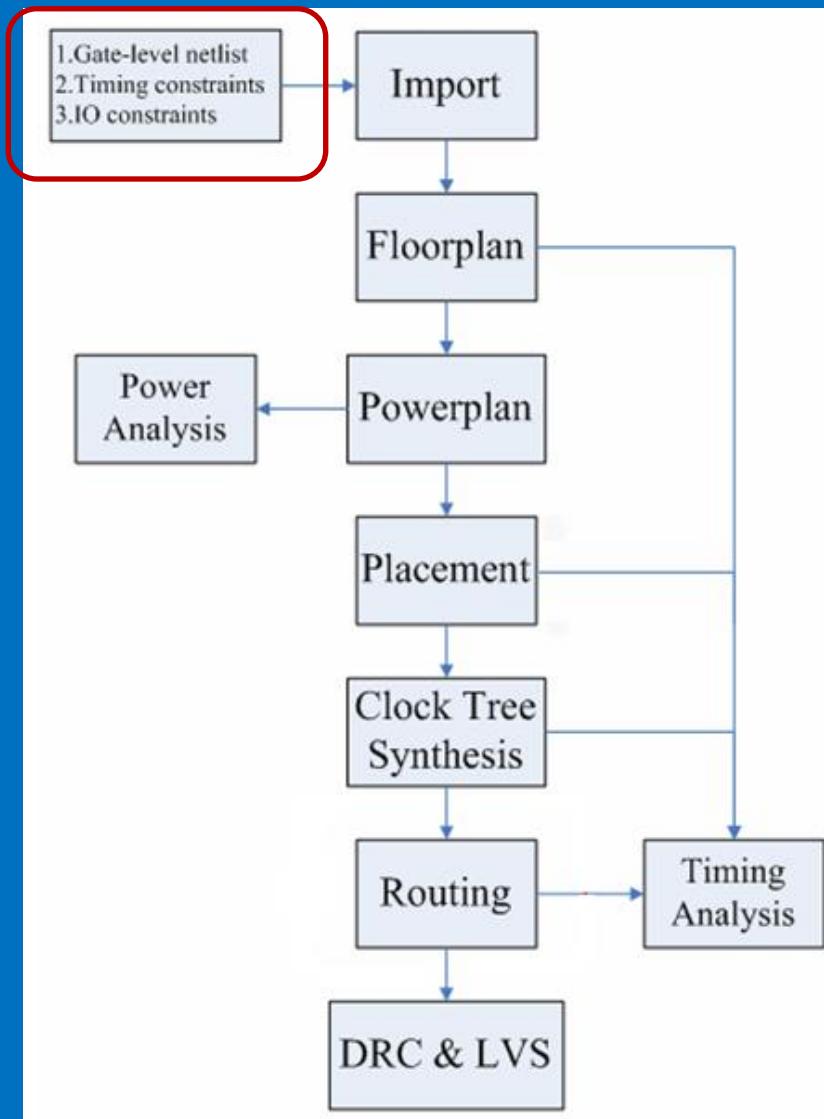




# Cell-Based IC Physical Design and Verification with Innovus



# Prepare Data



# Prepare Data



- ◆ Library
  - Physical Library (LEF)—描述cell的格式與連線方式
  - Timing Library (LIB)—描述cell的timing狀況
- ◆ User Data
  - Gate-Level netlist (verilog)
    - ❖ 做完DFT後的CHIP\_SCAN.vg改成CHIP\_SCAN.v，加一個CHIP的module將cell包起來，並且修改腳位資訊，來提供原本Gate-Level netlist所沒有的IO PAD資訊
  - SDC constraints
    - ❖ \*\*\*\*\*.sdc
  - IO constraint
    - ❖ \*\*\*\*\*.io



# Gate-Level netlist

- 做完DFT後的CHIP\_SCAN.vg改成CHIP\_SCAN.v，加一個CHIP的module將cell包起來，並且修改腳位資訊，來提供原本Gate-Level netlist所沒有的IO PAD資訊。
- 範例：(用vi編輯器打開CHIP\_scan.v可以在最後的地方看到加進的CHIP module)

```
module CHIP(alu_out, opcode, data1, data2, clk, reset, SCAN_IN,SCAN_OUT,SCAN_EN);  
  
    input [2:0] opcode;  
    input [7:0] data1;  
    input [7:0] data2;  
    input clk, reset;  
    output [7:0] alu_out;  
    input SCAN_IN,SCAN_EN;  
    output SCAN_OUT;  
  
    wire [2:0] i_opcode;  
    wire [7:0] i_data1;  
    wire [7:0] i_data2;  
    wire i_clk,i_reset;  
    wire [7:0] i_alu_out;  
    wire i_SCAN_IN,i_SCAN_EN;  
    wire i_SCAN_OUT;  
  
    alu alu(.alu_out(i_alu_out),.opcode(i_opcode), .data1(i_data1),.data2(i_data2),.clk(i_clk),.reset(i_reset),  
    .SCAN_IN(i_SCAN_IN),SCAN_OUT(i_SCAN_OUT),.SCAN_EN(i_SCAN_EN));
```

宣告的順序要與之前的一樣

可自己命名

名稱要與之前的module名稱一樣

# Gate-Level Netlist



```
PDIDGZ ipad_clk (.PAD(clk), .C(i_clk));  
PDIDGZ ipad_reset (.PAD(reset), .C(i_reset));  
PDIDGZ ipad_opcode0 (.PAD(opcode[0]), .C(i_opcode[0]));  
PDIDGZ ipad_opcode1 (.PAD(opcode[1]), .C(i_opcode[1]));  
PDIDGZ ipad_opcode2 (.PAD(opcode[2]), .C(i_opcode[2]));  
PDIDGZ ipad_data10 (.PAD(data1[0]), .C(i_data1[0]));  
PDIDGZ ipad_data11 (.PAD(data1[1]), .C(i_data1[1]));  
PDIDGZ ipad_data12 (.PAD(data1[2]), .C(i_data1[2]));  
PDIDGZ ipad_data13 (.PAD(data1[3]), .C(i_data1[3]));  
PDIDGZ ipad_data14 (.PAD(data1[4]), .C(i_data1[4]));  
PDIDGZ ipad_data15 (.PAD(data1[5]), .C(i_data1[5]));  
PDIDGZ ipad_data16 (.PAD(data1[6]), .C(i_data1[6]));  
PDIDGZ ipad_data17 (.PAD(data1[7]), .C(i_data1[7]));  
PDIDGZ ipad_data20 (.PAD(data2[0]), .C(i_data2[0]));  
PDIDGZ ipad_data21 (.PAD(data2[1]), .C(i_data2[1]));  
PDIDGZ ipad_data22 (.PAD(data2[2]), .C(i_data2[2]));  
PDIDGZ ipad_data23 (.PAD(data2[3]), .C(i_data2[3]));  
PDIDGZ ipad_data24 (.PAD(data2[4]), .C(i_data2[4]));  
PDIDGZ ipad_data25 (.PAD(data2[5]), .C(i_data2[5]));  
PDIDGZ ipad_data26 (.PAD(data2[6]), .C(i_data2[6]));  
PDIDGZ ipad_data27 (.PAD(data2[7]), .C(i_data2[7]));  
PDIDGZ ipad_SCAN_IN (.PAD(SCAN_IN), .C(i_SCAN_IN));  
PDIDGZ ipad_SCAN_EN (.PAD(SCAN_EN), .C(i_SCAN_EN));
```

```
PDO12CDG opad_SCAN_OUT (.I(i_SCAN_OUT), .PAD(SCAN_OUT));  
PDO12CDG opad_alu_out0 (.I(i_alu_out[0]), .PAD(alu_out[0]));  
PDO12CDG opad_alu_out1 (.I(i_alu_out[1]), .PAD(alu_out[1]));  
PDO12CDG opad_alu_out2 (.I(i_alu_out[2]), .PAD(alu_out[2]));  
PDO12CDG opad_alu_out3 (.I(i_alu_out[3]), .PAD(alu_out[3]));  
PDO12CDG opad_alu_out4 (.I(i_alu_out[4]), .PAD(alu_out[4]));  
PDO12CDG opad_alu_out5 (.I(i_alu_out[5]), .PAD(alu_out[5]));  
PDO12CDG opad_alu_out6 (.I(i_alu_out[6]), .PAD(alu_out[6]));  
PDO12CDG opad_alu_out7 (.I(i_alu_out[7]), .PAD(alu_out[7]));  
endmodule
```

PDIDGZ	Input Pad, 5V-Tolerant
PDISDGZ	Schmitt Trigger Input Pad, 5V-Tolerant
PDOxCDG	CMOS Output Pad

# IO Constraints



- ◆ 0.18um TSMC 所使用的P/G Pad、I/O Pad 和 Corner 名稱：
  - Core Pad : PVDD1DGZ, PVSS1DGZ
  - I/O Pad : PVDD2DGZ, PVSS2DGZ
  - Corner : PCORNERDG

◆ 晶片包裝：

包裝型號	單價(NTD/每顆)	包裝型號	單價(NTD/每顆)
18 S/B	450	84 CLCC	830
24 S/B	460	100 CQFP	1,150
28 S/B	520	128 CQFP	1,500
32 S/B	550	144 CQFP	1,650
40 S/B	610	160 CQFP	1,800
48 S/B	820	208 CQFP	2,100
68 CLCC	710		

Version: 2

Pad: CORNER0 NW PCORNER

Pad: PAD\_CLK N

Pad: PAD\_HALT N

Pad: CORNER1 NE PCORNER

Pad: PAD\_X1 W

Pad: PAD\_X2 W

Pad: CORNER2 SW PCORNER

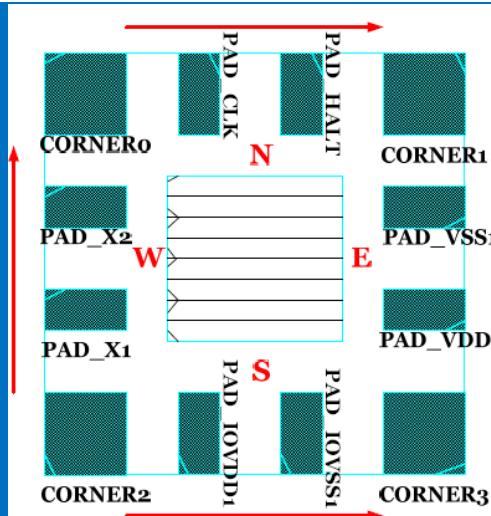
Pad: PAD\_IOVDD1 S PVDD2DGZ

Pad: PAD\_IOVSS1 S PVSS2DGZ

Pad: CORNER3 SE PCORNER

Pad: PAD\_VDD1 E PVDD1DGZ

Pad: PAD\_VSS1 E PVSS2DGZ



# IO Constraints



- ◆ 編輯IO Constraint (在Gate-level netlist 中沒有加入的cell instance，如P/G Pad、Corner Pad等，且必須在IO constraint 中加上相對應的cell name)。
- ◆ 由於CBDK\_TSMC018\_Arm\_v3.2 Design kit 使用新版的IO Pad library，本IO Pad library在每一個digital I/O domain必需擺放至少且只有一個PVDD2POC cell(Power on Control Power Pad)，IO方能正常運作。
- ◆ 範例：

Version: 1

Pad: CORNER0	NW PCORNER
Pad: ipad_data10	N
Pad: ipad_data11	N
Pad: ipad_data12	N
Pad: ipad_data13	N
Pad: ipad_CoreVDD1	N PVDD1DGZ
Pad: ipad_CLK	N
Pad: ipad_data14	N
Pad: ipad_data15	N
Pad: ipad_data16	N
Pad: ipad_data17	N

Pad: CORNER1	NE PCORNER
Pad: ipad_data20	W
Pad: ipad_data21	W
Pad: ipad_RESET	W
Pad: ipad_IOVDD1	W PVDD2DGZ
Pad: ipad_CoreVDD2	W PVDD1DGZ
Pad: ipad_data22	W
Pad: ipad_data23	W
Pad: ipad_data24	W
Pad: ipad_data25	W
Pad: ipad_data26	W

Pad: CORNER2	SW PCORNER
Pad: ipad_data27	S
Pad: ipad_opcode0	S
Pad: ipad_opcode1	S
Pad: ipad_opcode2	S
Pad: ipad_CoreVSS1	S PVSS1DGZ
Pad: opad_alu_out0	S
Pad: opad_alu_out1	S
Pad: opad_alu_out2	S
Pad: opad_alu_out3	S
Pad: opad_alu_out4	S

Pad: CORNER3	SE PCORNER
Pad: opad_alu_out5	E
Pad: opad_alu_out6	E
Pad: ipad_IOVSS1	E PVSS2DGZ
Pad: ipad_CoreVSS2	E PVSS1DGZ
Pad: opad_alu_out7	E
Pad: ipad_SCAN_IN	E
Pad: ipad_SCAN_EN	E
Pad: opad_SCAN_OUT	E
Pad: opad_carry_out	E
Pad: ipad_POC	E PVDD2POC

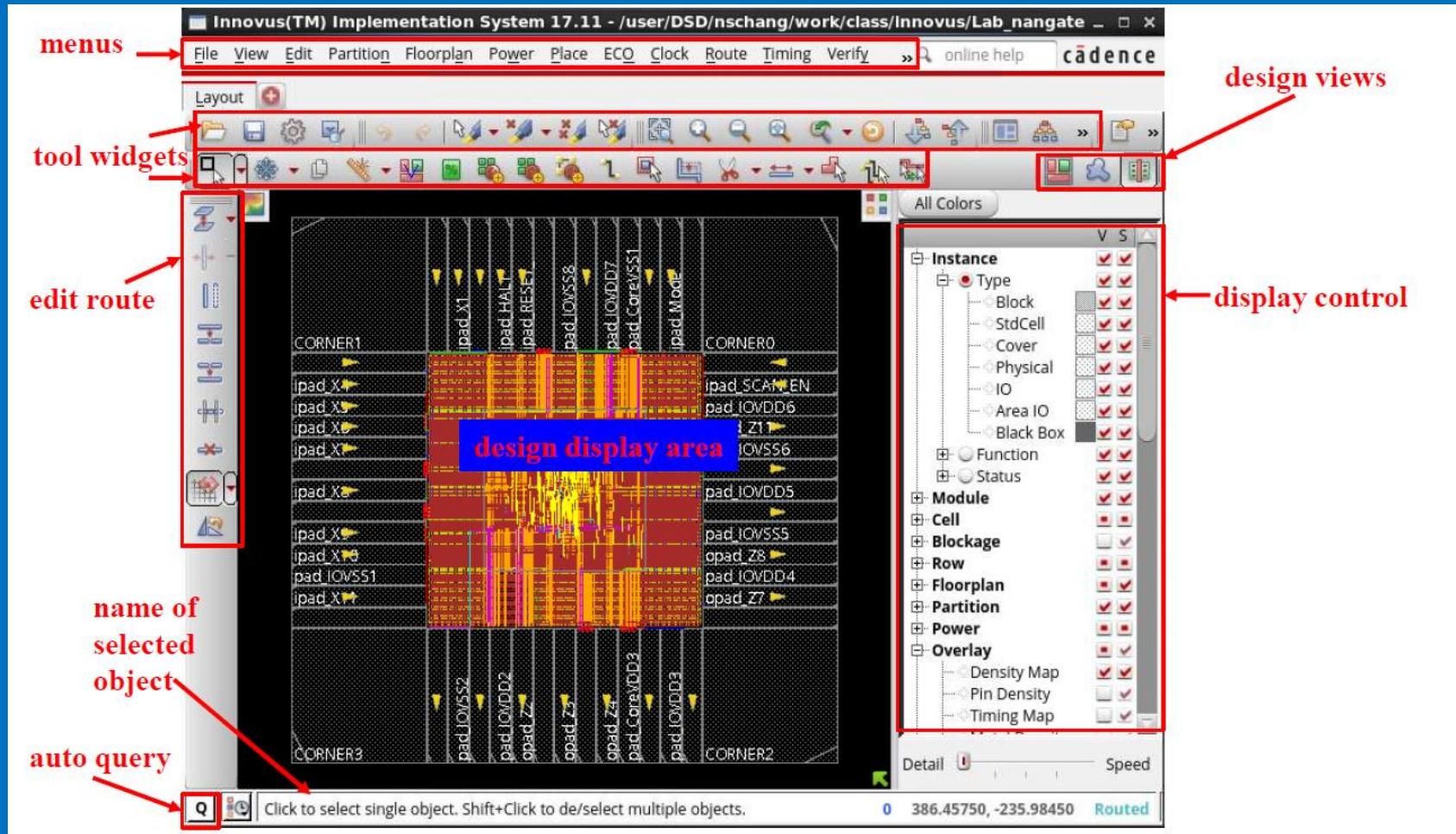
Cell name



# System Startup

- ◆ 第一次使用工作站，先**copy .cshrc**檔案到自己的資料夾
  - > **cp /home/standard/Environment\_Setup\_File/cshrc .cshrc**
  - > **source .cshrc**
  - 接著重新開啟終端機
- ◆ 由於**Innovus**使用時會產生很多記錄的檔案，所以建議先使用**mkdir APR** 創建一個名為**APR** 的資料夾，在使用**cd** 切換到**APR**的目錄下，並準備好3種**prepare data**，執行**Innovus**
  - > **mkdir APR**
  - > **cd APR**
  - > **cp /home/standard/multimedia/apr/\* .** 千萬別忘了這個點  
記得cp後以及\*後按空白鍵
- ◆ 執行**Innovus**軟體
  - > **source /usr/cad/cadence/CIC/innovus.cshrc**
  - > **innovus**

# Overview - GUI





# Overview - Design View



## ◆ Floorplan View

- displays the hierarchical module and block guides, connection flight lines and floorplan objects



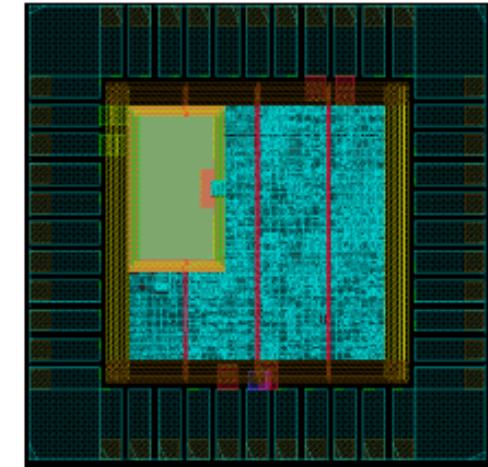
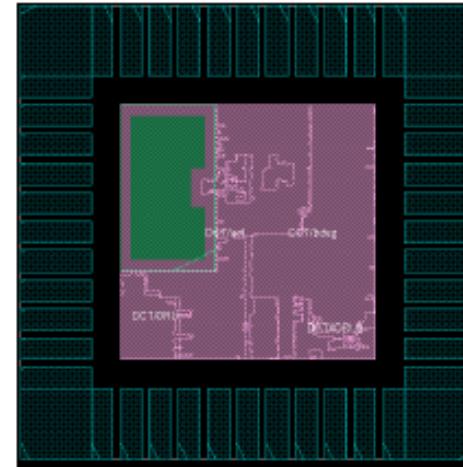
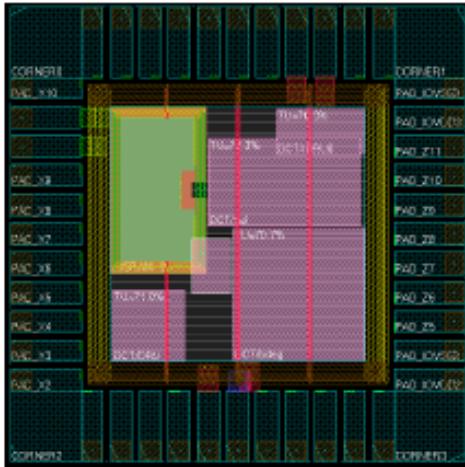
## ◆ Amoeba View

- display the outline of modules after placement

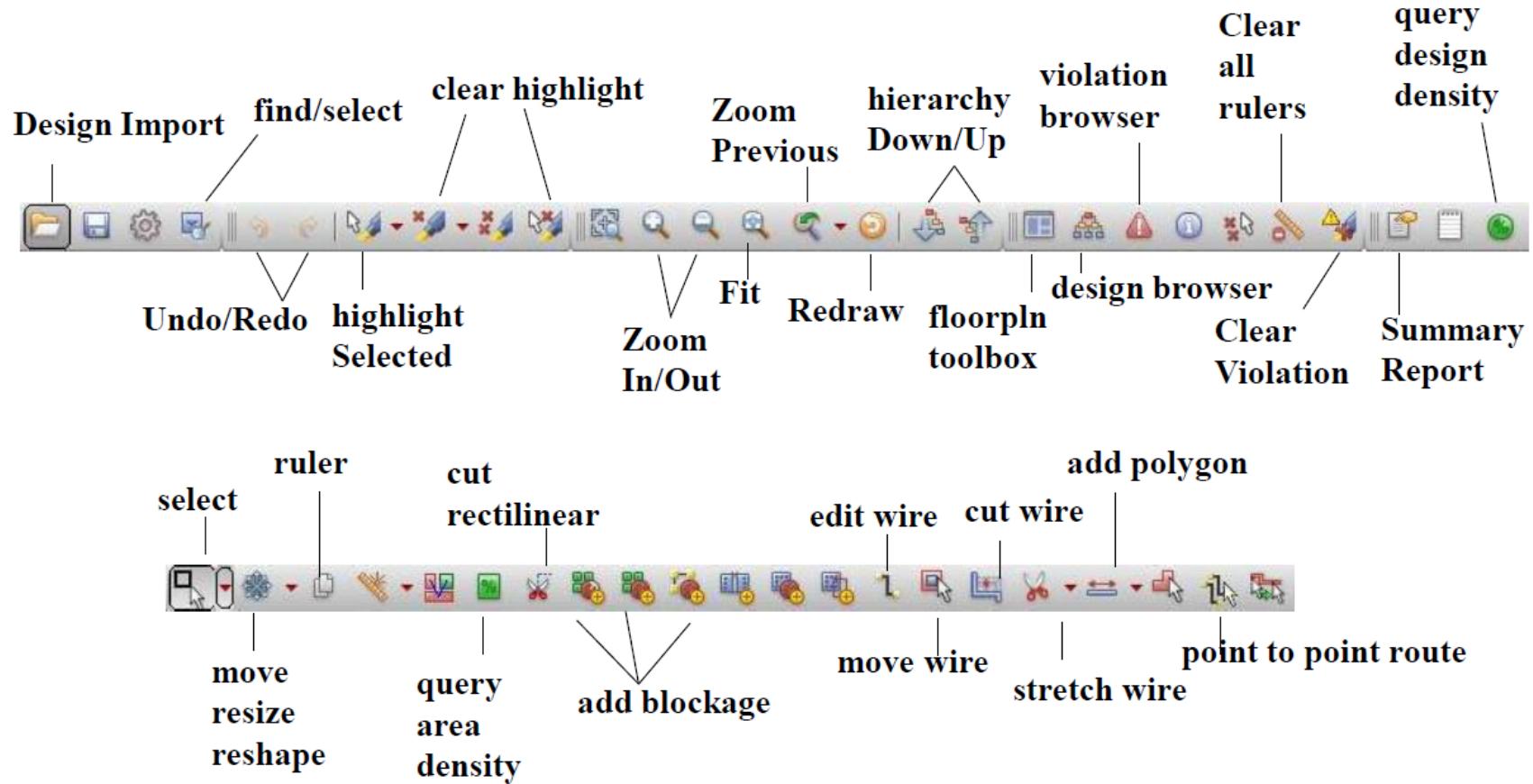


## ◆ Physical View

- display the detailed placements of cells, blocks.



# Overview - Tool Widget



# Overview – Layer Control



All Colors		
	V	S
<b>Instance</b>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Type	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Block	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
StdCell	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Cover	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Physical	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
IO	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Area IO	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Black Box	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Function	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Status	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<b>Module</b>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Module	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Guide	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Fence	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Region	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Partition	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<b>Cell</b>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Pin Shapes	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Cell Blockage	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Cell Layout/GD	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<b>Blockage</b>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Obstruct	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Area Density	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Macro Blkg	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Routing Blkg	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Fill Blkg	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Trim Blkg	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Drc Region	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Block Halo	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Routing Halo	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Litho Halo	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Blockage Link	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<b>Row</b>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Standard Row	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
IO Row	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Row Pattern	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Macro Pattern	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<b>Floorplan</b>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Rel. FPlan	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
SizeBlkg	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
S. Resize Line	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
E. Resize Line	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
MP CongTag	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
IO Cluster	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Overlap Macro	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Overlap Guide	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Overlap Block	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Datapath	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<b>Partition</b>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Pin Guide	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Ptn Pin Blk	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Ptn Feedthru	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<b>Power</b>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Power Domain	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Power Graph	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Sub. Noise	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
IR Drop & EM	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<b>Overlay</b>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Density Map	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Pin Density	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Timing Map	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal Density	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Power Density	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Congestion	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<b>Track</b>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Pref Track	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
NPref Track	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<b>Net</b>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Signal	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Special Net	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Power	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Ground	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Clock	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<b>Route</b>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Shield	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Early Global	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal Fill	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Wire	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Via	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Patch Wire	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Trim Metal	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<b>Bump</b>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Bump(Normal)	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Bump(Back)	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Bump Connect	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<b>Grid</b>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Manufacture	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Placement	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
User-defined	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Instance	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
FinFET Manufa	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
FinFET Instanc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
FinFET Placem	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
GCell	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Trim Grid	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
PG Via Grid	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<b>Miscellaneous</b>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
PVS GDS Fill	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Terminal	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Violation	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Bus Guide	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Aggressor	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Text	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Pin Text	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Flight Line	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Port Number	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Double Pattern	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>



# Overview - Hot Key

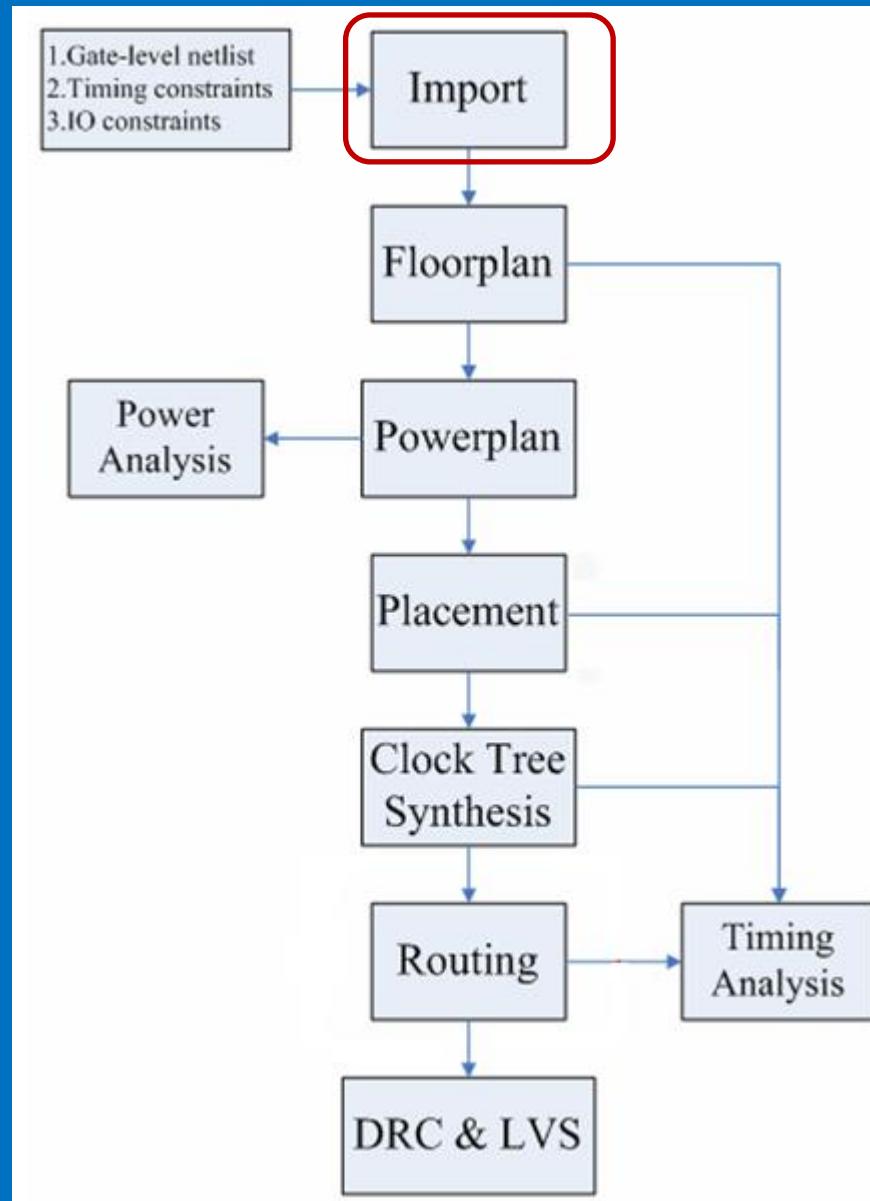
Key	Action
q	Edit attribute
f	Fits display
z	Zoom in
Z	Zoom out
↑↓←→	pans design area in the direction of the arrow
Esc	Cancel
K	Clear all rulers

Key	Action
space	Select Next
e	popup Edit
T	editTrim
0-9	toggle layer[0-9] visibility
V	clear Violation
N	next via
F12	Dim selection background

Looking for more bindkey:  
*View → Set Preference, Binding Key*

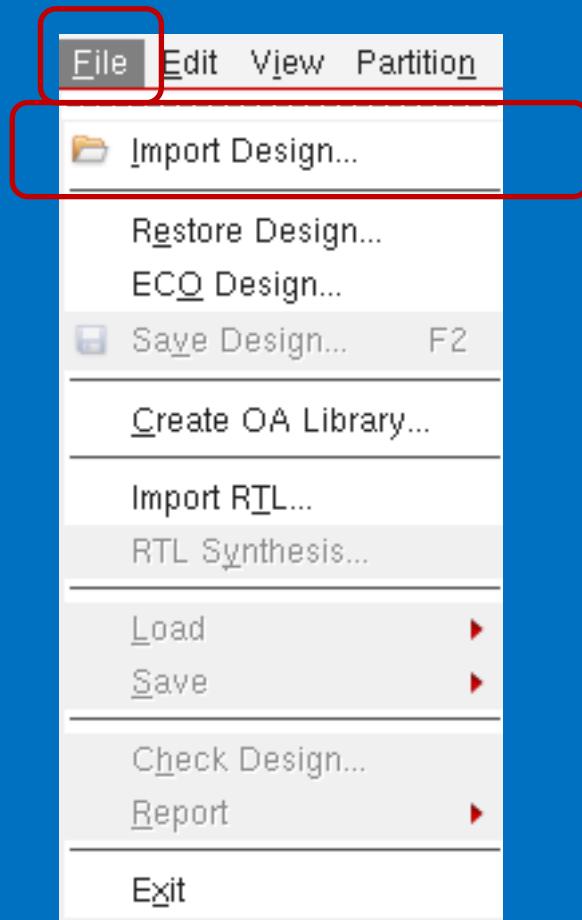


# Import



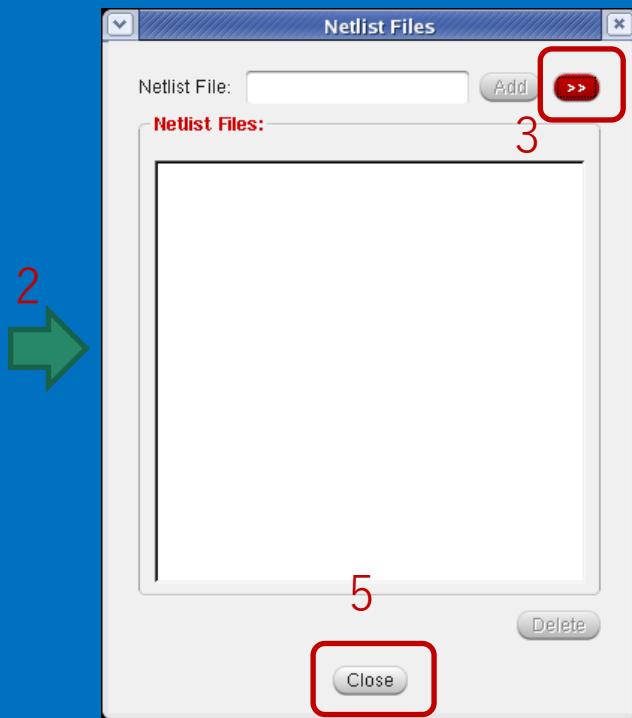
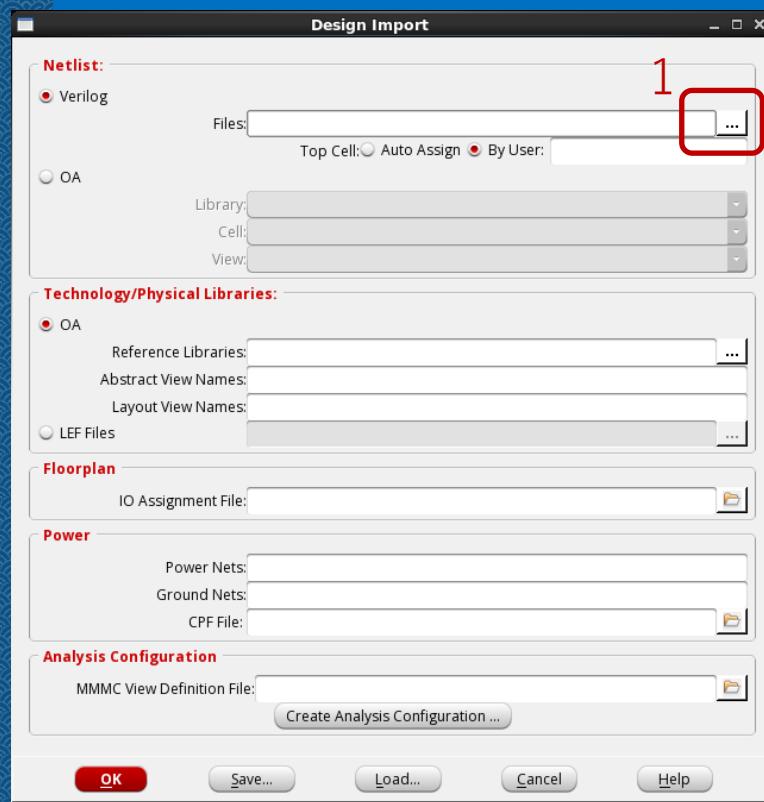


# Import





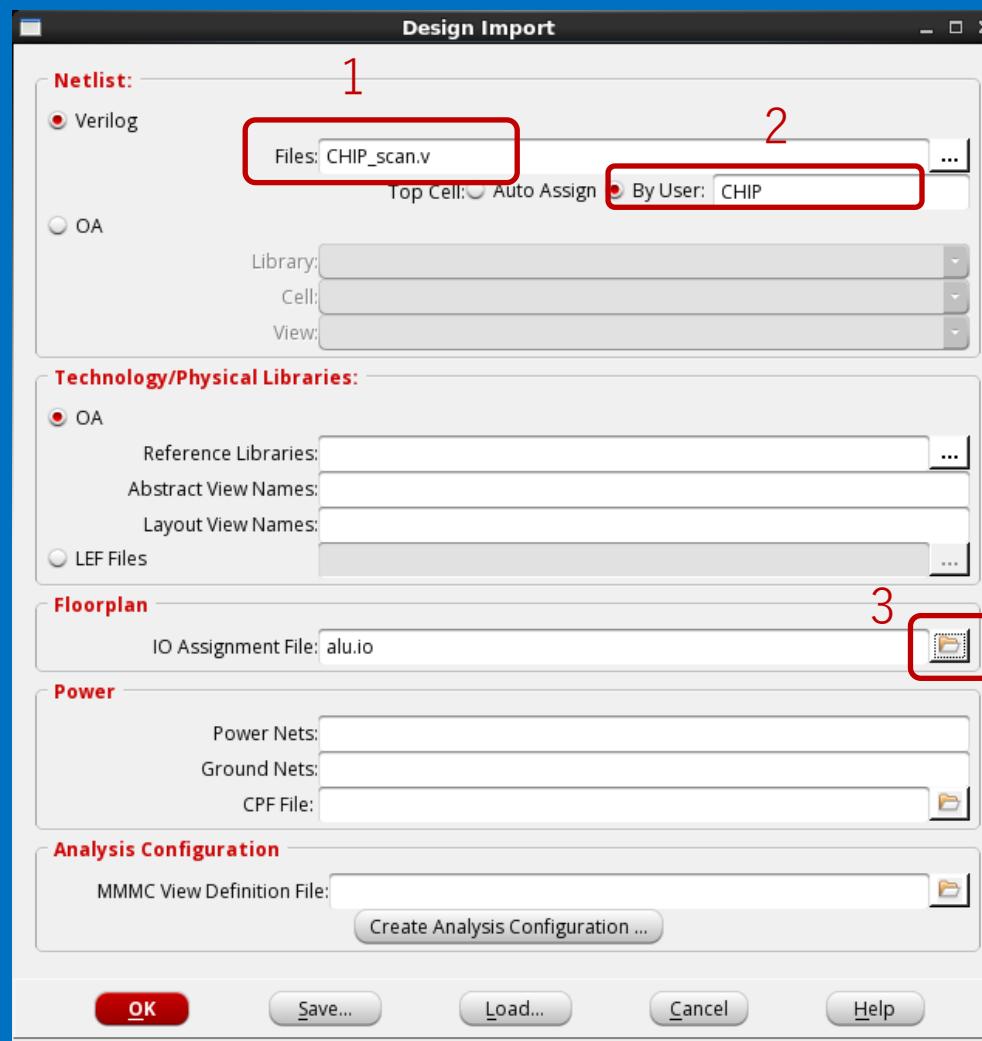
# Import



4  
extend 出 file browser，選擇 CHIP\_scan.v，然後按 Add 把CHIP\_scan.v 加到 Netlist Files



# Import

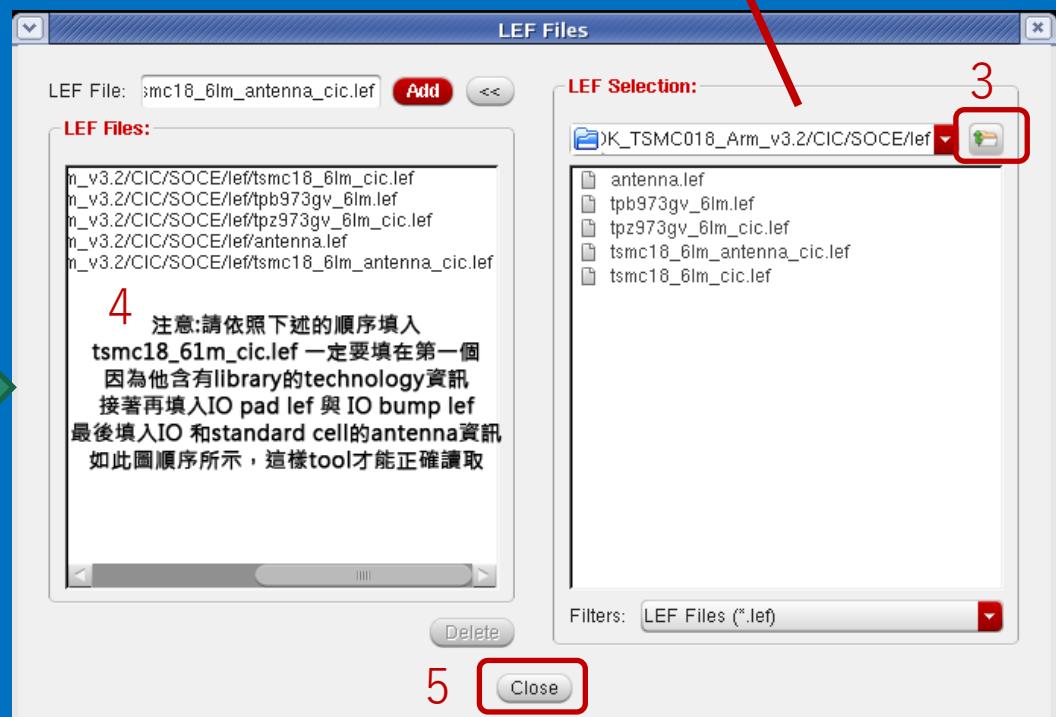
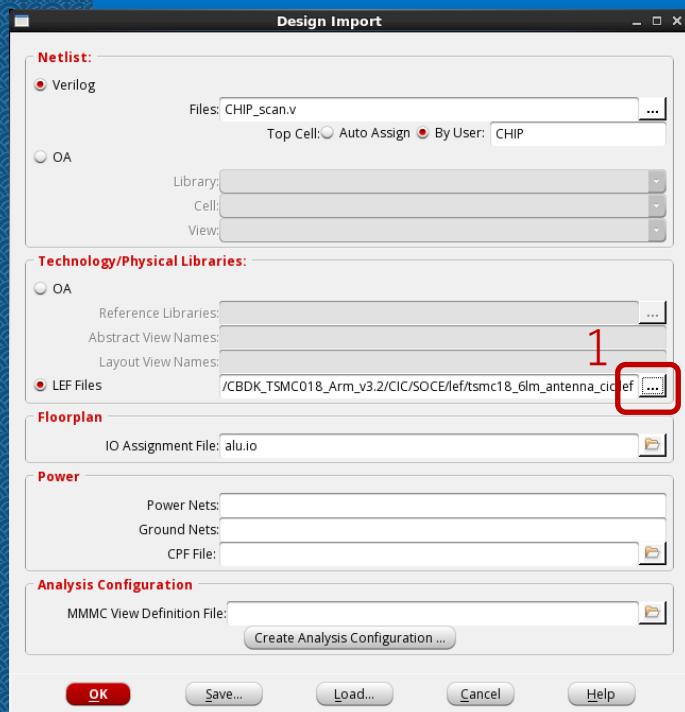


# Import



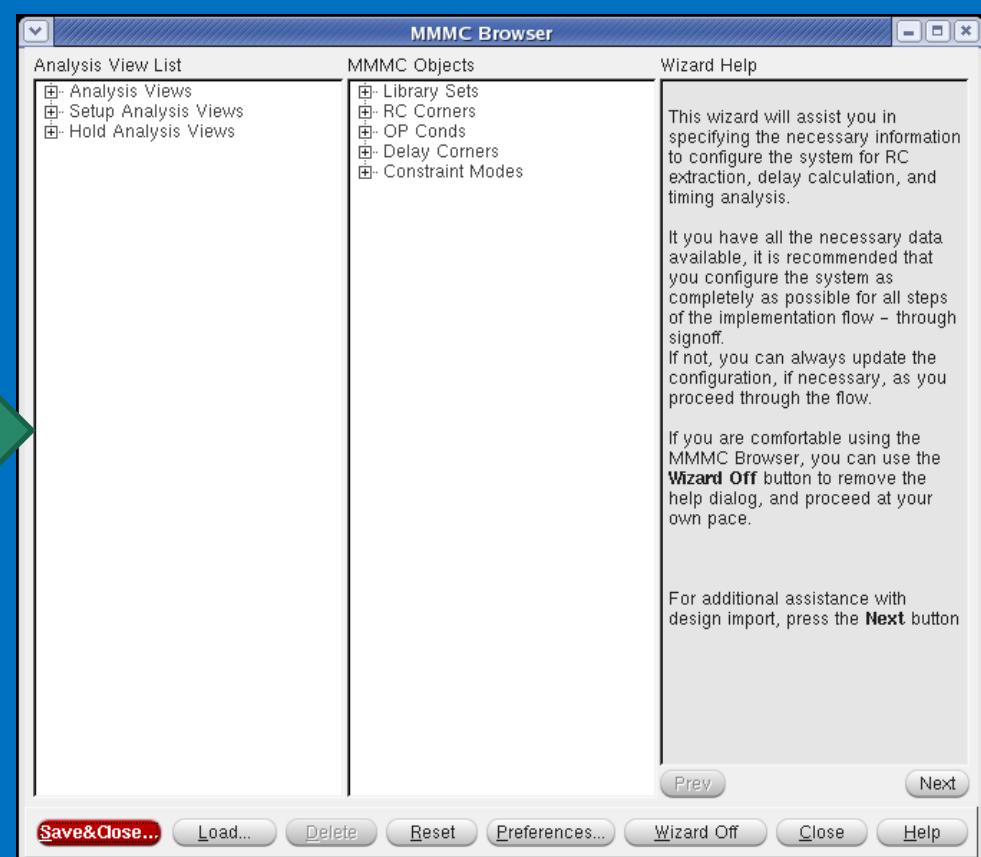
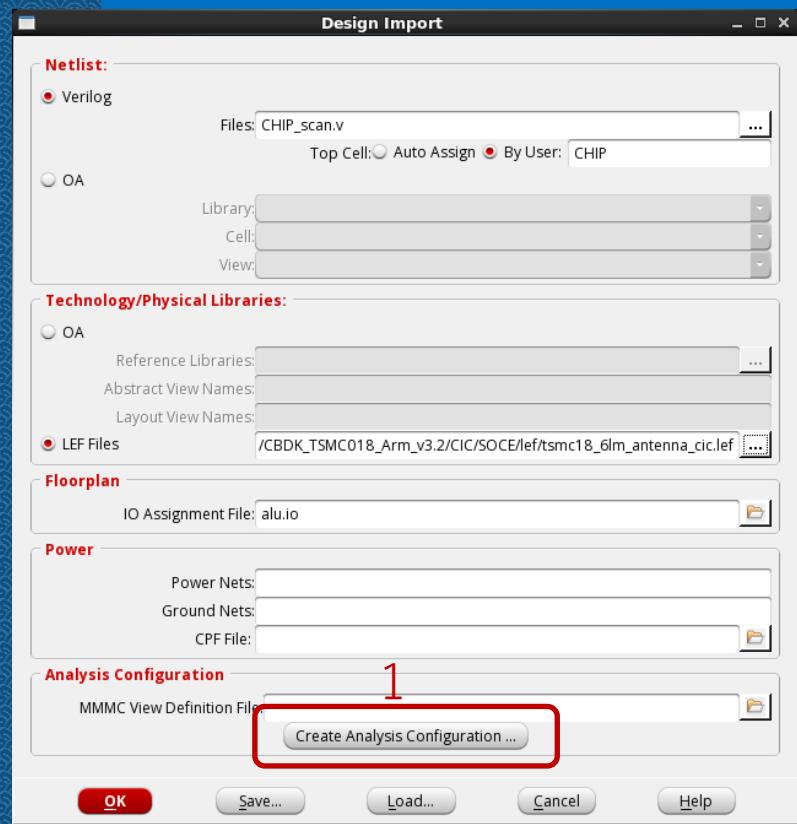
/home/cell\_lib/CBDK\_TSMC018\_Arm\_v3.2/CIC/S  
OCE/lef (islabx5在Design\_kit內)

路徑檔



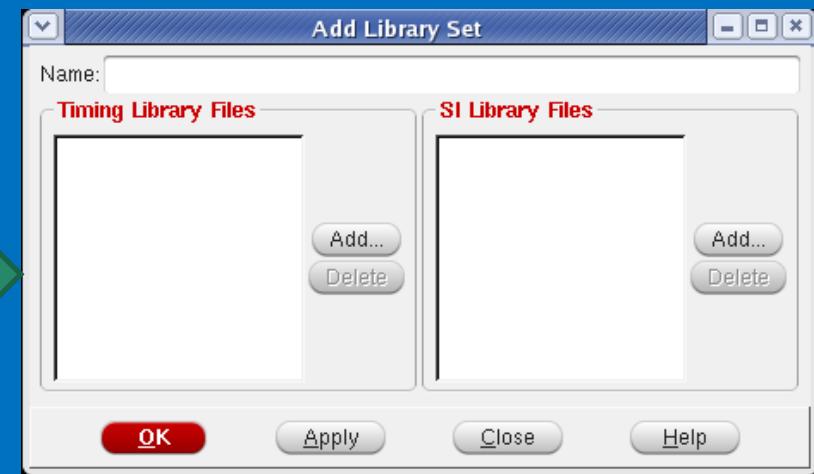
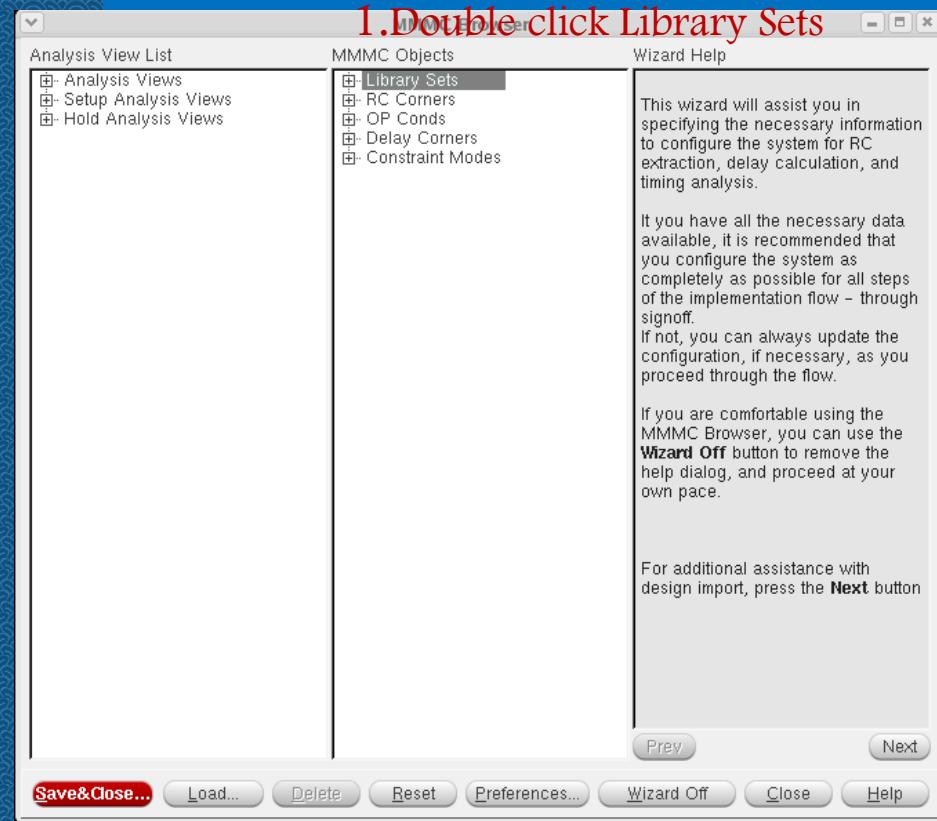


# Import





# Import



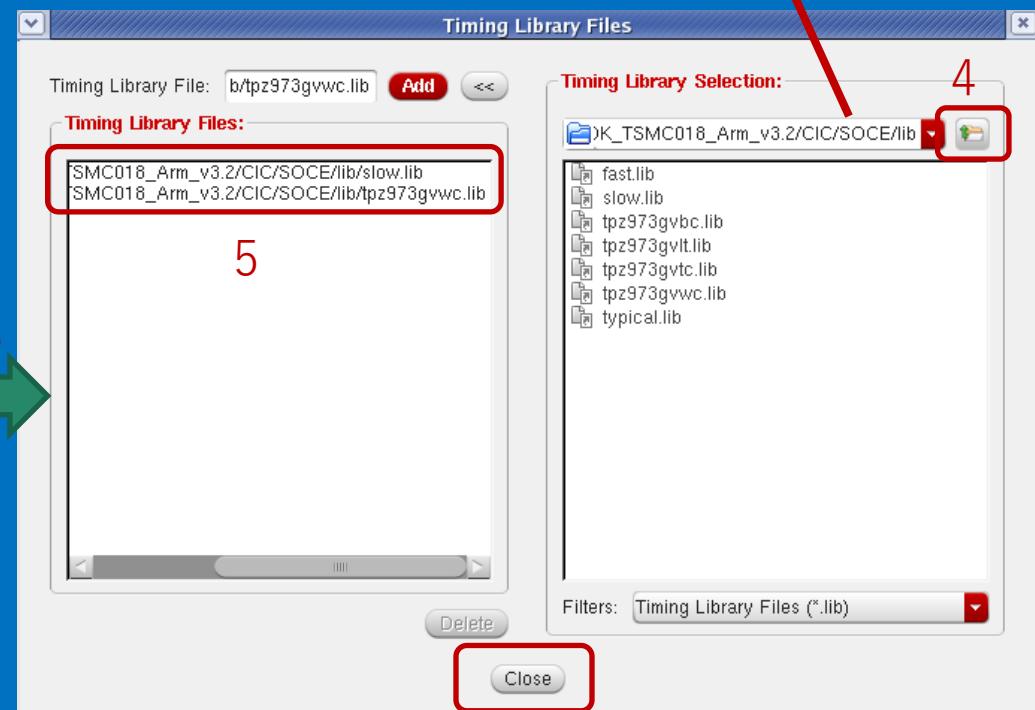
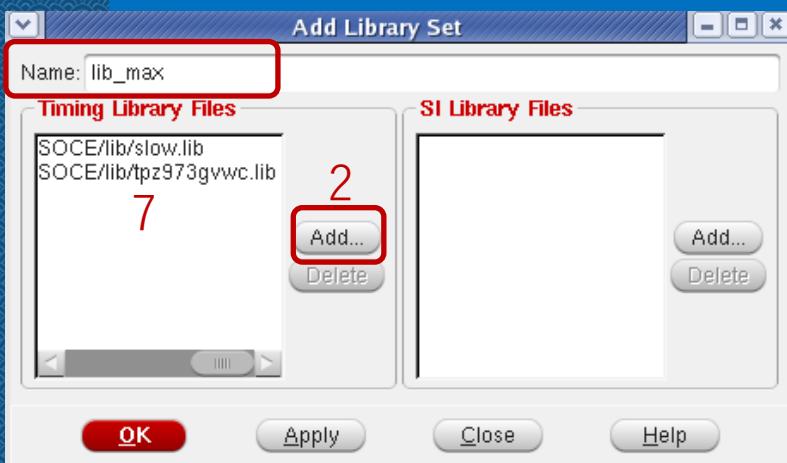


# Import

/home/cell\_lib/CBDK\_TSMC018\_Arm\_v3.2/CIC/SOCE/lib (islabx5在Design\_kit內)

路徑檔

1. 填入lib\_max

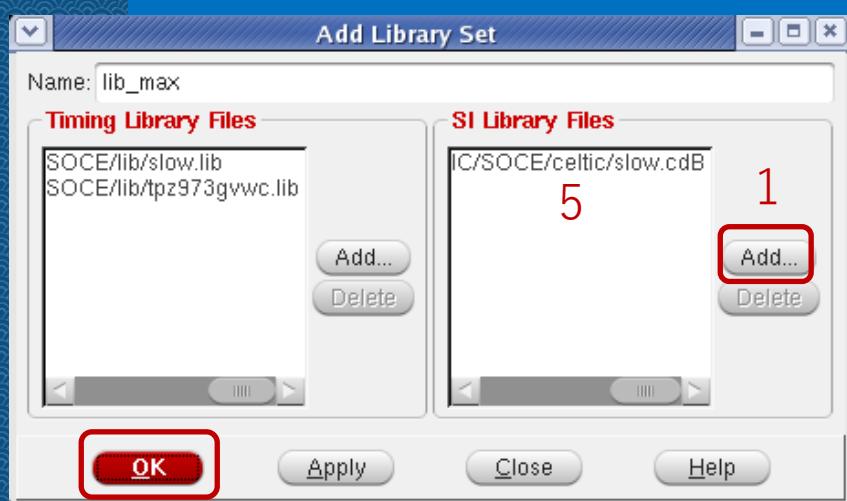
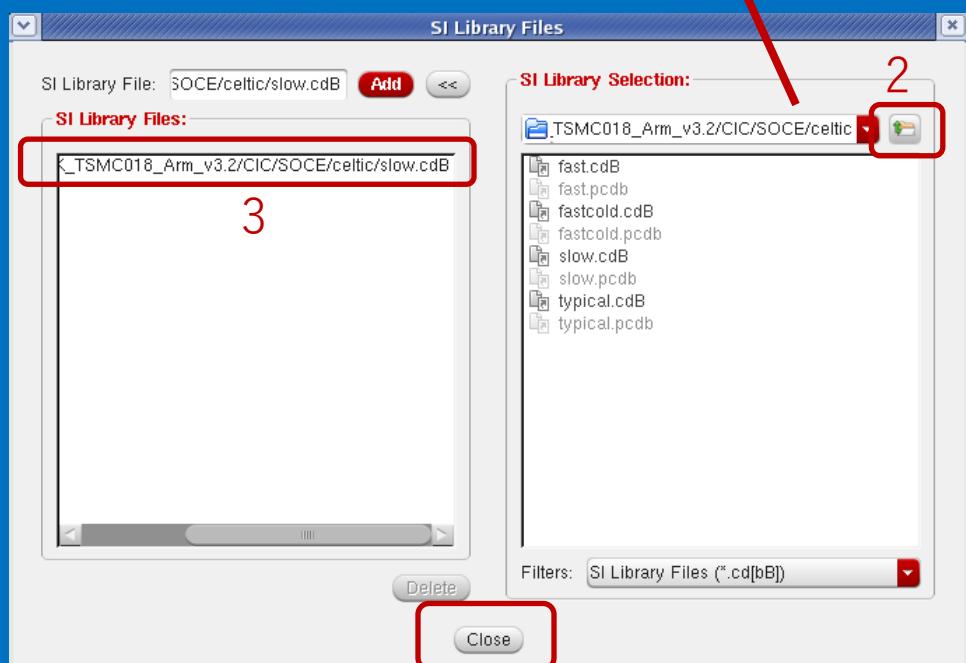




# Import

/home/cell\_lib/CBDK\_TSMC018\_Arm\_v3.2/CIC/  
SOCE/celtic (islabx5在Design\_kit內)

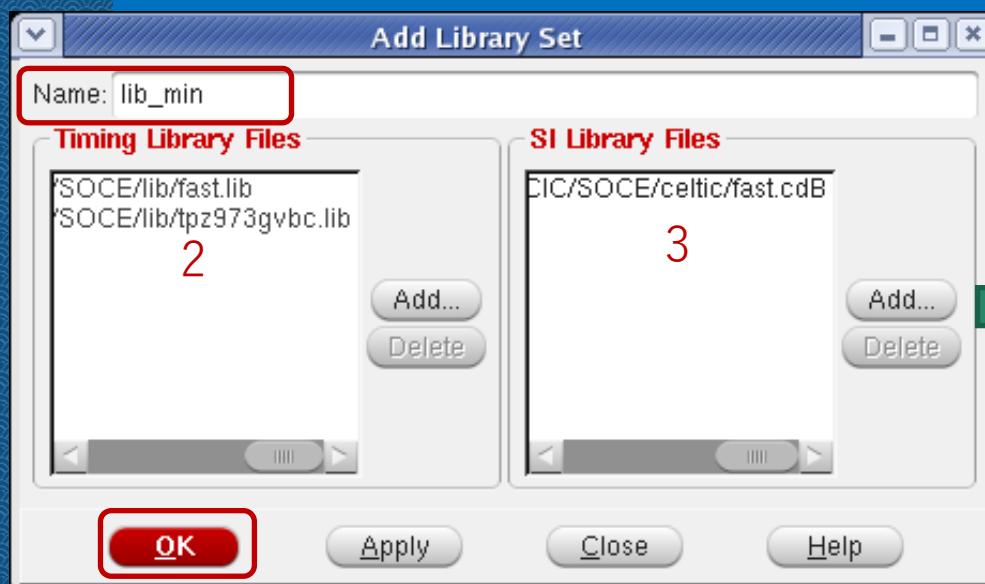
路徑檔



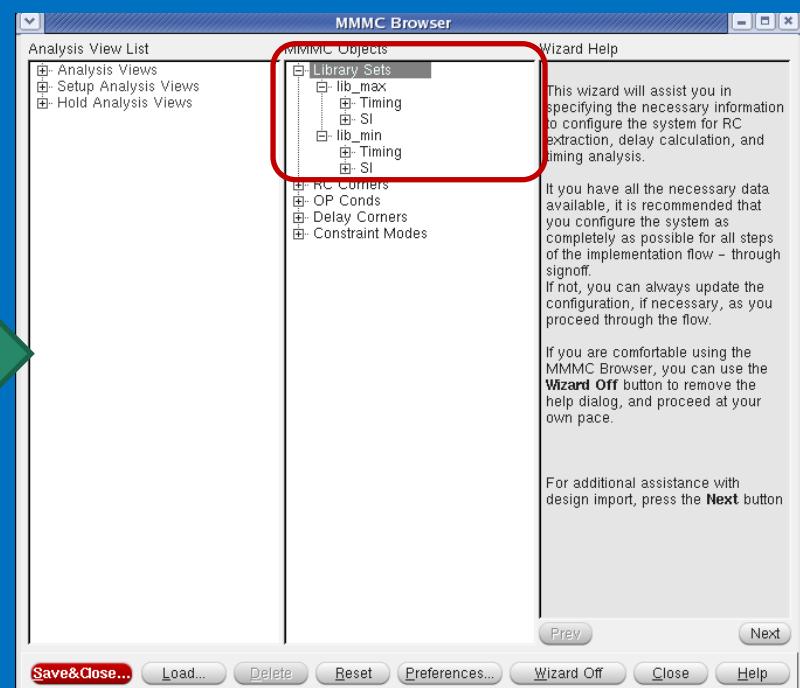


# Import

1. 填入lib\_min



4

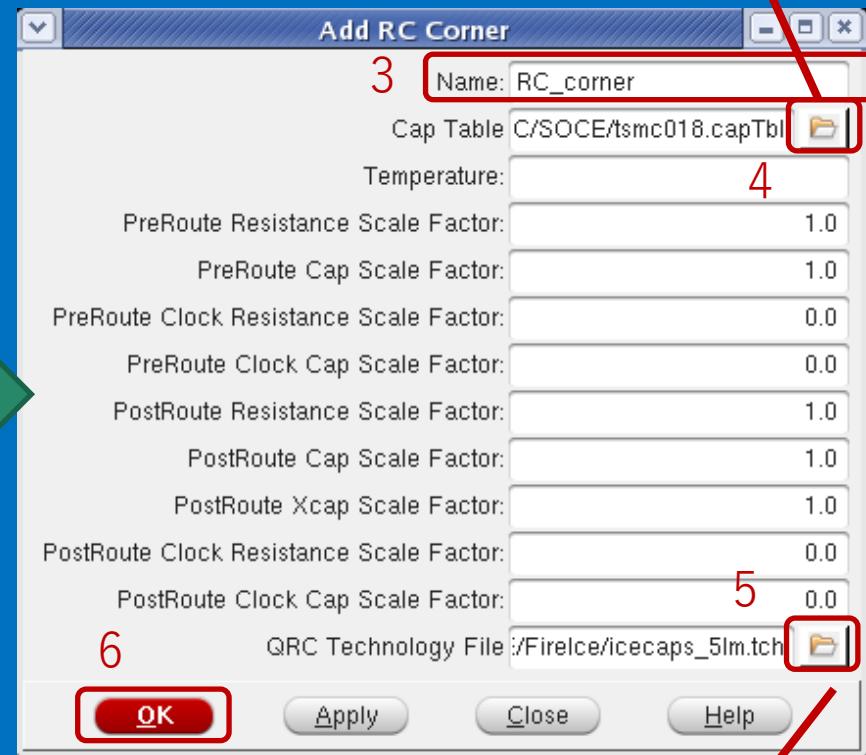
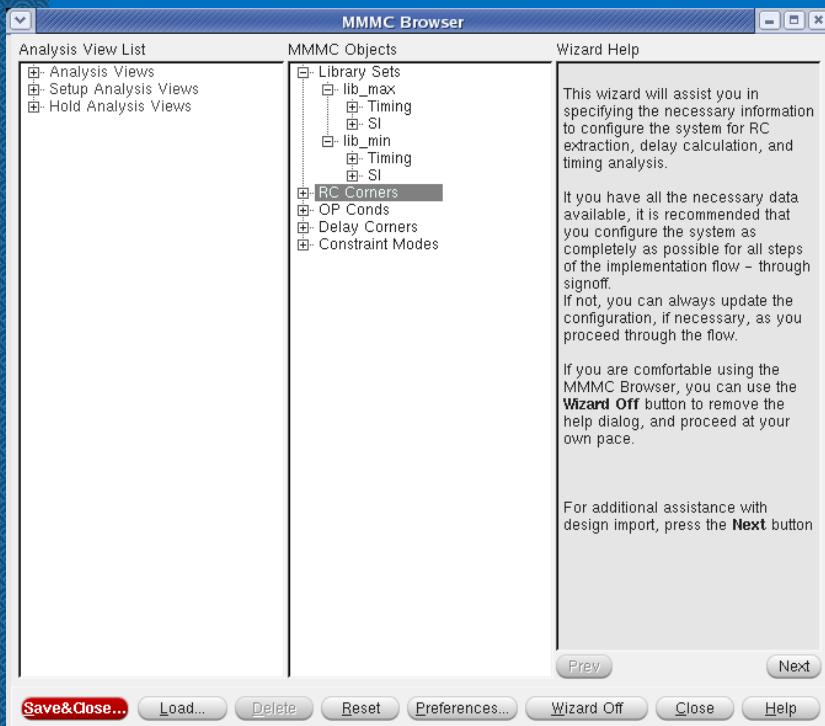


5

# Import



1.Double click RC Corners

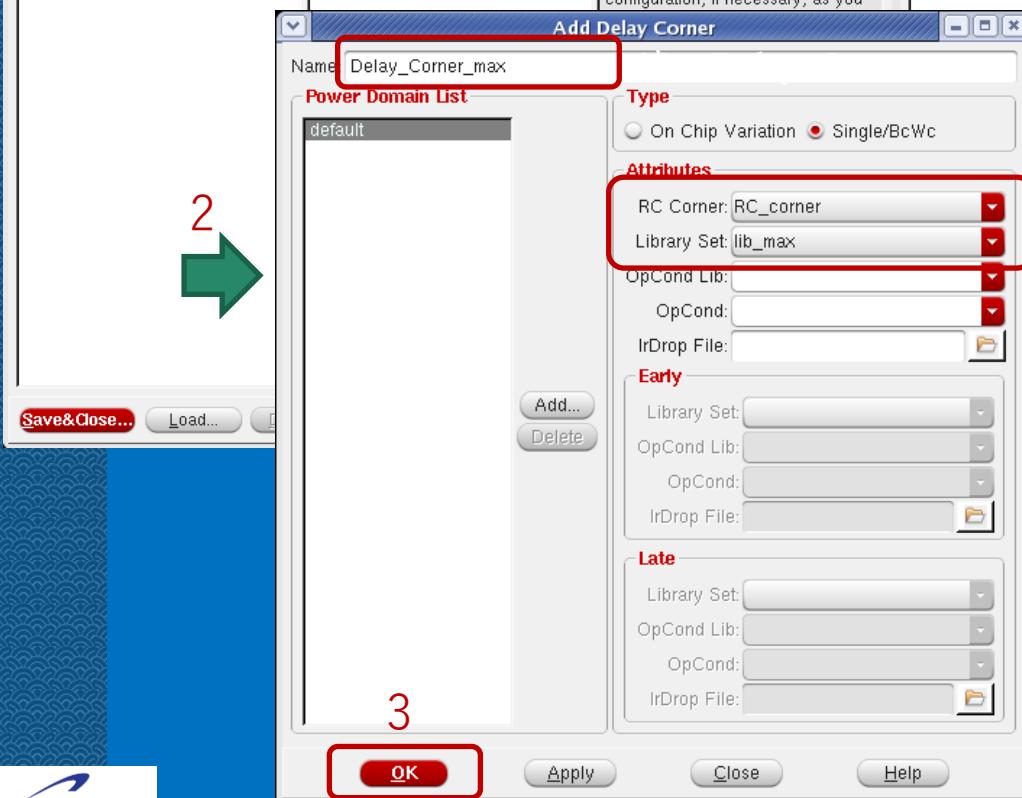


/home/cell\_lib/CBDK\_TSMC018\_Arm\_v3.2/CIC/  
SOCE/tsmc018.capTbl (islabx5在Design\_kit內)

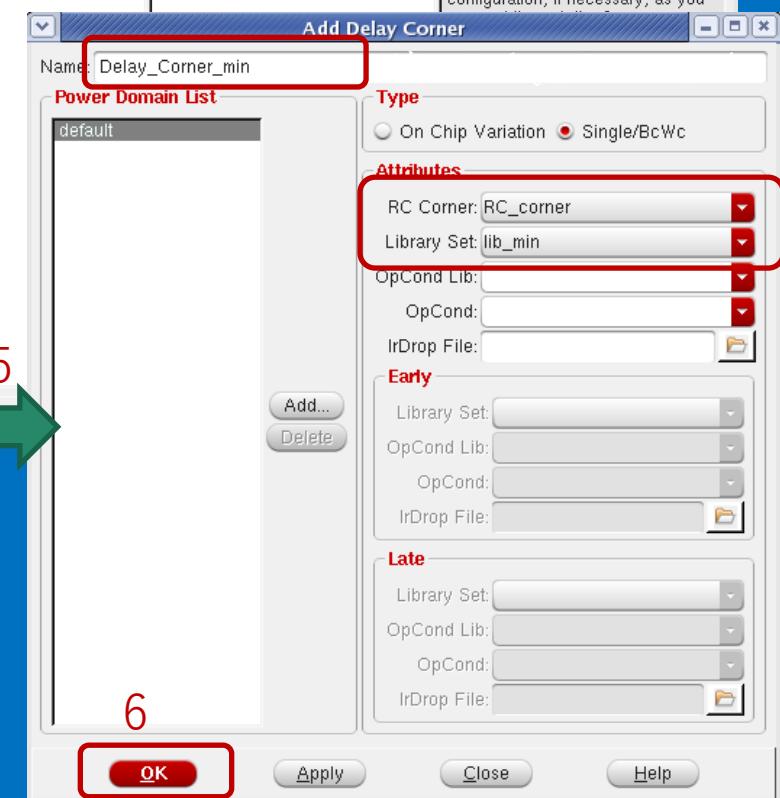
# Import



1. Double click Delay Corners

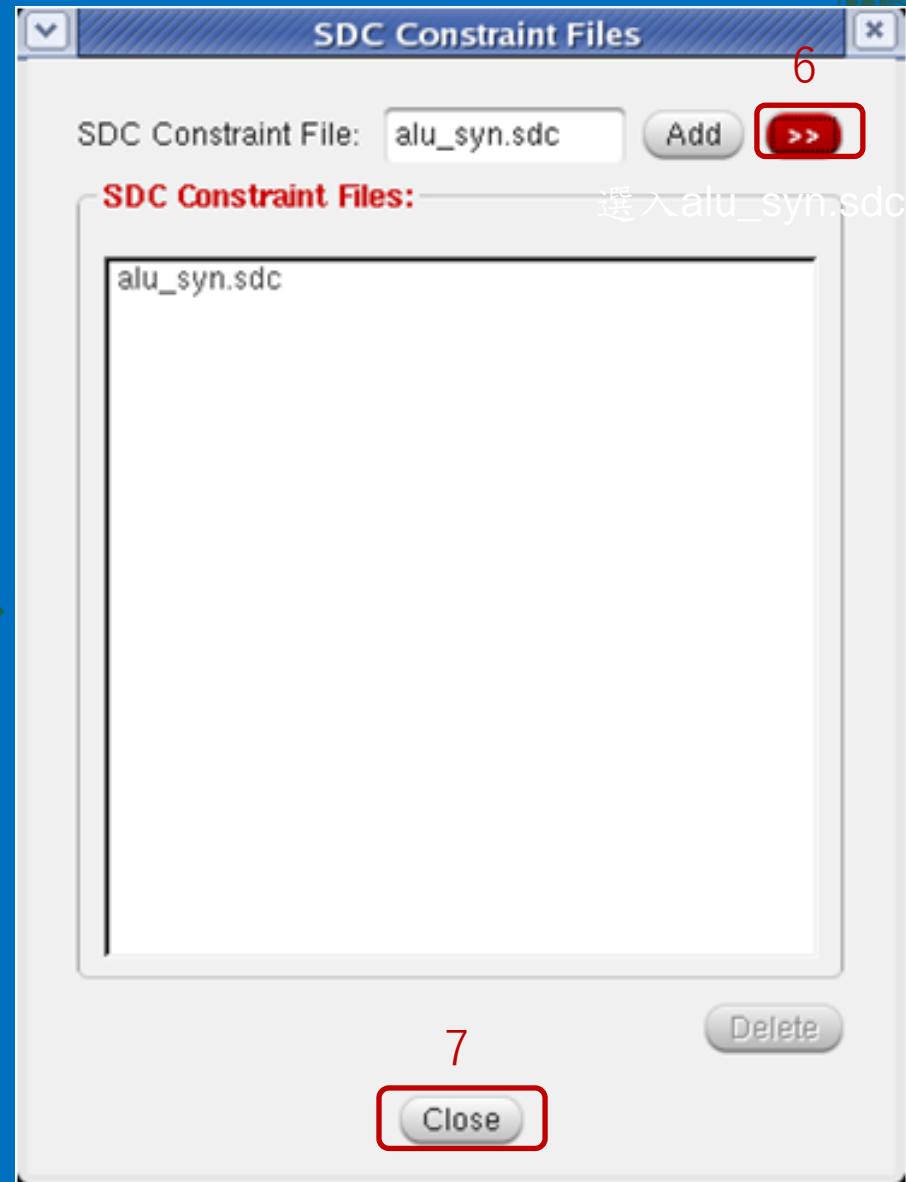
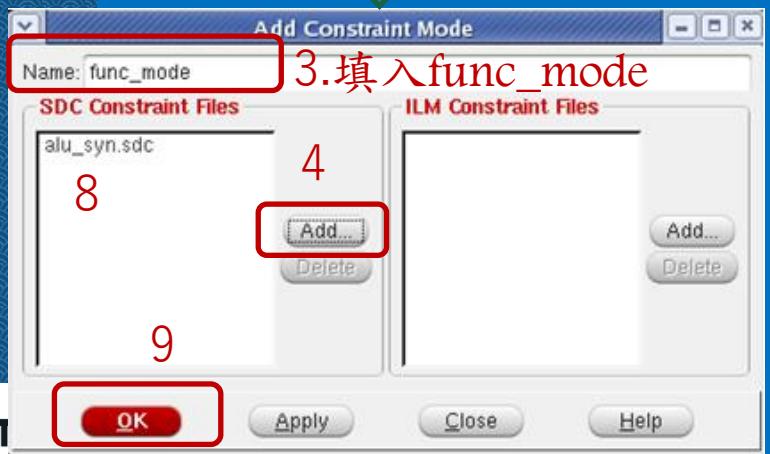
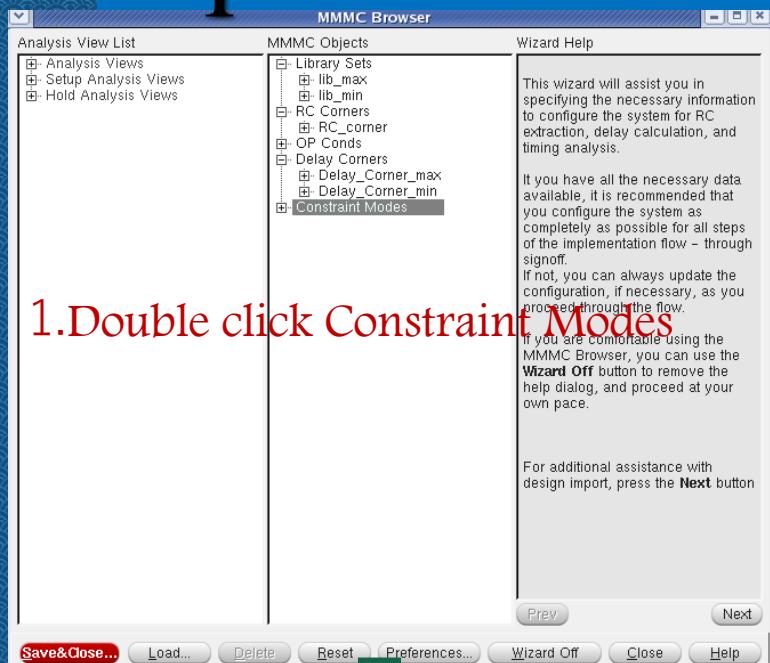


4. Double click Delay Corners



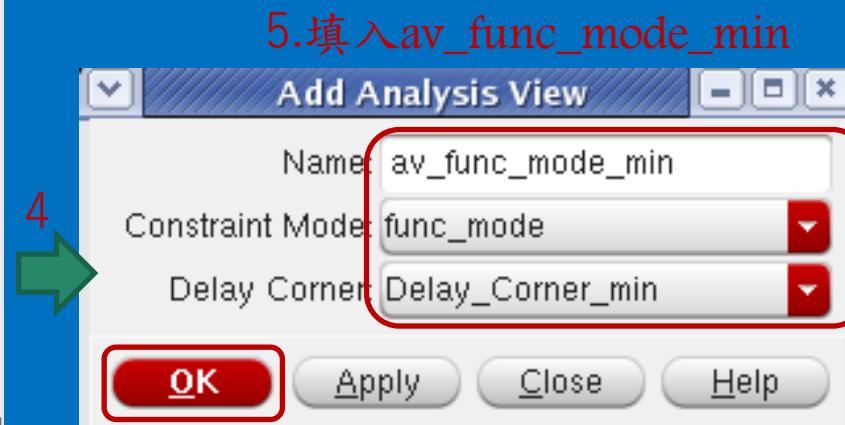
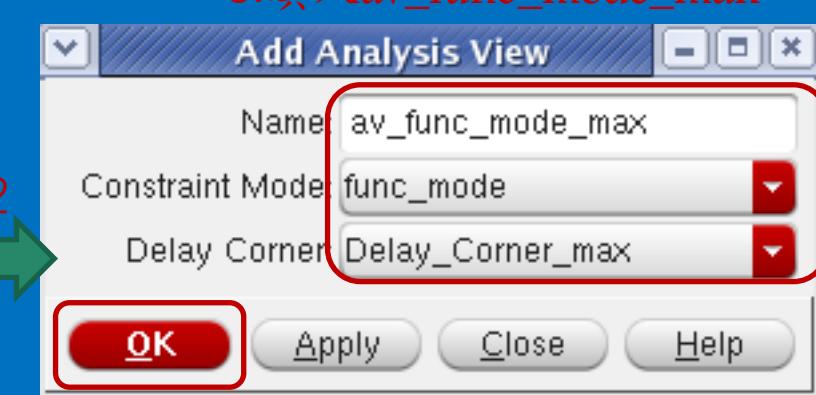
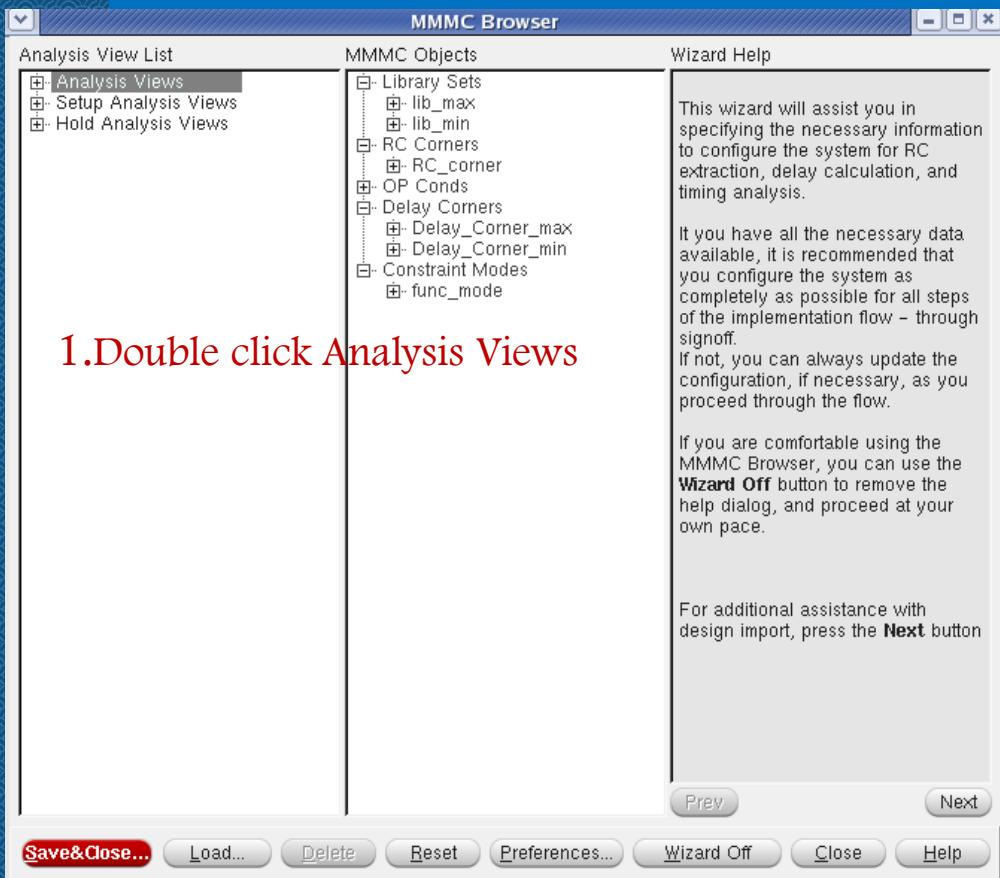


# Import





# Import





# Import

**MMMC Browser**

Analysis View List	MMMC Objects	Wizard Help
<ul style="list-style-type: none"> <li> - Analysis Views           <ul style="list-style-type: none"> <li> - av_func_mode_max</li> <li> - av_func_mode_min</li> </ul> </li> <li> - Setup Analysis Views</li> <li> - Hold Analysis Views</li> </ul>	<ul style="list-style-type: none"> <li> - Library Sets           <ul style="list-style-type: none"> <li> - lib_max</li> <li> - lib_min</li> </ul> </li> <li> - RC Corners           <ul style="list-style-type: none"> <li> - RC_corner</li> </ul> </li> <li> - OP Conds</li> <li> - Delay Corners           <ul style="list-style-type: none"> <li> - Delay_Corner_max</li> <li> - Delay_Corner_min</li> </ul> </li> <li> - Constraint Modes           <ul style="list-style-type: none"> <li> - func_mode</li> </ul> </li> </ul>	<p>This wizard will assist you in specifying the necessary information to configure the system for RC extraction, delay calculation, and timing analysis.</p> <p>If you have all the necessary data available, it is recommended that you configure the system as completely as possible for all steps of the implementation flow – through signoff. If not, you can always update the configuration, if necessary, as you proceed through the flow.</p> <p>If you are comfortable using the MMMC Browser, you can use the <b>Wizard Off</b> button to remove the help dialog, and proceed at your own pace.</p> <p>For additional assistance with design import, press the <b>Next</b> button</p>

Save&Close... Load... Delete Reset Preferences... Wizard Off Close Help

1.Double click Setup Analysis Views

**Add Setup Analysis View**

2

3

Analysis View: **av\_func\_mode\_max**

4

OK Apply Close Help



# Import

**1. Double click Hold Analysis Views**

**MMMC Browser**

Analysis View List

- Analysis Views
  - + av\_func\_mode\_max
  - + av\_func\_mode\_min
- Setup Analysis Views
  - + av\_func\_mode\_max
- Hold Analysis Views

MMMC Objects

- Library Sets
  - + lib\_max
  - + lib\_min
- RC Corners
  - + RC\_Corner
- OP Conds
- Delay Corners
  - + Delay\_Corner\_max
  - + Delay\_Corner\_min
- Constraint Modes
  - + func\_mode

Wizard Help

This wizard will assist you in specifying the necessary information to configure the system for RC extraction, delay calculation, and timing analysis.

If you have all the necessary data available, it is recommended that you configure the system as completely as possible for all steps of the implementation flow – through signoff. If not, you can always update the configuration, if necessary, as you proceed through the flow.

If you are comfortable using the MMMC Browser, you can use the **Wizard Off** button to remove the help dialog, and proceed at your own pace.

For additional assistance with design import, press the **Next** button

Prev Next

Save&Close... Load... Delete Reset Preferences... Wizard Off Close Help

**Add Hold Analysis View**

3

2

Analysis View **av\_func\_mode\_min**

4

OK Apply Close Help



# Import

**MMMC Browser**

Analysis View List      MMMC Objects      Wizard Help

1. **Save&Close...**

Analysis Views:  
- av\_func\_mode\_max  
- av\_func\_mode\_min  
Setup Analysis Views  
- av\_func\_mode\_max  
Hold Analysis Views  
- av\_func\_mode\_min

MMMC Objects:  
- Library Sets:  
  - lib\_max  
    - Timing  
    - SI  
  - lib\_min  
    - Timing  
    - SI  
- RC Corners  
- RC\_corner  
- OP\_Cond  
- Delay Corners  
- Delay\_Corner\_max  
- Delay\_Corner\_min  
- Constraint Modes  
- func\_mode

This wizard will assist you in specifying the necessary information to configure the system for RC extraction, delay calculation, and timing analysis.

If you have all the necessary data available, it is recommended that you configure the system as completely as possible for all steps of the implementation flow - through signoff. If not, you can always update the configuration, if necessary, as you proceed through the flow.

If you are comfortable using the MMC Browser, you can use the **Wizard Off** button to remove the help dialog, and proceed at your own pace.

For additional assistance with design import, press the **Next** button.

Prev      Next

Save&Close... Load... Delete Reset Preferences... Wizard Off Close Help

**Save MMC View Definition File**

Look in: /home/t00418078/alu\_syn

2. 存檔成 mmmc.view

File name: mmmc.view

Save

Files of type: MMC View Definition File (\*.view)

3. Save

Cancel

**Design Import**

**Netlist:**

Verilog (radio button selected)  
Files: CHIP\_scan.v  
Top Cell: Auto Assign By User: CHIP

OA

Library:  
Cell:  
View:

**Technology/Physical Libraries:**

OA  
Reference Libraries:  
Abstract View Names:  
Layout View Names:

LEF Files (radio button selected)  
/CBDK\_TSMC018\_Arm\_v3.2/CIC/SOCE/lef/tsmc18\_6lm\_antenna\_cic.lef

**Floorplan**

IO Assignment File: alu.io

**Power**

Power Nets:  
Ground Nets:  
CPF File:

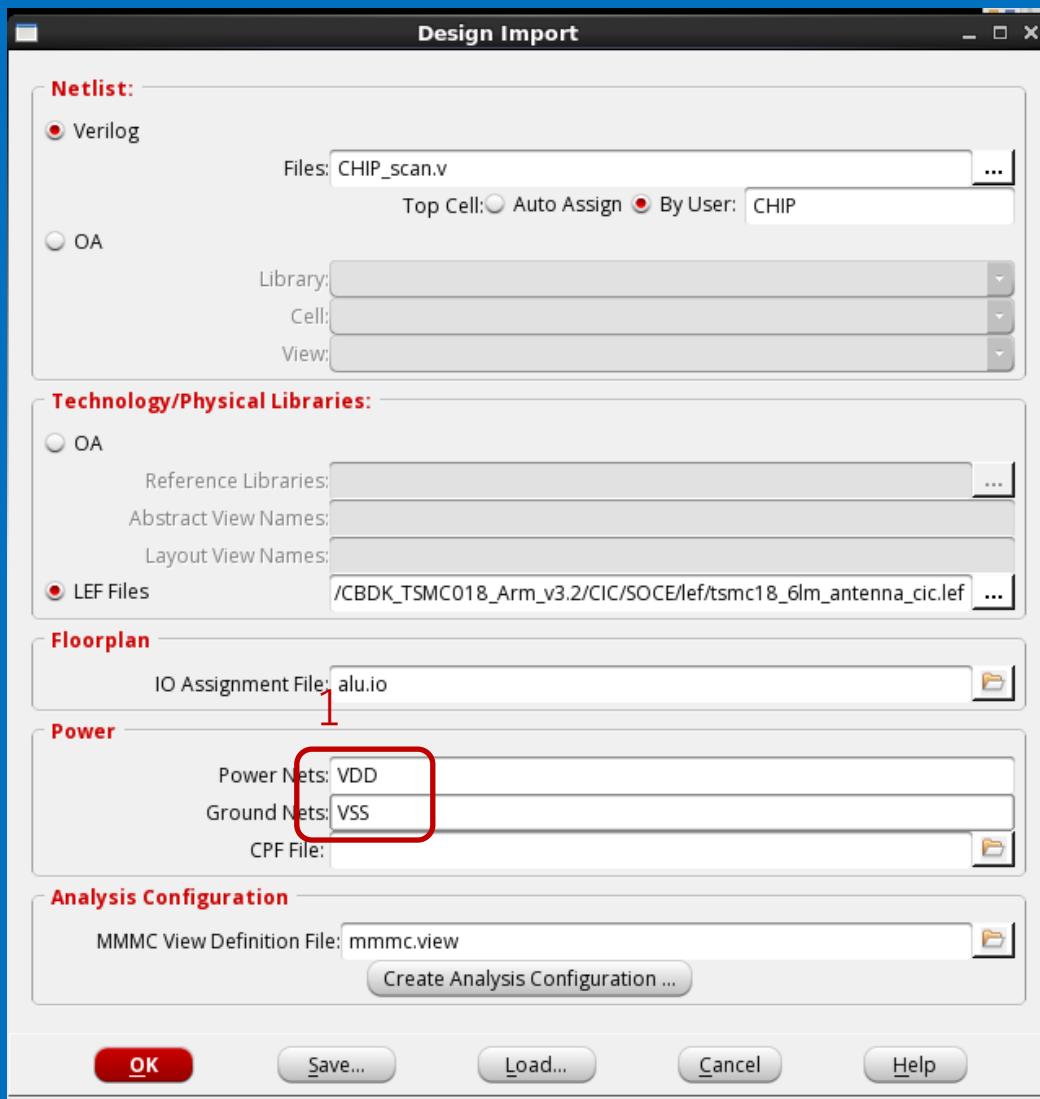
**Analysis Configuration**

MMMC View Definition File: mmmc.view (radio button selected)  
Create Analysis Configuration ...

OK Save... Load... Cancel Help



# Import

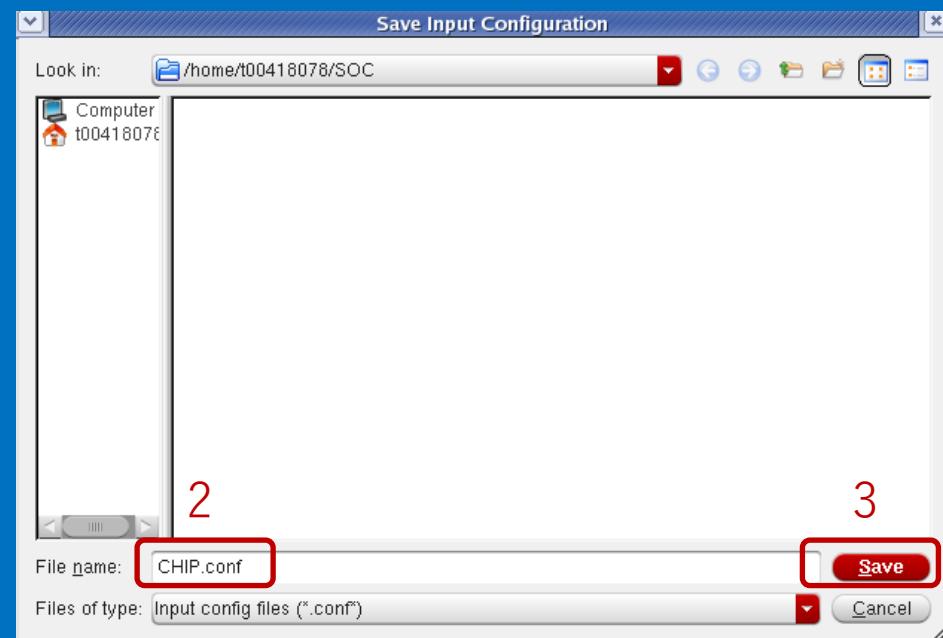
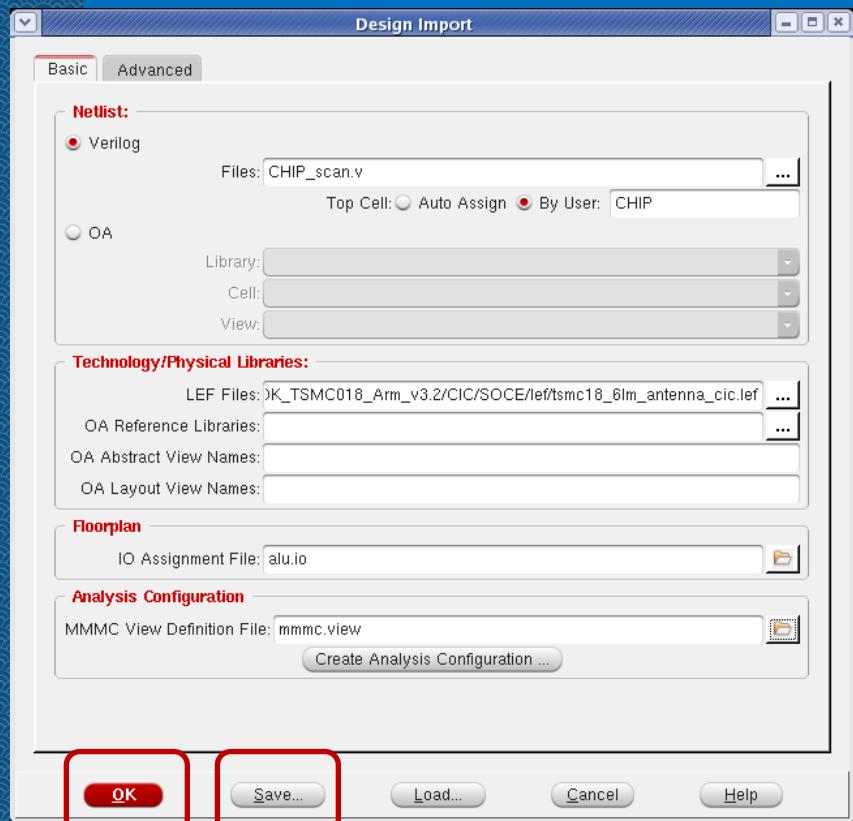


Power Nets 填入VDD  
Ground Nets 填入VSS

填完後就完成所有Import的設定



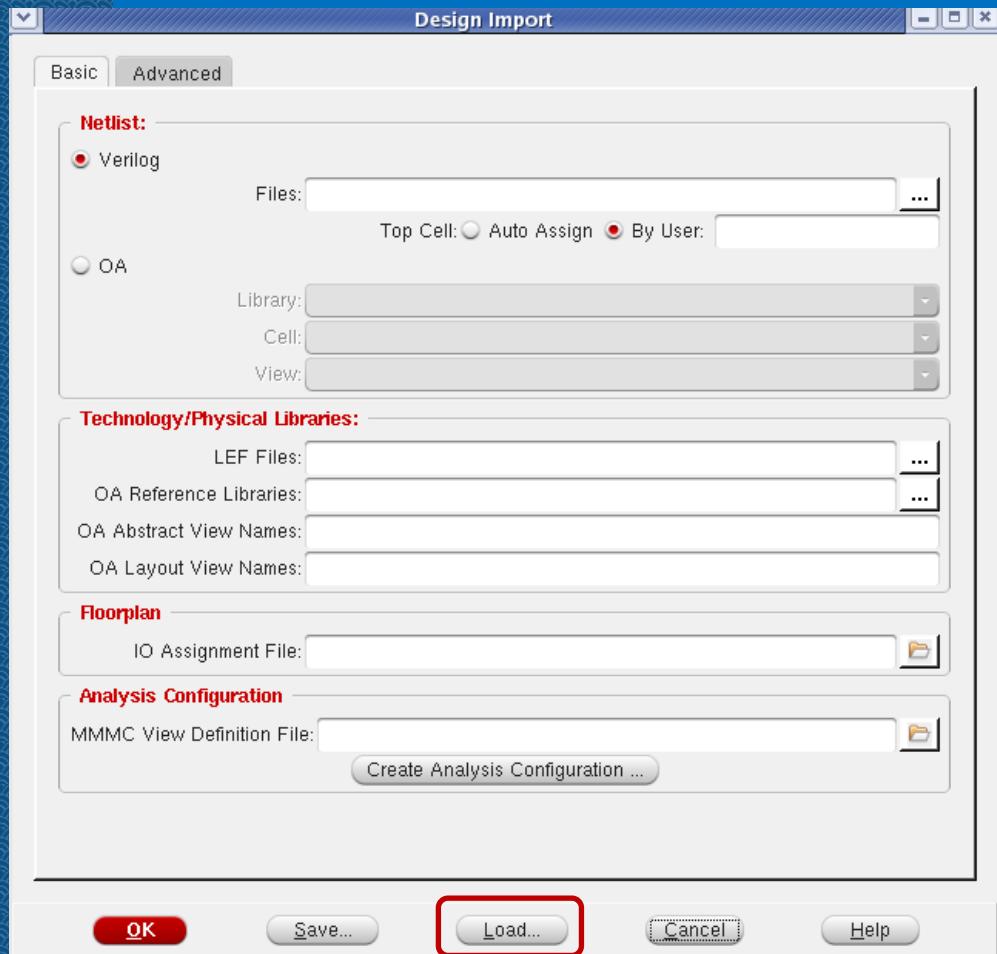
# Import



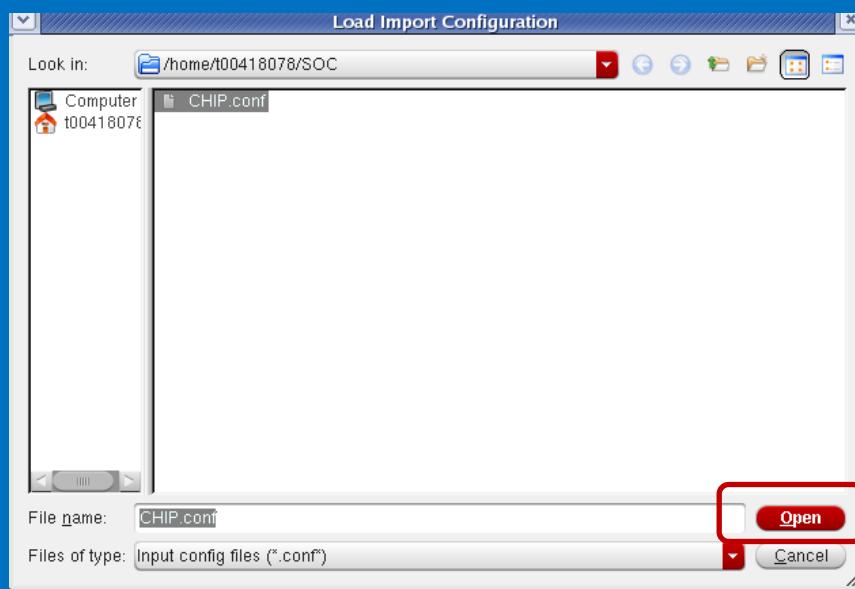
將剛剛所設定的所有資料都存下來，如果以後要 Import 設定檔就可以直接讀取這個 CHIP.conf  
(新版的為 ".globals")



# Import

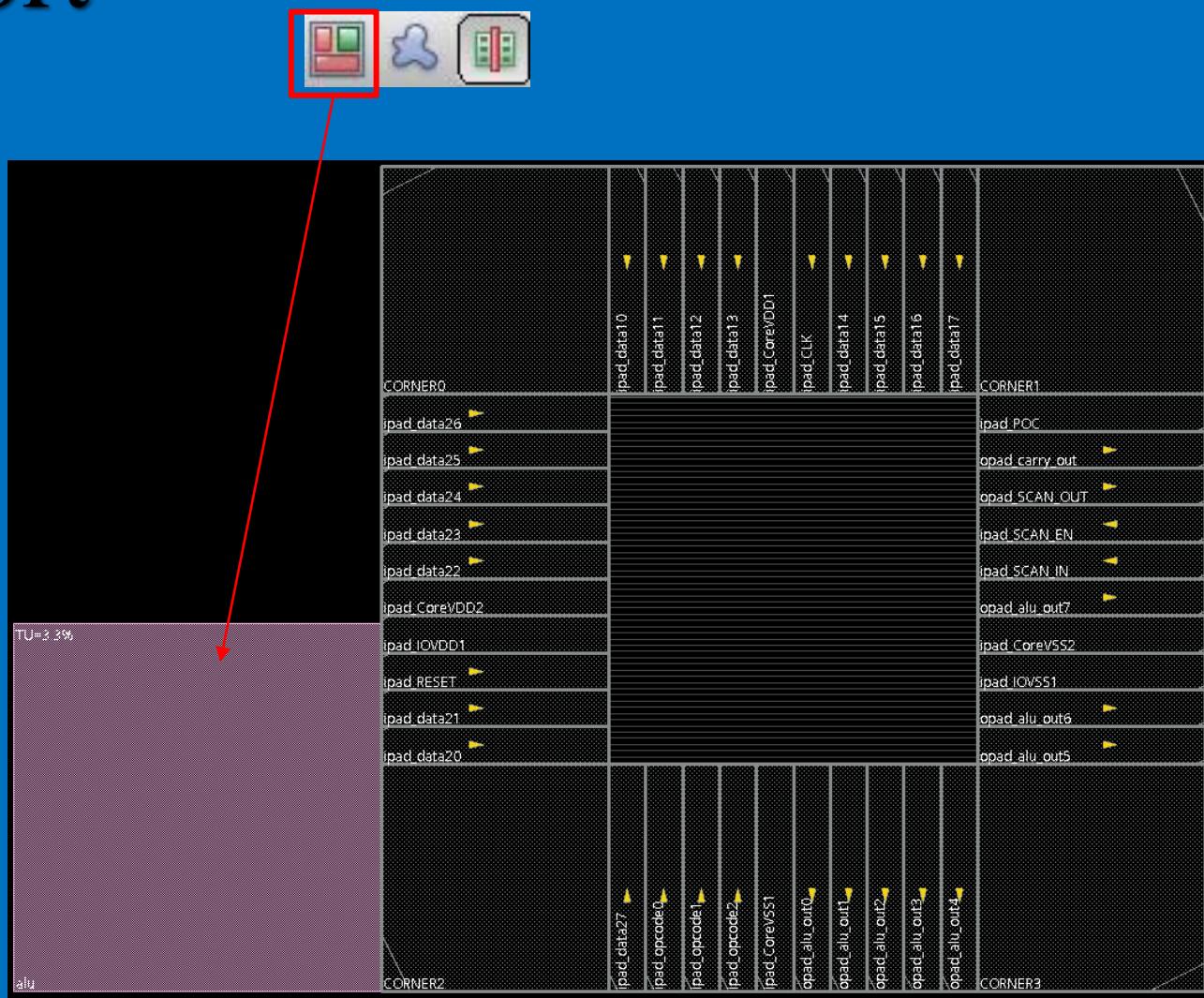


◆ 因為讀檔的設定繁雜，如果跟先前的設定一樣的話，可以load先前存的.conf檔(新版的為”.globals”)，就可以完成所有設定





# Import





# Global Net Connections

**Power** Place Optimize Clock

Connect Global Nets...  
Multiple Supply Voltage  
Power Planning  
Power Analysis

Global Net Connections

**Connection List**

VDD:PIN:\*,VDD:All 5

**Power Ground Connection**

**Connect**

- Pin 1
- Tie High
- Tie Low

Instance Basename: \*  
Pin Name(s): VDD 2

**Scope**

- Single Instance:
- Under Module:
- Under Power Domain:
- Under Region: llx: 0.0 lly: 0.0 urx: 0.0 3
- Apply All

To Global Net: VDD 4

Override prior connection

Verbose Output

**Add to List** 4

**Update**

**Apply**

**Check**

**Reset**

**Cancel**

**Help**

**Connection List**

VDD:PIN:\*,VDD:All  
VSS:PIN:\*,VSS:All 9

**Power Ground Connection**

**Connect**

- Pin 6
- Tie High
- Tie Low

Instance Basename: \*  
Pin Name(s): VSS 7

**Scope**

- Single Instance:
- Under Module:
- Under Power Domain:
- Under Region: llx: 0.0 lly: 0.0 urx: 0.0 ury: 0.0
- Apply All

To Global Net: VSS 8

Override prior connection

Verbose Output

**Add to List** 8

**Update**

**Delete**

**Apply**

**Check** 10

**Reset**

**Cancel**



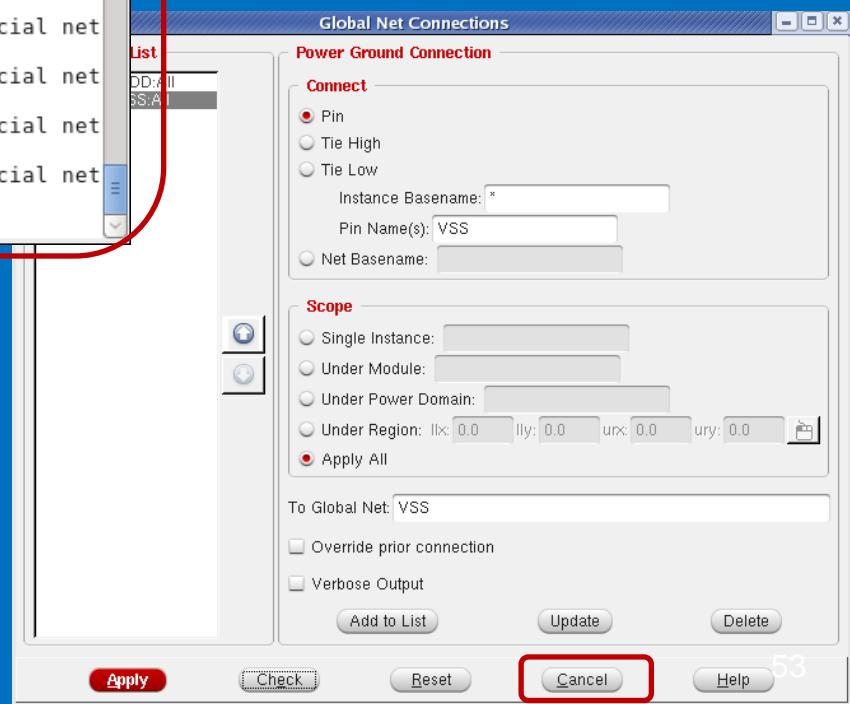
# Global Net Connections

```
t106368059@islabx7:SOC
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
WARNING TCLNL-330      2  set_input_delay on clock root '%s' is no...
WARNING TECHLIB-302     20 No function defined for cell '%s'. The c...
WARNING TECHLIB-436     20 Attribute '%s' on '%s' pin '%s' of cell ...
*** Message Summary: 1604 warning(s), 1 error(s)

innovus 1> QClipboard::setData: Cannot set X11 selection owner for CLIPBOARD
Warning: term SN of inst alu/alu_out_reg_0_ is not connect to global special net

Warning: term SN of inst alu/carry_out_reg is not connect to global special net.
Warning: term SN of inst alu/alu_out_reg_2_ is not connect to global special net

Warning: term SN of inst alu/alu_out_reg_4_ is not connect to global special net
Warning: term SN of inst alu/alu_out_reg_1_ is not connect to global special net
Warning: term SN of inst alu/alu_out_reg_6_ is not connect to global special net
Warning: term SN of inst alu/alu_out_reg_5_ is not connect to global special net
Warning: term SN of inst alu/alu_out_reg_3_ is not connect to global special net
Warning: term SN of inst alu/alu_out_reg_7_ is not connect to global special net
```



◆ 這些Warning訊息是說某些cell pin  
連到1'b1或1'b0，但還沒設定要怎麼  
連到Power或Ground，後面的步驟會加  
入Tie high/low解決



# Scan Chain

- ◆ 在Terminal 輸入下面兩行指令

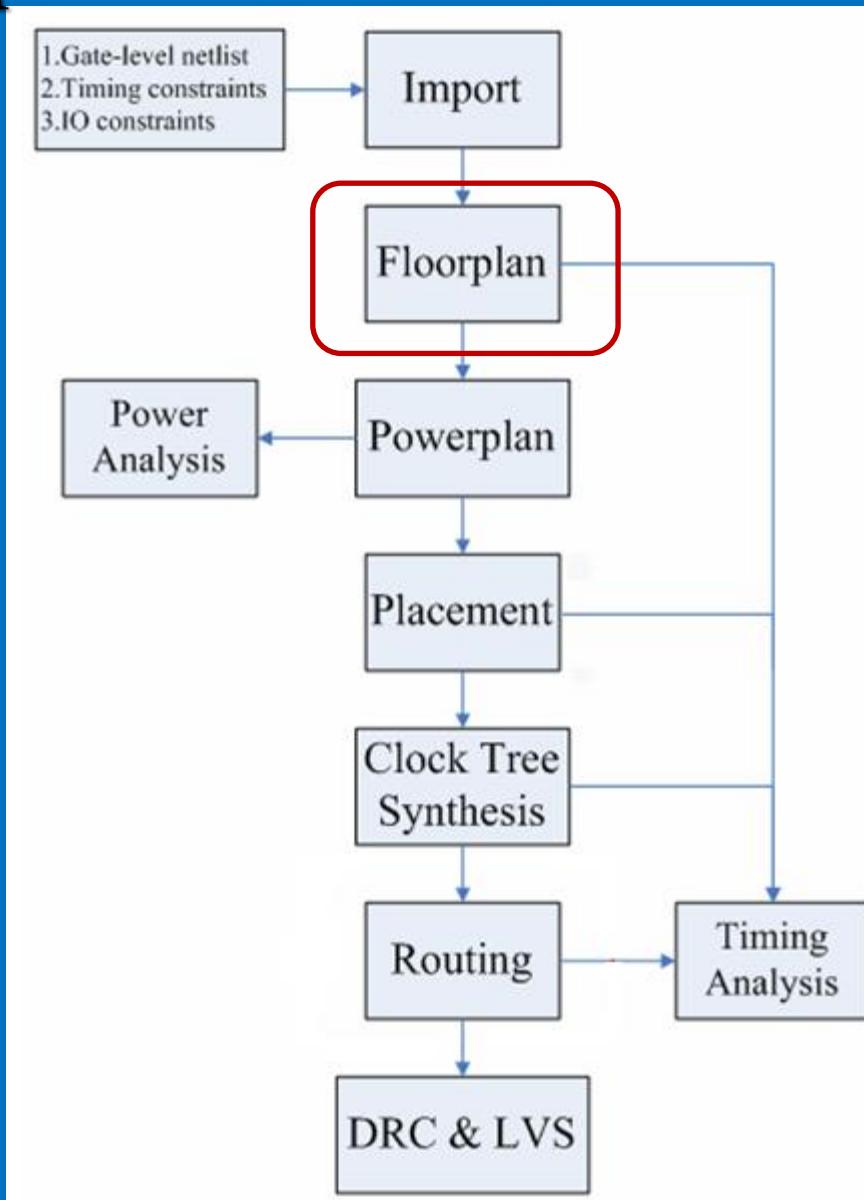
```
innovus > specifyScanChain scan1 -start ipad_SCAN_IN/C -stop  
opad_SCAN_OUT/I
```

```
innovus > scantrace
```

```
t106368059@islabx7:SOC  
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)  
specifyBlackBox specifyCellEdgeSpacing specifyCellEdgeType  
specifyCellPad specifyIIm specifyInstPad  
specifyJtag specifyLockupElement specifyNetWeight  
specifyPartition specifyScanCell specifyScanChain  
specifyScanChainPartition specifySelectiveBlkgGate specifySpareGate  
specify_lib specify_pg_keepout spefIn  
innovus 1> specify  
specifyBlackBox specifyCellEdgeSpacing specifyCellEdgeType  
specifyCellPad specifyIIm specifyInstPad  
specifyJtag specifyLockupElement specifyNetWeight  
specifyPartition specifyScanCell specifyScanChain  
specifyScanChainPartition specifySelectiveBlkgGate specifySpareGate  
specify_lib specify_pg_keepout  
innovus 1> specifySc  
specifyScanCell specifyScanChain specifyScanChainPartition  
innovus 1> specifyScancha  
specifyScanChain specifyScanChainPartition  
innovus 1> specifyScanChain scan1 -start ipad_SCAN_IN/C -stop opad_SCAN_OUT/I  
innovus 2> scantrace  
*** Scan Trace Summary (runtime: cpu: 0:00:00.0 , real: 0:00:00.0):  
Successfully traced 1 scan chain (total 9 scan bits).  
*** Scan Sanity Check Summary:  
*** 1 scan chain passed sanity check.  
innovus 3> ■
```

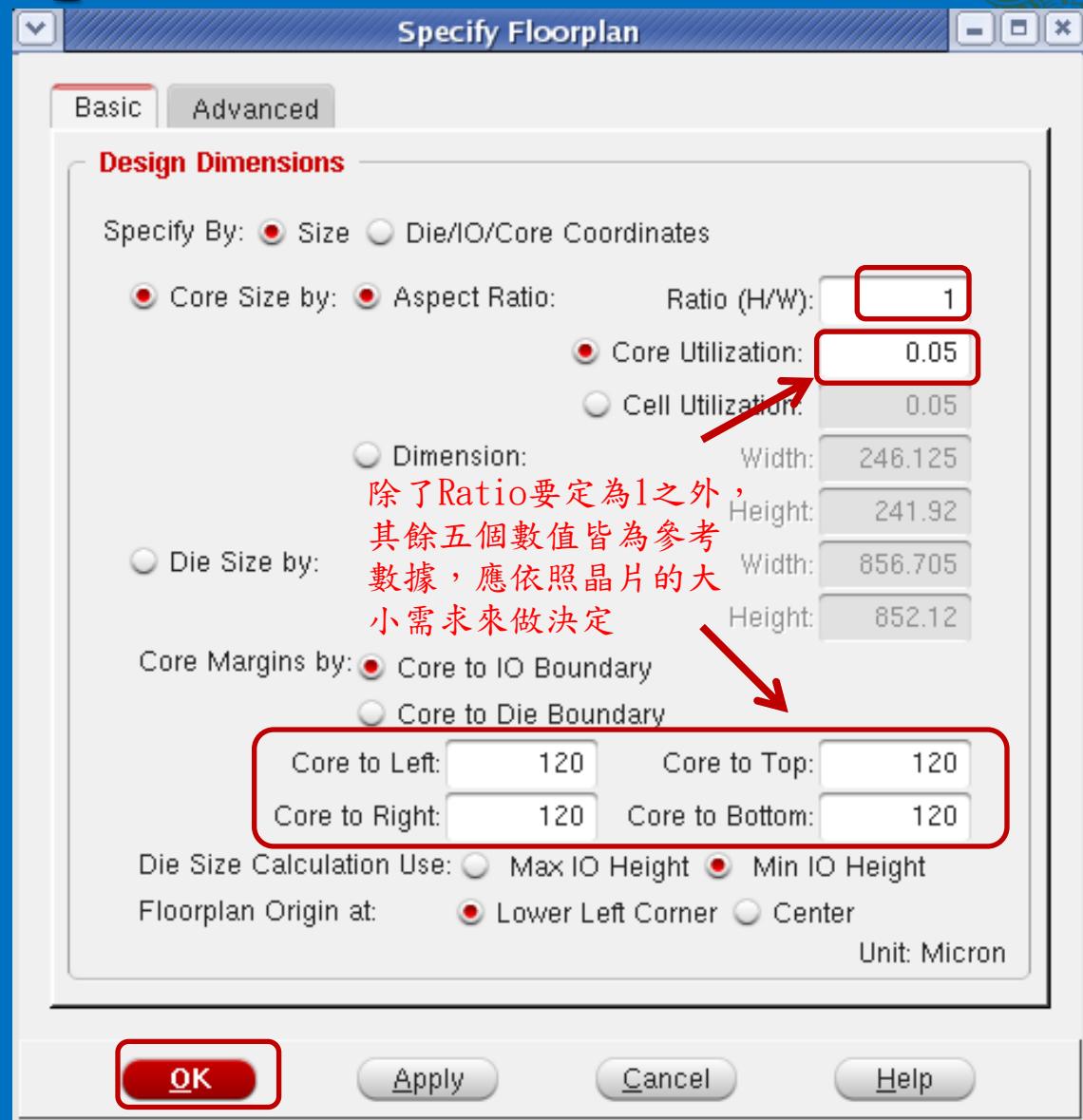
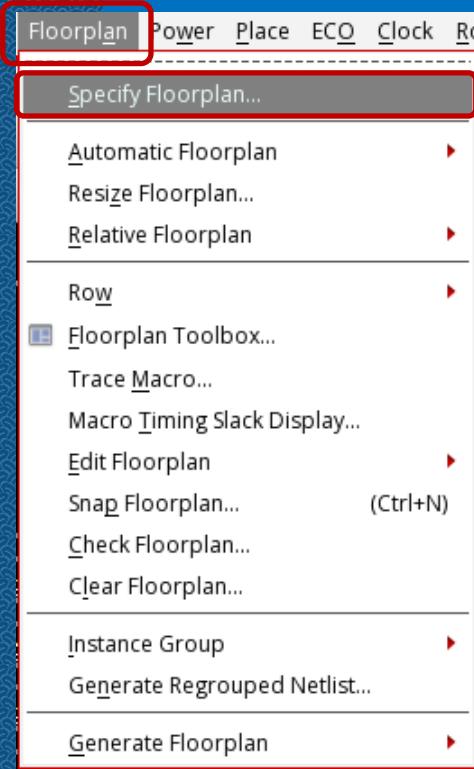


# Floorplan



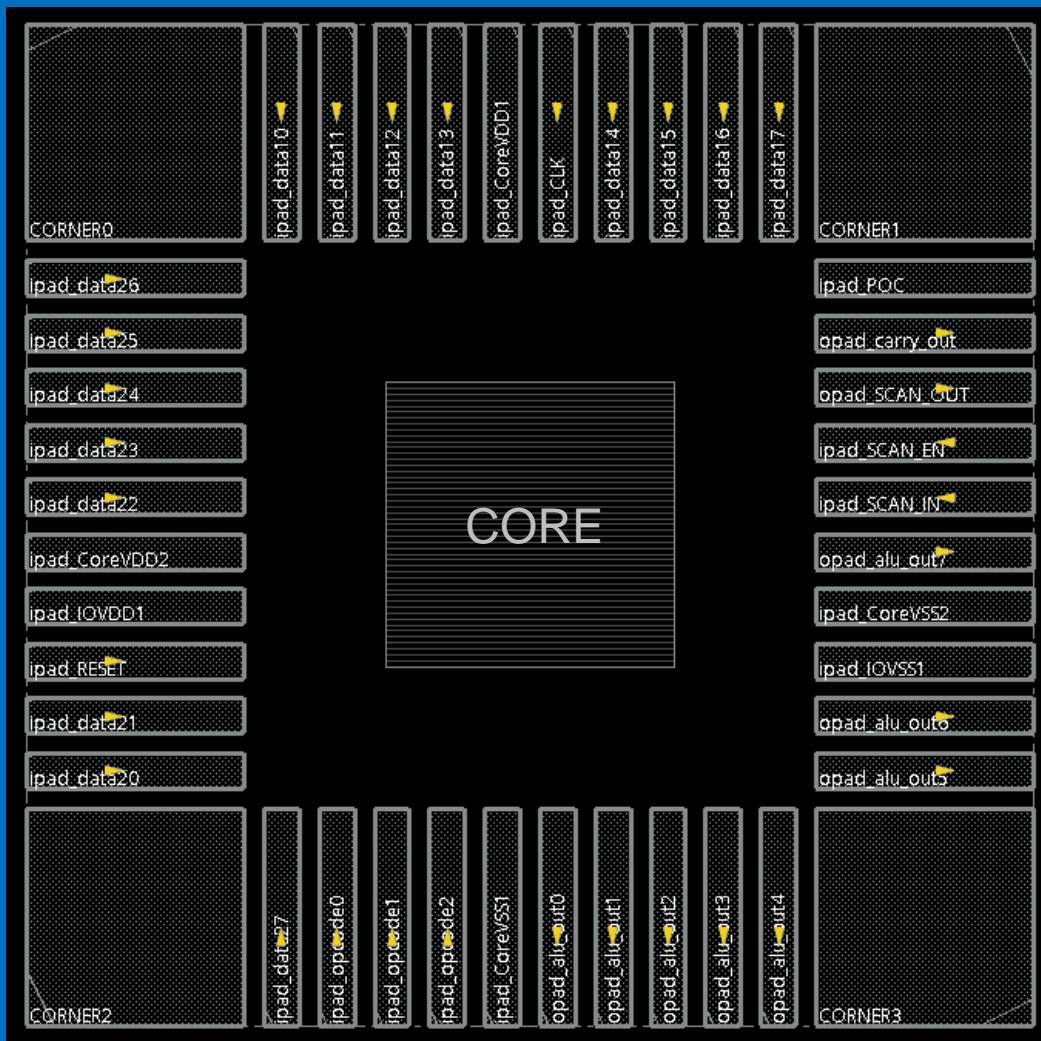


# Specify Floorplan



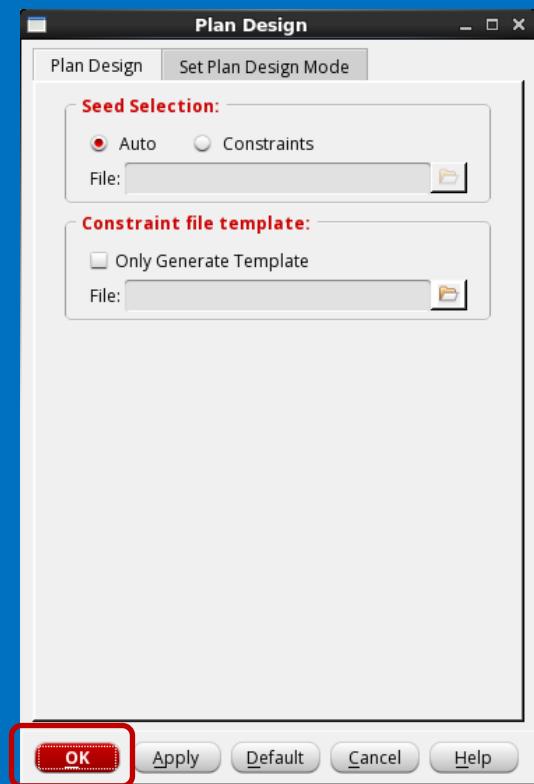
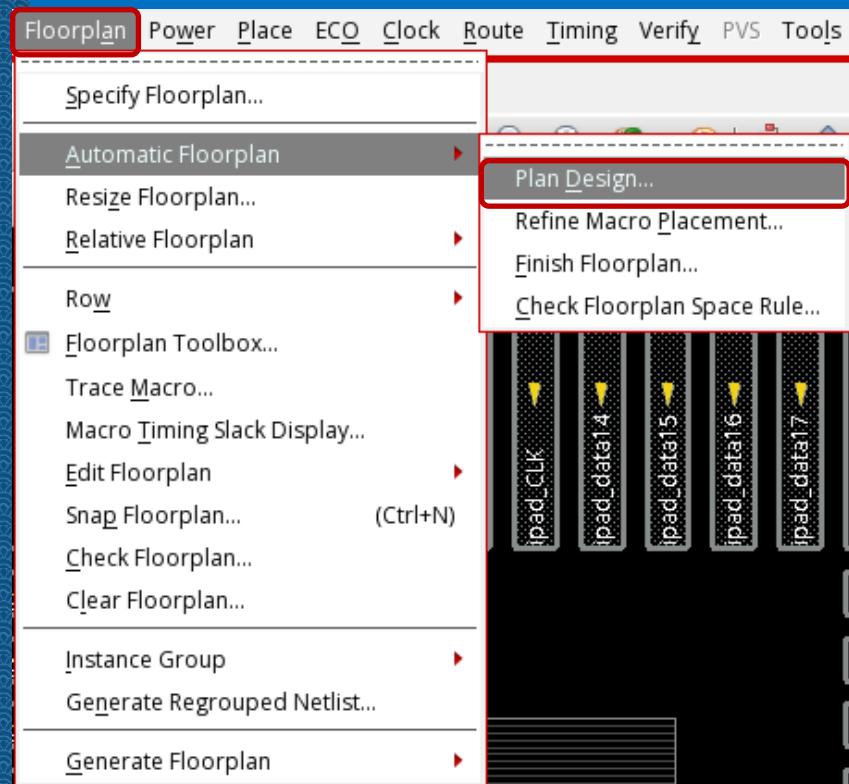


# Specify Floorplan

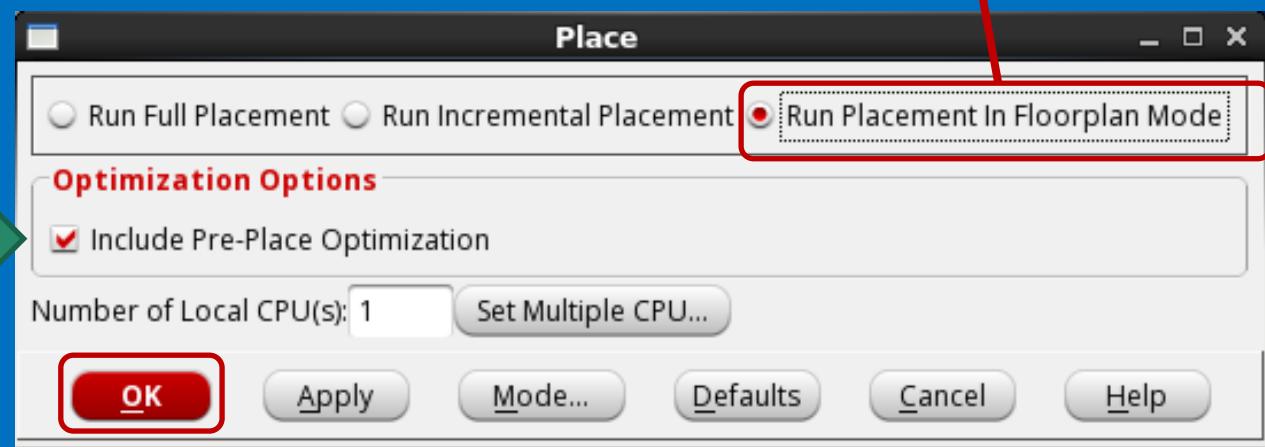
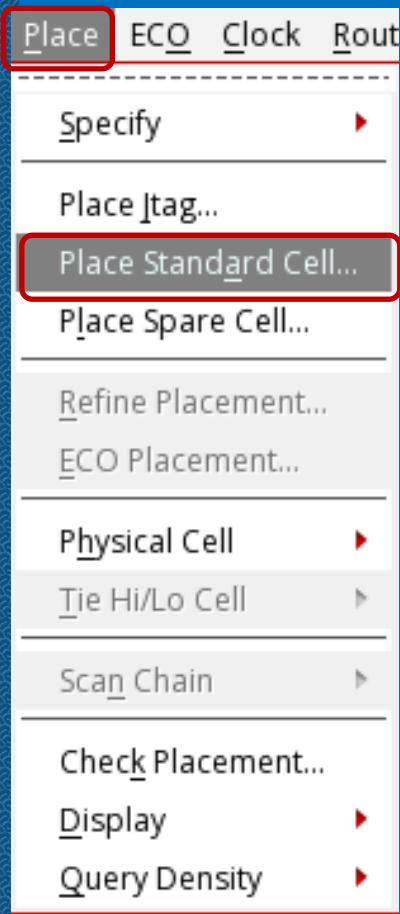




# Automatic Floorplan



# Run Placement in Floorplan Mode



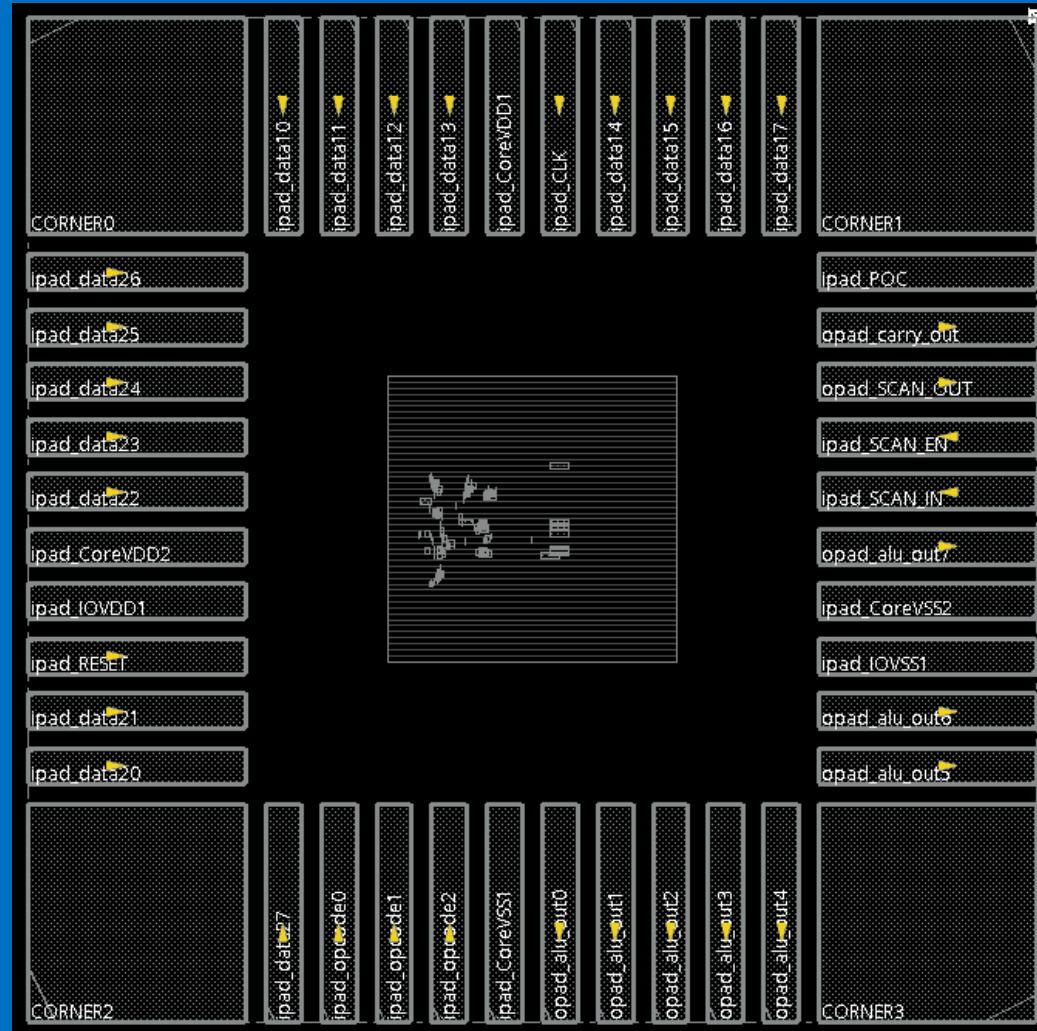
將cell做粗略擺放



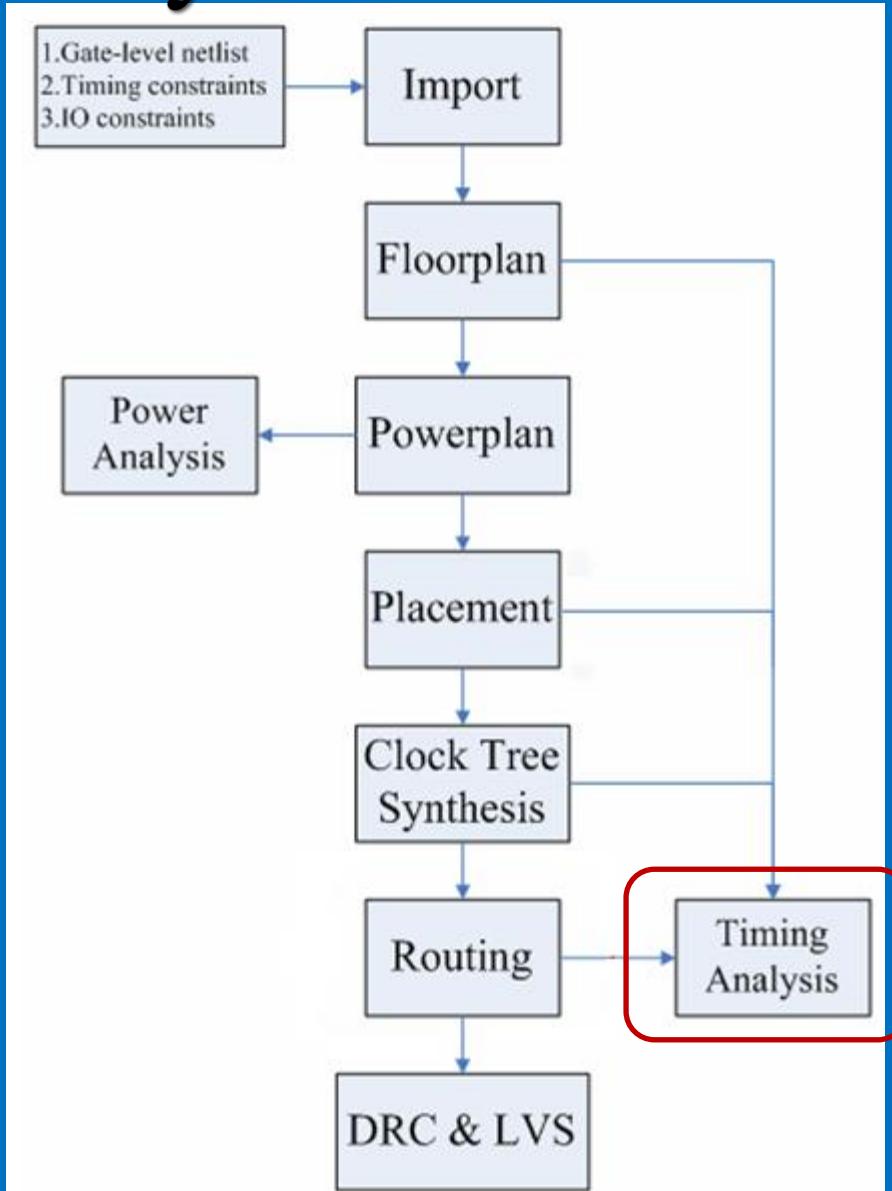
# Physical View



切換到Physical View，  
應該可以看到cell被  
擺進晶片內部



# Timing Analysis



# Timing Analysis



- ◆ 在Terminal 輸入下面指令

```
innovus > createBasicPathGroups -expanded
```

Setup mode	all	reg2reg	default
WNS (ns):	-0.068	4.205	-0.068
TNS (ns):	-0.068	0.000	-0.068
Violating Paths:	0	1	
All Paths:	36	8	28

DRVs	Real		Total	
	Nr nets(terms)	Worst Vio	Nr nets(terms)	
max_cap	0 (0)	0.000	0 (0)	
max_tran	0 (0)	0.000	21 (21)	
max_fanout	0 (0)	0	21 (21)	
max_length	0 (0)	0	0 (0)	

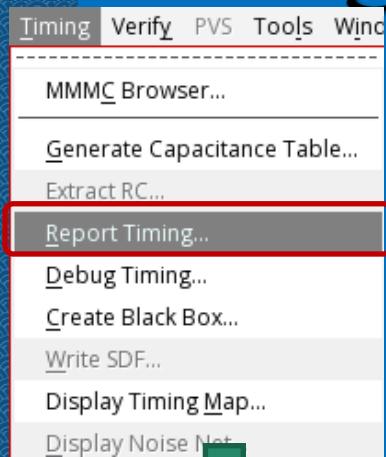
Setup mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	0.012	4.241	0.012	0.438	N/A	0.000
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	N/A	0
All Paths:	36	8	19	9	N/A	0

- ◆ 因為Innovus預設Report Timing顯示的項目不完整，因此需要先下指令增加所需參數項目。

延遲0.068ns

經最佳化後提前0.012ns就已經將資料ready

# Timing Analysis

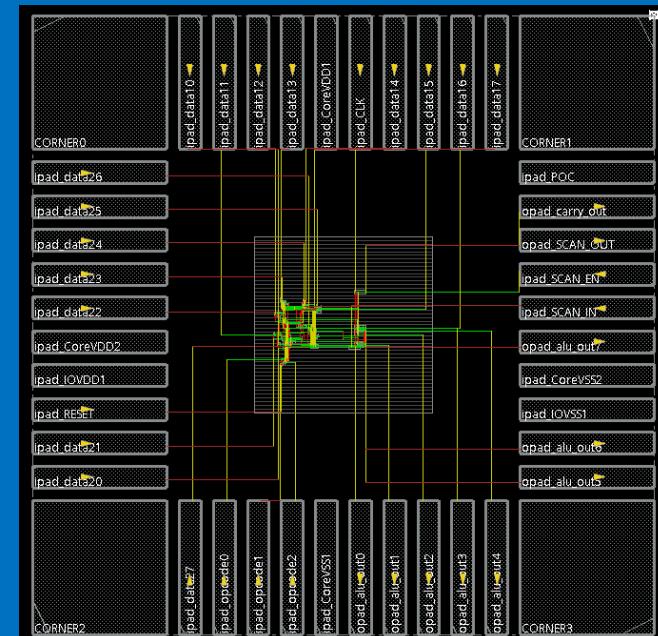
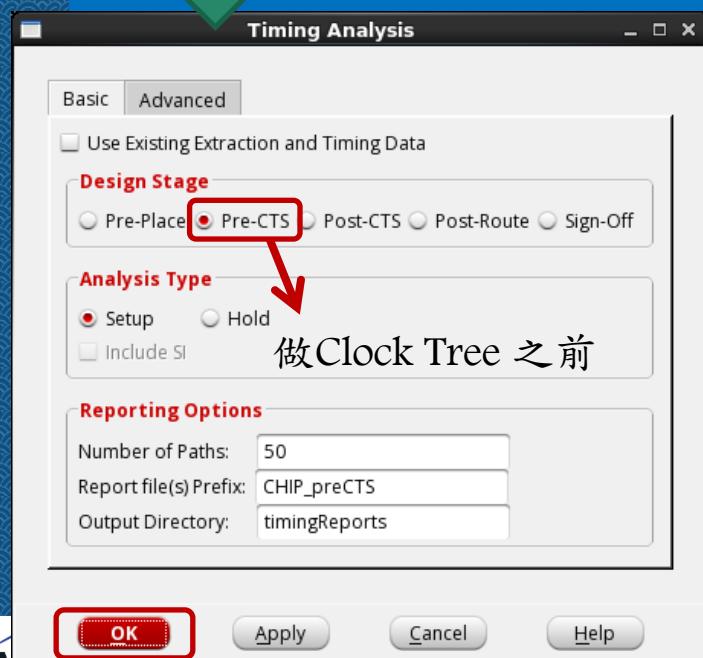


t106368059@islabx7:SOC

檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)

Setup views included:  
av\_func\_mode\_max

Setup mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	0.012	4.241	0.012	0.438	N/A	0.000
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	N/A	0
All Paths:	36	8	19	9	N/A	0



呼叫Trial Route

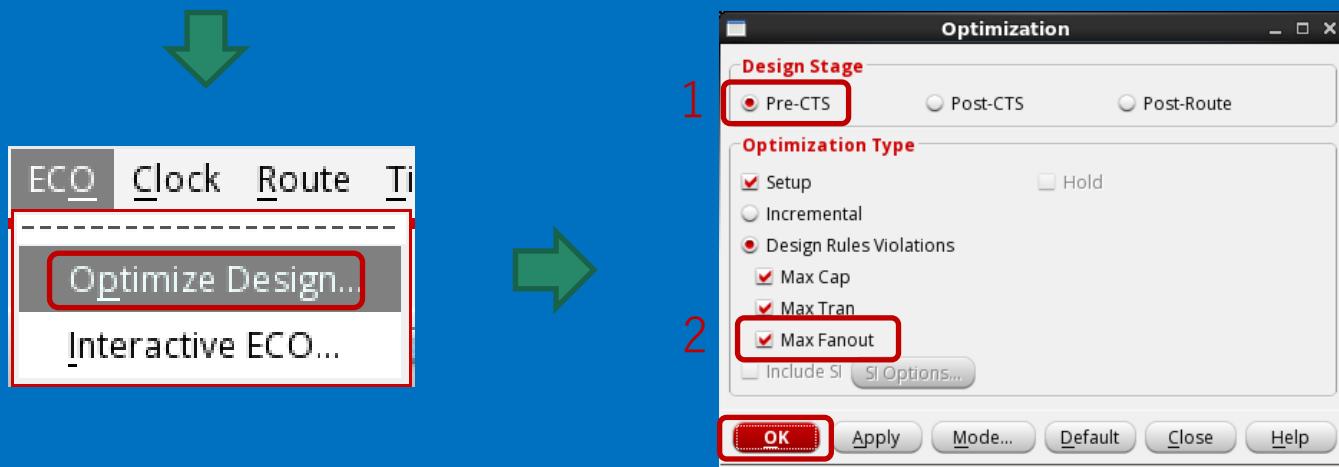


# Timing Optimization

先在終端機輸入以下指令

**setPlaceMode -place\_design\_floorplan\_mode false**

```
innovus 1>
innovus 1> setPlaceMode -place_design_floorplan_mode false
innovus 2> █
```

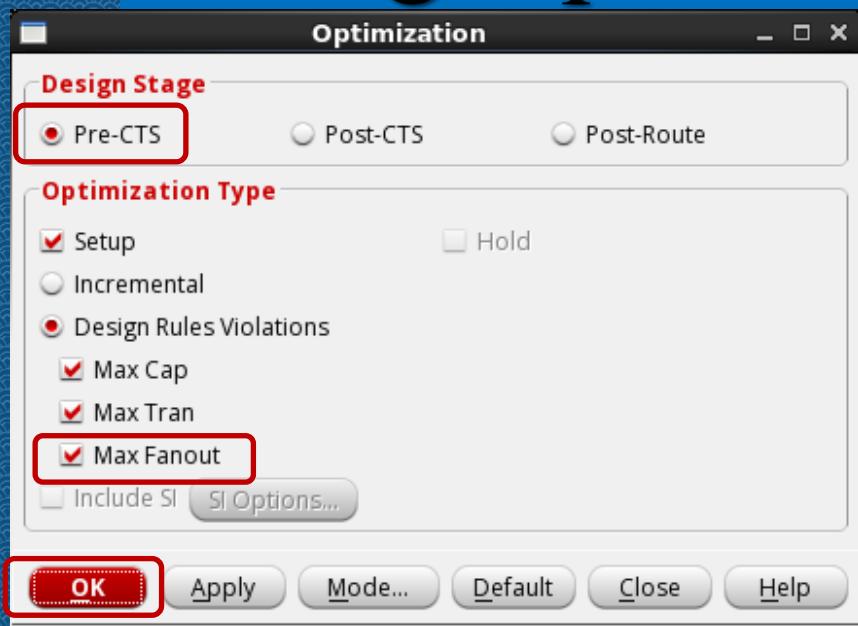


3

(做完的結果請參考下一頁ppt)



# Timing Optimization



t106368059@islabx7:SOC

檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)

Setup views included:  
av\_func\_mode\_max

Setup mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	0.007	4.233	0.007	0.494	N/A	0.000
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	N/A	0
All Paths:	36	8	19	9	N/A	0

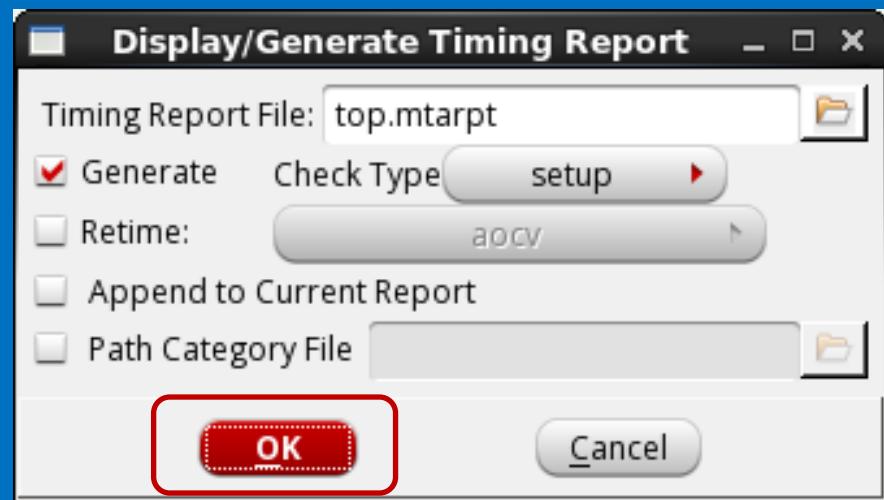
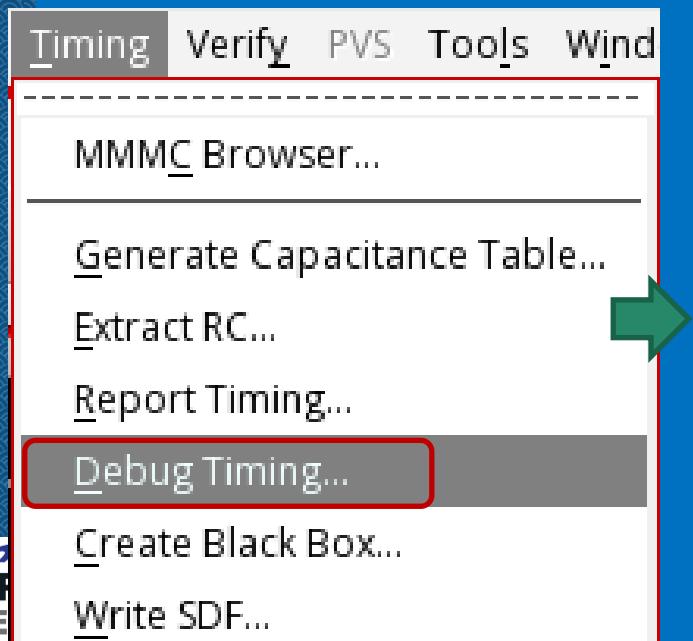
- ◆ 如果最佳化後Slack還是沒有變為正數，可再做二至三次直到無法再修正為止，此時如果Slack還是負數，則將進行下頁投影片所介紹的Timing分析，知道哪裡的Delay最為嚴重，並回去修改合成步驟或是verilog code



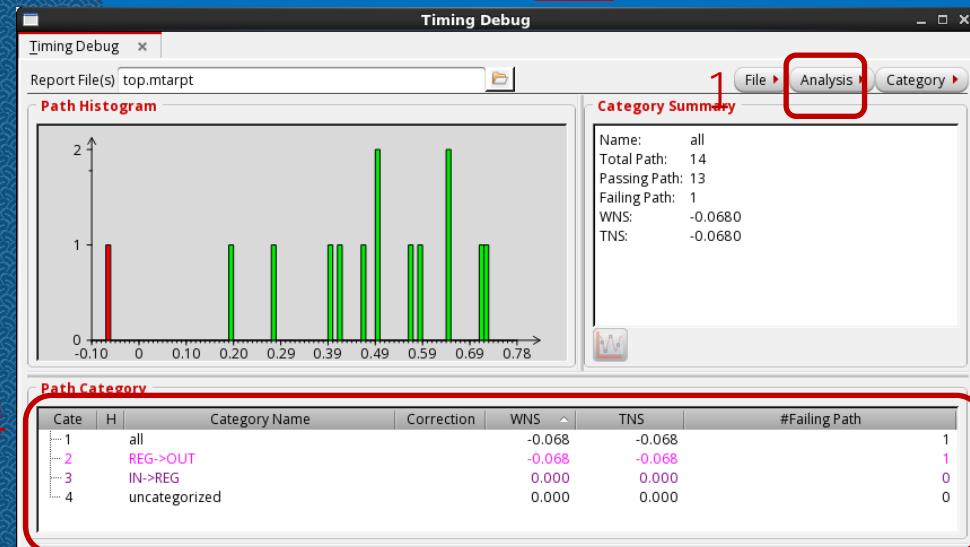
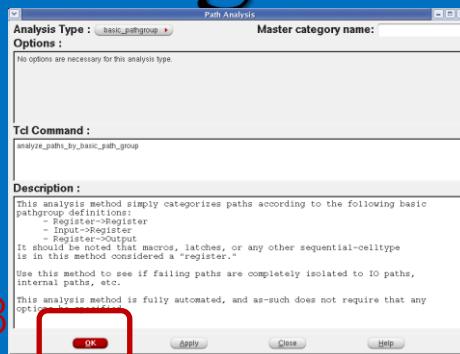
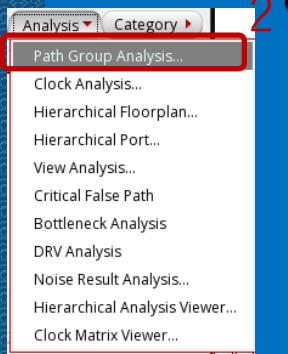
# Debug timing

Setup views included: av_func_mode_max						
Setup mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	-0.043	4.235	-0.043	0.363	N/A	0.000
TNS (ns):	-0.043	0.000	-0.043	0.000	N/A	0.000
Violating Paths:	1	0	1	0	N/A	0
All Paths:	36	8	19	9	N/A	0

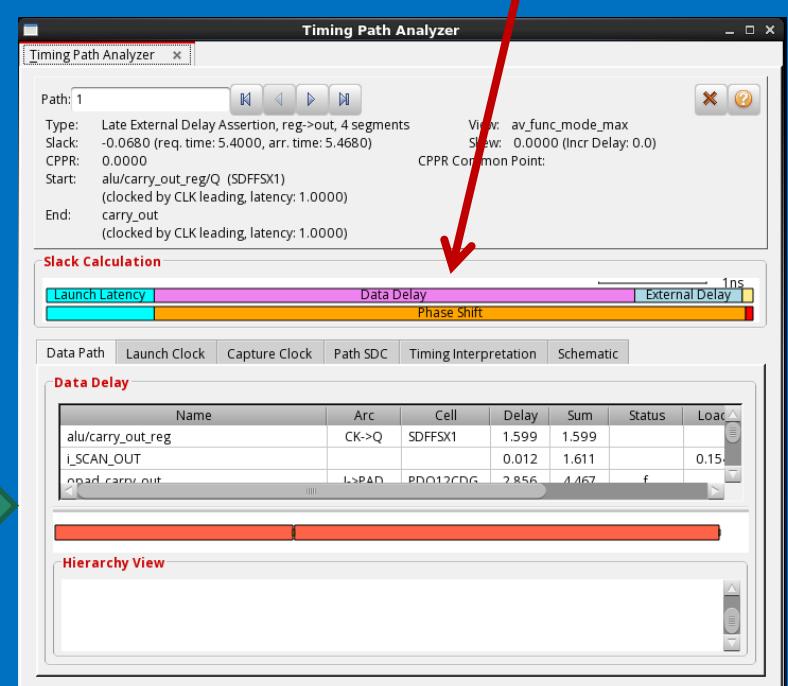
◆ 當Slack為負且無法再利用最佳化修正時，此時使用Debug Timing來尋找Delay嚴重的Path，分析並解決Timing的問題



# Debug timing



5 Double click



# Debug timing

◆ 這次實習最佳化後Slack應該都會是正的，當Slack為都為正時，此時Path Histogram就不會有紅色的Failing path存在，如此圖所示

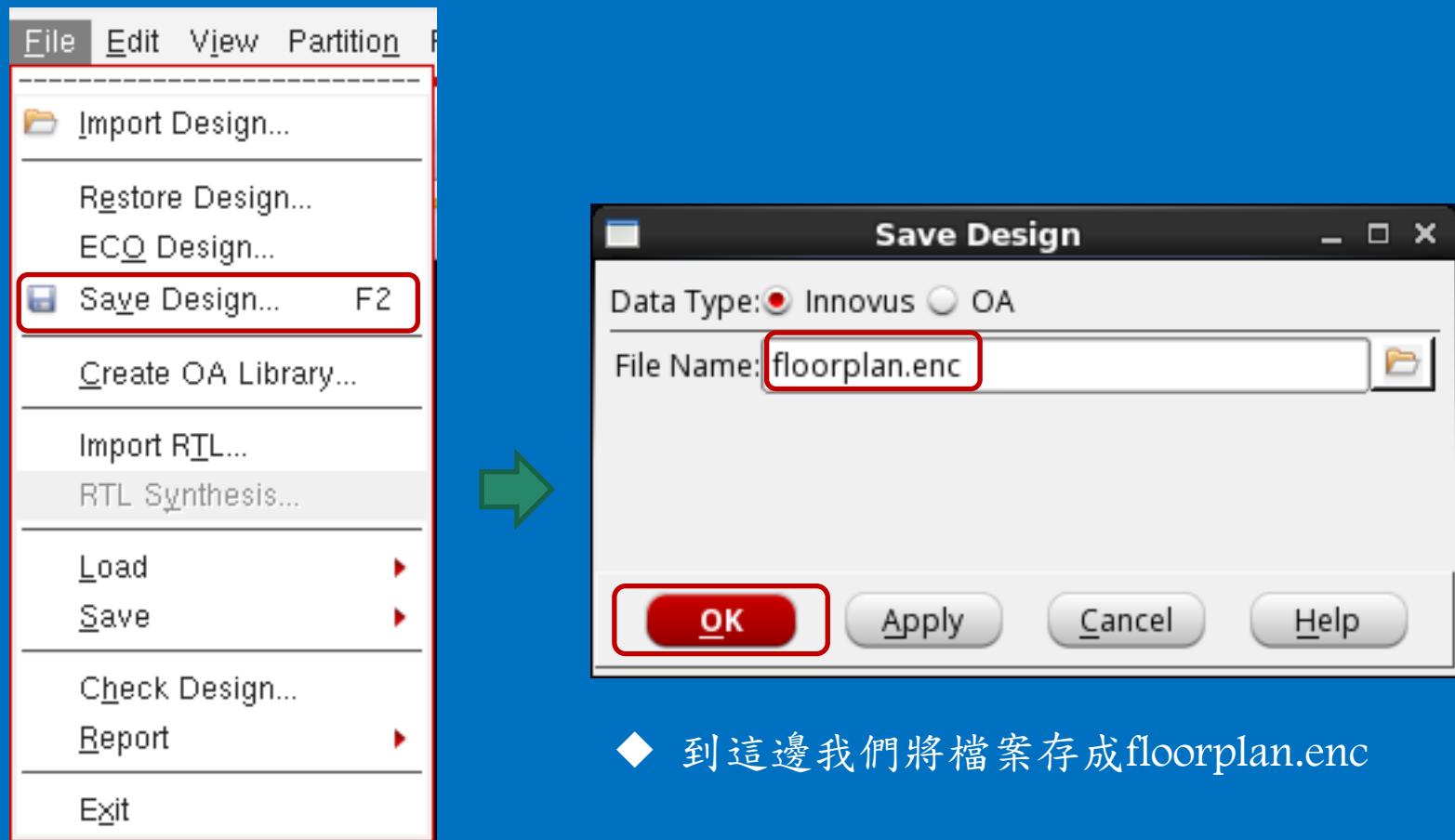
The screenshot illustrates the workflow for debugging timing in a digital design tool. It starts with a menu bar containing Timing, Verify, PVS, Tools, and Wind. The Tools menu is open, showing options like MMMC Browser..., Generate Capacitance Table..., Extract RC..., Report Timing..., Debug Timing... (which is highlighted with a red box), Create Black Box..., and Write SDF... . A large green arrow points downwards from this menu to a 'Display/Generate Timing Report' dialog. This dialog has a 'Timing Report File' field set to 'top.mtarpt', a checked 'Generate' checkbox, a 'Check Type' dropdown set to 'setup', and an 'OK' button (which is also highlighted with a red box). A second green arrow points from this dialog to a 'Timing Debug' window. The 'Timing Debug' window displays a 'Path Histogram' with green bars, a 'Category Summary' table, and a 'Path List' table. The 'Category Summary' table shows the following data:

Name:	all
Total Path:	14
Passing Path:	14
Failing Path:	0
WNS:	0.0000
TNS:	0.0000

A red box highlights the entire 'Category Summary' table. Below the table, a tooltip provides the same information: Category: all, Total Path: 14, Passing Path: 14, Failing Path: 0, WNS: 0.0000, TNS: 0.0000, and Norm. Delay: 0.9177.



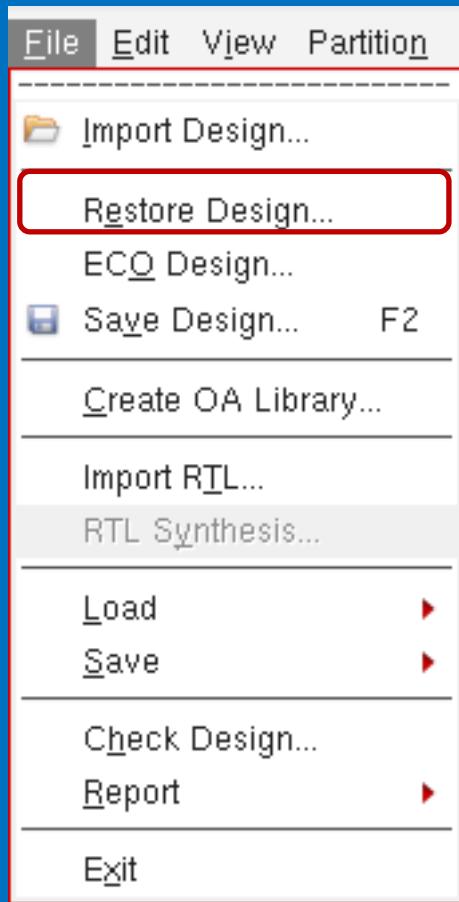
# Save Design



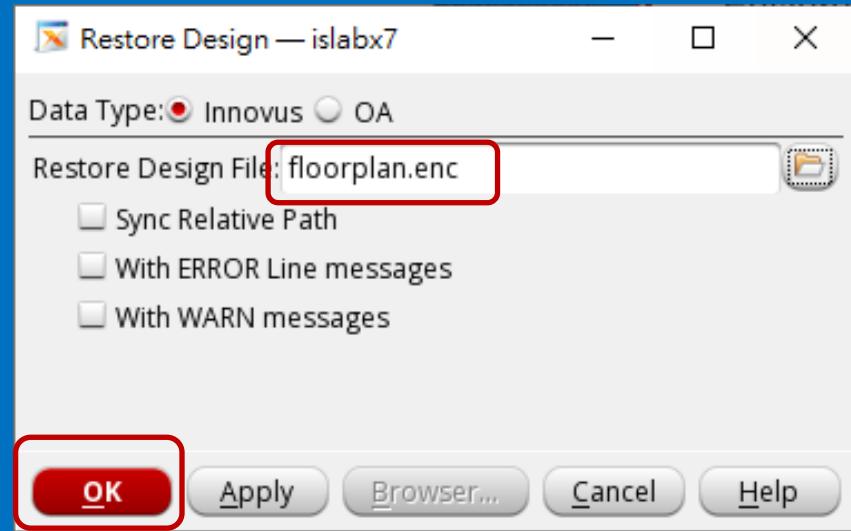
◆ 到這邊我們將檔案存成floorplan.enc



# Restore Design

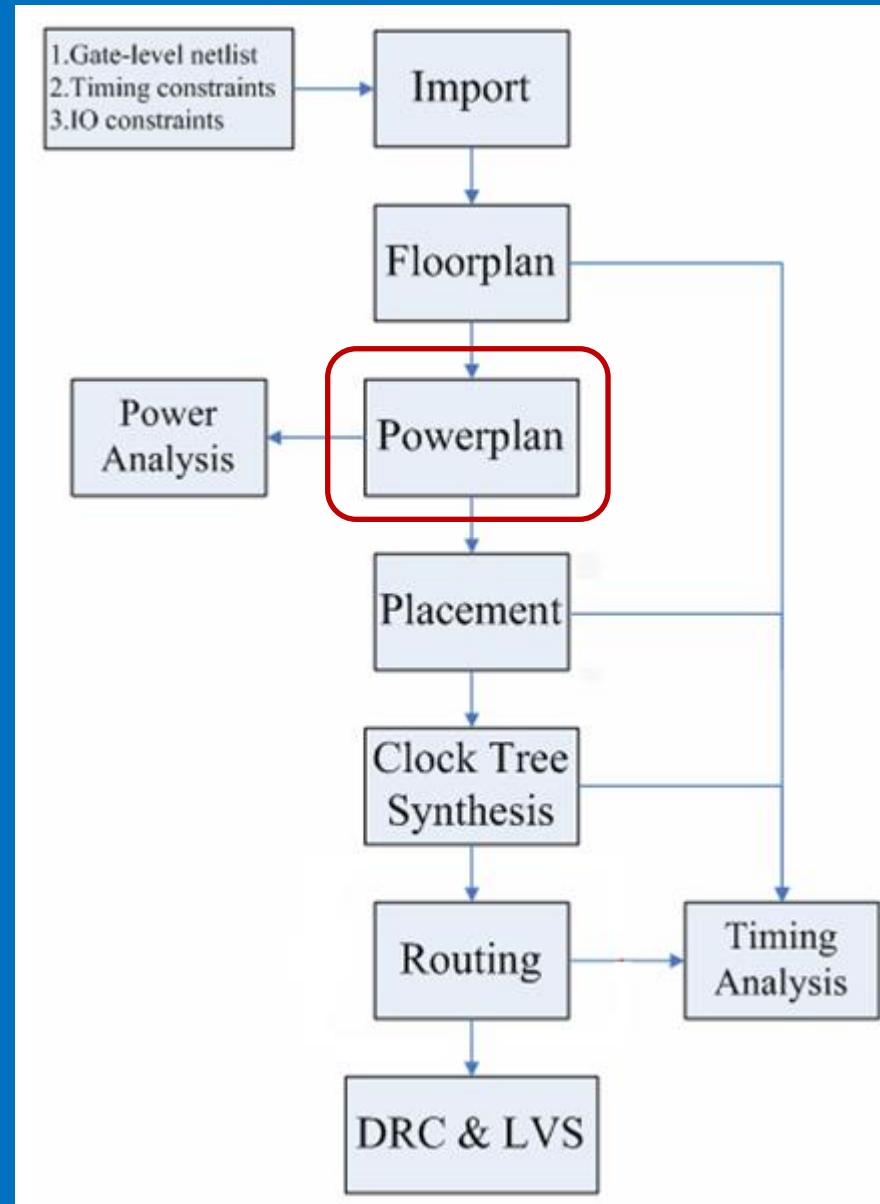


- ◆ 如果下次使用要載進之前的進度(例如: floorplan.enc)
- ◆ File>Restore Design





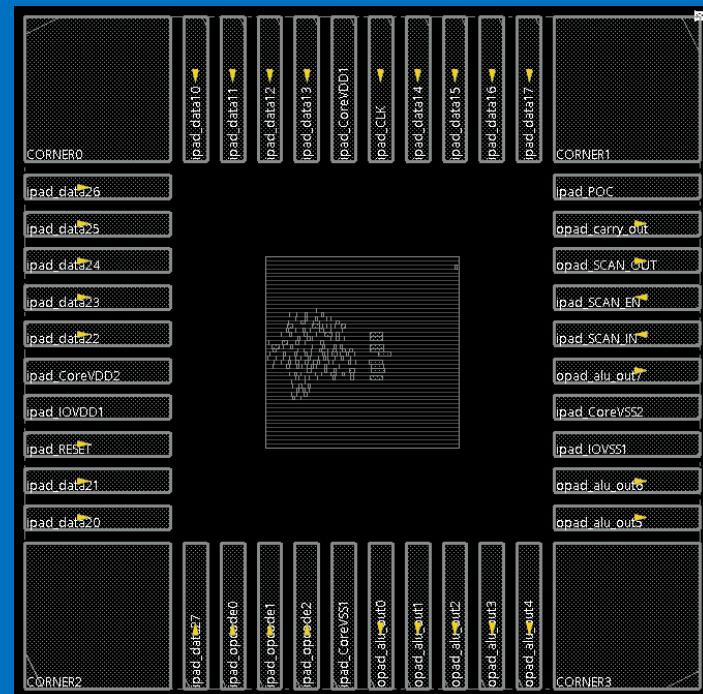
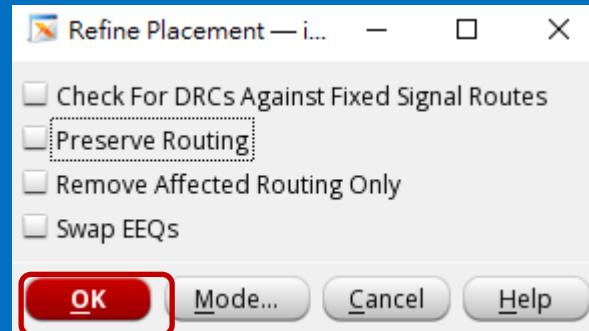
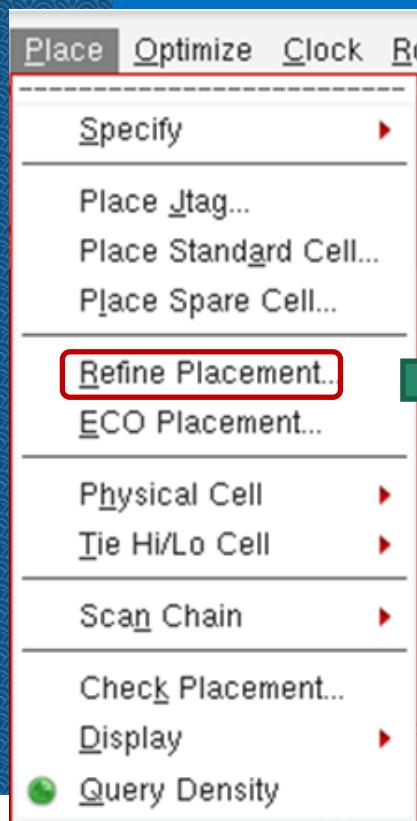
# Powerplan





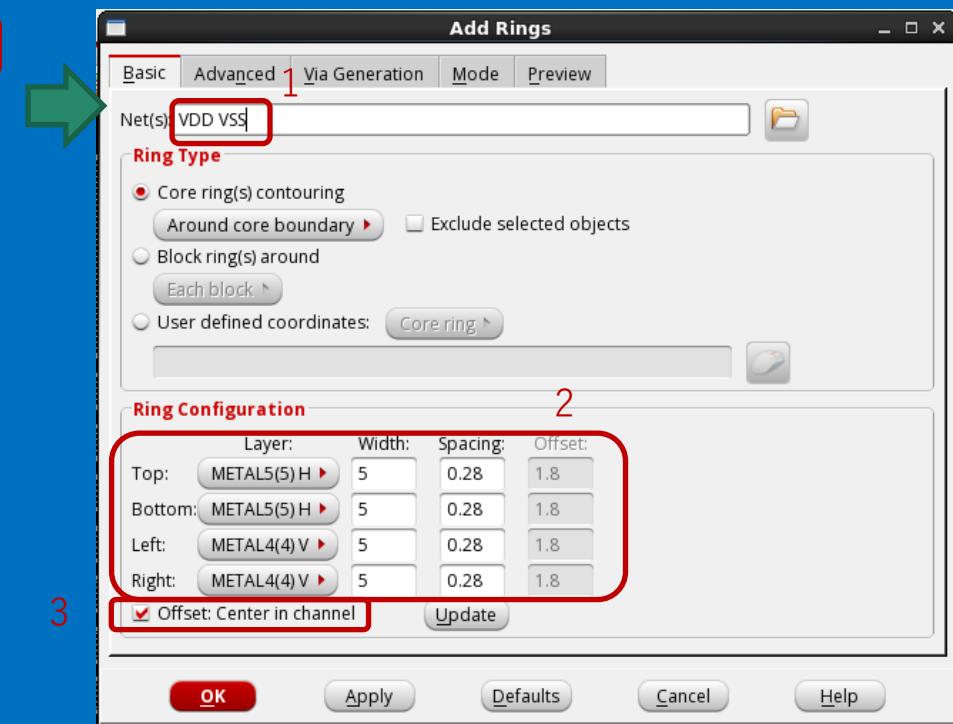
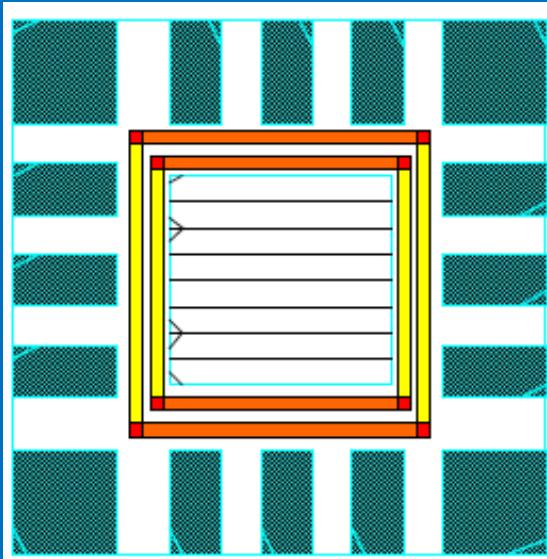
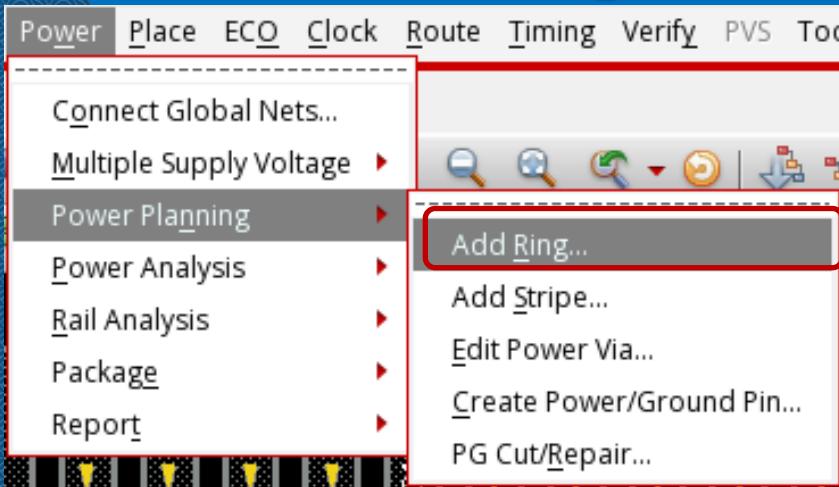
# Refine Placement

- ◆ 因為我們在分析Timing時，Innovus會呼叫Trial Route幫我們繞線來做Timing分析，此時因為要架設Power，我們必須將剛剛所呼叫的繞線拿掉，以免產生錯誤



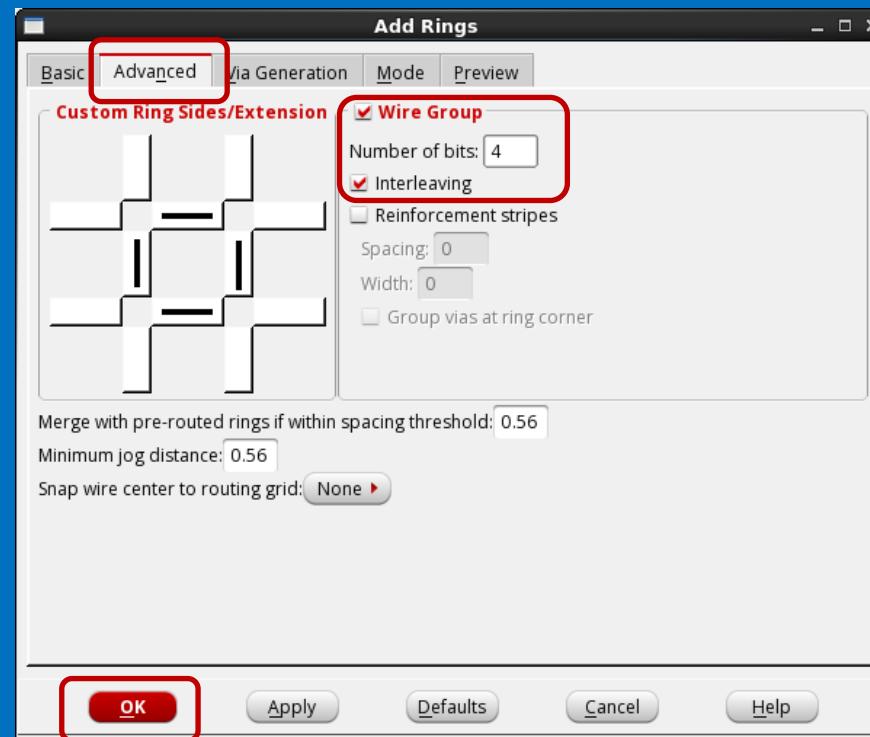


# Power Ring





# Power Ring





# Power Ring

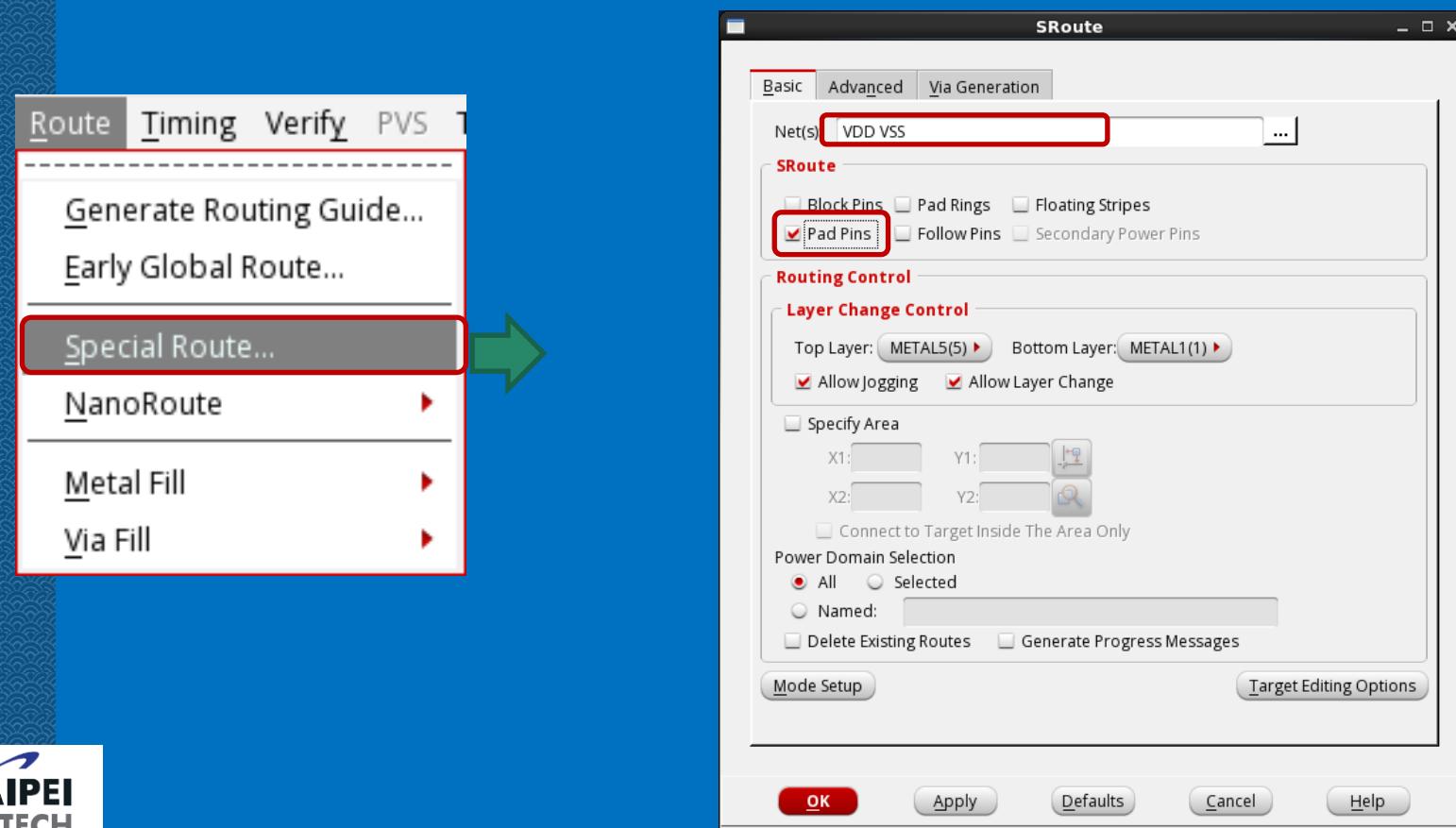
- ◆ 可以看到我們將Power ring架設上去了，上下為METAL5，左右為METAL4，且採交錯式的排列





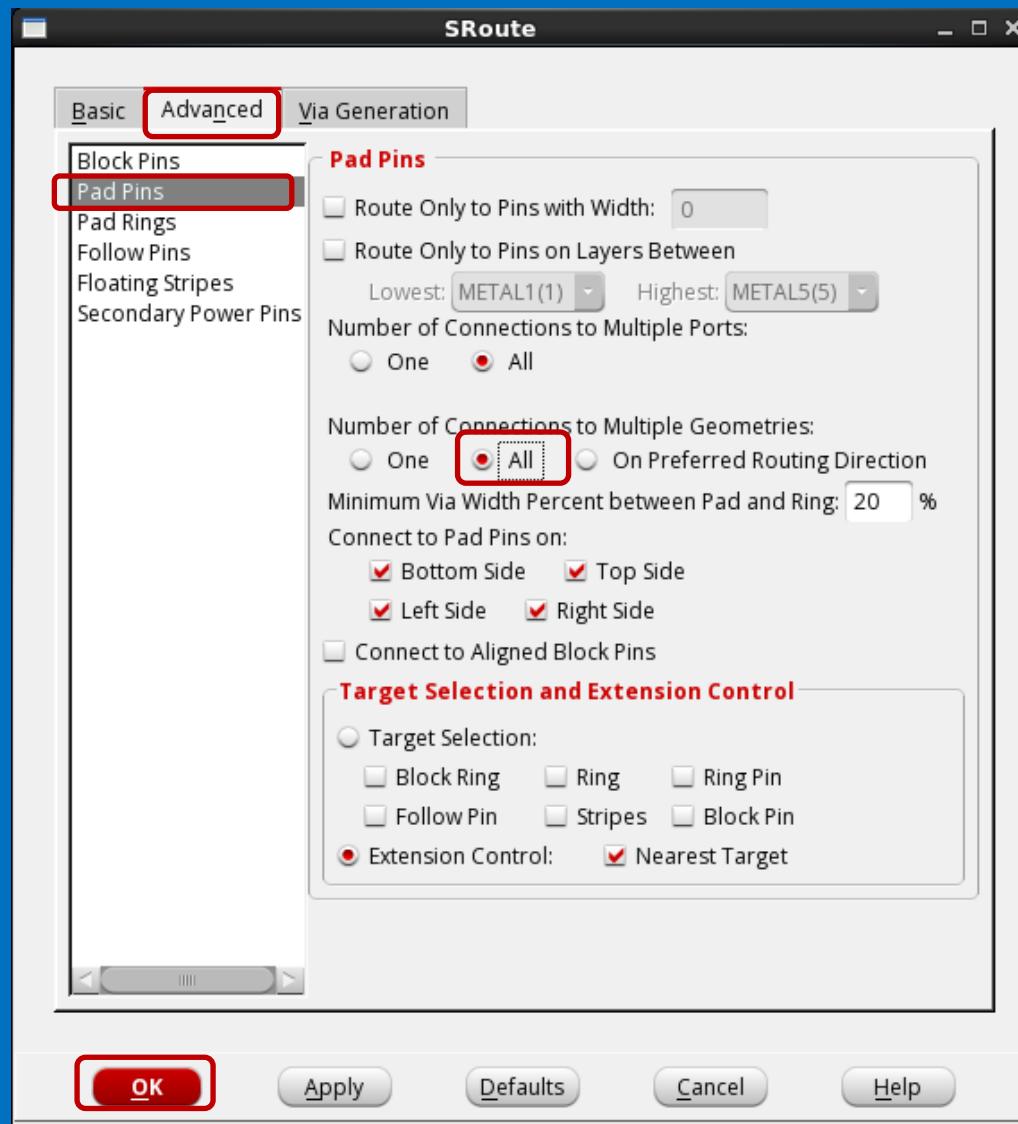
# Pad Pins

- ◆ 執行 Route → Special Route..., 在 Net(s) 欄位只留下 VDD VSS, Route 部分只留下 Pad pins 部分, 其它 Block pins/Pad rings / Follow Pins 都設成不選取, 切換頁面至 Advanced





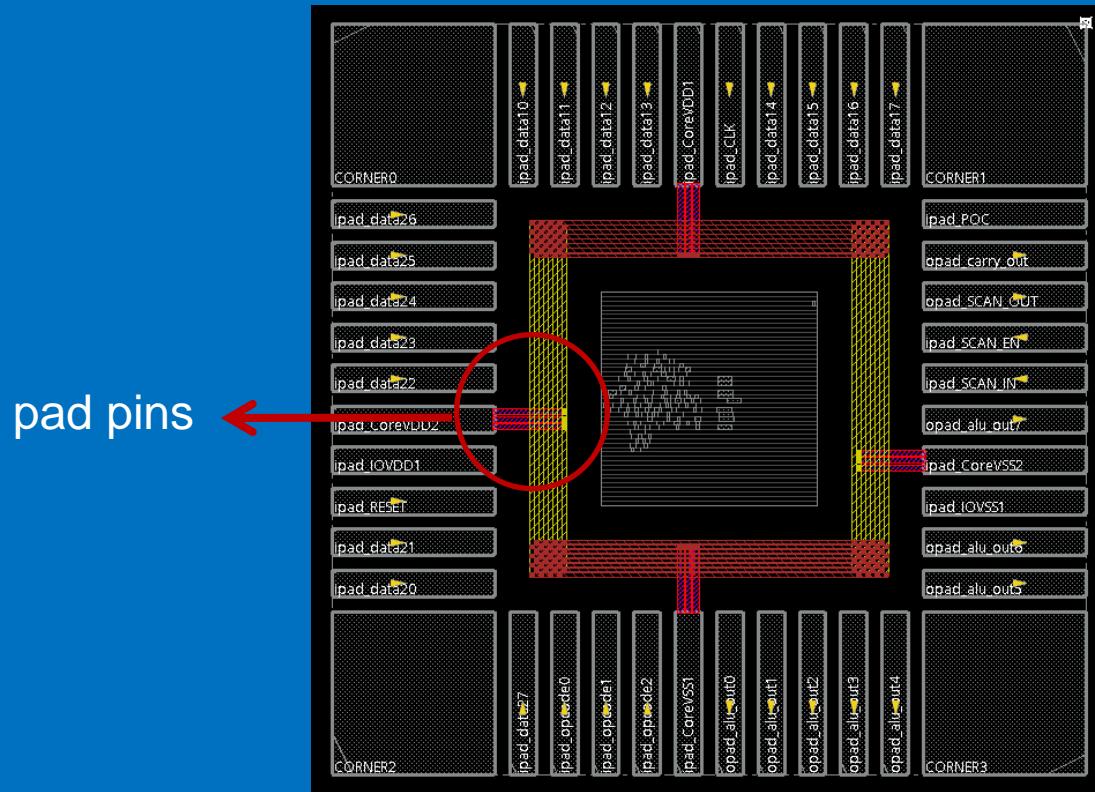
# Pad Pins





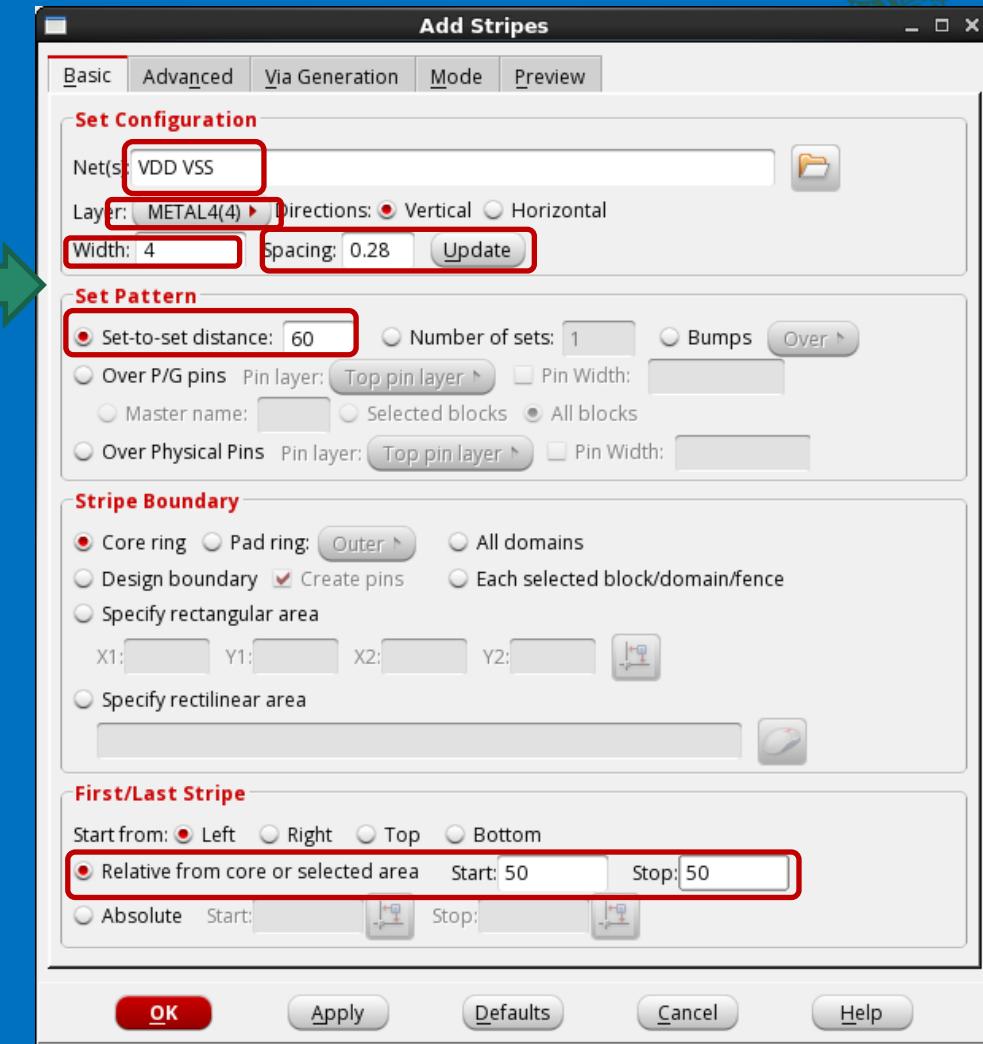
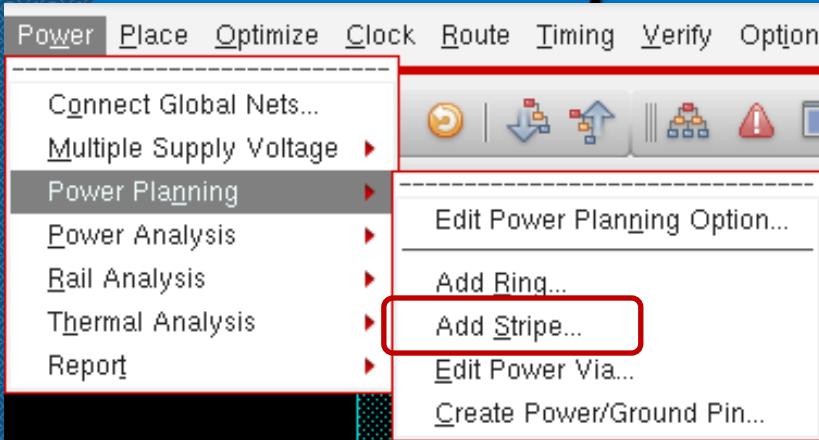
# Pad Pins

- ◆ 應該可看到四條pad pins從power pad連到power ring上
- ◆ You can save design again and set the file name is powerplan.enc





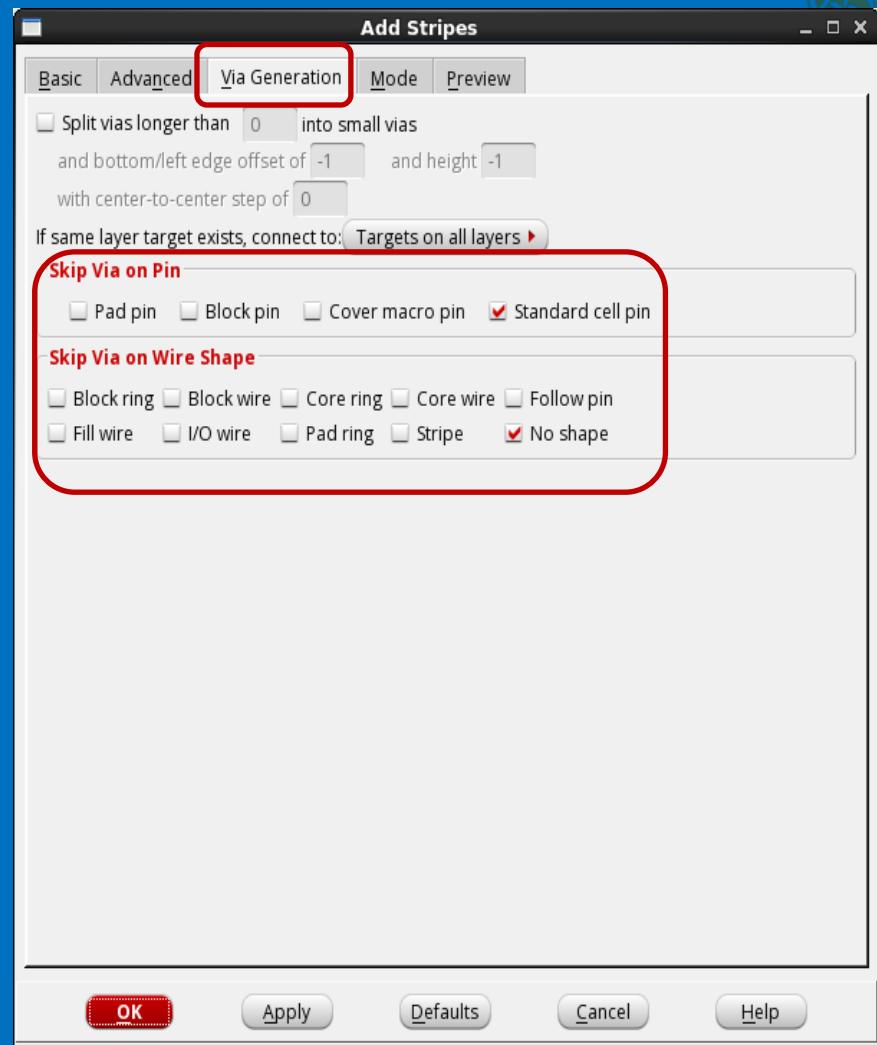
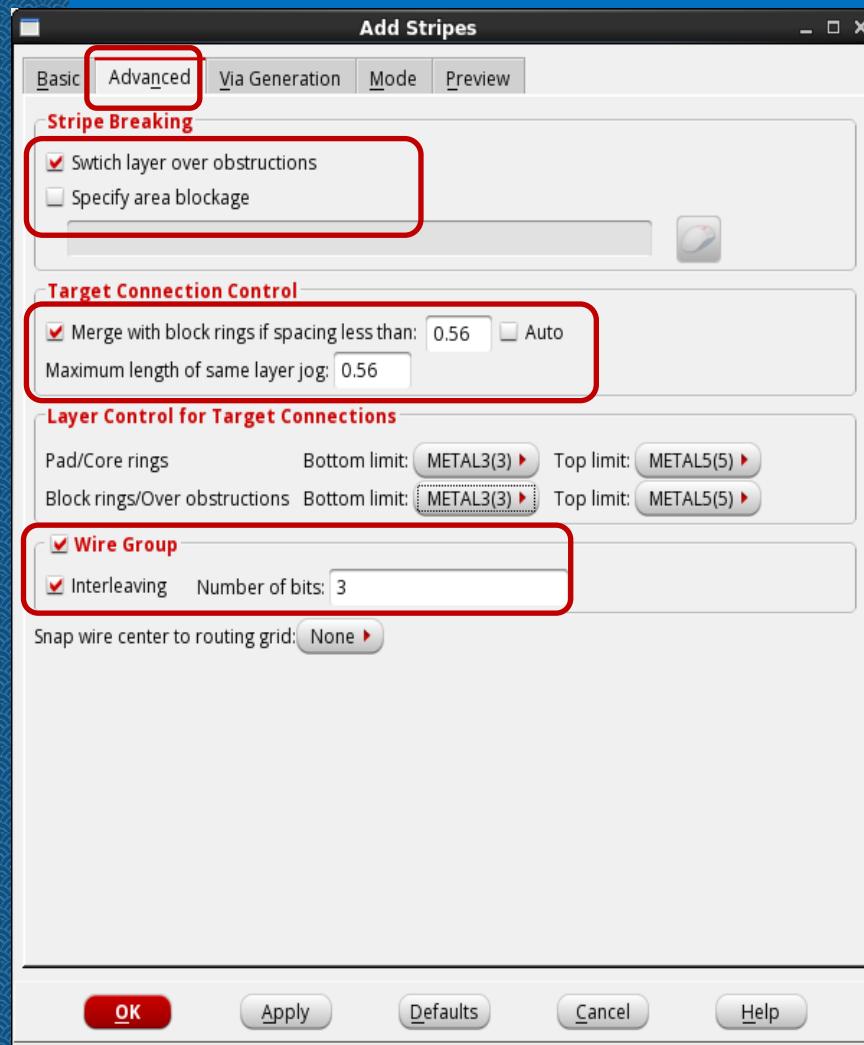
# Power Stripe



- ◆ 執行 Power → Power Planning → Add Stripes... , Net(s) 填入 VDD VSS , Layer 選 METAL4 , Width 設成 4 , 選擇 Sets-to-set distance , 並把 Set-to-set distance 設成 60 , X from left 設成 50 , X form right 設成 50 , 接著切換到 Advanced 和 Via Generation 做設定

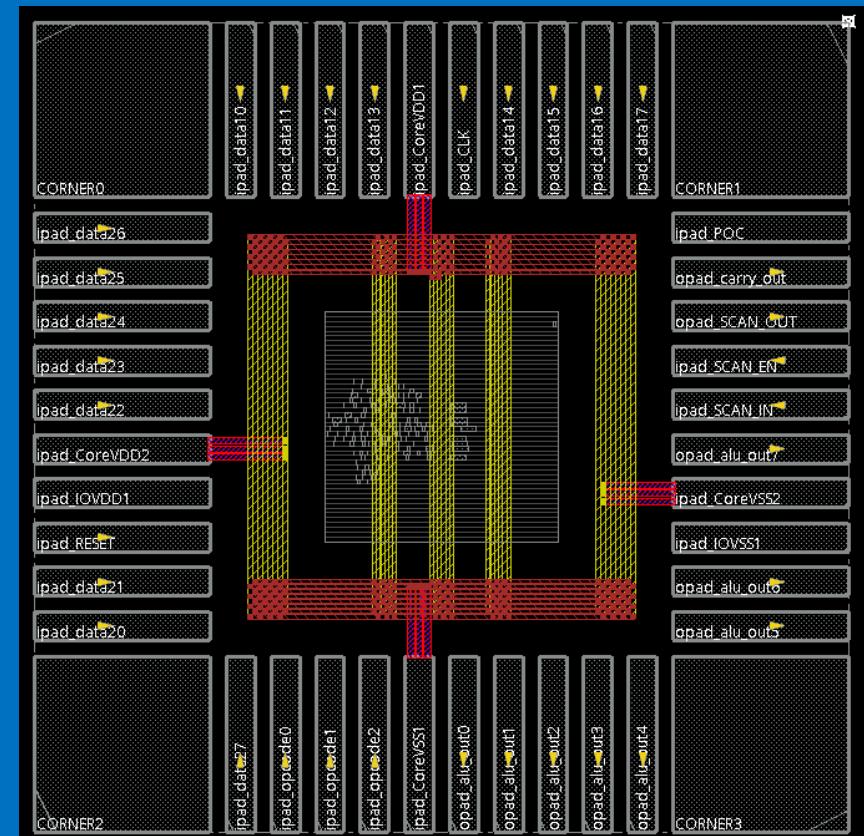
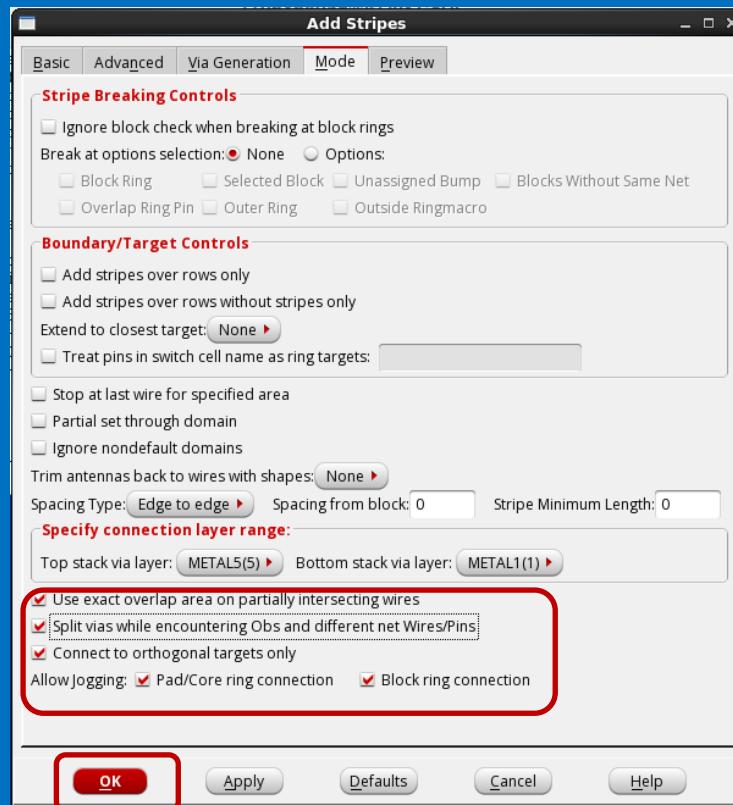
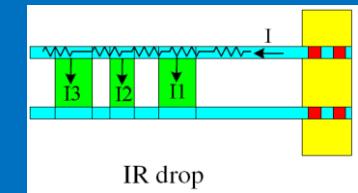


# Power Stripe



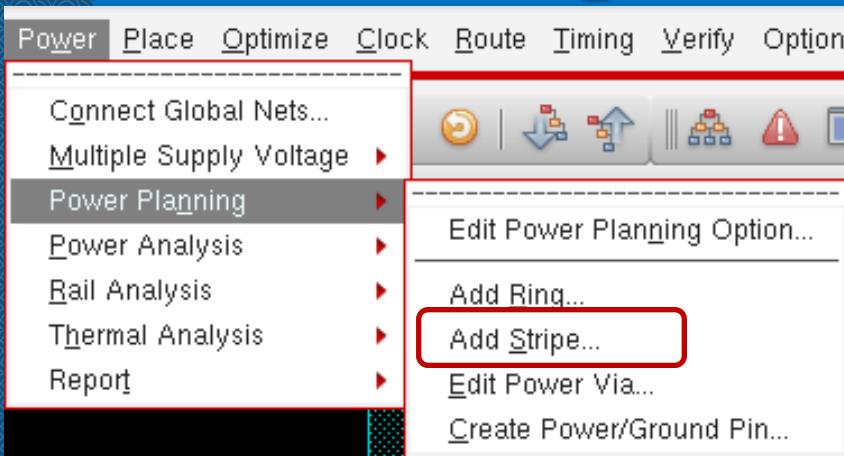
# Power Stripe

- ◆ 我們看到加進了3組stripe，且stripe的上下已經接到Power ring，power stripe是用來防止IR drop的效應

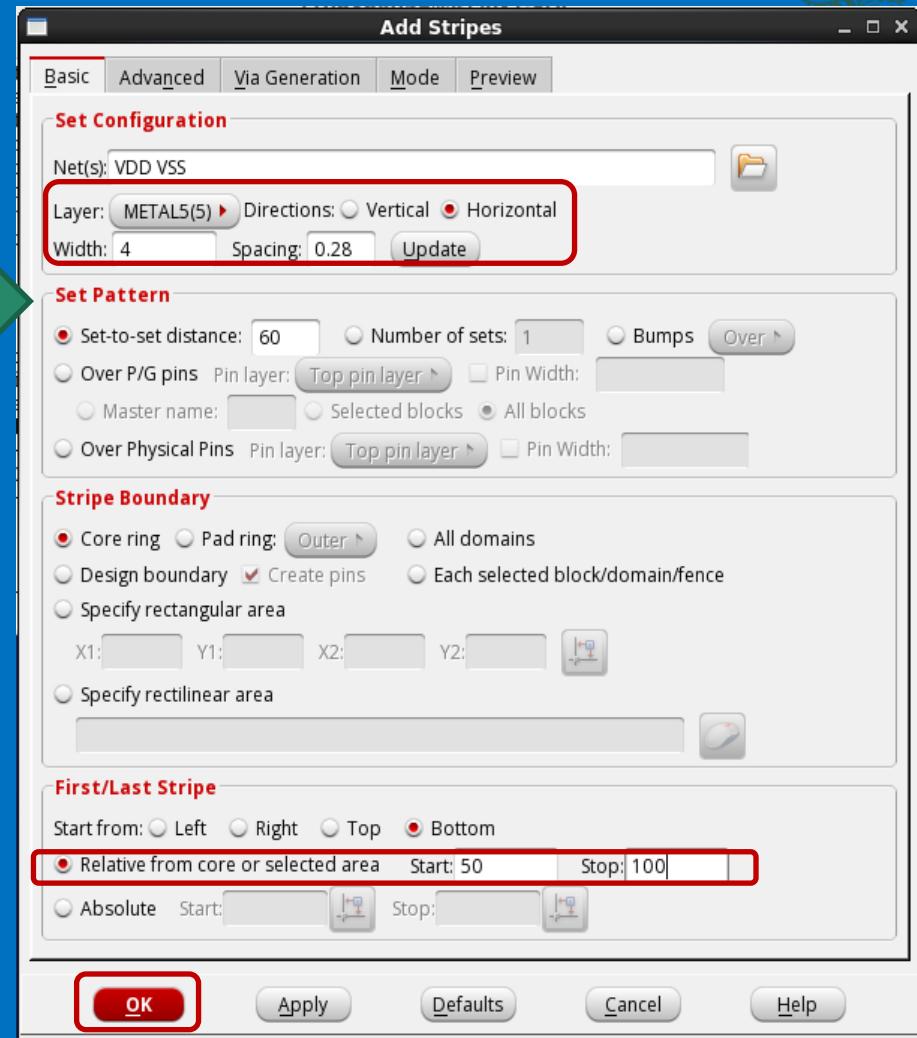




# Power Stripe



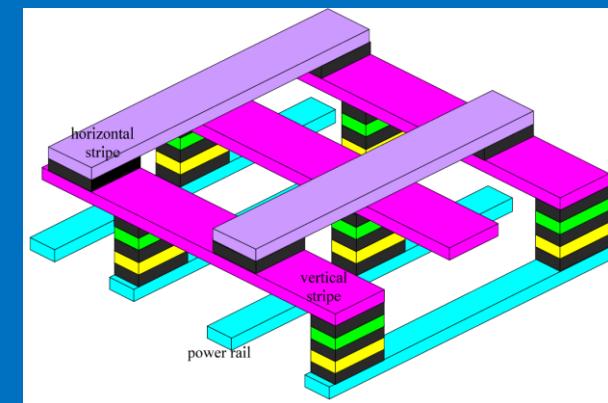
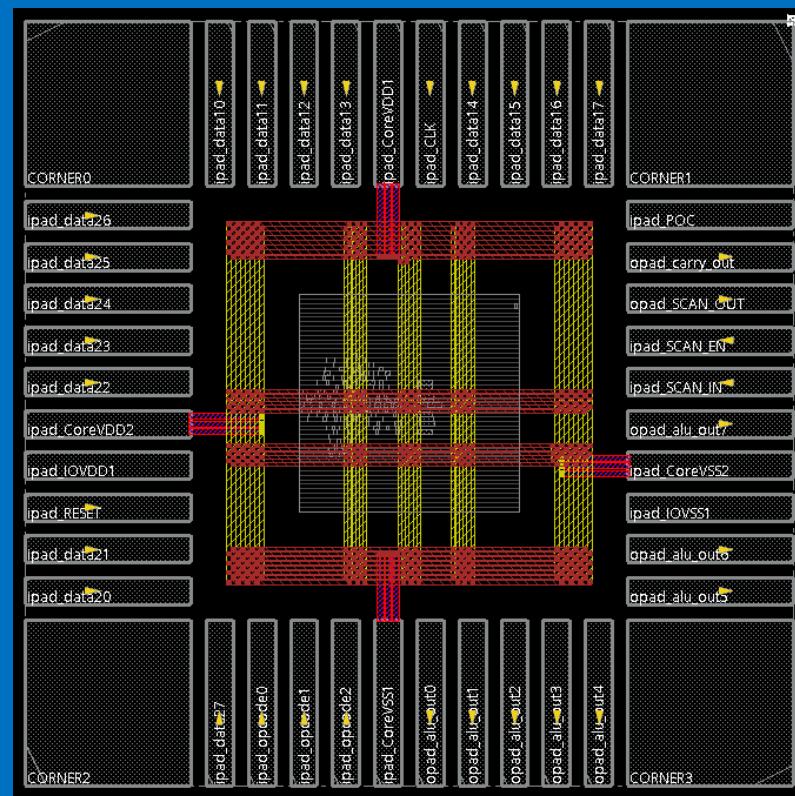
◆若還不滿意現在的架構，打算再加  
上橫的power stripe, 執行 *Power* →  
*Power Planning* → *Add Stripes...*，  
切換到Basic page，這次Layer選  
*METAL5*，你會看到Direction自動換到  
Horizontal，Advanced page和Via  
Generation的設定和剛才的設定一樣



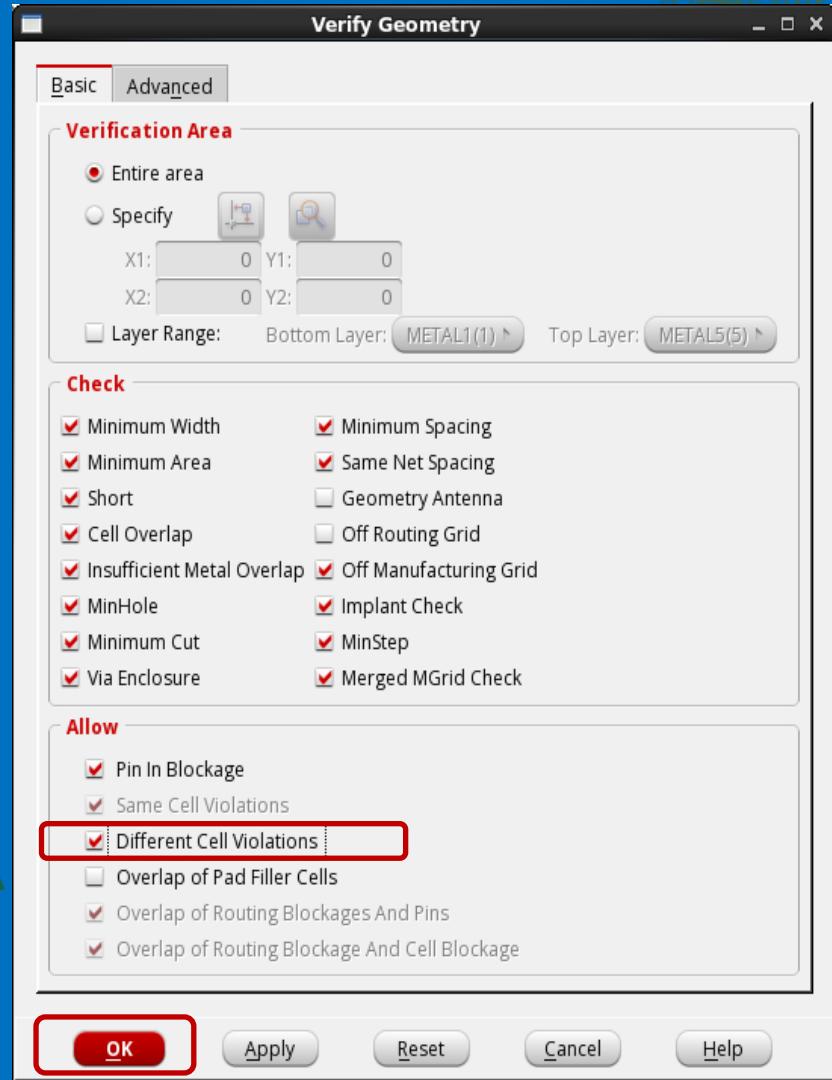
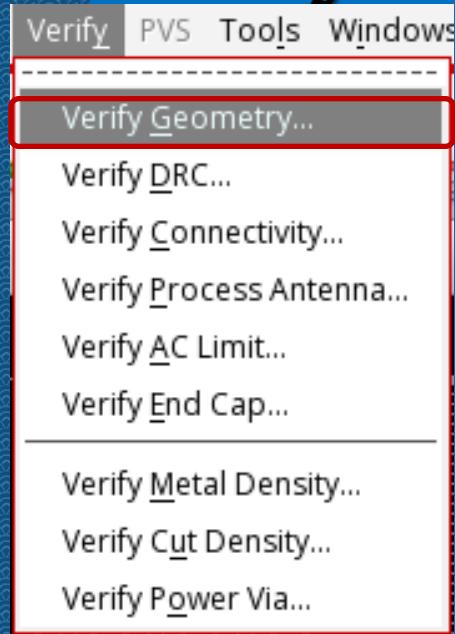


# Power Stripe

- ◆ 我們看到橫向的加進了2組stripe，且stripe的左右已經接到Power ring，因為Power rail的關係，所以水平的Stripe一定要比垂直的還高。



# Verify



```
t106368059@slabx7:SOC
VERIFY GEOMETRY ..... Creating Sub-Areas
          .... bin size: 7040
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells      : 0 Viols.
VERIFY GEOMETRY ..... SameNet    : 0 Viols.
VERIFY GEOMETRY ..... Wiring     : 0 Viols.
VERIFY GEOMETRY ..... Antenna   : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 0.00
Begin Summary ...
Cells      : 0
SameNet    : 0
Wiring     : 0
Antenna   : 0
Short      : 0
Overlap    : 0
End Summary
Verification Complete : 0 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:00.1 MEM: 15.7M)

innovus 3> ■
```



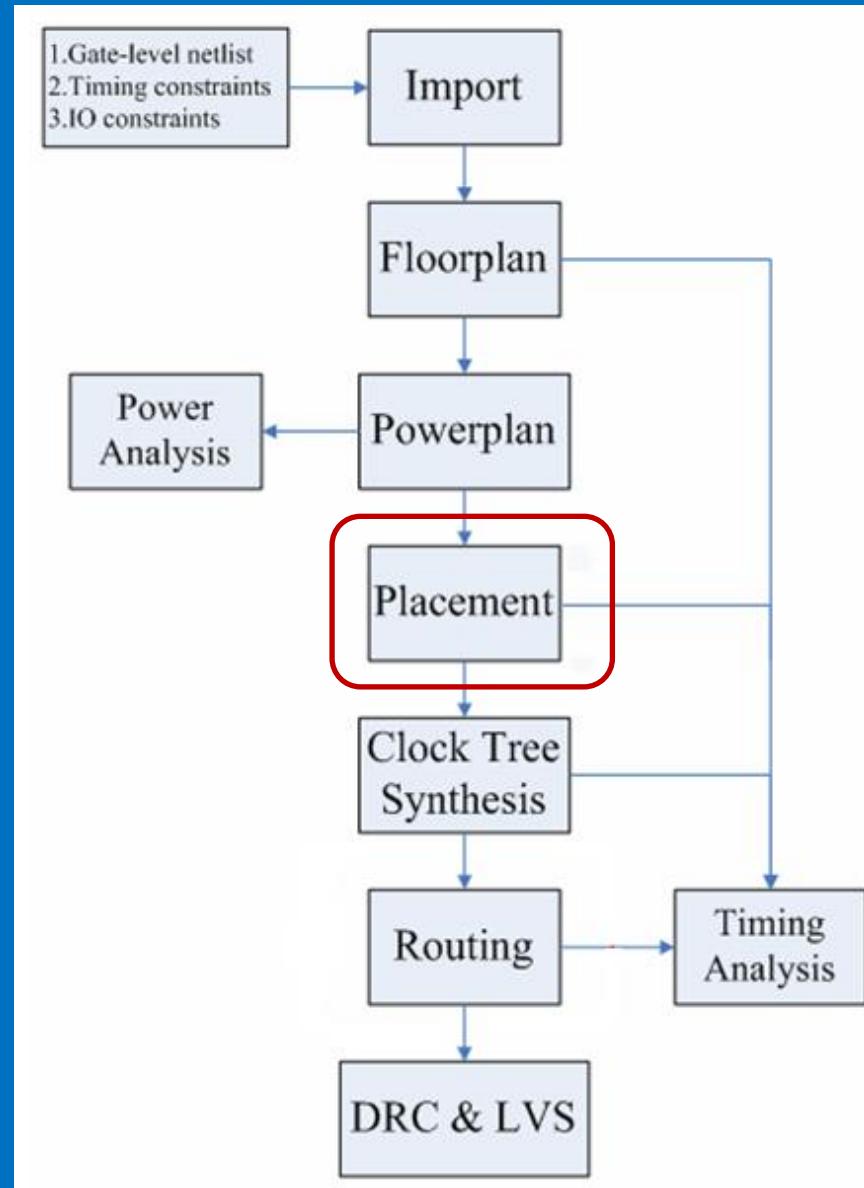
# Save Design



◆ 到這邊我們將檔案存成powerplan.enc

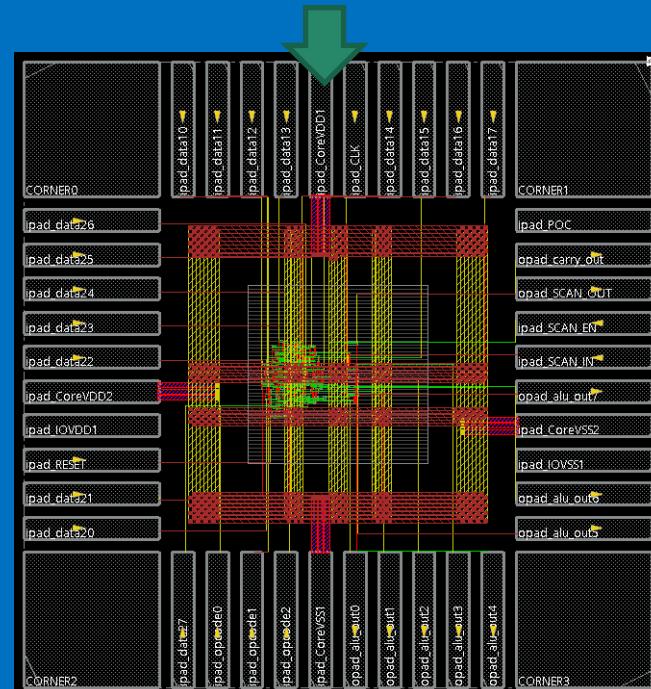


# Placement





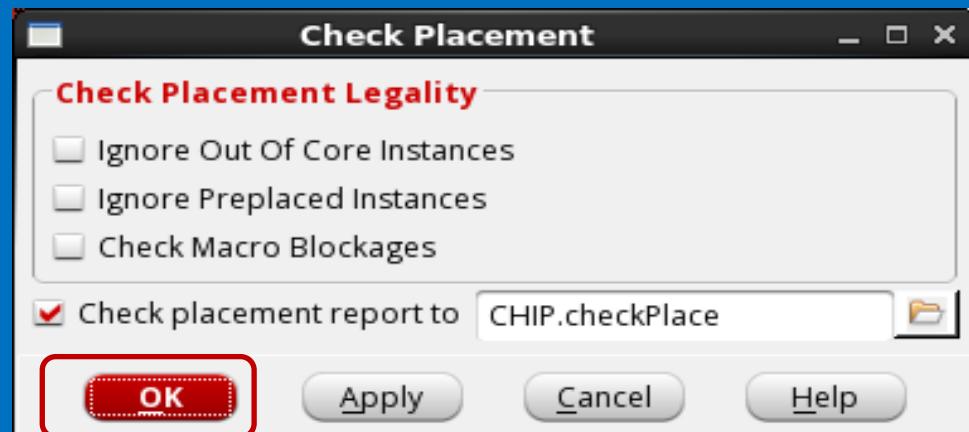
# Placement



做實際擺放



# Check Placement



```
t106368059@islabx7:SOC
[ NR-eGR] Total length: 1.512803e+04um, number of vias: 1370
[ NR-eGR]
[ NR-eGR] Total clock nets wire length: 3.069600e+02um
[ NR-eGR]
End of congRepair (cpu=0:00:00.0, real=0:00:00.0)
*** Finishing placeDesign default flow ***
***** Total cpu 0:0:1
***** Total real time 0:0:1
**placeDesign ... cpu = 0: 0: 1, real = 0: 0: 1, mem = 1213.9M **

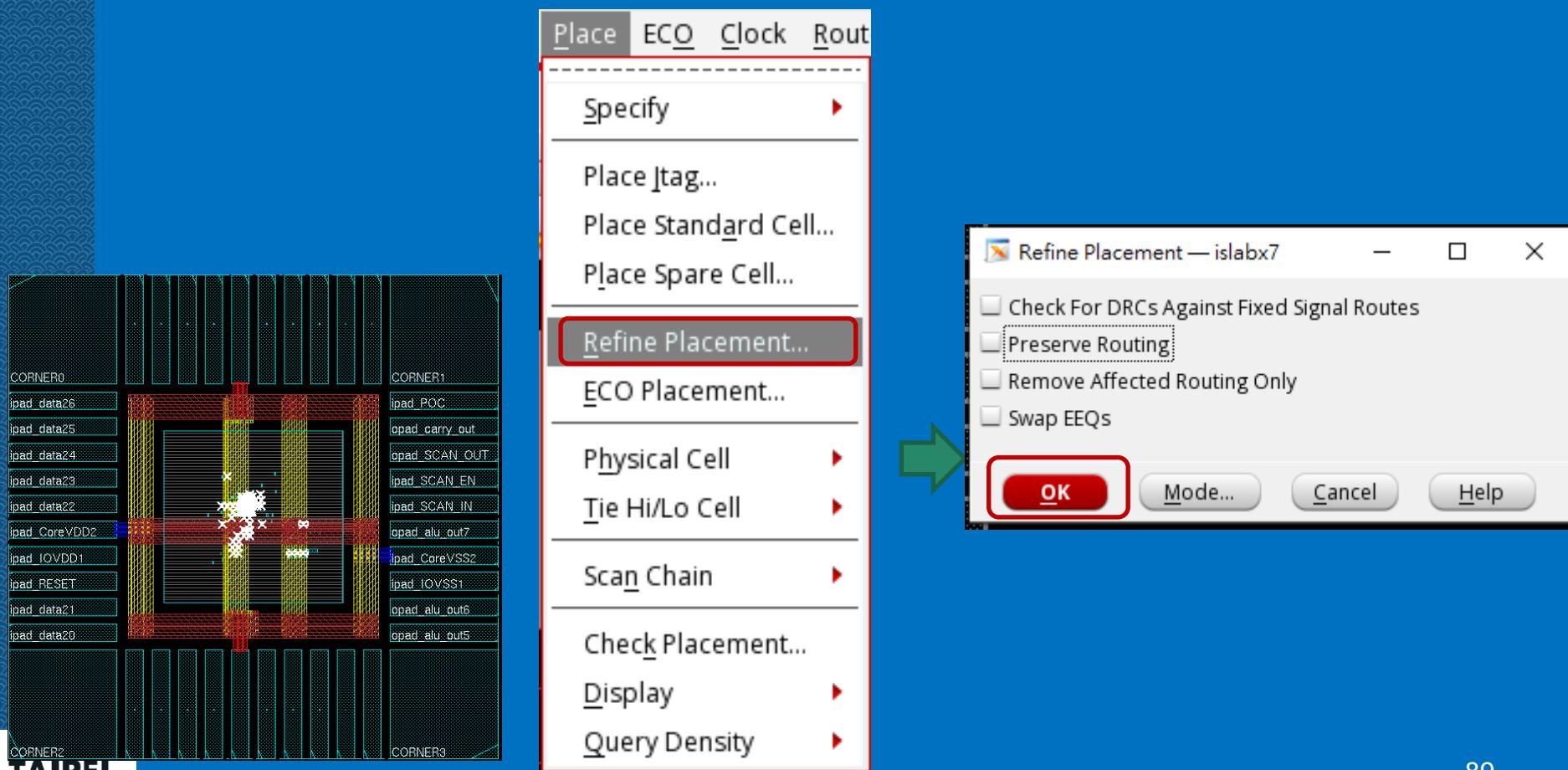
*** Summary of all messages that are not suppressed in this session:
Severity ID Count Summary
WARNING IMPEXT-3493 1 The design extraction status has been re...
WARNING IMPDC-1629 1 The default delay limit was set to %d. T...
WARNING IMPSC-1750 1 scanReorder is running on autoFlow mode, ...
*** Message Summary: 3 warning(s), 0 error(s)

innovus 3> Begin checking placement ... (start mem=1214.5M, init mem=1214.5M)
*info: Placed = 147
*info: Unplaced = 0
Placement Density: 4.34%(2585/59556)
Placement Density (including fixed std cells): 4.34%(2585/59556)
Finished checkPlace (cpu: total=0:00:00.0, vio checks=0:00:00.0; mem=1214.5M)
innovus 3>
```



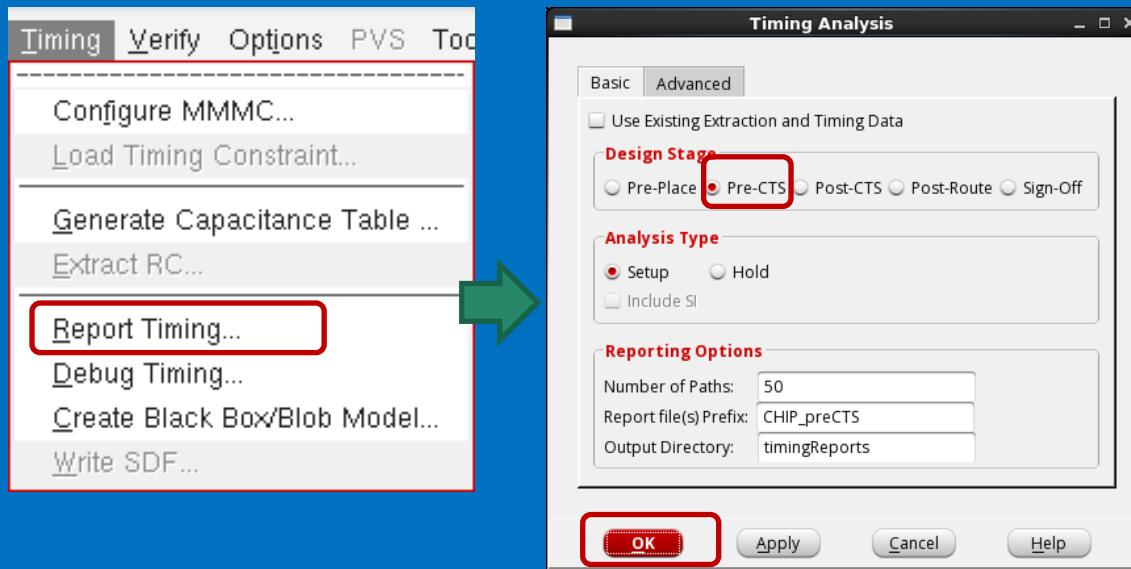
# Check Placement

- ◆ 如果cell擺放完遇到錯誤，請Refine Placement去回復並做修正，然後再Check Placement一次，看看是否還有Violation存在





# Timing Analysis



Setup mode	all	reg2reg	in2reg	reg2out	in2out	default	
WNS (ns):	-0.043	4.235	-0.043	0.363	N/A	0.000	
TNS (ns):	-0.043	0.000	-0.043	0.000	N/A	0.000	
Violating Paths:	1	0	1	0	N/A	0	
All Paths:	36	8	19	9	N/A	0	



# Timing Optimization

The diagram illustrates the workflow for timing optimization:

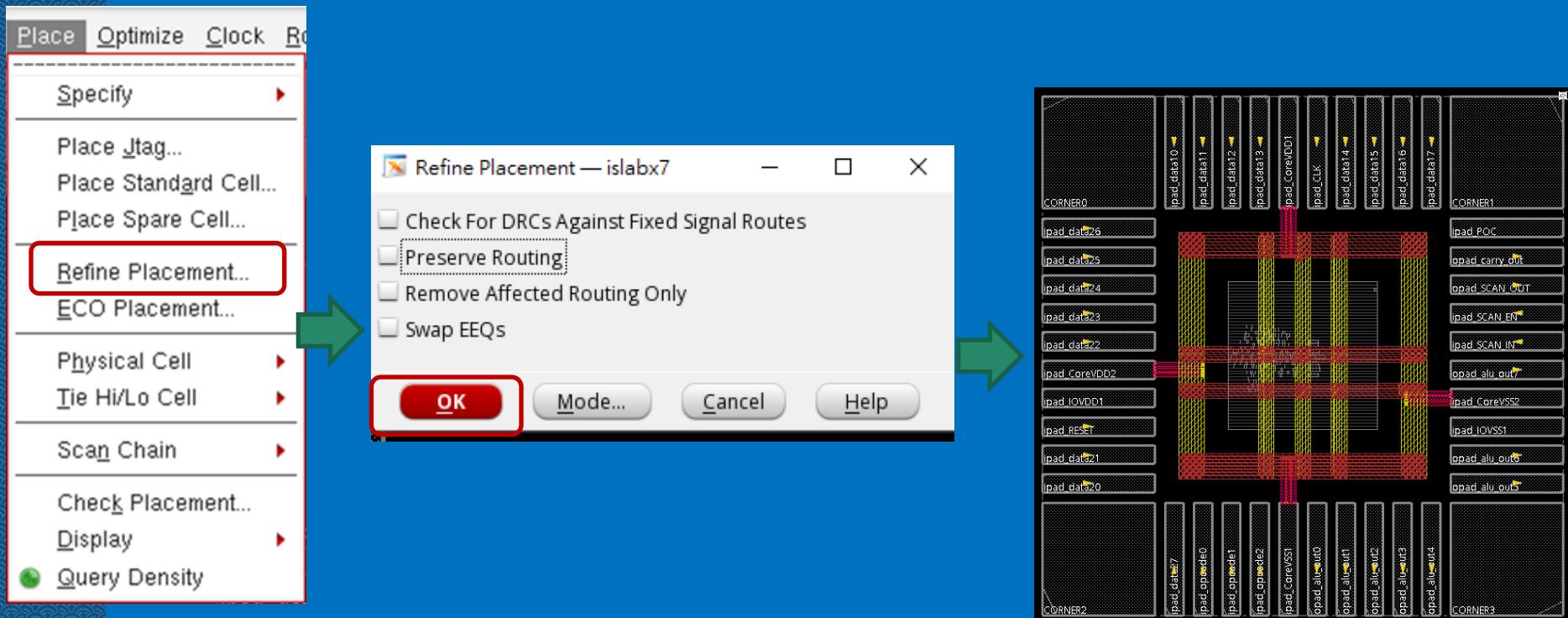
- Initial Interface:** A screenshot of a software interface showing tabs for ECO, Clock, Route, and Timing. The ECO tab is selected. A red box highlights the "Optimize Design..." button, which is also highlighted by a green arrow pointing to the next window.
- Optimization Settings:** A dialog box titled "Optimization" is shown. It has a "Design Stage" section with "Pre-CTS" selected (highlighted with a red box). The "Optimization Type" section contains several checkboxes:
  - Setup
  - Incremental
  - Design Rules Violations
  - Max Cap
  - Max Tran
  - Max FanoutA "Hold" checkbox is also present. At the bottom are buttons for OK (highlighted with a red box), Apply, Mode..., Default, Close, and Help.
- Terminal Output:** A terminal window titled "t106368059@islabx7:SOC" displays command-line output. It shows setup views included: "av\_func\_mode\_max". Below this is a table of timing parameters:

Setup mode	all	reg2reg	in2reg	reg2out	in2out	default	
WNS (ns):	0.018	4.198	0.018	0.095	N/A	0.000	
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000	
Violating Paths:	0	0	0	0	N/A	0	
All Paths:	36	8	19	9	N/A	0	



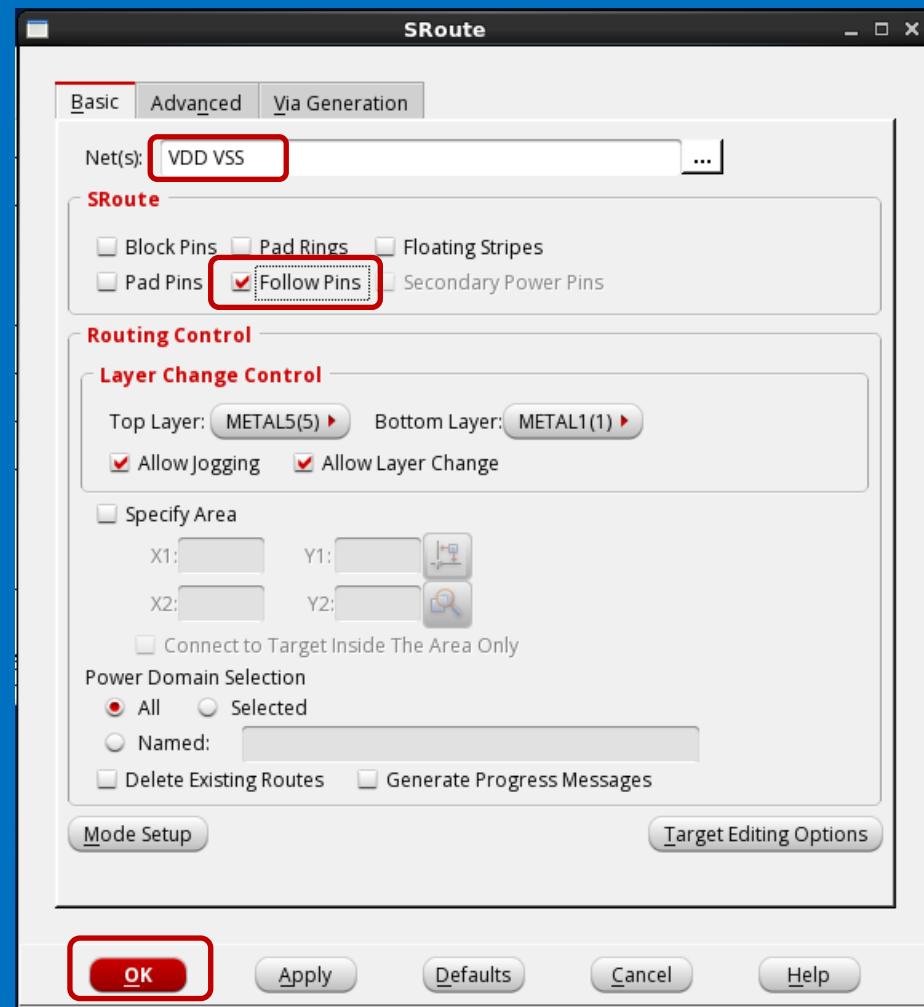
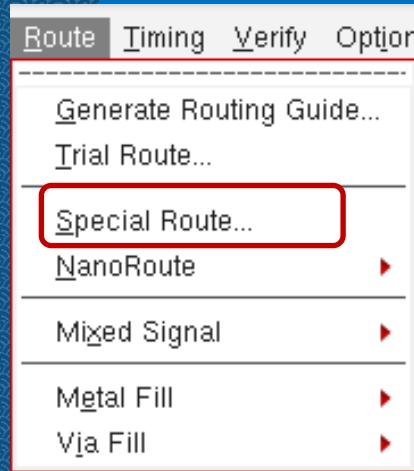
# Refine Placement

◆ 等等因為要架設Follow pins，我們必須將剛剛所呼叫的Trial Route拿掉，以免產生錯誤





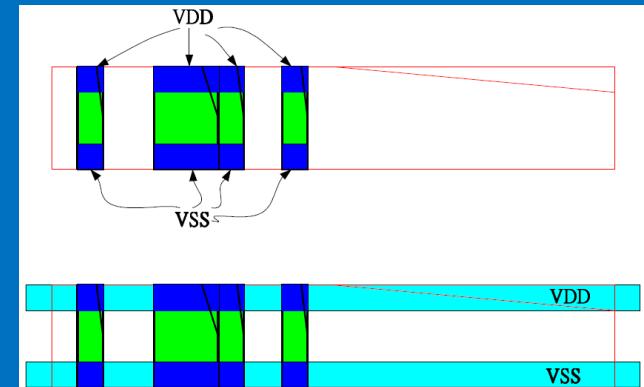
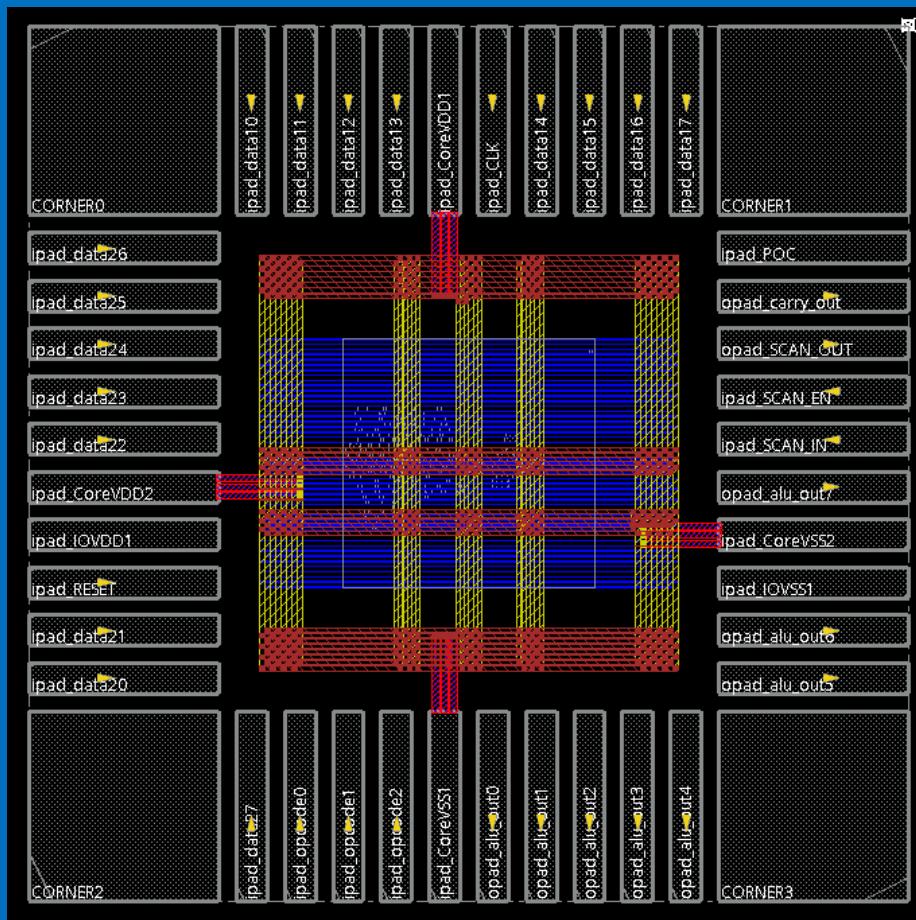
# Follow Pins





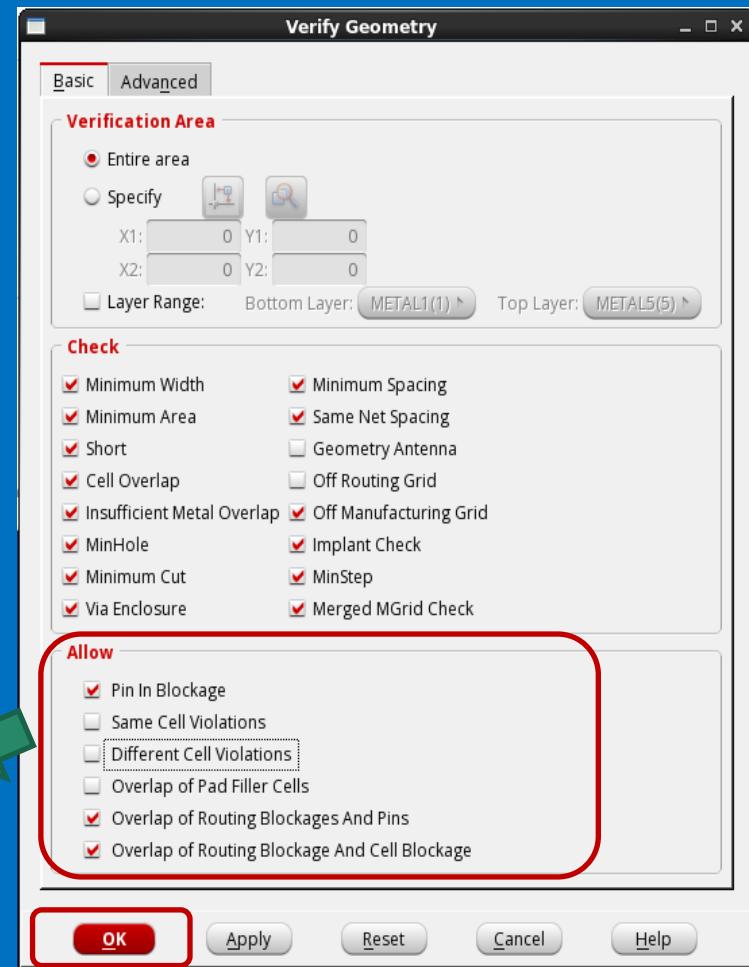
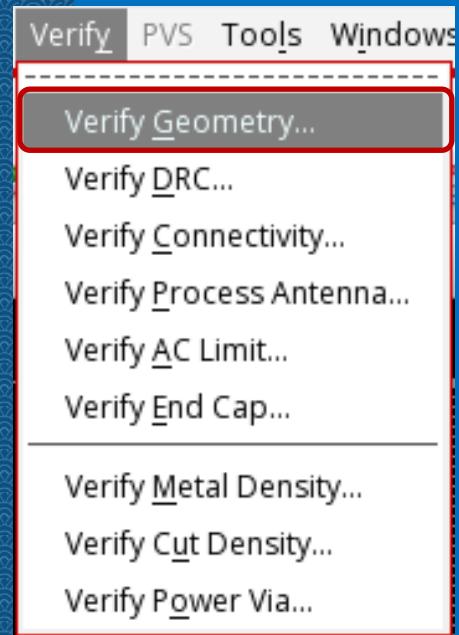
# Follow Pins

- ◆ 可以看到Standard cell的Power已經連上了





# Verify

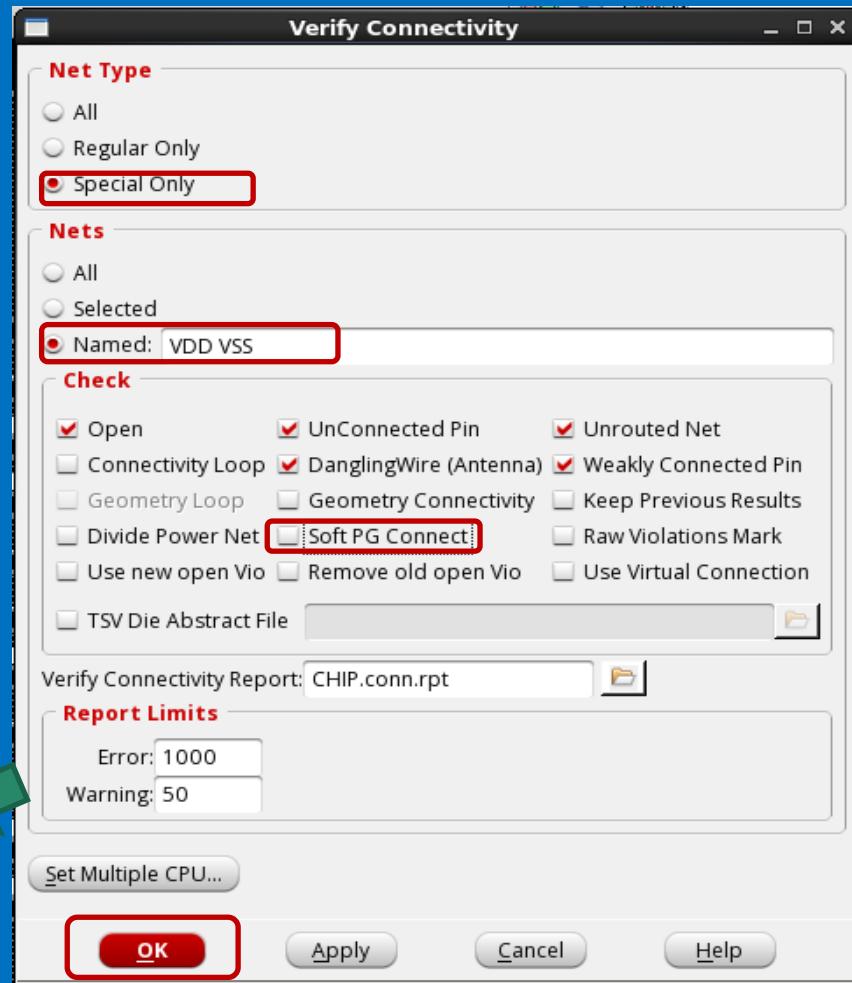
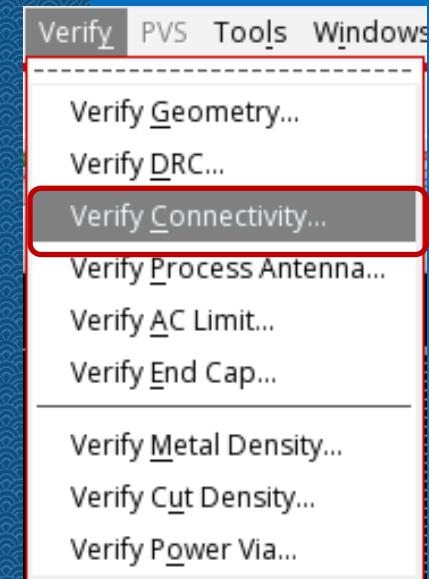


```
t106368059@islabx7:SOC
VERIFY GEOMETRY ..... Creating Sub-Areas
VERIFY GEOMETRY ..... bin size: 7040
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 0.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary ...

Verification Complete : 0 Viols. 0 Wrngs.
*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:00.1 MEM: 60.9M)
innovus 1>
```



# Verify

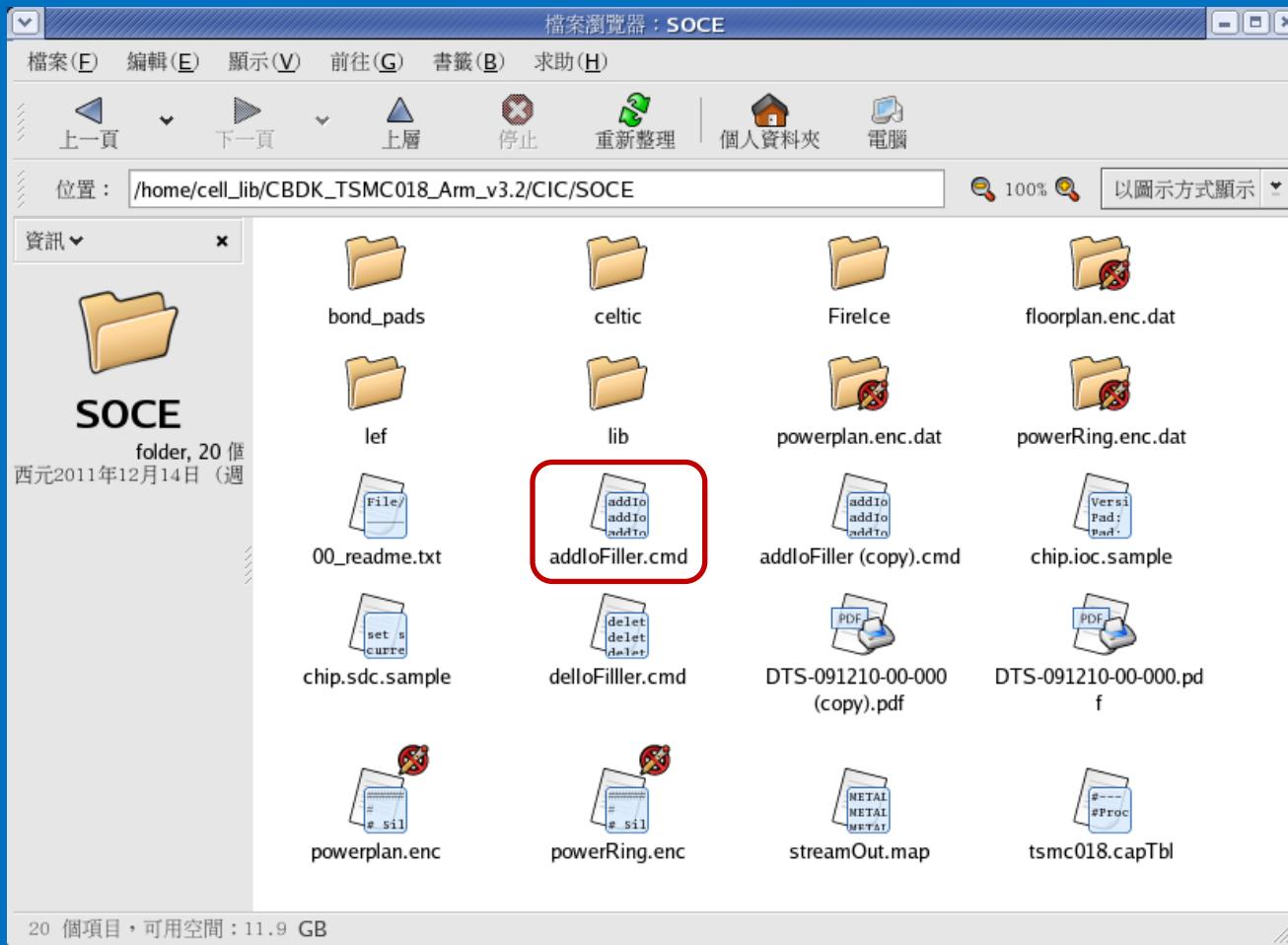


```
t106368059@islabx7: SOC
VERIFY GEOMETRY ..... Creating Sub-Areas
VERIFY GEOMETRY ..... bin size: 7040
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 0.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary
Verification Complete : 0 Viols. 0 Wrngs.
*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:00.1 MEM: 60.9M)
innovus 1
```





# Add IO Filler



cp /home/cell\_lib/CBDK\_TSMC018\_Arm\_v3.2/CIC/SOCE/addIoFiller.cmd .  
複製addIoFiller.cmd到自己的資料夾內 (islabx5在Design\_kit內)





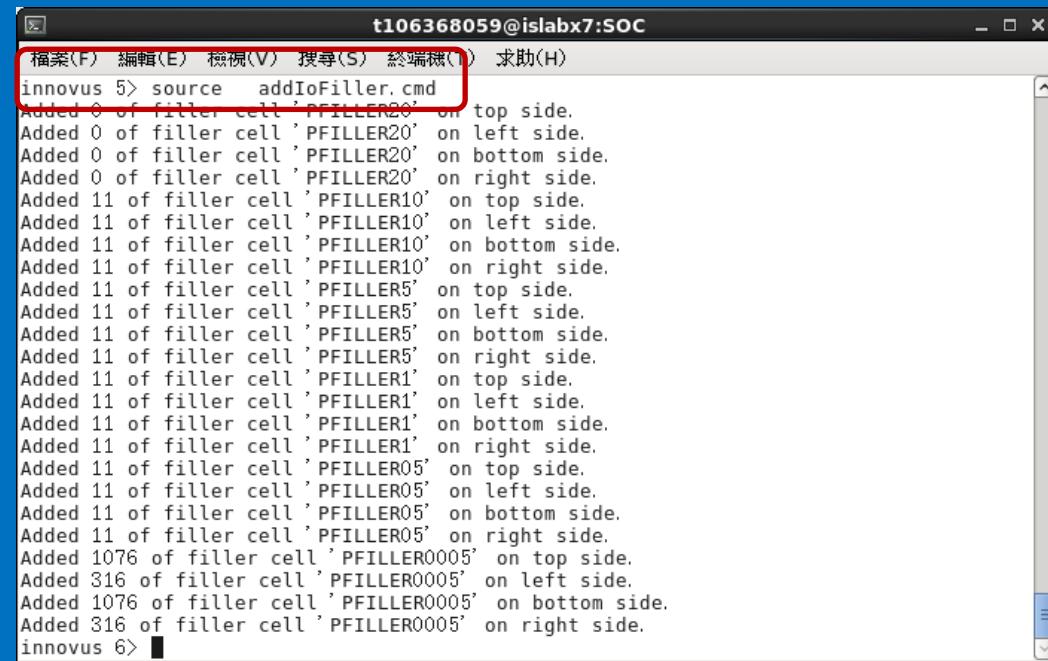
# Add IO Filler



```
[t00418078@islabx3 ~ ]$ more addIoFiller.cmd
addIoFiller -cell PFILLER20 -prefix IOFILLER
addIoFiller -cell PFILLER10 -prefix IOFILLER
addIoFiller -cell PFILLER5 -prefix IOFILLER
addIoFiller -cell PFILLER1 -prefix IOFILLER
addIoFiller -cell PFILLER05 -prefix IOFILLER
addIoFiller -cell PFILLER0005 -prefix IOFILLER -fillAnyGap

[t00418078@islabx3 ~ ]$
```

- ◆ 開起一個新的terminal，  
進入到自己的工作資料夾
- ◆ 利用 more addIoFiller.cmd  
可以查看檔案內指令的內容
- ◆ innovus > source  
addIoFiller.cmd
- ◆ 存檔成place\_IoFiller.enc

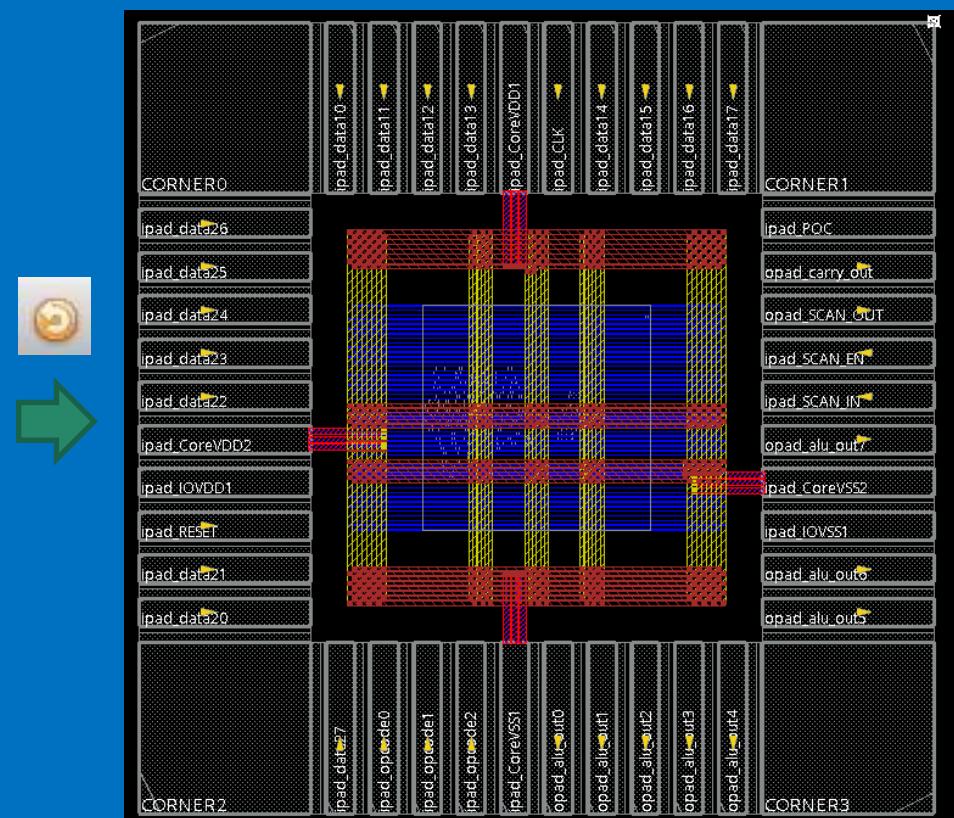
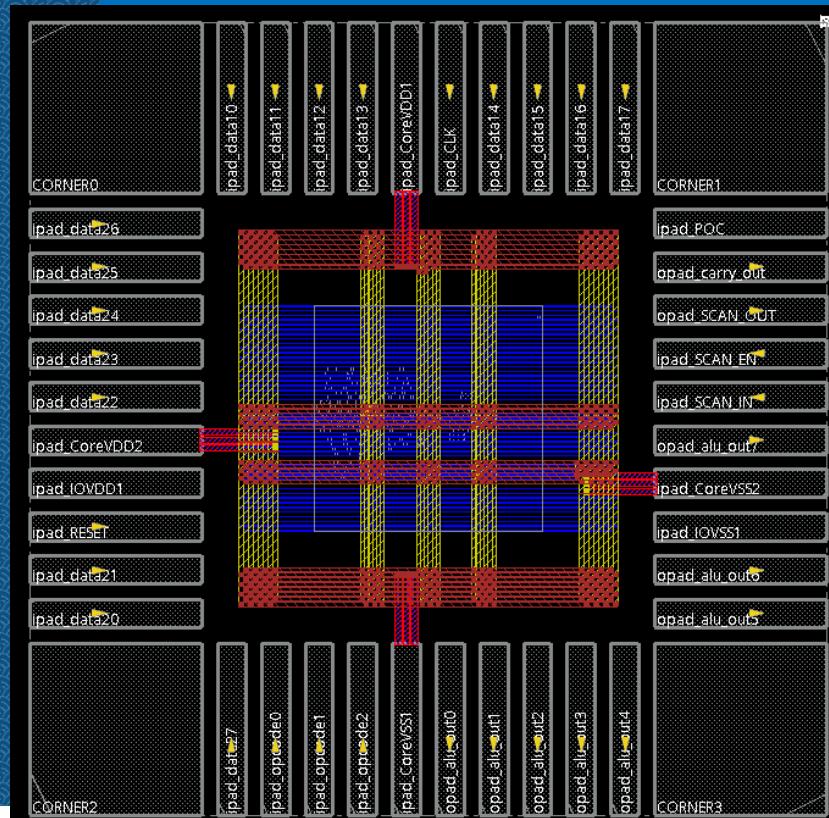
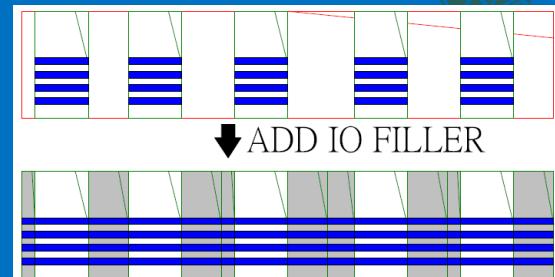


```
innovus 5> source addIoFiller.cmd
Added 0 of filler cell 'PFILLER20' on top side.
Added 0 of filler cell 'PFILLER20' on left side.
Added 0 of filler cell 'PFILLER20' on bottom side.
Added 0 of filler cell 'PFILLER20' on right side.
Added 11 of filler cell 'PFILLER10' on top side.
Added 11 of filler cell 'PFILLER10' on left side.
Added 11 of filler cell 'PFILLER10' on bottom side.
Added 11 of filler cell 'PFILLER10' on right side.
Added 11 of filler cell 'PFILLER5' on top side.
Added 11 of filler cell 'PFILLER5' on left side.
Added 11 of filler cell 'PFILLER5' on bottom side.
Added 11 of filler cell 'PFILLER5' on right side.
Added 11 of filler cell 'PFILLER1' on top side.
Added 11 of filler cell 'PFILLER1' on left side.
Added 11 of filler cell 'PFILLER1' on bottom side.
Added 11 of filler cell 'PFILLER1' on right side.
Added 11 of filler cell 'PFILLER05' on top side.
Added 11 of filler cell 'PFILLER05' on left side.
Added 11 of filler cell 'PFILLER05' on bottom side.
Added 11 of filler cell 'PFILLER05' on right side.
Added 1076 of filler cell 'PFILLER0005' on top side.
Added 316 of filler cell 'PFILLER0005' on left side.
Added 1076 of filler cell 'PFILLER0005' on bottom side.
Added 316 of filler cell 'PFILLER0005' on right side.

innovus 6>
```

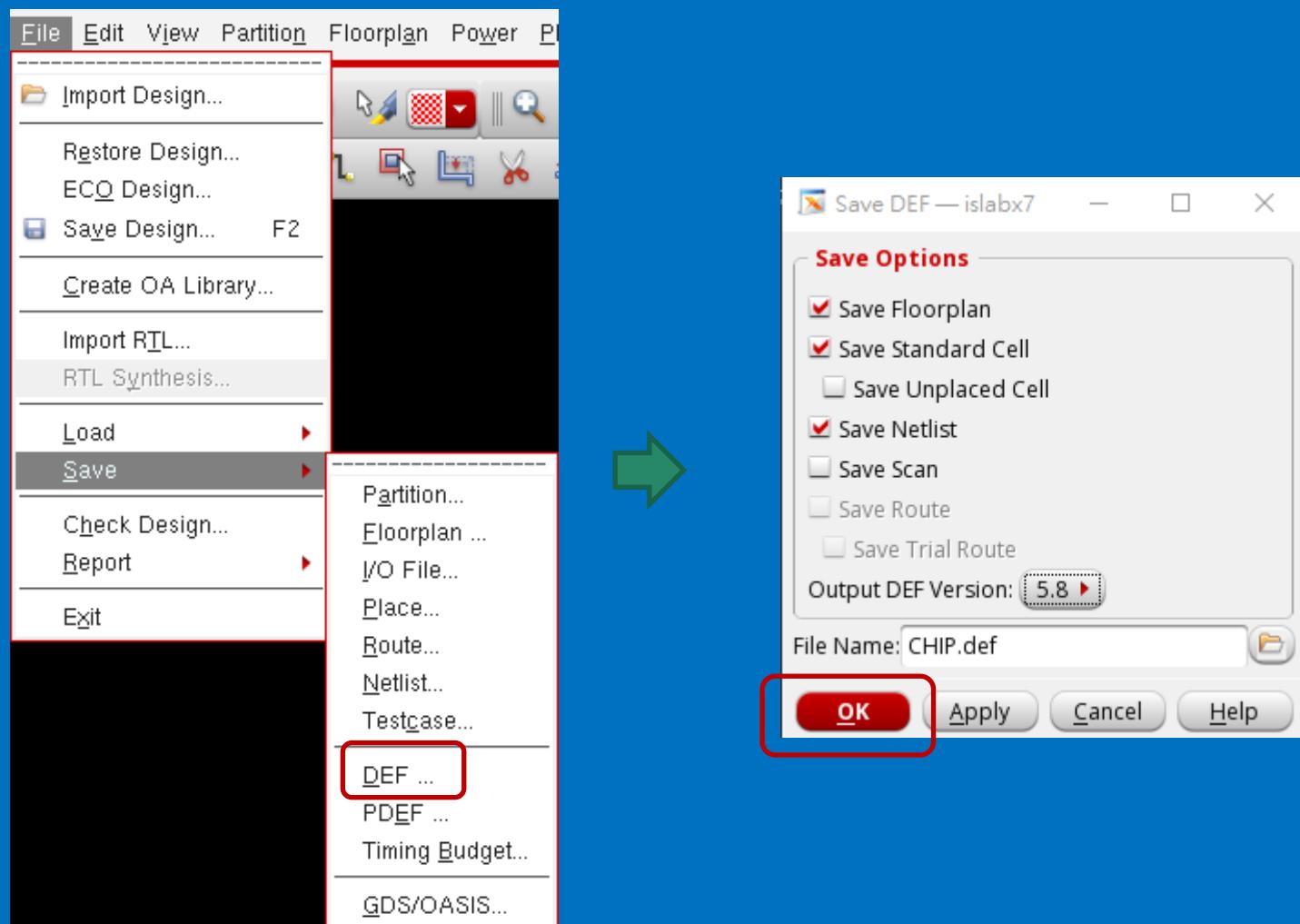
# Add IO Filler

- ◆ 按一下重新整理可以看到Iofiller已經被加入了



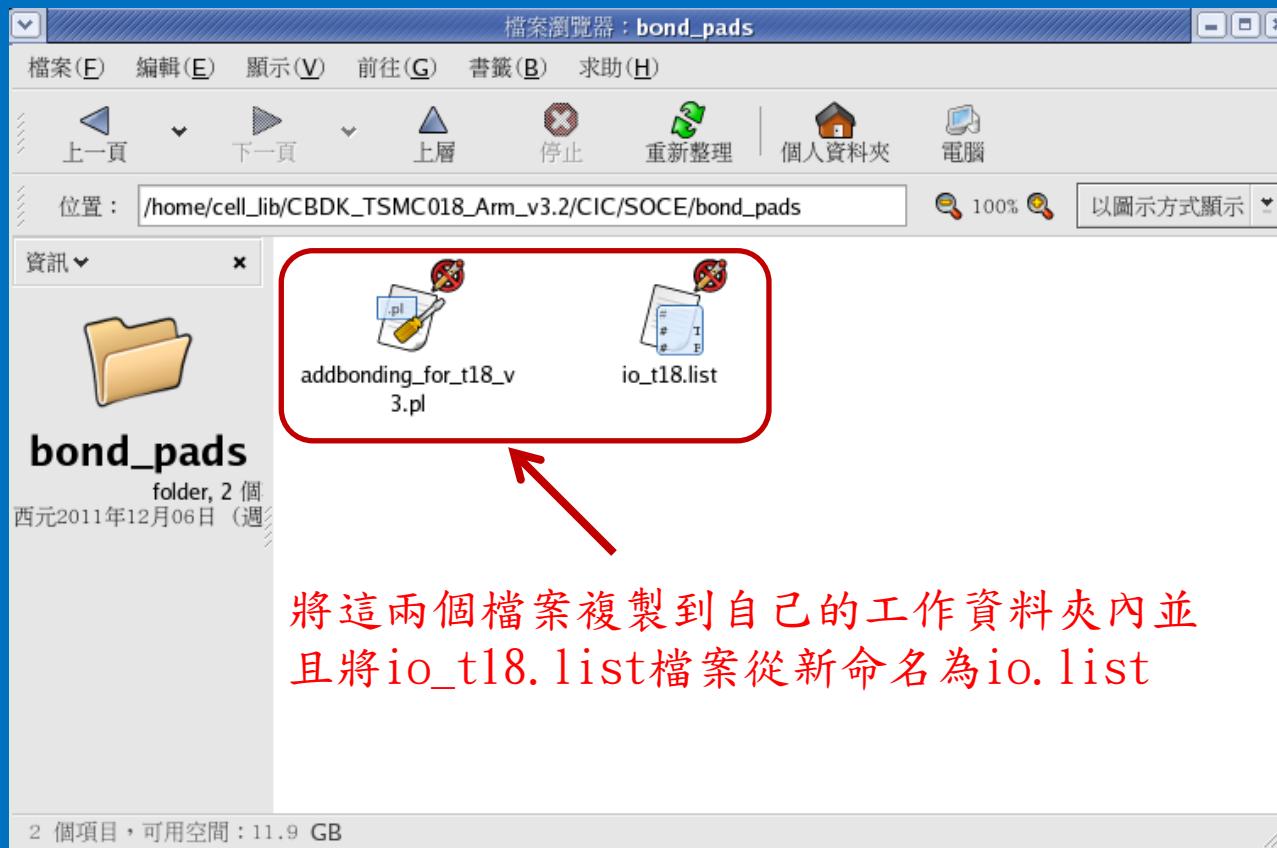


# Save DEF → 用來儲存繞線資訊





# Add Routing Blockage



路徑：

/home/cell\_lib/CBDK\_TSMC018\_Arm\_v3.2/CIC/SOCE/  
bond\_pads (islabx5在Design\_kit內)

# Add Routing Blockage

◆ 為了避免routing時繞線繞到IO Pad上

方，我們經由perl程式算出IO pad的位置，  
會先在上方加入routing blockage

◆ innovus >

perl ./addbonding\_for\_t18\_v3.pl CHIP.def

◆ 會產生兩個檔案：addRouteBlk.cmd和  
addbond.cmd

◆ innovus >

source addRouteBlk.cmd

◆ 存檔File->SaveDesign

存成place\_CUPPad.enc

```
t106368059@islabx7:SOC
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 幫助(H)
innovus 3> perl ./addbonding_for_t18_v3.pl CHIP.def
Overwrite files addbond.cmd.....
Overwrite files addRouteBlk.cmd.....
BPad_west1 PAD60GU west 40 216.645 R270
BPad_west2 PAD60NU west 135 263.29 R270
BPad_west3 PAD60GU west 40 309.935 R270
BPad_west4 PAD60NU west 135 356.58 R270
BPad_west5 PAD60GU west 40 403.22 R270
BPad_west6 PAD60NU west 135 449.86 R270
BPad_west7 PAD60GU west 40 496.5 R270
BPad_west8 PAD60NU west 135 543.145 R270
BPad_west9 PAD60GU west 40 589.79 R270
BPad_west10 PAD60NU west 135 636.435 R270
BPad_east1 PAD60NU east 721.88 216.645 R90
BPad_east2 PAD60GU east 816.88 263.29 R90
BPad_east3 PAD60NU east 721.88 309.935 R90
BPad_east4 PAD60GU east 816.88 356.58 R90
BPad_east5 PAD60NU east 721.88 403.22 R90
BPad_east6 PAD60GU east 816.88 449.86 R90
BPad_east7 PAD60NU east 721.88 496.5 R90
BPad_east8 PAD60GU east 816.88 543.145 R90
BPad_east9 PAD60NU east 721.88 589.79 R90
BPad_east10 PAD60GU east 816.88 636.435 R90
BPad_south1 PAD60NU south 216.99 135 R0
BPad_south2 PAD60GU south 263.98 40 R0
BPad_south3 PAD60NU south 310.97 135 R0
BPad_south4 PAD60GU south 357.96 40 R0
BPad_south5 PAD60NU south 404.95 135 R0
BPad_south6 PAD60GU south 451.935 40 R0
BPad_south7 PAD60NU south 498.92 135 R0
BPad_south8 PAD60GU south 545.91 40 R0
BPad_south9 PAD60NU south 592.9 135 R0
BPad_south10 PAD60GU south 639.89 40 R0
BPad_north1 PAD60GU north 216.99 813.08 R180
BPad_north2 PAD60NU north 263.98 718.08 R180
BPad_north3 PAD60GU north 310.97 813.08 R180
BPad_north4 PAD60NU north 357.96 718.08 R180
BPad_north5 PAD60GU north 404.95 813.08 R180
BPad_north6 PAD60NU north 451.935 718.08 R180
BPad_north7 PAD60GU north 498.92 813.08 R180
BPad_north8 PAD60NU north 545.91 718.08 R180
BPad_north9 PAD60GU north 592.9 813.08 R180
BPad_north10 PAD60NU north 639.89 718.08 R180
Create finish, you can execute it at SOC Encounter terminal:
If you are setting routing blockage:
Encounter> source addRouteBlk.cmd
If you are adding bonding pad:
Encounter> source addbond.cmd
innovus 4>
```

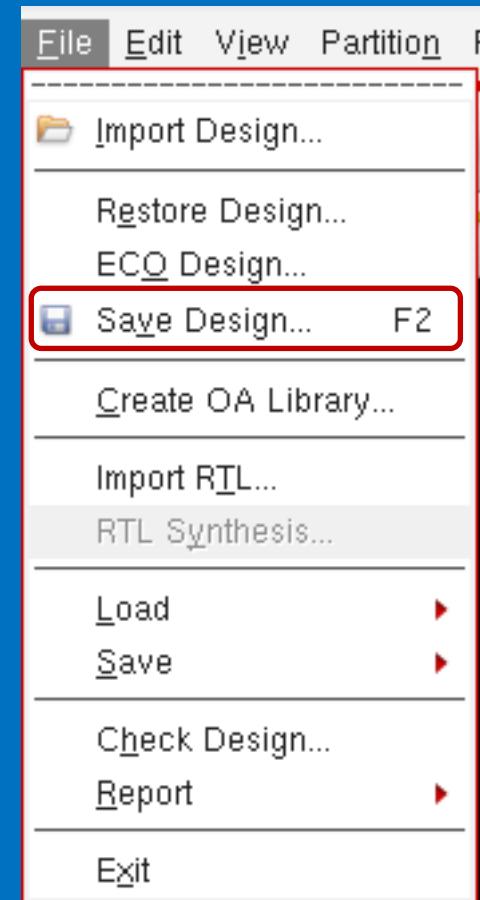
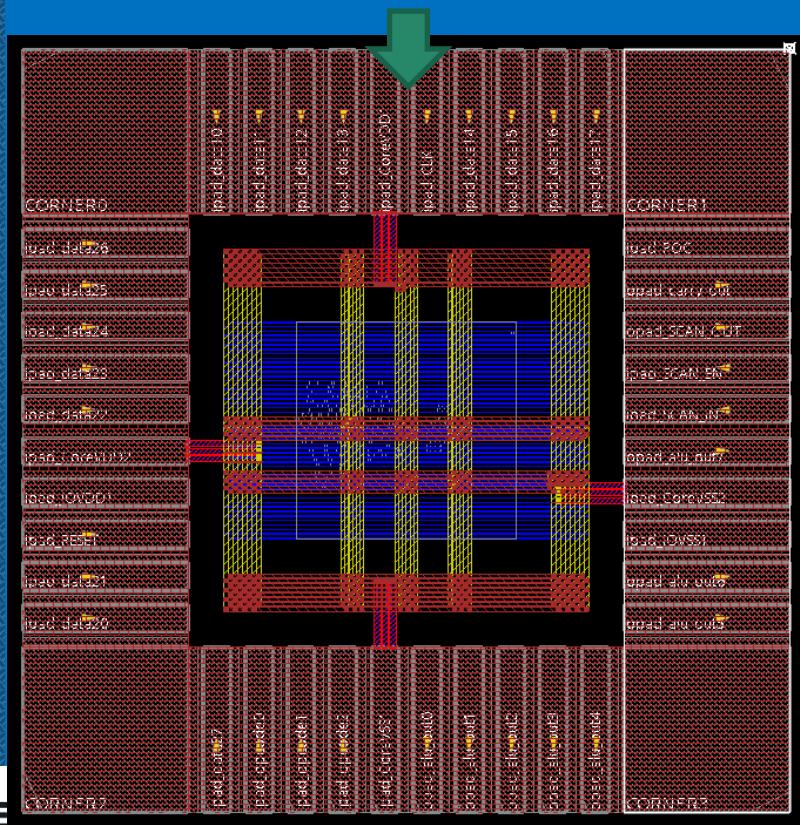


# Add Routing Blockage

終端機

檔案(E) 編輯(E) 顯示(V) 終端機(I) 分頁(B) 求助(H)

```
If you are setting routing blockage:  
Encounter> source addRouteB1k.cmd  
  
If you are adding bonding pad:  
Encounter> source addbond.cmd  
  
encounter 8> source addRouteB1k.cmd  
encounter 9>
```



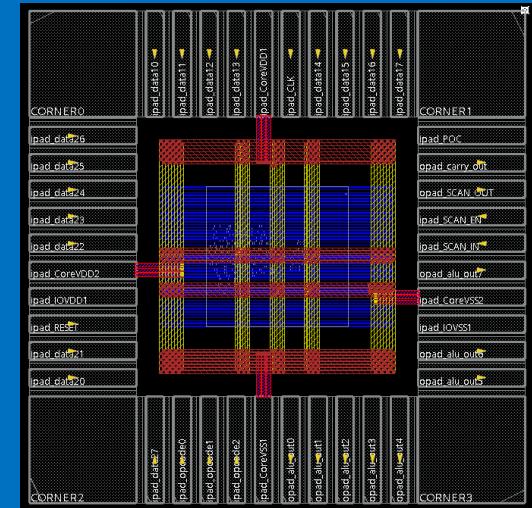
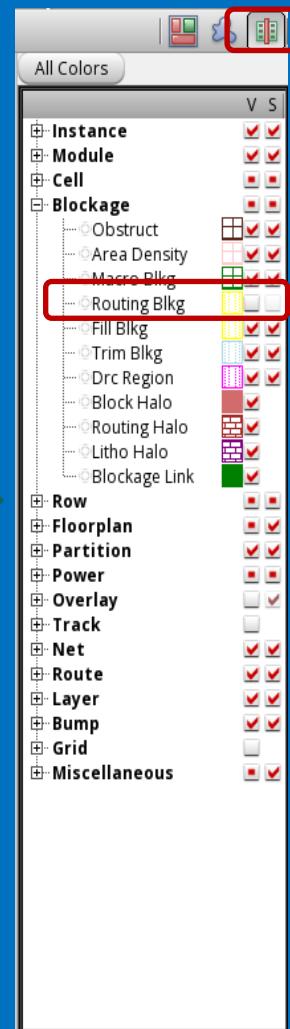
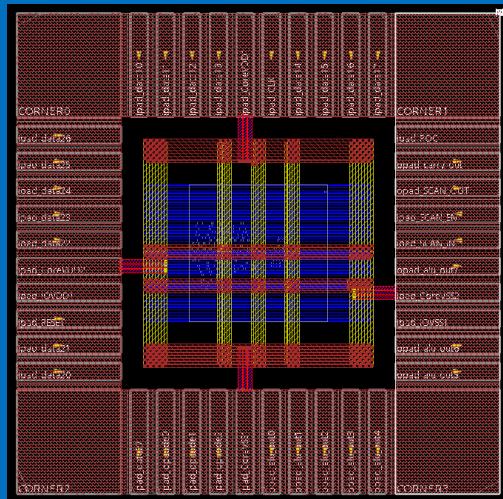
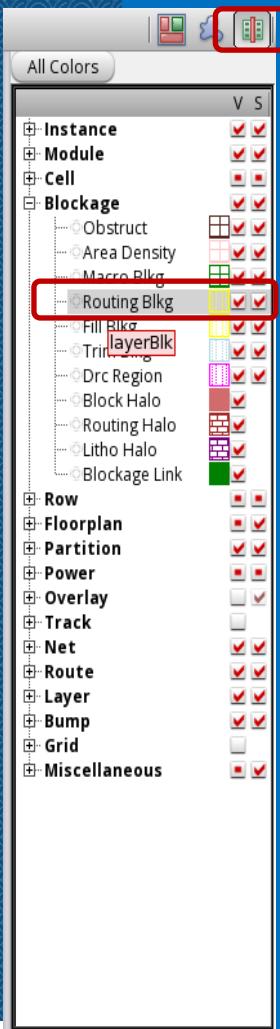


# Add Routing Blockage

◆ 為了方便檢視，我們

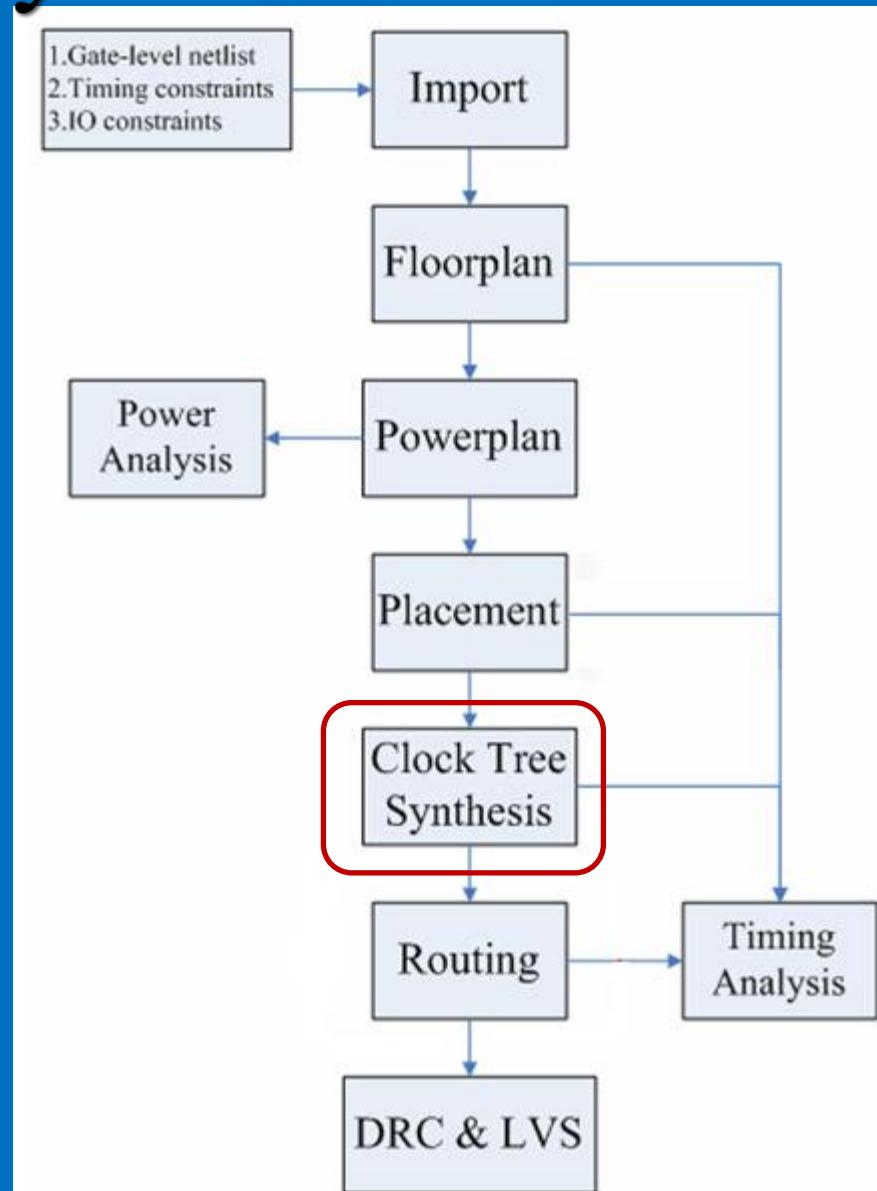
將剛剛加入的Routing

Blockage的顏色顯示關掉





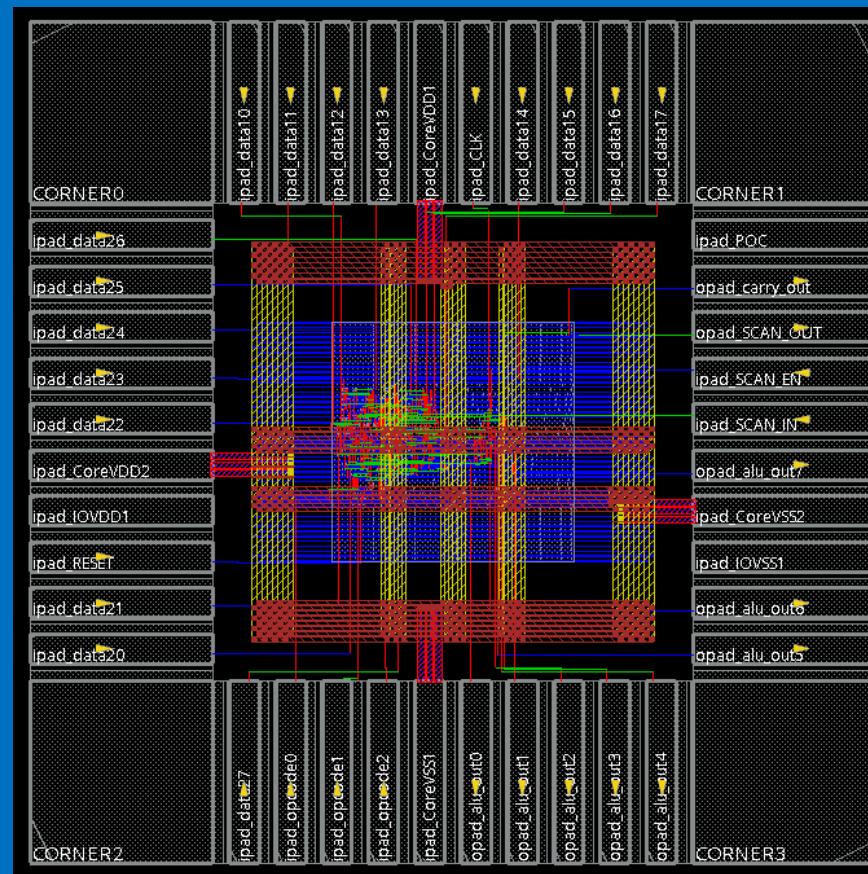
# Clock Tree Synthesis





# Clock Tree Synthesis

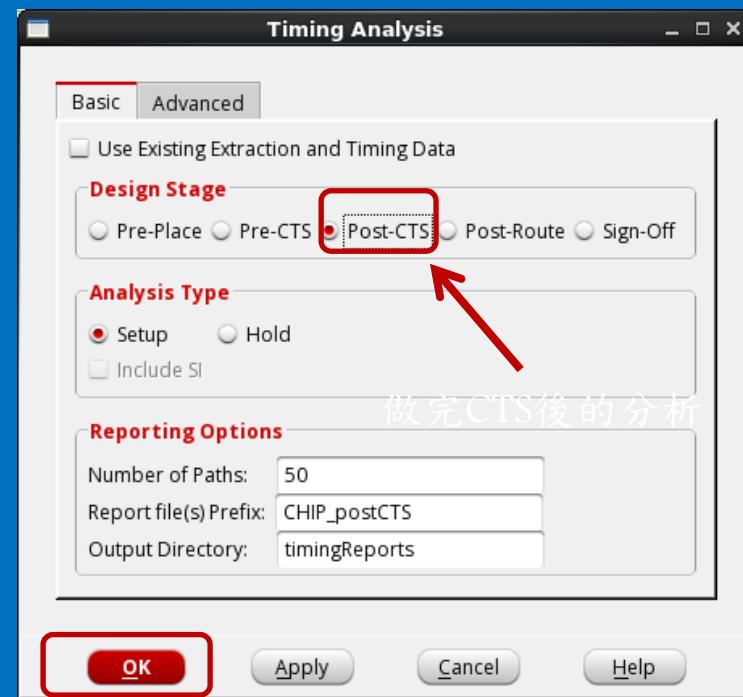
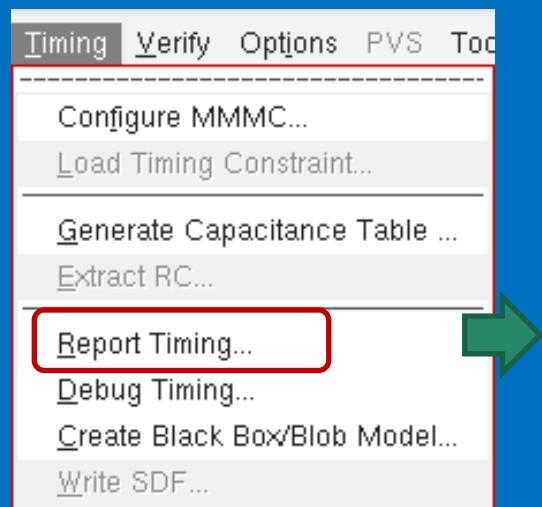
- ◆ innovus > ccopt\_design -cts
- ◆ CTS執行完的結果，接下來我們會對Clock Tree做Display和晶片的timing分析



儲存成cts.enc



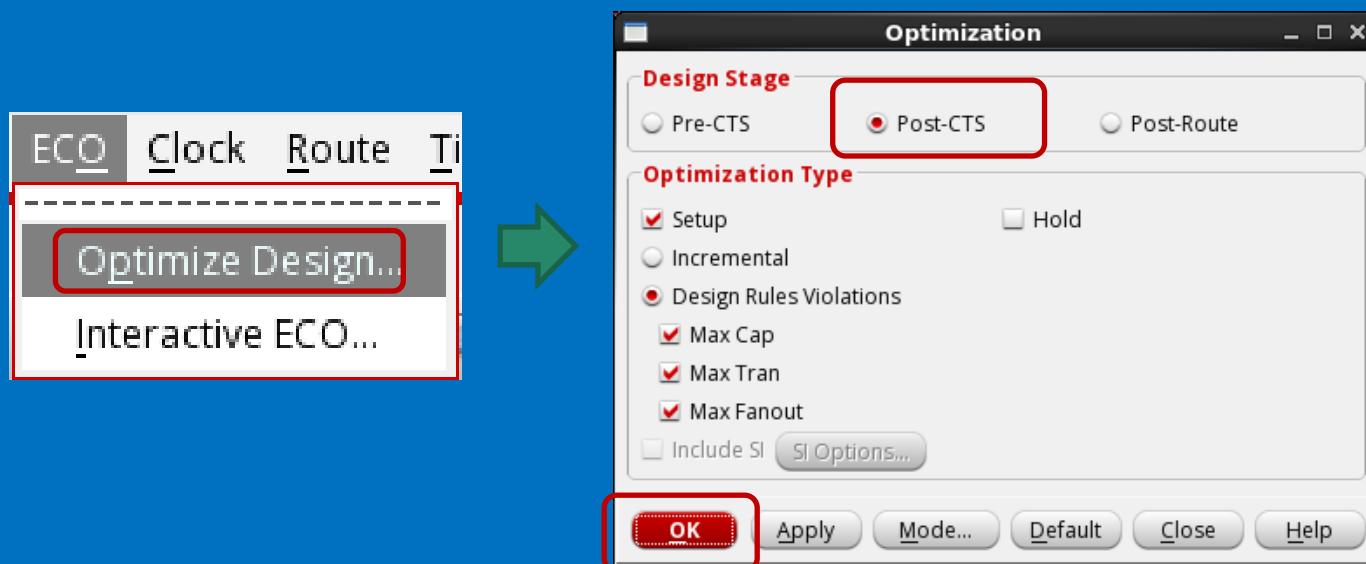
# Timing Analysis



Setup mode	all	reg2reg	in2reg	reg2out	in2out	default	
WNS (ns):	0.023	4.230	0.023	0.325	N/A	0.000	
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000	
Violating Paths:	0	0	0	0	N/A	0	
All Paths:	36	8	19	9	N/A	0	



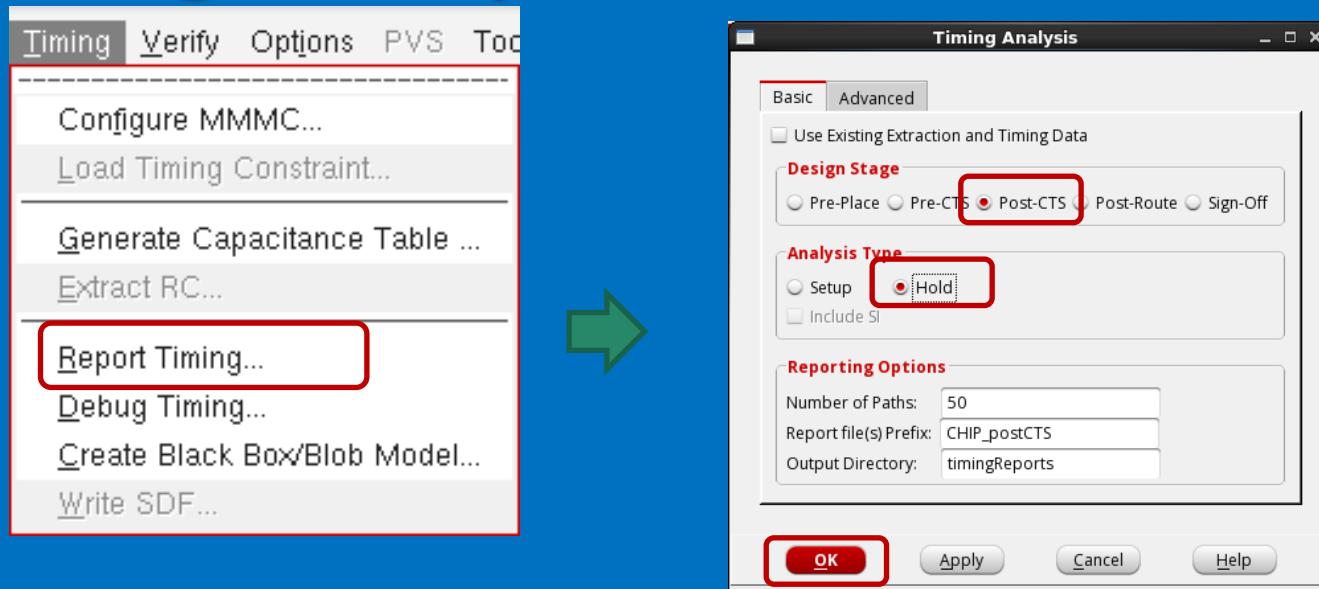
# Timing Optimization



Setup mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	0.023	4.230	0.023	0.325	N/A	0.000
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	N/A	0
All Paths:	36	8	19	9	N/A	0



# Timing Analysis



```
t106368059@islabx7:SOC
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)

timeDesign Summary

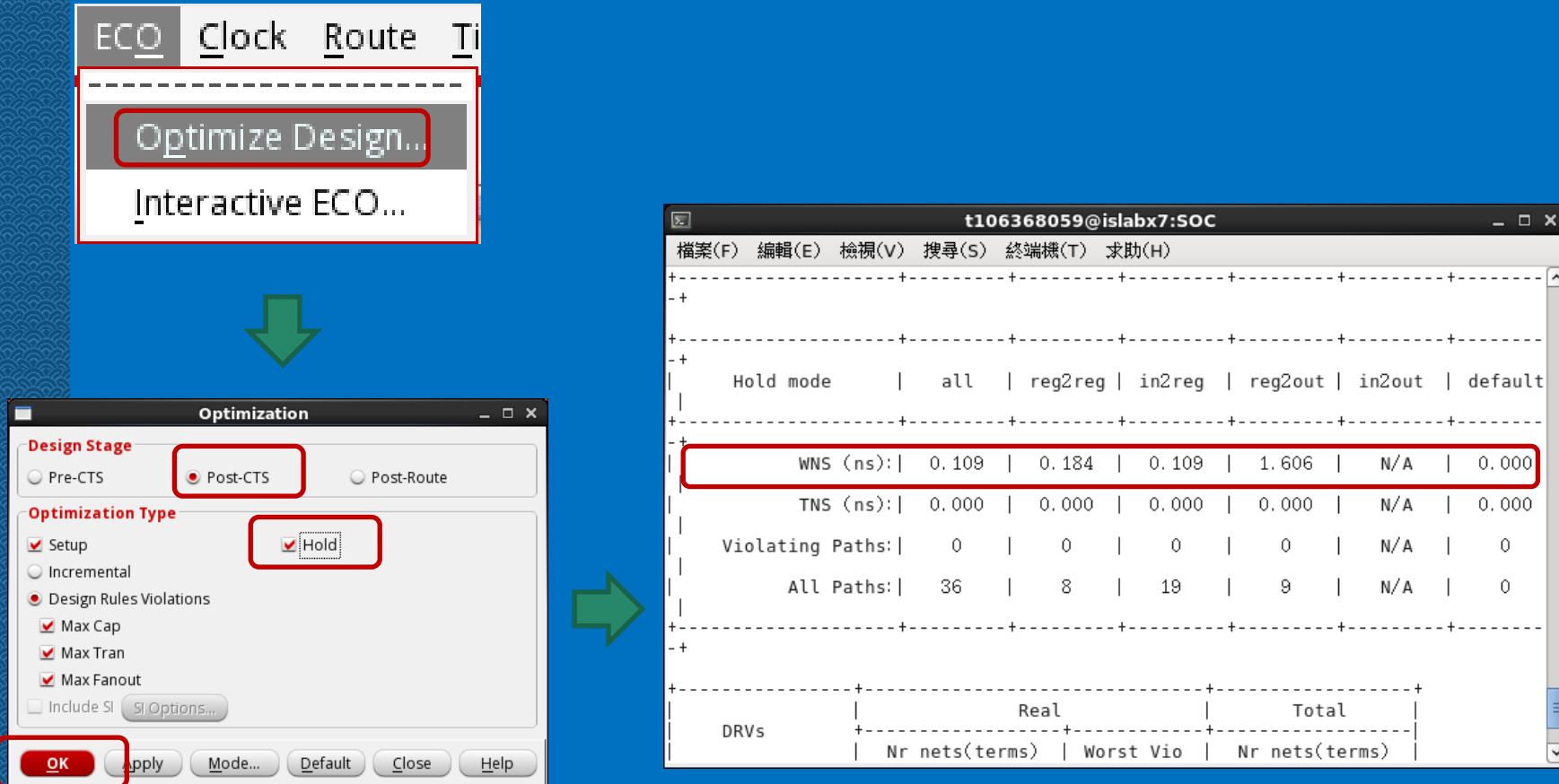
Hold views included:
av_func_mode_min

+-----+-----+-----+-----+-----+
| Hold mode | all | reg2reg | in2reg | regout | in2out | default |
+-----+-----+-----+-----+-----+
| WNS (ns): | -0.577 | 0.184 | -0.577 | 1.606 | N/A | 0.000 |
| TNS (ns): | -5.758 | 0.000 | -5.758 | 0.000 | N/A | 0.000 |
| Violating Paths: | 10 | 0 | 10 | 0 | N/A | 0 |
| All Paths: | 36 | 8 | 19 | 9 | N/A | 0 |
+-----+-----+-----+-----+-----+
```

若只有些微的負slack  
可等到Routing結束後  
再看看是否仍為負

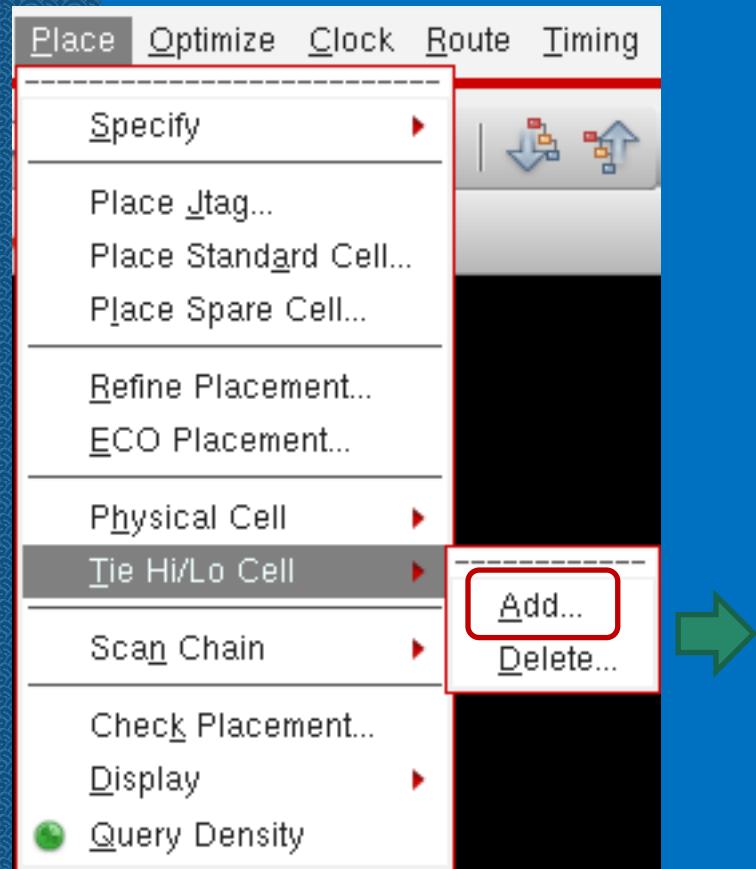


# Timing Optimization





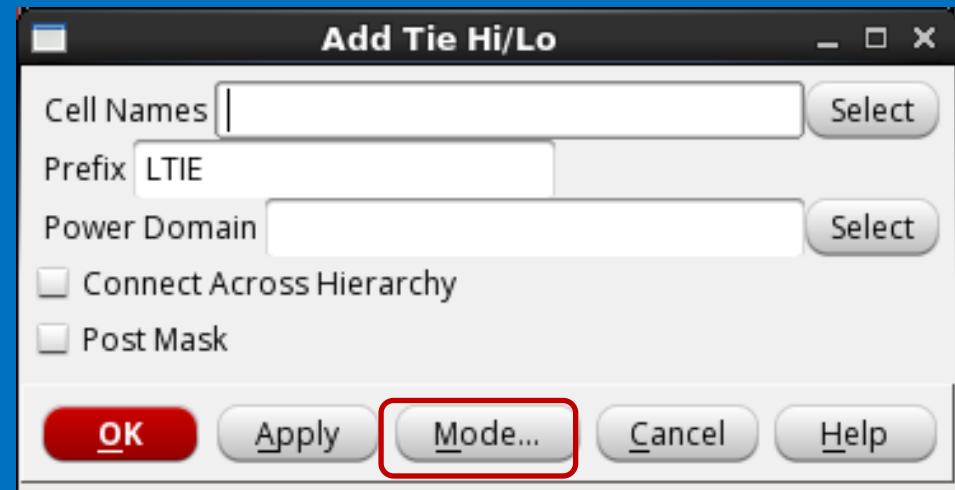
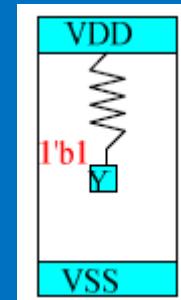
# Add Tie Hi/Lo



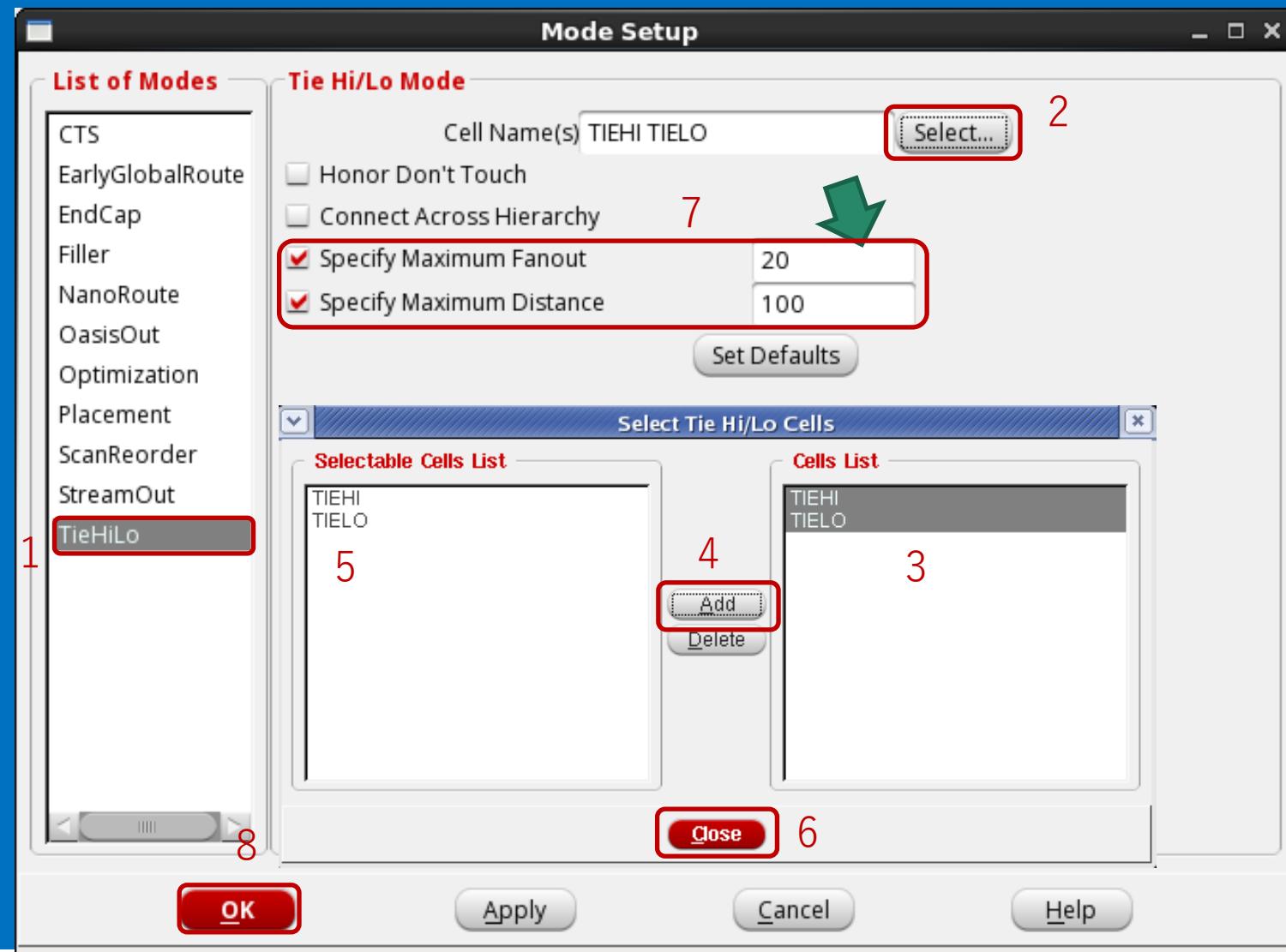
◆ 加入 Tie Hi/Lo

For ESD protection

◆ Tie Hi 只有一個 Output，  
將 VDD 經 Output 連到 1'b1，  
Tie Hi 具有保護電路，可  
以避免 ESD



# Add Tie Hi/Lo



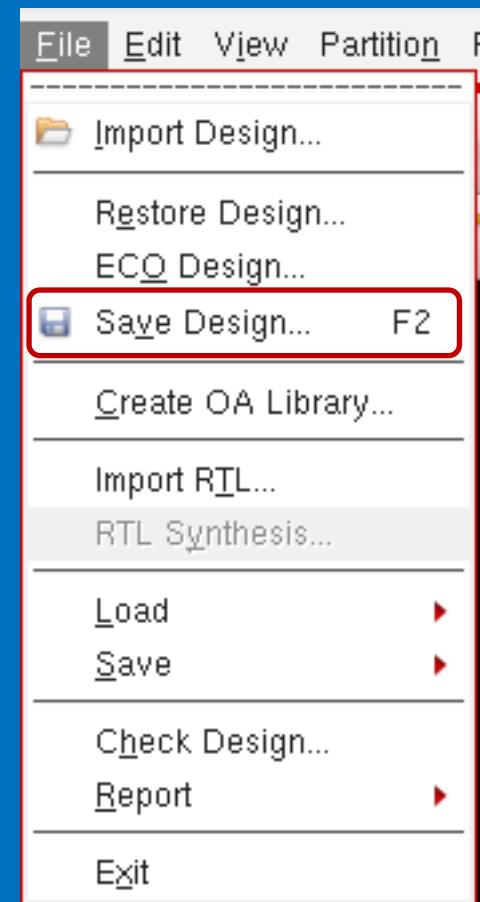


# Add Tie Hi/Lo



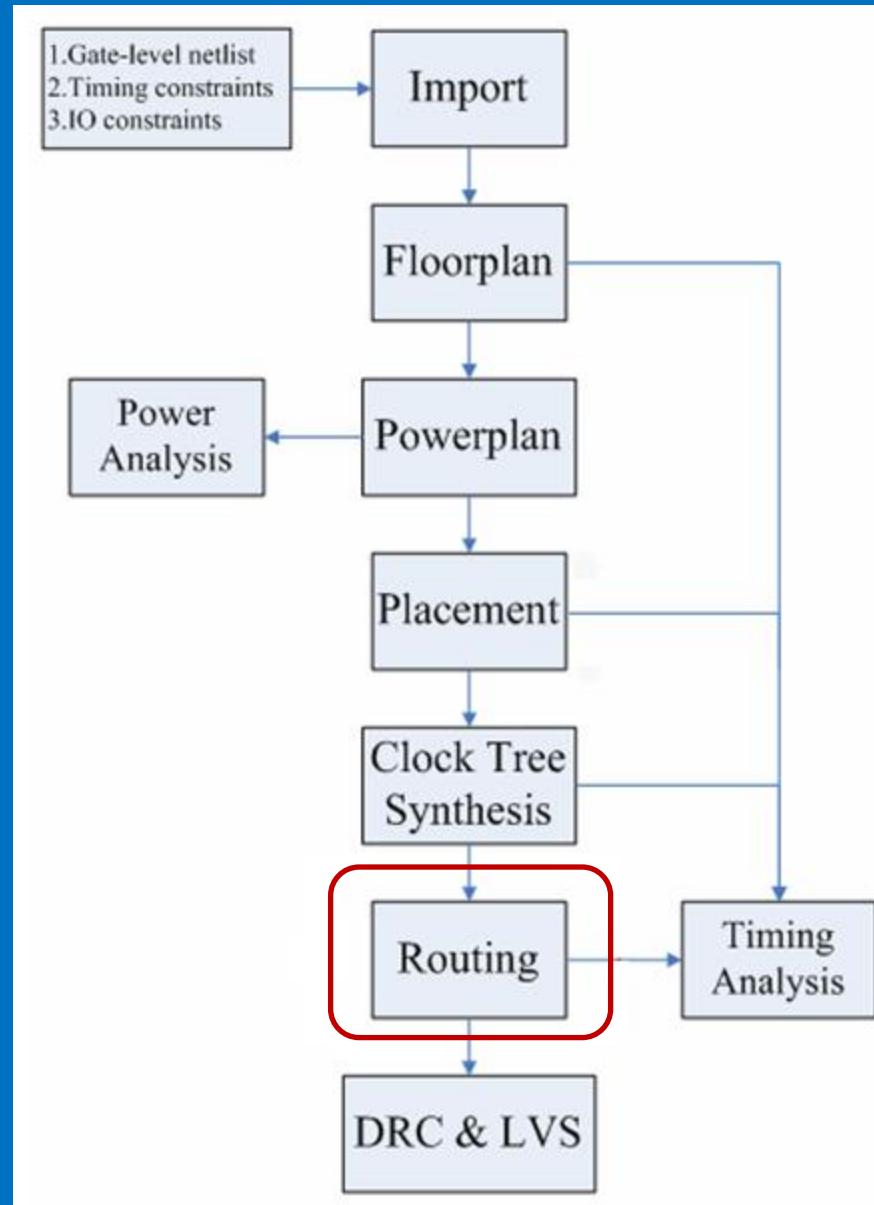
```
t106368059@islabx7:SOC
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
Re-routed 1 nets
INFO: Total Number of Tie Cells (TIEHI) placed: 1
INFO: Total Number of Tie Cells (TIELO) placed: 0
innovus 2>
```

會視電路情況加入 Tie High/Low  
因此也有可能出現0

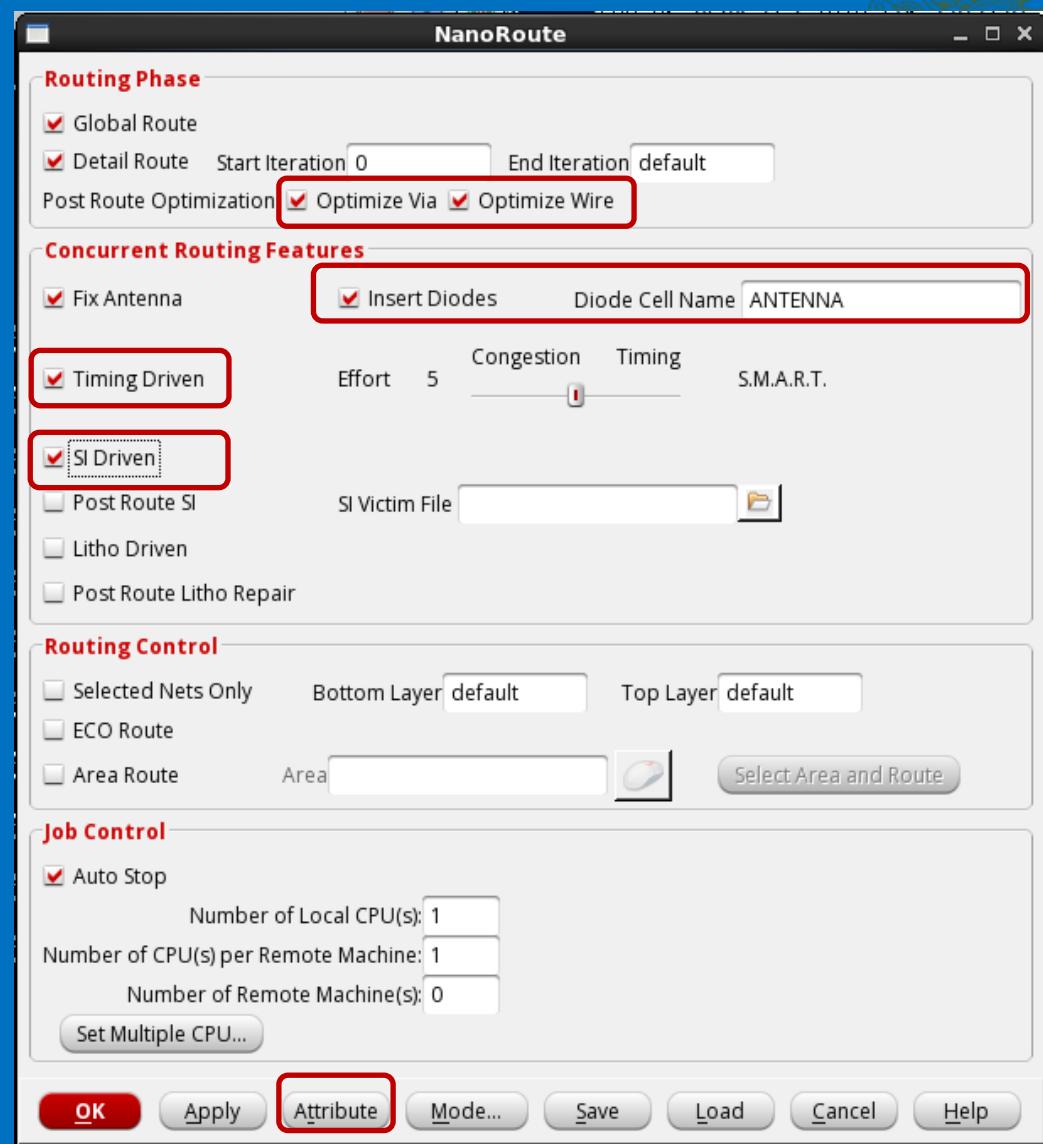
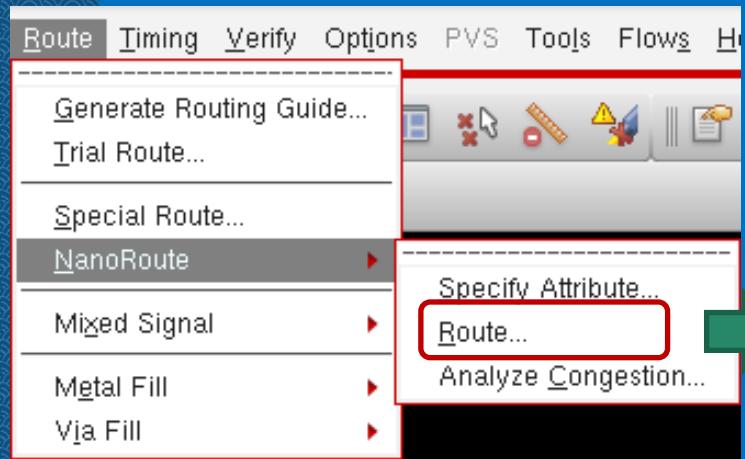


存檔成cts\_hilo.enc

# Routing



# Route





# Route

### Route Attributes

**Net Attributes**

Net Type(s):  Clock Nets  External Nets  Critical Nets  Selected Nets

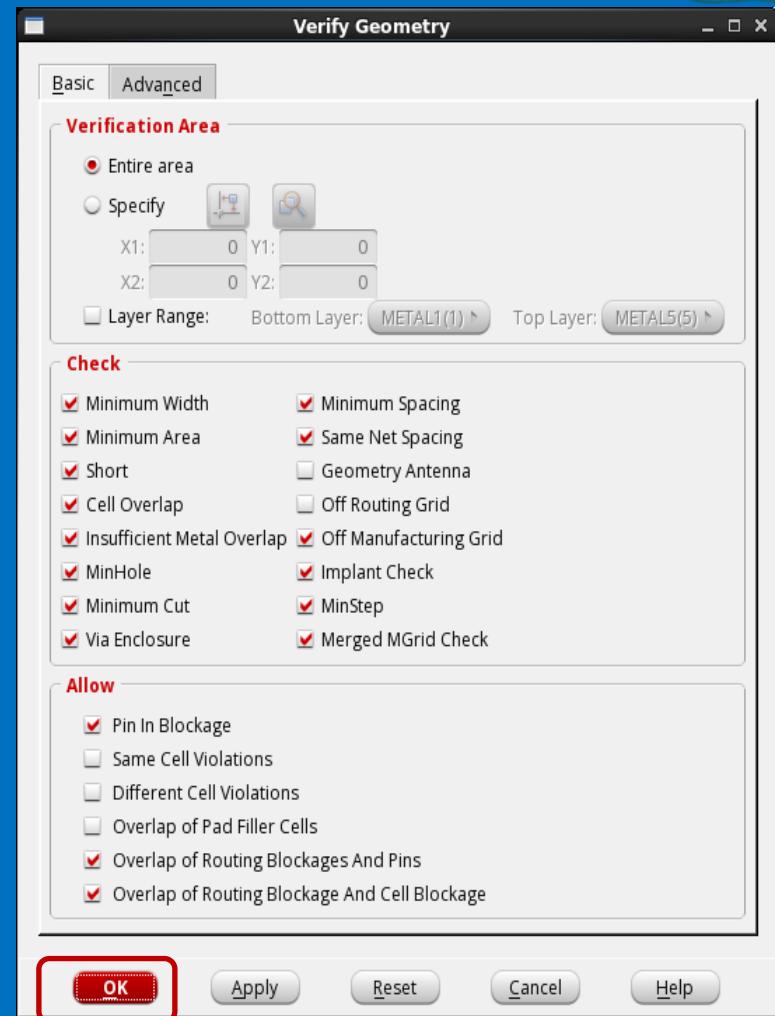
Net Name(s):

Skip Antenna	<input type="radio"/> TRUE	<input type="radio"/> FALSE	<input checked="" type="radio"/> ASIS	Top Layer ASIS	Bottom Layer ASIS
Skip Routing	<input type="radio"/> TRUE	<input type="radio"/> FALSE	<input checked="" type="radio"/> ASIS	Weight 10	Spacing 1
Avoid Detour	<input type="radio"/> TRUE	<input type="radio"/> FALSE	<input checked="" type="radio"/> ASIS	Shield Net(s) ASIS	
SI Prevention	<input type="radio"/> TRUE	<input type="radio"/> FALSE	<input checked="" type="radio"/> ASIS	Nondefault Rule ASIS	
SI Post Route Fix	<input type="radio"/> TRUE	<input type="radio"/> FALSE	<input checked="" type="radio"/> ASIS	Pattern ASIS	

**Buttons:** **OK** **Apply** **Select** **Cancel** **Help**



# Verify(可略)



```
t106368059@islabx7:SOC
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 55.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary

Verification Complete : 0 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:55.0 MEM: 7486.8M)

innovus 8>
```

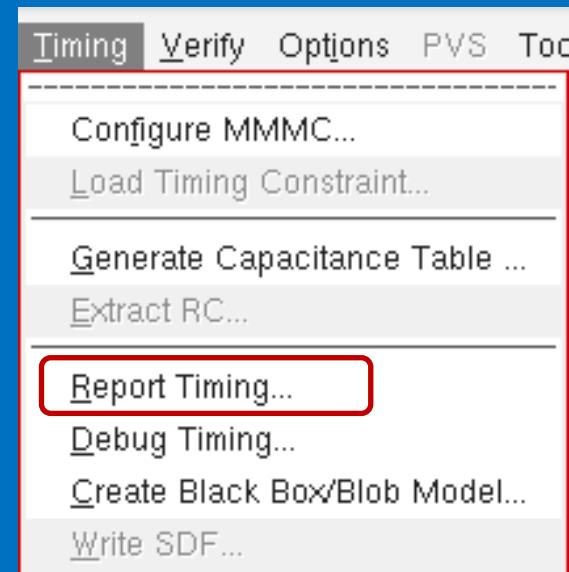
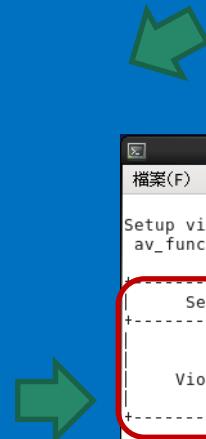
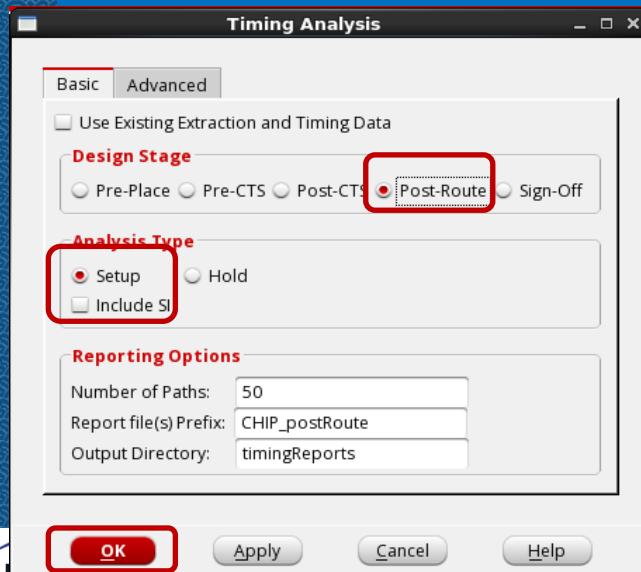




# Timing Analysis

◆innovus >

setAnalysisMode - analysisType onChipVariation



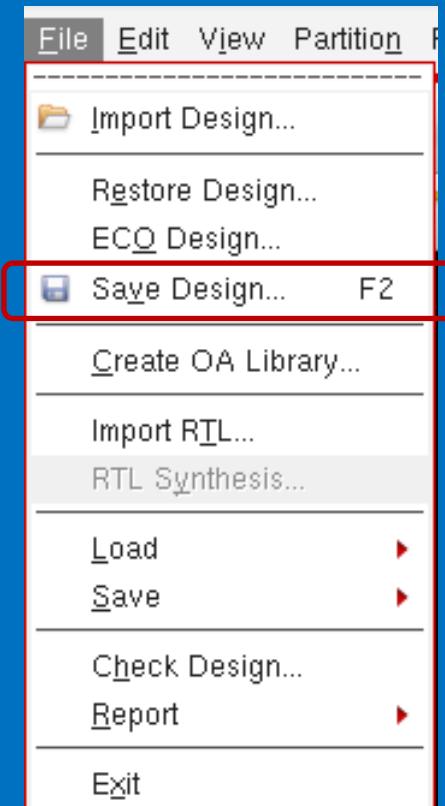
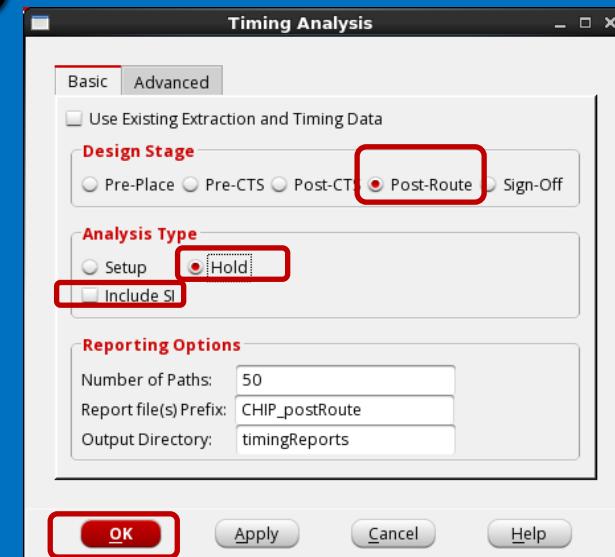
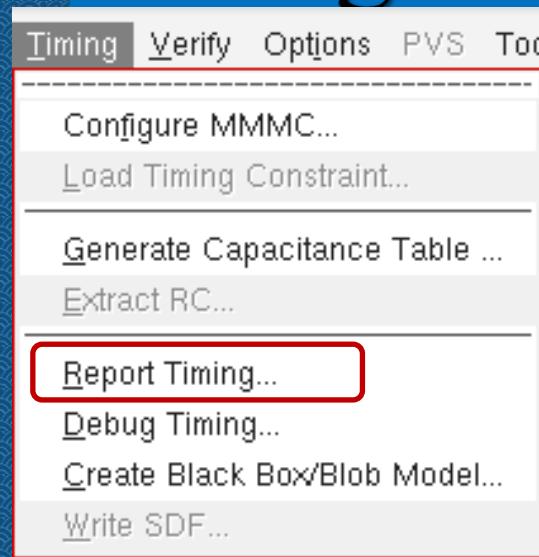
Setup mode	all	reg2reg	default
WNS (ns):	0.051	4.238	0.051
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	36	8	28

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	21 (21)
max_fanout	0 (0)	0	21 (21)
max_length	0 (0)	0	0 (0)



# Timing Analysis

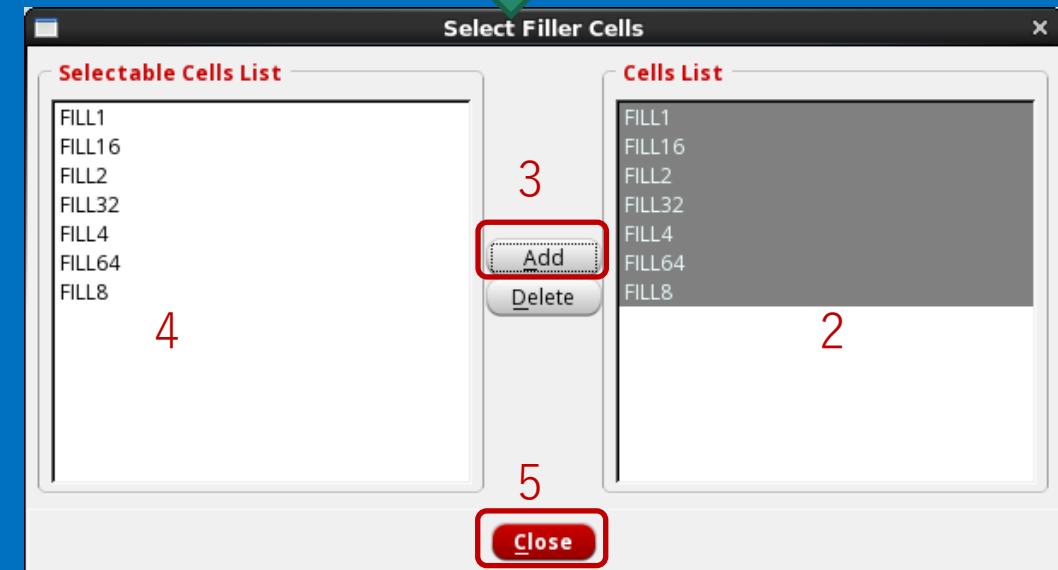
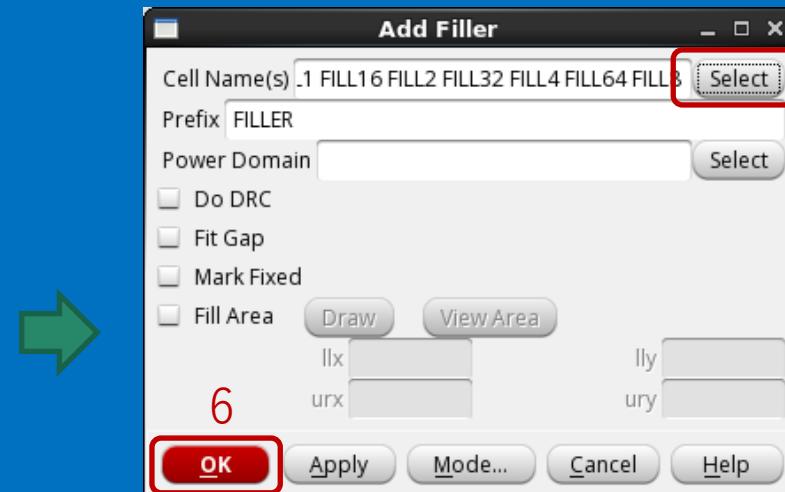
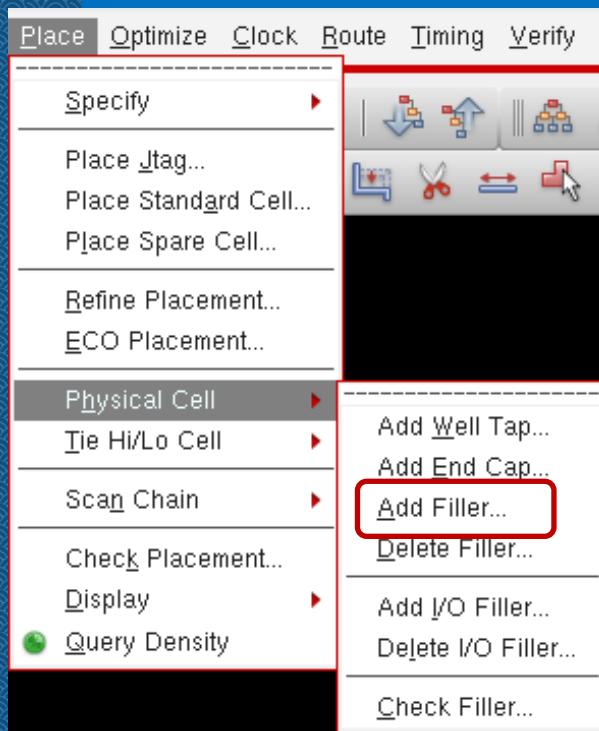


存檔成route.enc

timeDesign Summary							
Hold views included: av_func_mode_min							
Hold mode	all	reg2reg	in2reg	reg2out	in2out	default	
WNS (ns):	0.101	0.184	0.101	1.606	N/A	0.000	
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000	
Violating Paths:	0	0	0	0	N/A	0	
All Paths:	36	8	19	9	N/A	0	



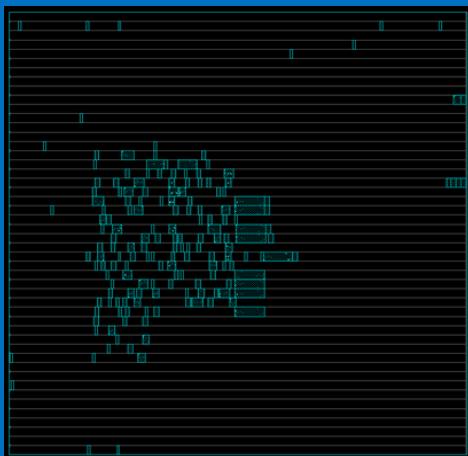
# Add Filler



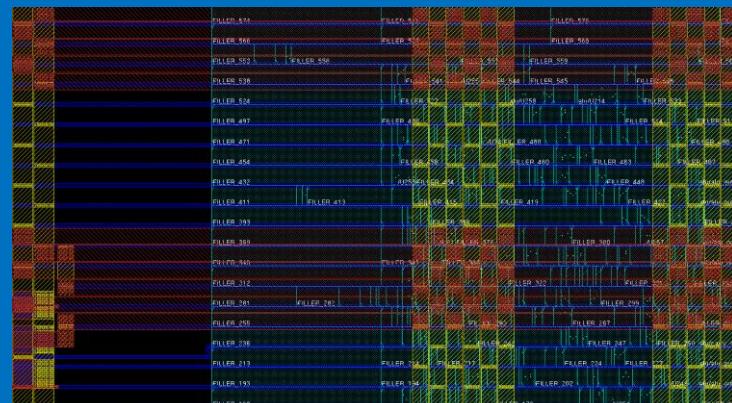
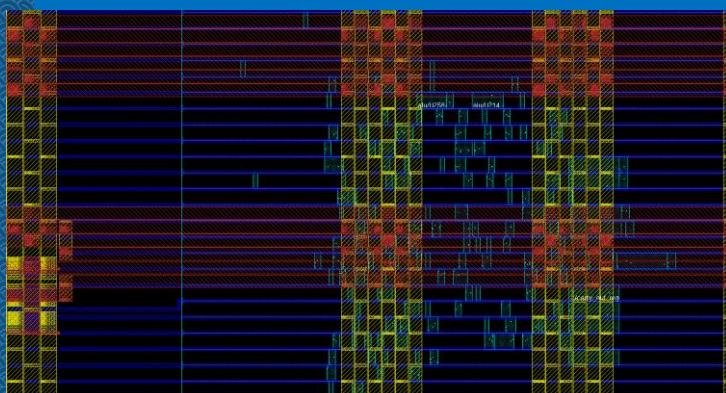


# Add Filler

- ◆ Core Filler會將core間的空隙填滿，以連接NWELL/PWELL layer，如圖所示

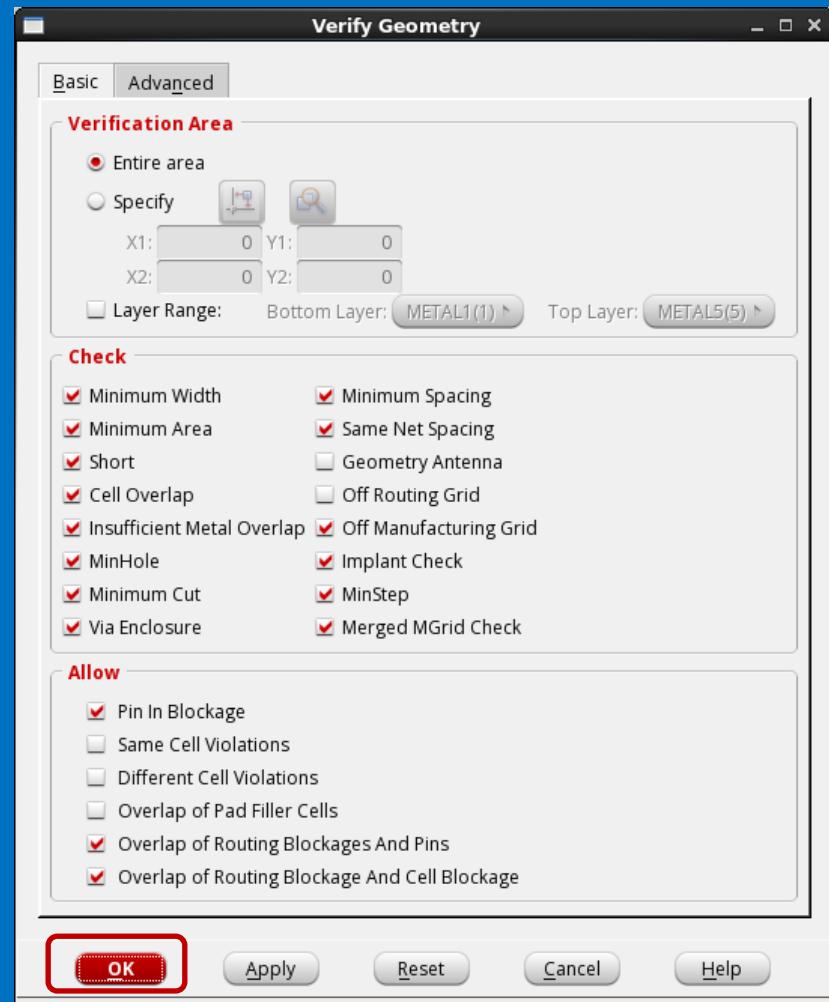
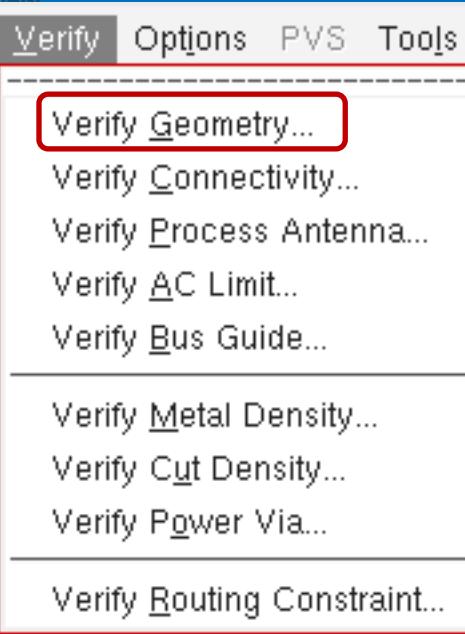


FILLER_699	FILLER_699	FILLER_691	FILLER_692	FILLER_675	FILLER_693
FILLER_692	FILLER_692	FILLER_677	FILLER_678	FILLER_690	FILLER_690
FILLER_691	FILLER_691	FILLER_653	FILLER_654	FILLER_655	FILLER_656
FILLER_641	FILLER_641	FILLER_643	FILLER_643	FILLER_639	FILLER_647
FILLER_626	FILLER_626	FILLER_627	FILLER_627	FILLER_629	FILLER_629
FILLER_617	FILLER_617	FILLER_619	FILLER_620	FILLER_621	FILLER_621
FILLER_601	FILLER_601	FILLER_602	FILLER_603	FILLER_604	FILLER_605
FILLER_593	FILLER_594	FILLER_595	FILLER_596	FILLER_597	FILLER_597
FILLER_574	FILLER_575	FILLER_576	FILLER_577	FILLER_578	FILLER_578
FILLER_565	FILLER_567	FILLER_568	FILLER_569	FILLER_570	FILLER_570
FILLER_556	FILLER_556	FILLER_561	FILLER_560	FILLER_562	FILLER_556
FILLER_497	FILLER_497	FILLER_498	FILLER_499	FILLER_517	FILLER_518
FILLER_471	FILLER_471	FILLER_472	FILLER_473	FILLER_490	FILLER_491
FILLER_432	FILLER_432	FILLER_433	FILLER_434	FILLER_457	FILLER_452
FILLER_391	FILLER_391	FILLER_392	FILLER_393	FILLER_422	FILLER_430
FILLER_363	FILLER_363	FILLER_364	FILLER_365	FILLER_366	FILLER_367
FILLER_340	FILLER_340	FILLER_341	FILLER_342	FILLER_361	FILLER_364
FILLER_311	FILLER_311	FILLER_312	FILLER_313	FILLER_324	FILLER_324
FILLER_295	FILLER_295	FILLER_296	FILLER_297	FILLER_308	FILLER_309
FILLER_274	FILLER_274	FILLER_275	FILLER_276	FILLER_324	FILLER_325
FILLER_253	FILLER_253	FILLER_254	FILLER_255	FILLER_351	FILLER_352
FILLER_213	FILLER_213	FILLER_214	FILLER_215	FILLER_232	FILLER_233
FILLER_193	FILLER_193	FILLER_194	FILLER_195	FILLER_209	FILLER_210
FILLER_149	FILLER_149	FILLER_149	FILLER_150	FILLER_165	FILLER_166
FILLER_135	FILLER_135	FILLER_140	FILLER_141	FILLER_144	FILLER_145
FILLER_122	FILLER_122	FILLER_127	FILLER_128	FILLER_159	FILLER_160
FILLER_110	FILLER_110	FILLER_111	FILLER_112	FILLER_119	FILLER_120
FILLER_95	FILLER_95	FILLER_97	FILLER_98	FILLER_91	FILLER_92
FILLER_76	FILLER_77	FILLER_78	FILLER_79	FILLER_80	FILLER_81
FILLER_61	FILLER_61	FILLER_62	FILLER_63	FILLER_85	FILLER_86
FILLER_52	FILLER_52	FILLER_54	FILLER_55	FILLER_56	FILLER_57
FILLER_44	FILLER_44	FILLER_46	FILLER_47	FILLER_48	FILLER_49
FILLER_28	FILLER_28	FILLER_29	FILLER_30	FILLER_31	FILLER_32
FILLER_20	FILLER_20	FILLER_21	FILLER_22	FILLER_23	FILLER_24
FILLER_13	FILLER_13	FILLER_14	FILLER_15	FILLER_16	FILLER_17
FILLER_1	FILLER_1	FILLER_5	FILLER_6	FILLER_7	FILLER_8





# Verify



```
t106368059@islabx7:SOC
VERIFY GEOMETRY ..... Starting Verification
VERIFY GEOMETRY ..... Initializing
VERIFY GEOMETRY ..... Deleting Existing Violations
VERIFY GEOMETRY ..... Creating Sub-Areas
VERIFY ..... bin size: 7040
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 54.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary
Verification Complete : 0 Viols. 0 Wrngs.
*****End: VERIFY GEOMETRY*****
```



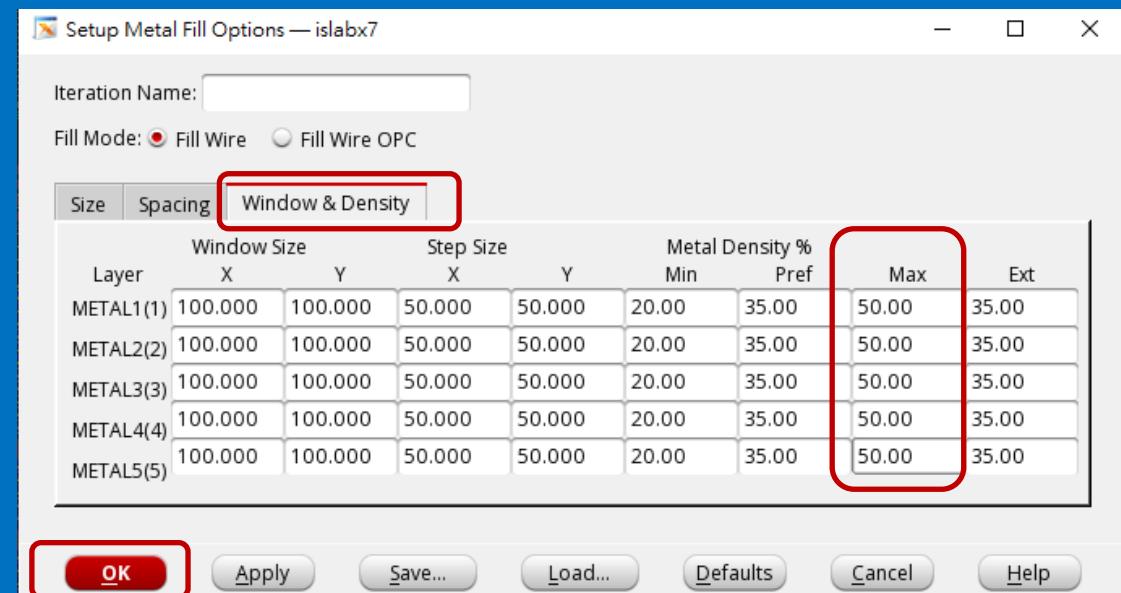
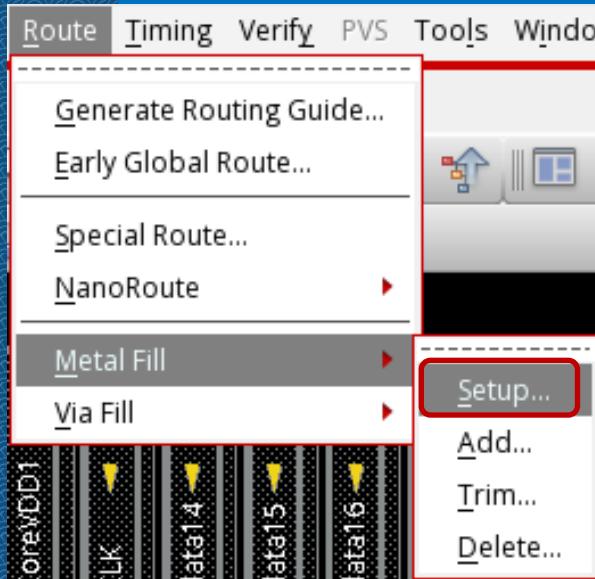
# Save Design



存檔成Corefiller.enc

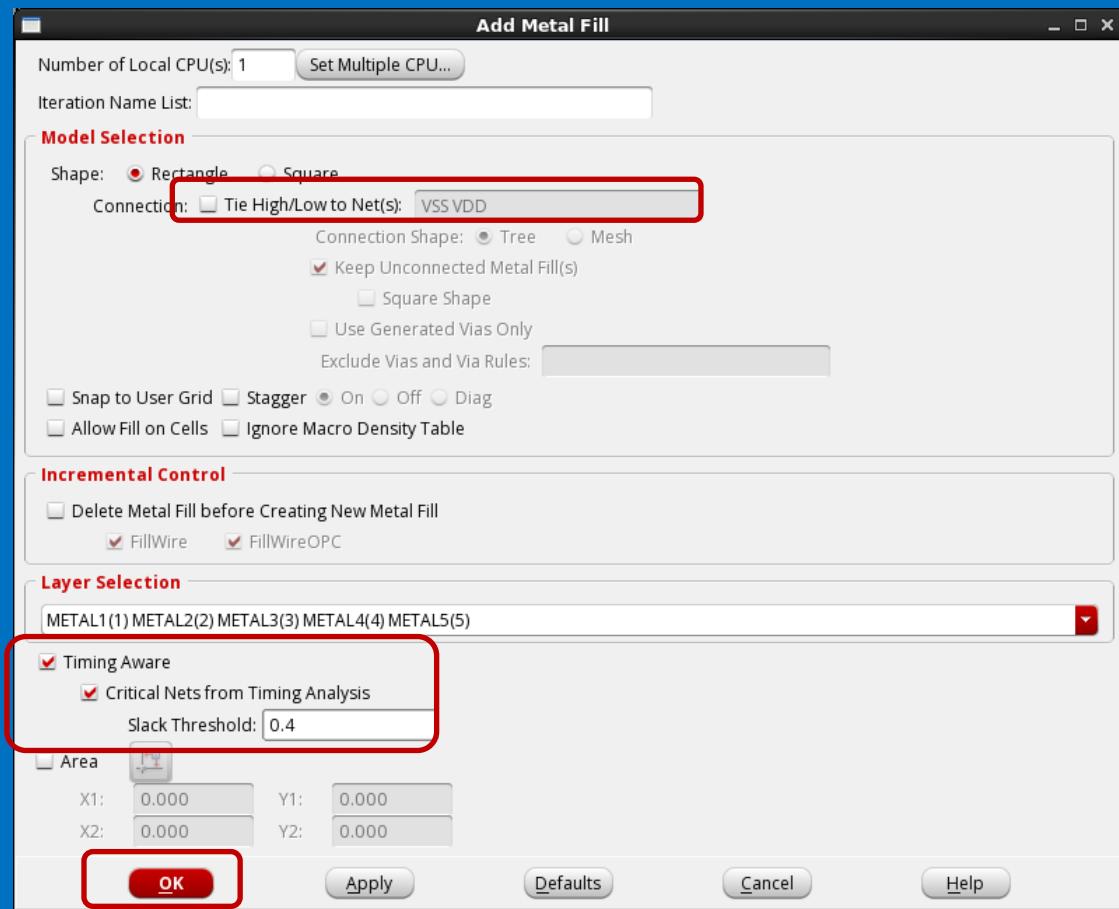
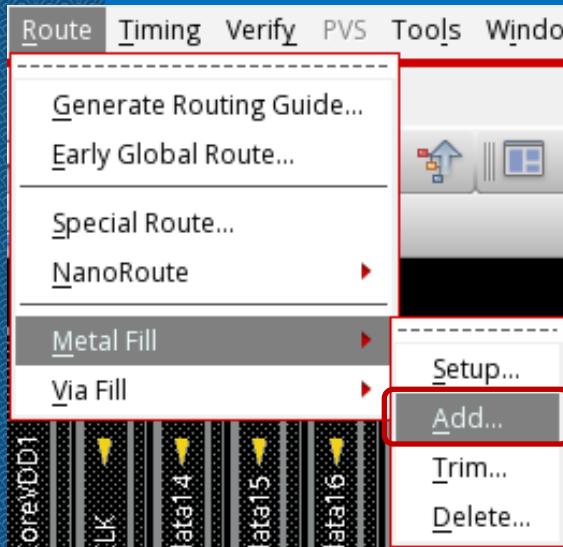


# Metal Fill





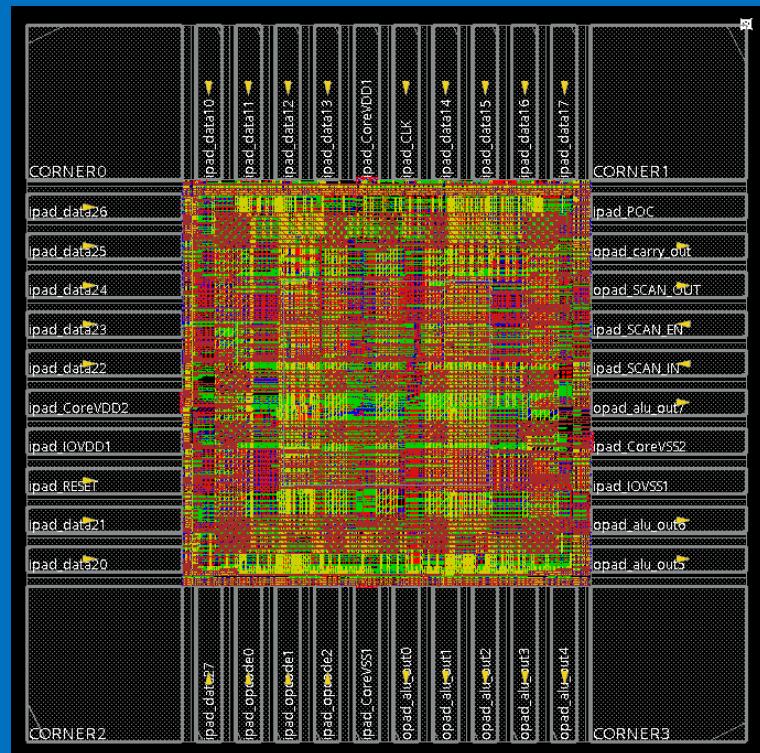
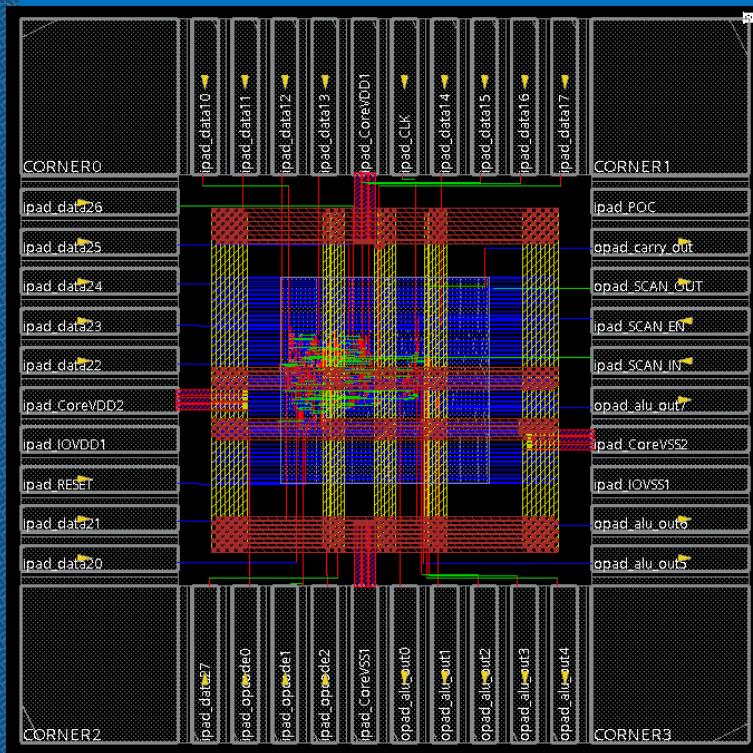
# Metal Fill





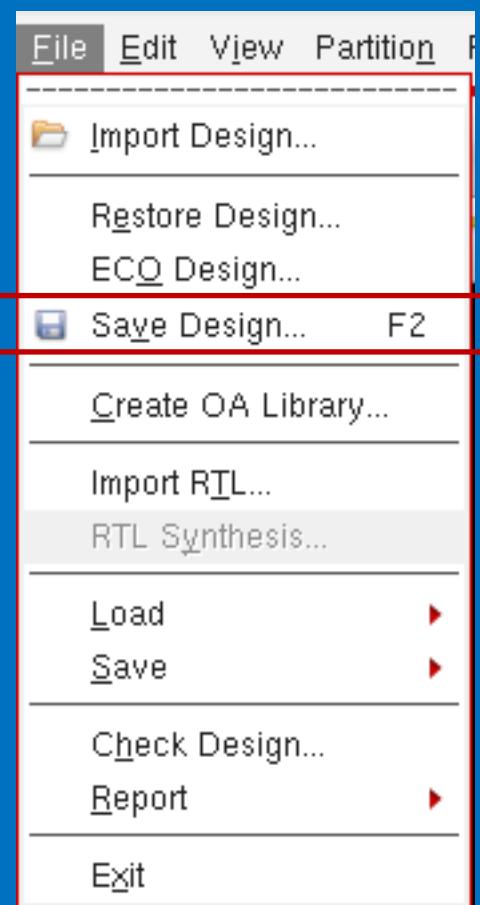
# Metal Fill

◆ 可以看到整個layout全部被dummy metal填滿





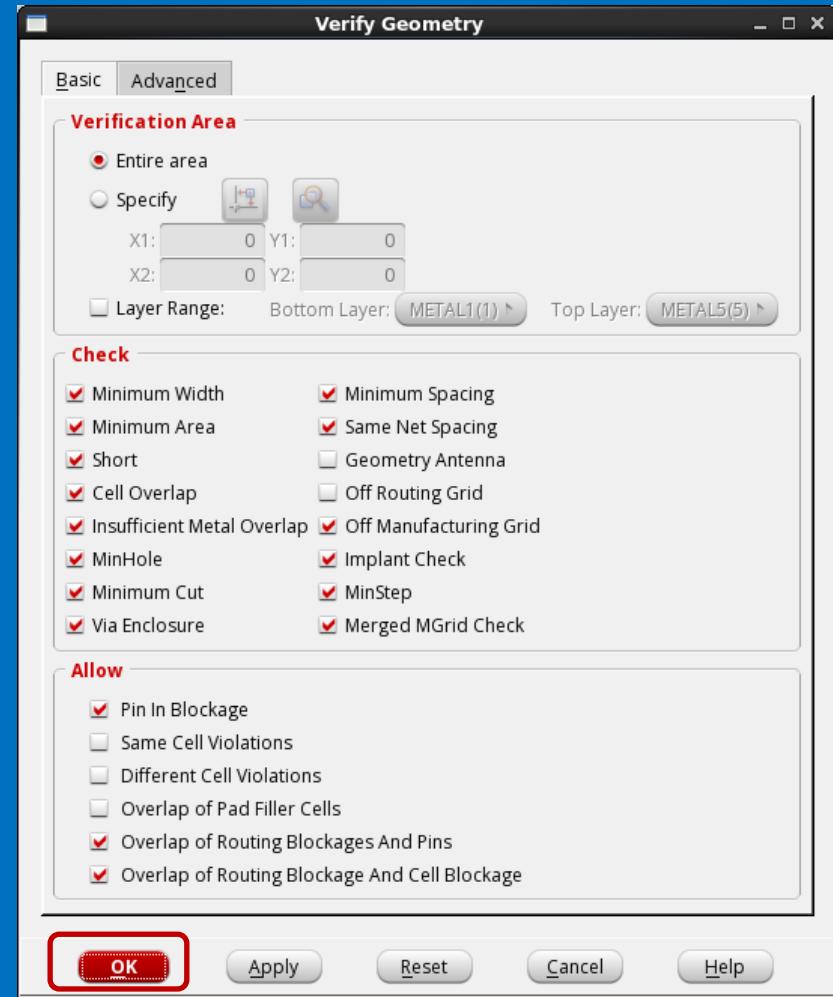
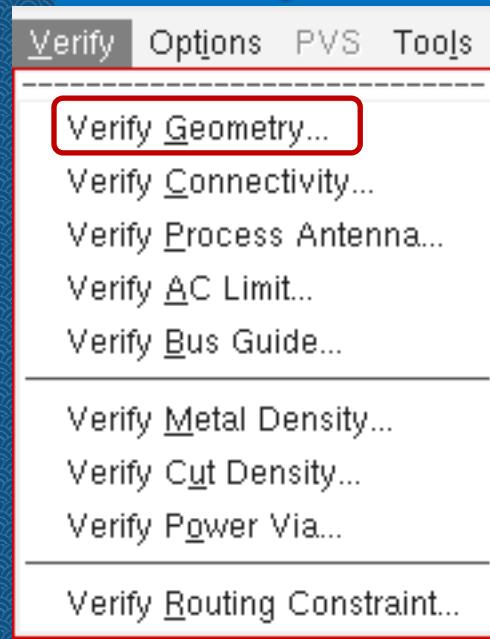
# Save Design



存檔成metalfill.enc



# Verify



```
t106368059@islabx7:SOC
[...]
VERIFY GEOMETRY ..... Sub-Area : 3 complete 0 Viols. 0 Wrngs.
VERIFY GEOMETRY ..... SubArea : 4 of 4
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 4 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 56.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary
Verification Complete : 0 Viols. 0 Wrngs.
*****END: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:56.5 MEM: 2131.7M)
innovus 1> **INFO (INTERRUPT): One more Ctrl-C to exit Innovus ...
```



# Verify

Verify PVS Tools Windows

Verify Geometry...  
Verify DRC...  
**Verify Connectivity...**  
Verify Process Antenna...  
Verify AC Limit...  
Verify End Cap...

Verify Metal Density...  
Verify Cut Density...  
Verify Power Via...

→

**Verify Connectivity**

**Net Type**  
 All  
 Regular Only  
 Special Only

**Nets**  
 All  
 Selected  
 Named:

**Check**

<input checked="" type="checkbox"/> Open	<input checked="" type="checkbox"/> UnConnected Pin	<input checked="" type="checkbox"/> Unrouted Net
<input type="checkbox"/> Connectivity Loop	<input checked="" type="checkbox"/> DanglingWire (Antenna)	<input checked="" type="checkbox"/> Weakly Connected Pin
<input type="checkbox"/> Geometry Loop	<input type="checkbox"/> Geometry Connectivity	<input type="checkbox"/> Keep Previous Results
<input type="checkbox"/> Divide Power Net	<input type="checkbox"/> Soft PG Connect	<input type="checkbox"/> Raw Violations Mark
<input type="checkbox"/> Use new open Vio	<input type="checkbox"/> Remove old open Vio	<input type="checkbox"/> Use Virtual Connection
<input type="checkbox"/> TSV Die Abstract File <input type="file"/>		

Verify Connectivity Report: CHIP.conn.rpt

**Report Limits**  
 Error: 1000  
 Warning: 50

**Set Multiple CPU...**

**OK** **Apply** **Cancel** **Help**

t106368059@islabx7:SOC

檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)

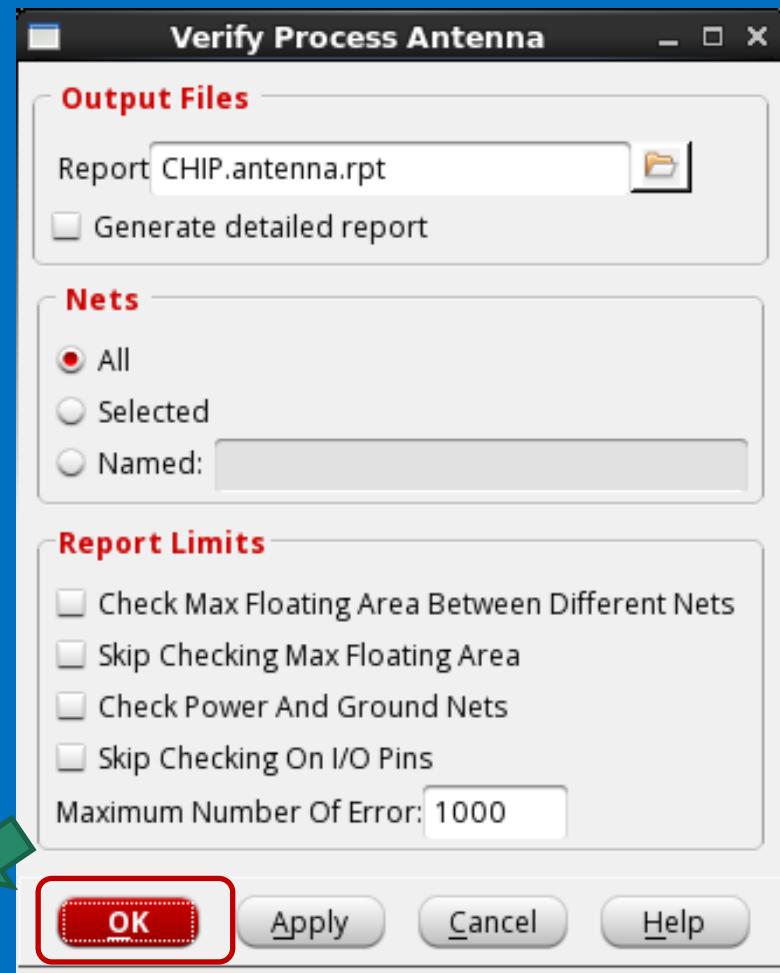
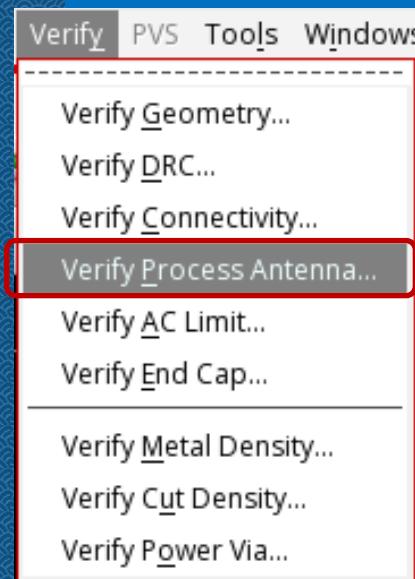
End Time: Wed Aug 15 21:35:50 2018  
 Time Elapsed: 0:00:00.0

\*\*\*\*\* End: VERIFY CONNECTIVITY \*\*\*\*\*  
 Verification Complete : 0 Viols. 0 Wrngs.  
 (CPU Time: 0:00:00.0 MEM: 0.000M)

innovus Z>

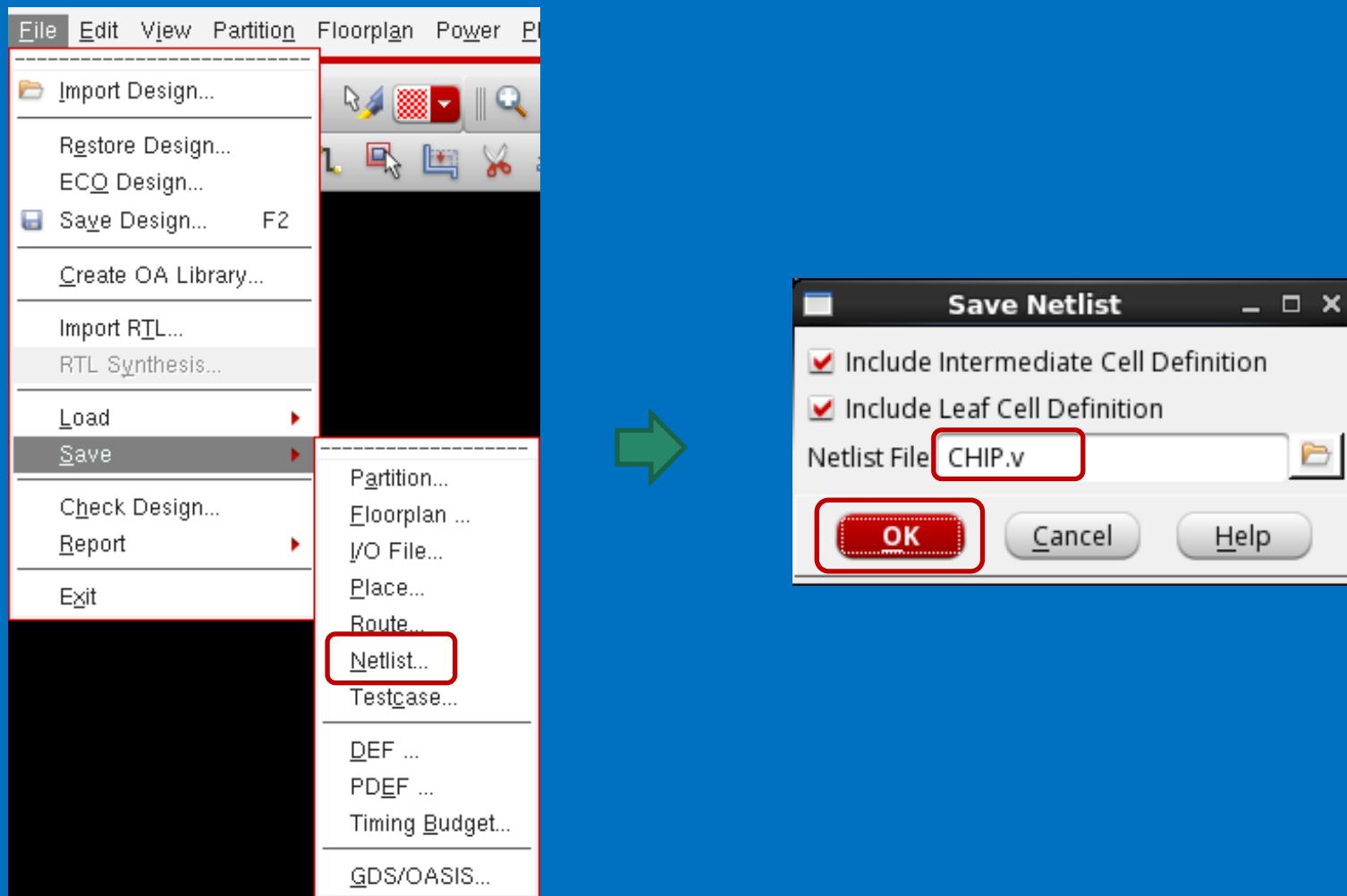


# Verify





# Save Netlist





# Save .sdf

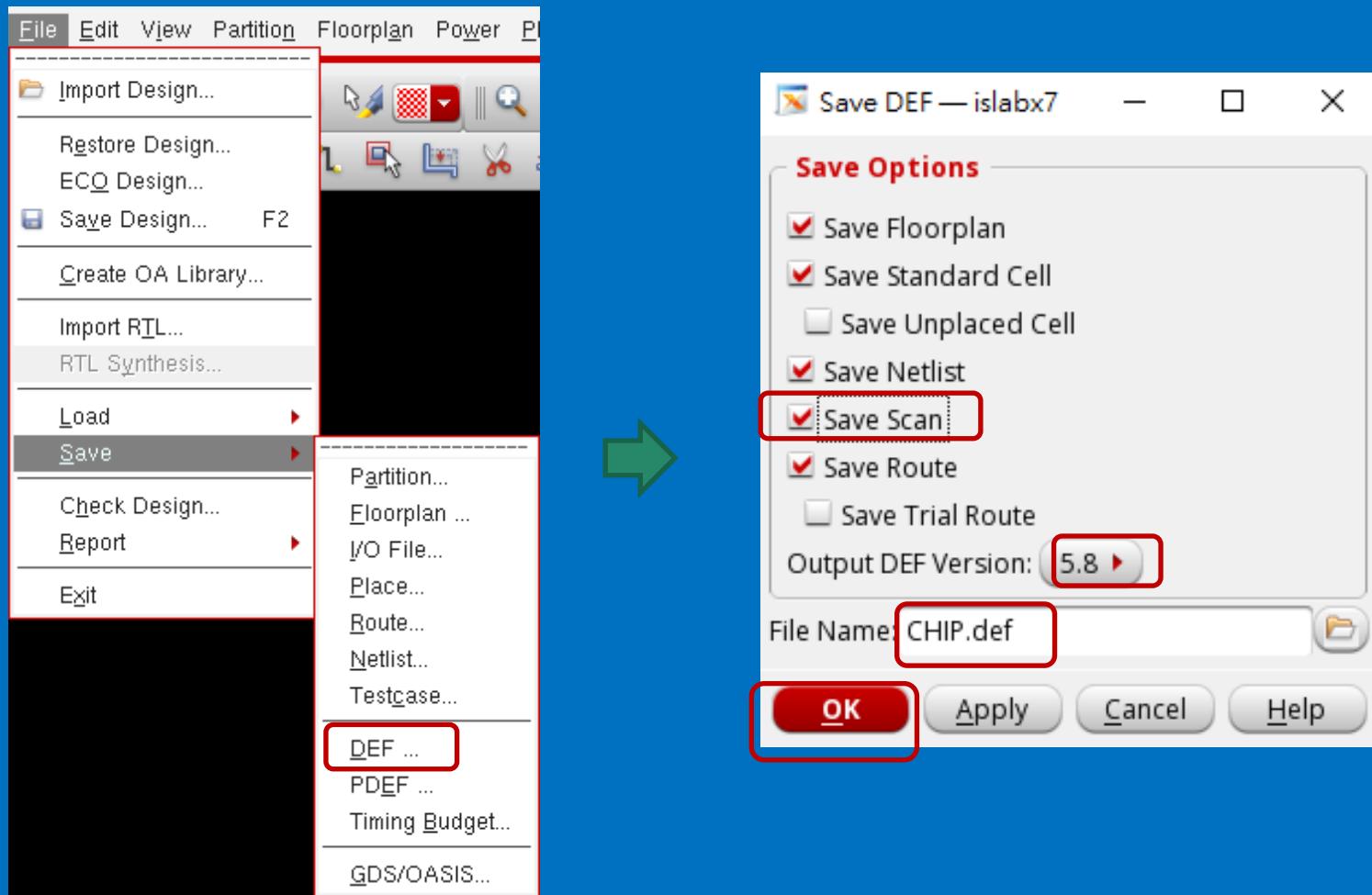
- ◆ innovus > setAnalysisMode -analysisType bcwc
- ◆ innovus > write\_sdf -max\_view av\_func\_mode\_max -min\_view av\_func\_mode\_min -edges noedge -splitsetuphold -remashold -splitrecr -min\_period\_edges none CHIP.sdf
- ◆ 因為GUI無法設定一些參數，所以我們使用指令的方式存.sdf檔

```
t106368059@islabx7:SOC
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
innovus 1>
innovus 1> setAnalysisMode -analysisType bcwc
innovus 2> write_sdf -max_view av_func_mode_max -min_view av_func_mode_min -edges noedge -splitsetuphold -remashold -splitrecr -min_period_edges none CHIP.sdf
**WARNING: (SDF-808): The software is currently operating in a high performance mode which optimizes the handling of multiple timing arcs between input and output pins in pairs. With the current settings, the SDF file generated will contain the same delay information for all of these arcs. To have the SDF recalculated with explicit pin pair data, you should use the option '-recompute_parallel_arcs'. This setting is recommended for generating SDF for functional simulation applications.
Starting SI iteration 1 using Infinite Timing Windows
#####
# Design Stage: PostRoute
# Design Name: CHIP
# Design Mode: 90nm
# Analysis Mode: MMMC Non-OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI On
#####
Extraction called for design 'CHIP' of instances=3899 and nets=221 using extraction engine 'postRoute' at effort level 'low'.
**WARNING: (IMPEXT-3530): The process node is not set. Use the command setDesignMode -process <process node> prior to extraction for maximum accuracy and optimal automatic threshold setting.
Type 'man IMPEXT-3530' for more detail.
PostRoute (effortLevel low) RC Extraction called for design CHIP.
RC Extraction called in multi-corner(1) mode.
Process corner(s) are loaded.
Corner: RC_corner
extractDetailRC Option : -outfile /tmp/innovus_temp_115682_islabx7_t106368059_kLfdi0/CHIP_115682_Yjvy0Z.rcdb.d -extended
```





# Save .def



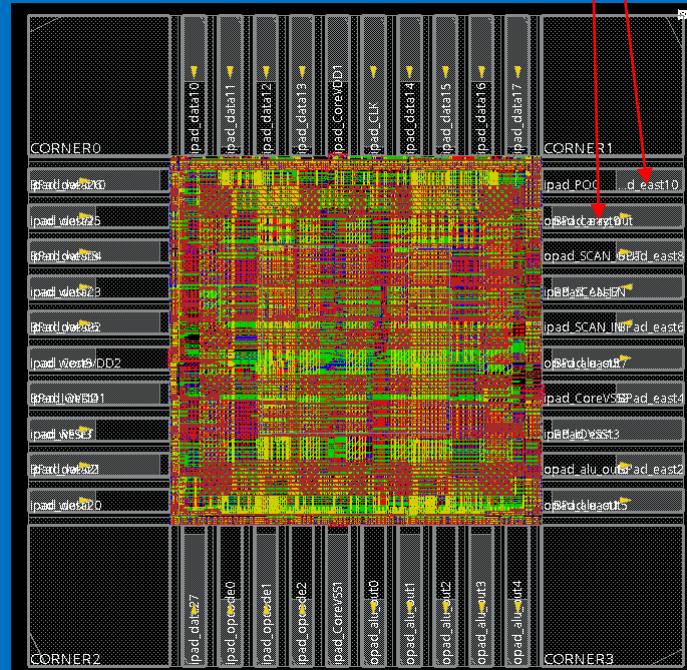
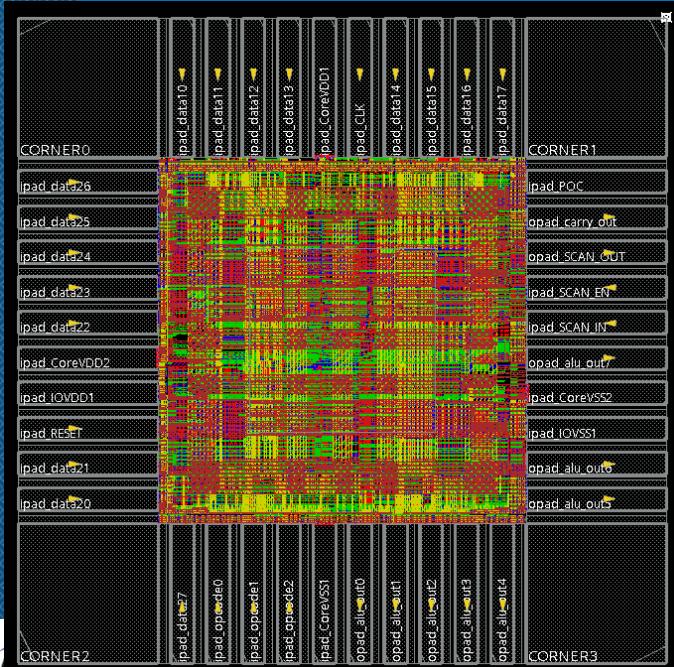


# Add Bounding Pads

灰色的地方為打線的Pad

- ◆ innovus > source addbond.cmd

```
t106368059@islabx7:SOC
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
which is outside of core box.
**WARN: (IMPSYC-6308): Instance 'BPad_north9' is placed at (1155800, 1531700) w
hich is outside of core box.
**WARN: (IMPSYC-6308): Instance 'BPad_north10' is placed at (1249780, 1361700)
which is outside of core box.
innovus 2> source addbond.cmd
```



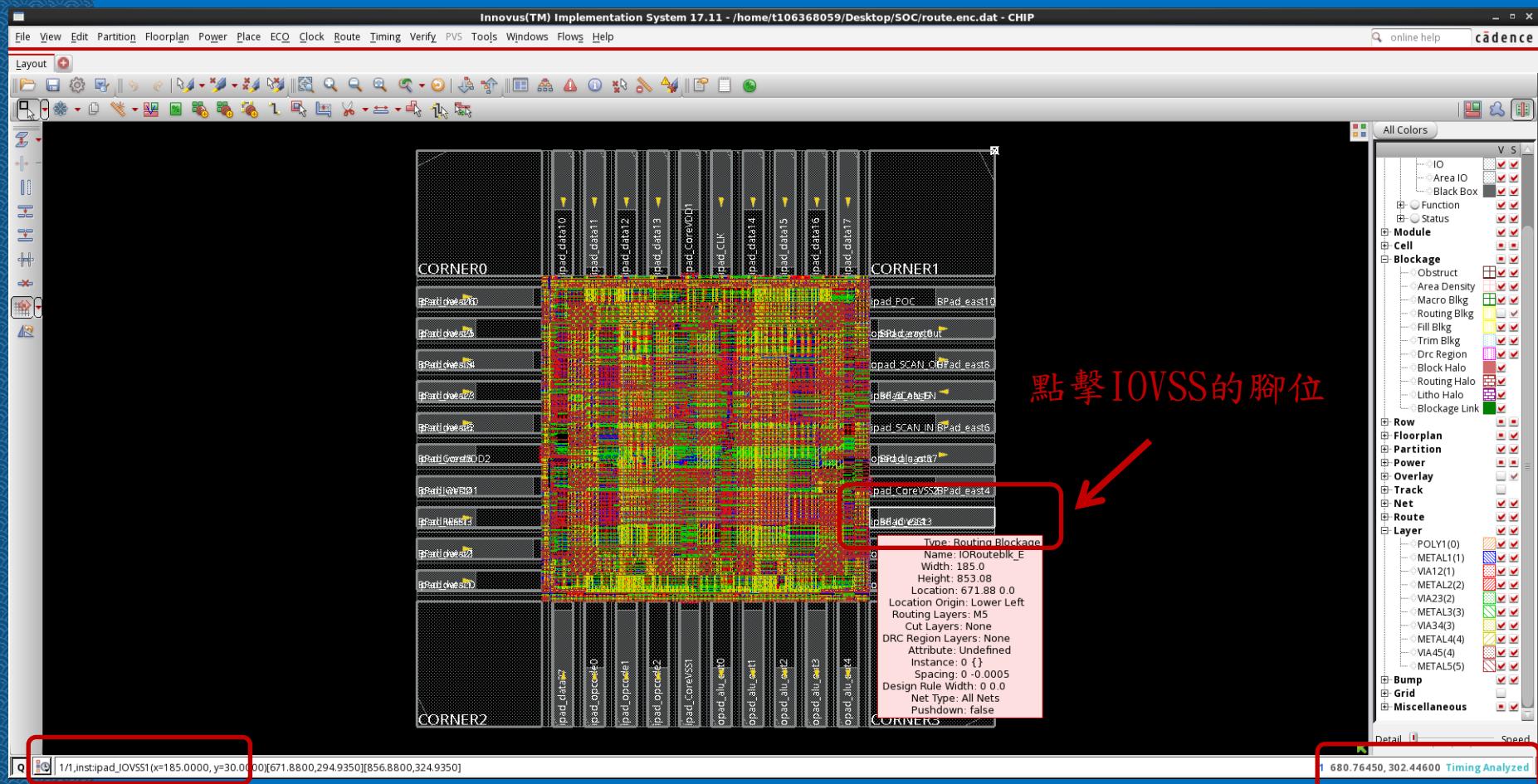
# Add Text

The screenshot shows the Innovus Implementation System interface with a routing blockage highlighted for the IOVDD pin. A red arrow points to the 'Pad IOVDD1' entry in the 'Partitions' panel, which displays detailed information about the blockage:

- Type: Routing Blockage
- Name: IORouteblk\_W
- Width: 185.0
- Height: 853.08
- Location: 0.0 0.0
- Origin: Lower Left
- Routing Layers: M5
- Cut Layers: None
- DRC Region Layers: None
- Instance: 0 {}}
- Attribute: Undefined
- Spacing: 0 -0.0005
- Design Rule Width: 0.0
- Net Type: All Nets
- Pushdown: false

The status bar at the bottom left shows the coordinates: 1/2, inst.ipad\_IOVDD1(x=185.0000, y=30.0000)[0.0000,341.5800][185.0000,371.5800]. The status bar at the bottom right shows: 1 52.02100, 352.08350 Timing Analyzed.

# Add Text



名稱

指在IOVSS上會出現座標



# Add Text

◆innovus >

```
add_text -layer METAL5 -label IOVDD -pt 80 350 -height 10
```

◆innovus >

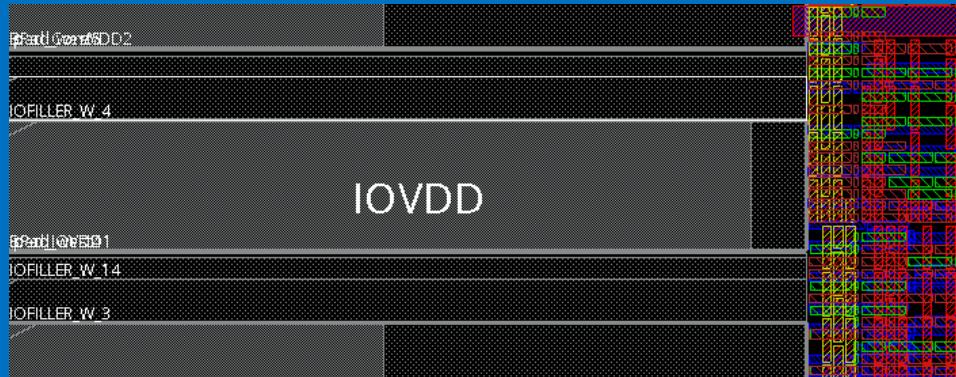
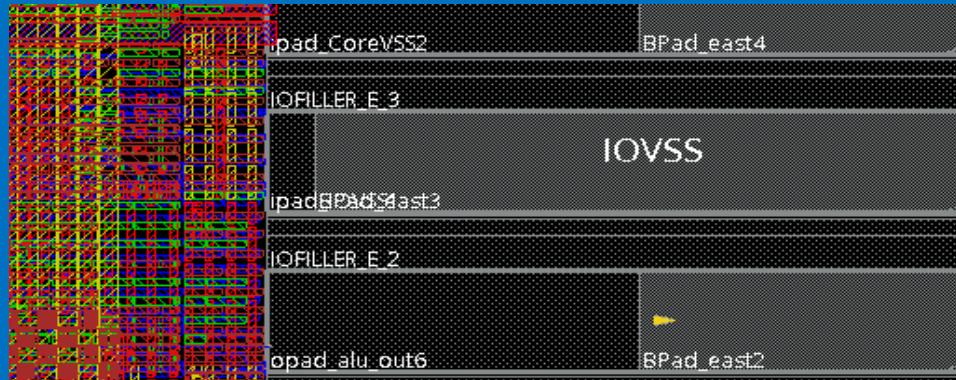
```
add_text -layer METAL5 -label IOVSS -pt 760 310 -height 10
```

```
t106368059@islabx7:SOC
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
innovus 6> add_text -layer METAL5 -label IOVDD -pt 80 350 -height 10
0x7ff22b13c9f8
innovus 7> add_text -layer METAL5 -label IOVSS -pt 760 310 -height 10
0x7ff22b142250
innovus 8> █
```



# Add Text

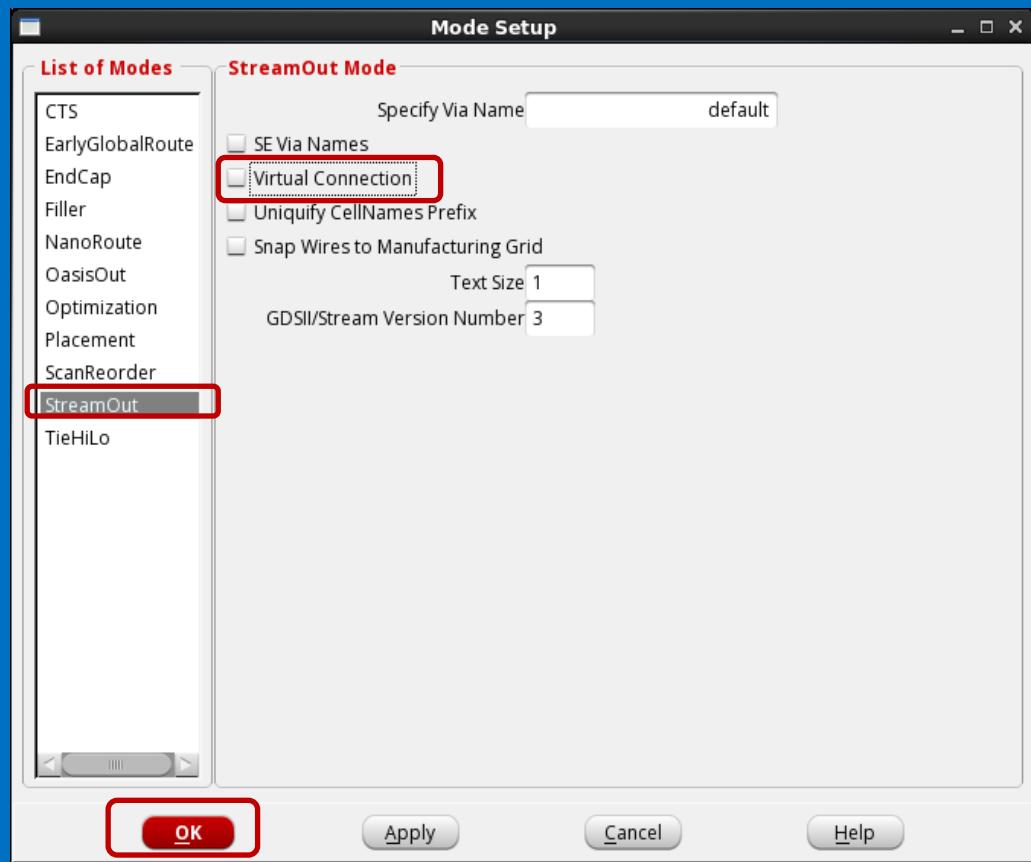
- ◆ 可以看到IOVDD和IOVSS都已經打上label，這麼做的原因是為了在posim extraction時可以找到IO power的位置





# Stream Out

- ◆ 取消Virtual Connection：讓產生出來的gds檔的pin name是pin\_name而不是pin\_name: (多了一個冒號)





# Stream Out

檔案瀏覽器 : SOCE

檔案(E) 編輯(E) 顯示(V) 前往(G) 書籤(B) 求助(H)

位置 : /home/cell\_lib/CBDK\_TSMC018\_Arm\_v3.2/CIC/SOCE

資訊

**SOCE**  
folder, 20 個  
西元2011年12月14日 (週

bond_pads	celtic	FireIce	floorplan.enc.dat
lef	lib	powerplan.enc.dat	powerRing.enc.dat
00_readme.txt	addIOFiller.cmd	addIOFiller (copy).cmd	chip.ioc.sample
chip.sdc.sample	delloFiller.cmd	DTS-091210-00-000 (copy).pdf	DTS-091210-00-000.pdf
powerplan.enc	powerRing.enc	streamOut.map	tsmc018.capTbl

20 個項目，可用空間 : 11.9 GB

複製到自己的工作資料夾

↓

cp /home/cell\_lib/CBDK\_TSMC018\_Arm\_v3.2/CIC/SOCE/streamOut.map .  
(islabx5在Design\_kit內)





# Stream Out

File Edit View Partition Floorplan Power Pl

- Import Design...
- Restore Design...
- ECO Design...
- Save Design... F2
- Create OA Library...
- Import RTL...
- RTL Synthesis...
- Load
- Save
- Check Design...
- Report
- Exit

GDS/OASIS...

Partition... Floorplan ... I/O File... Place... Route... Netlist... Testcase... DEF ... PDEF ... Timing Budget... GDS/OASIS...

**GDS/OASIS Export**

Output Format  GDSII/Stream  OASIS

Output File CHIP.gds

Map File streamOut.map

Library Name DesignLib

Structure Name CHIP

Attach Instance Name to Attribute Number

Attach Net Name to Attribute Number

Merge Files CIC/Phantom/tsmc18\_io.gds  Uniquify Cell Names

Stripes 1

Write Die Area as Boundary

Write abstract information for LEF Macros

Units 1000

Mode ALL

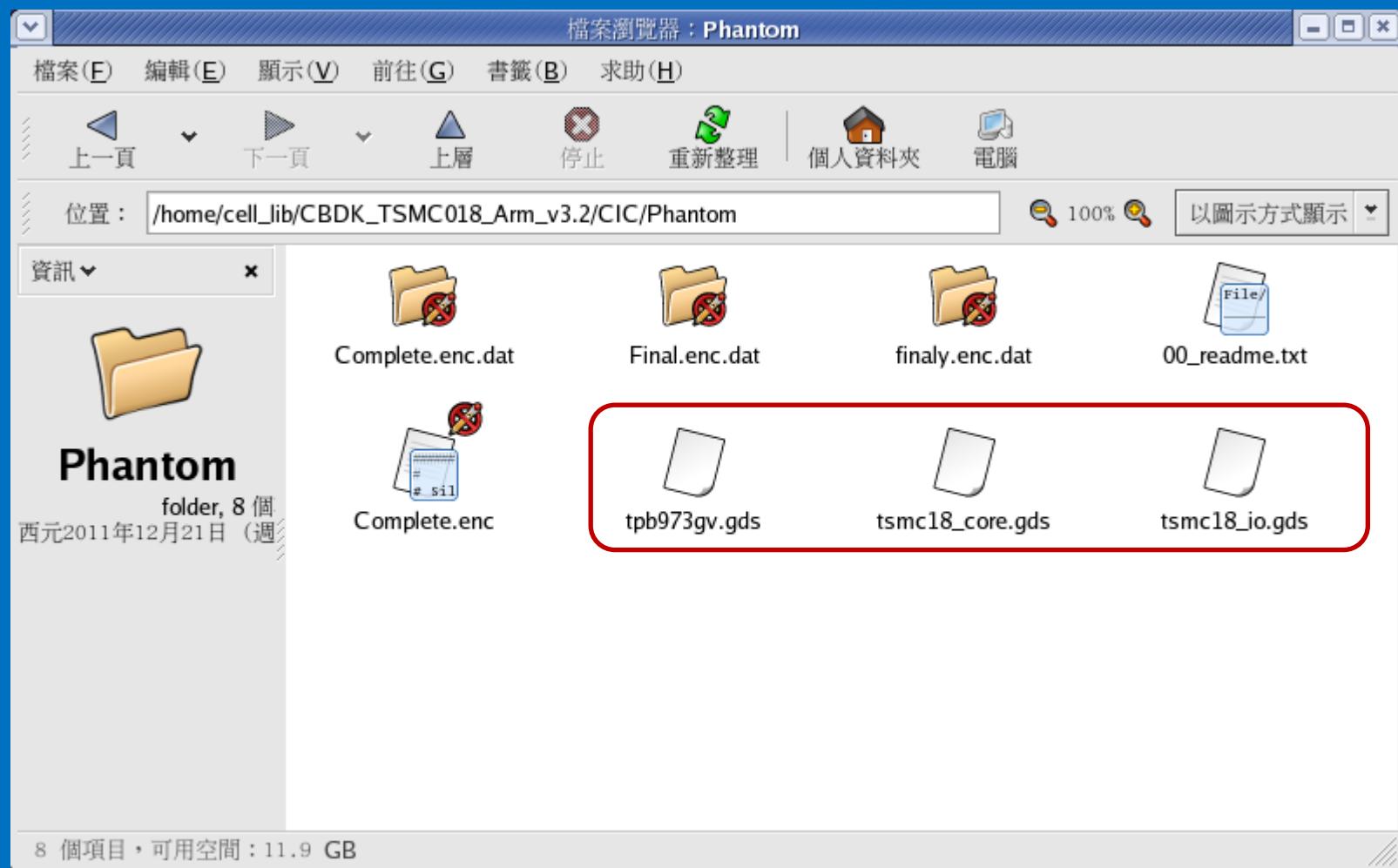
OK Apply Cancel Help

分三次讀取

檔案來源在下一頁PPT



# Stream Out

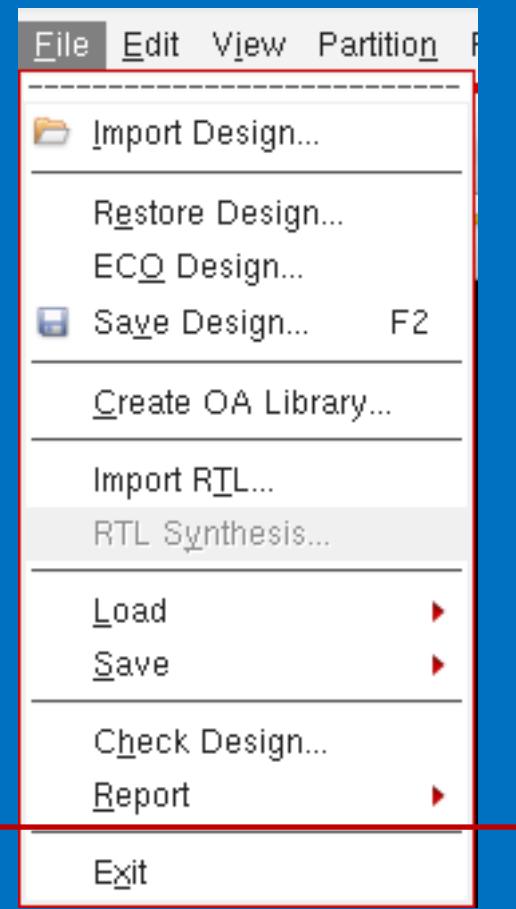


路徑 : /home/cell\_lib/CBDK\_TSMC018\_Arm\_v3.2/CIC/Phantom  
(islabx5在Design\_kit內)



# Exit

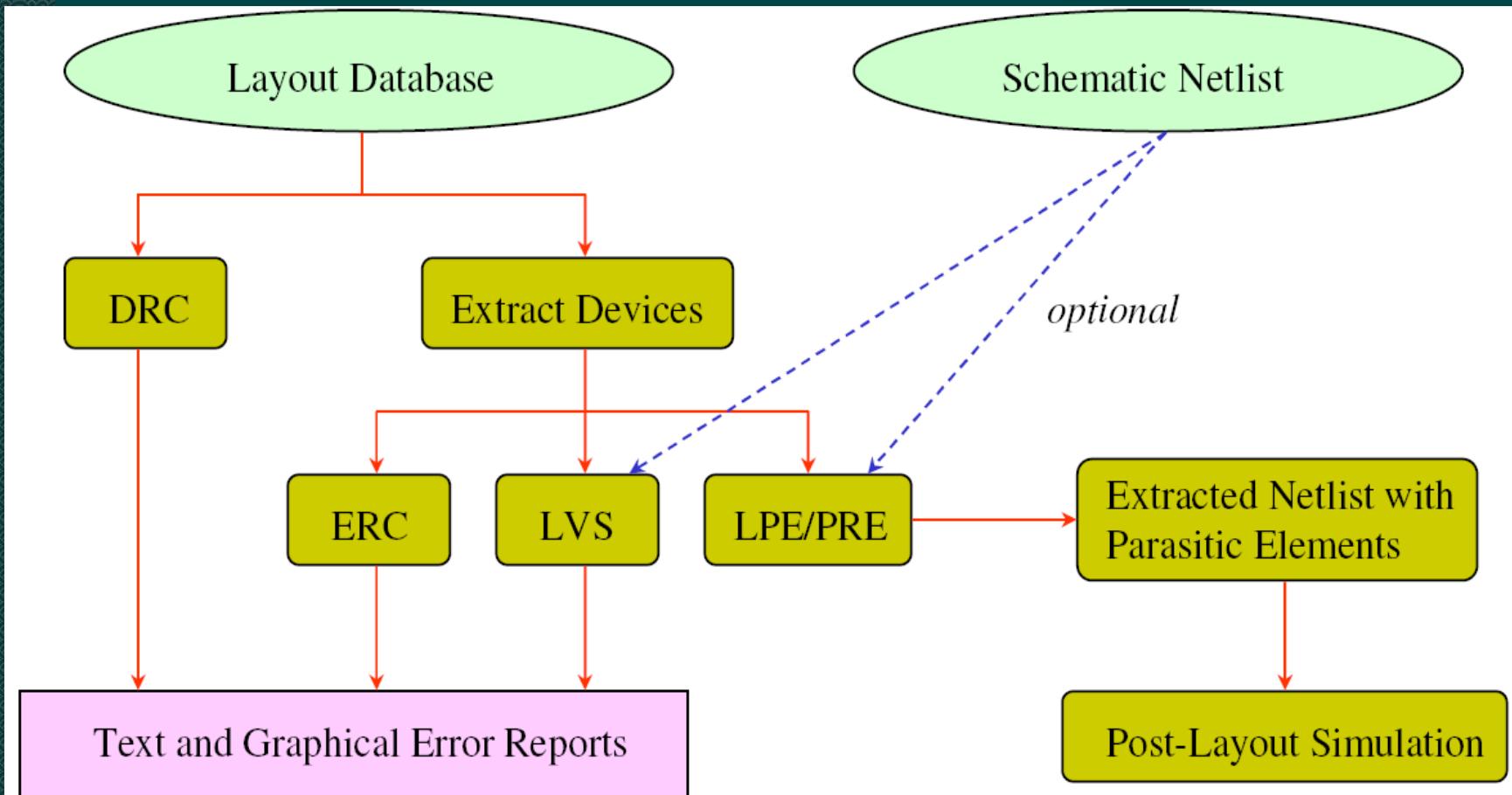
- ◆退出innovus軟體前存檔成final.enc
- ◆到此我們完成了晶片的自動佈局繞線流程，接下來我們要用剛剛所匯出的GDS檔案來作DRC和LVS的驗證



# DRC & LVS

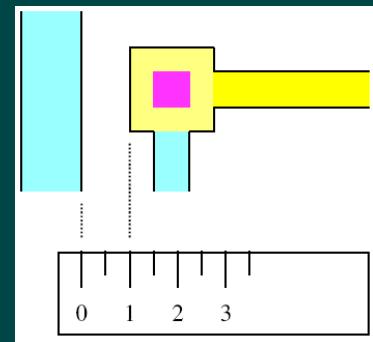


# Post-Layout Verification





# Post-Layout Verification DRC





# Create Folders

- ◆ 請在剛剛SOC的工作資料夾內新增兩個資料夾，  
分別命名為DRC和LVS
- ◆ mkdir DRC
- ◆ mkdir LVS





# Prepared Files

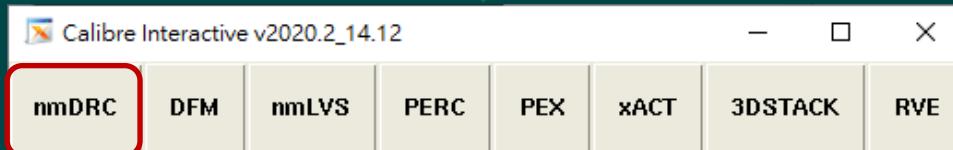
- ◆ CLM18\_LM16\_6M.28a\_m.drc
- ◆ .gds file

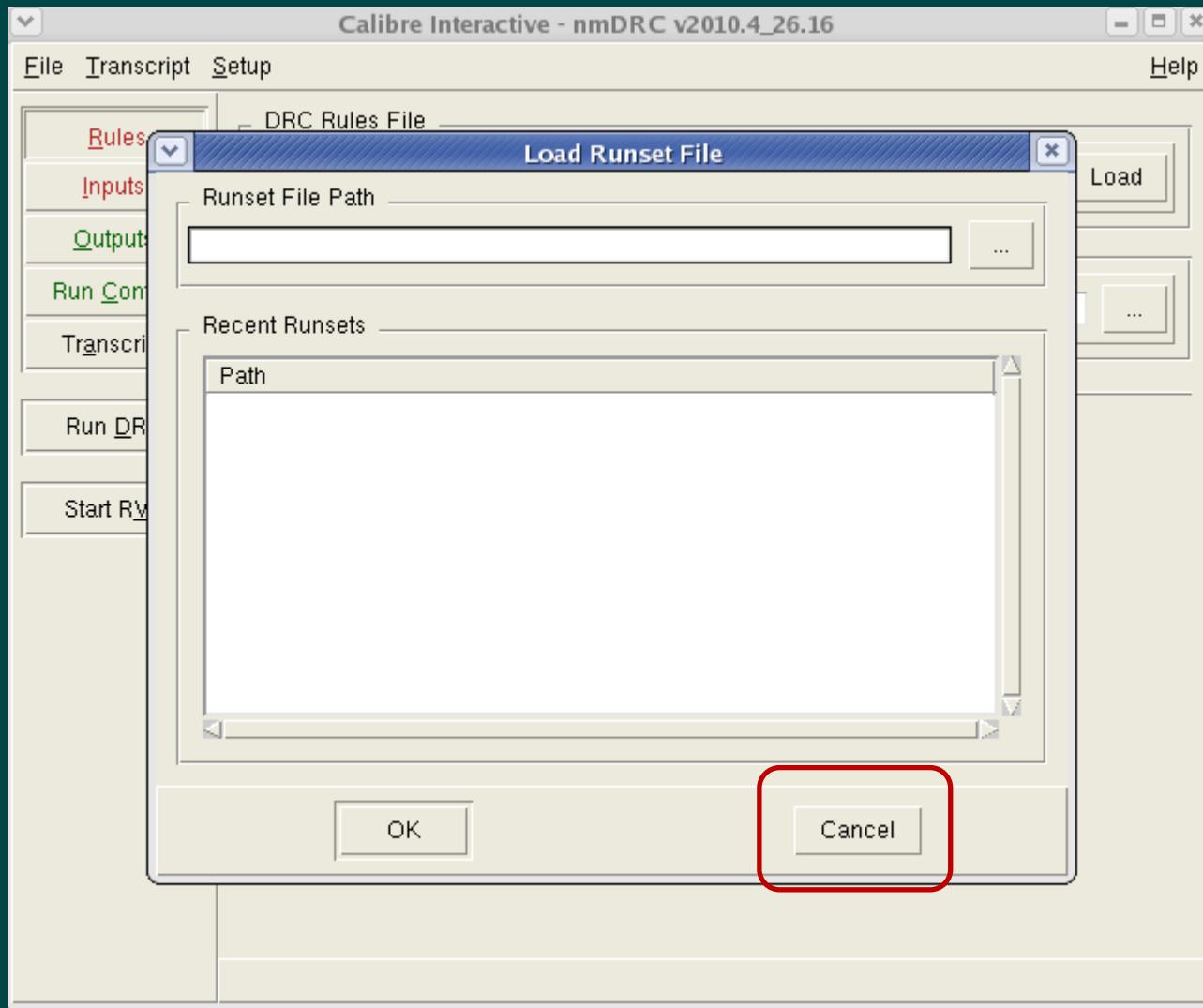


# Create Folders

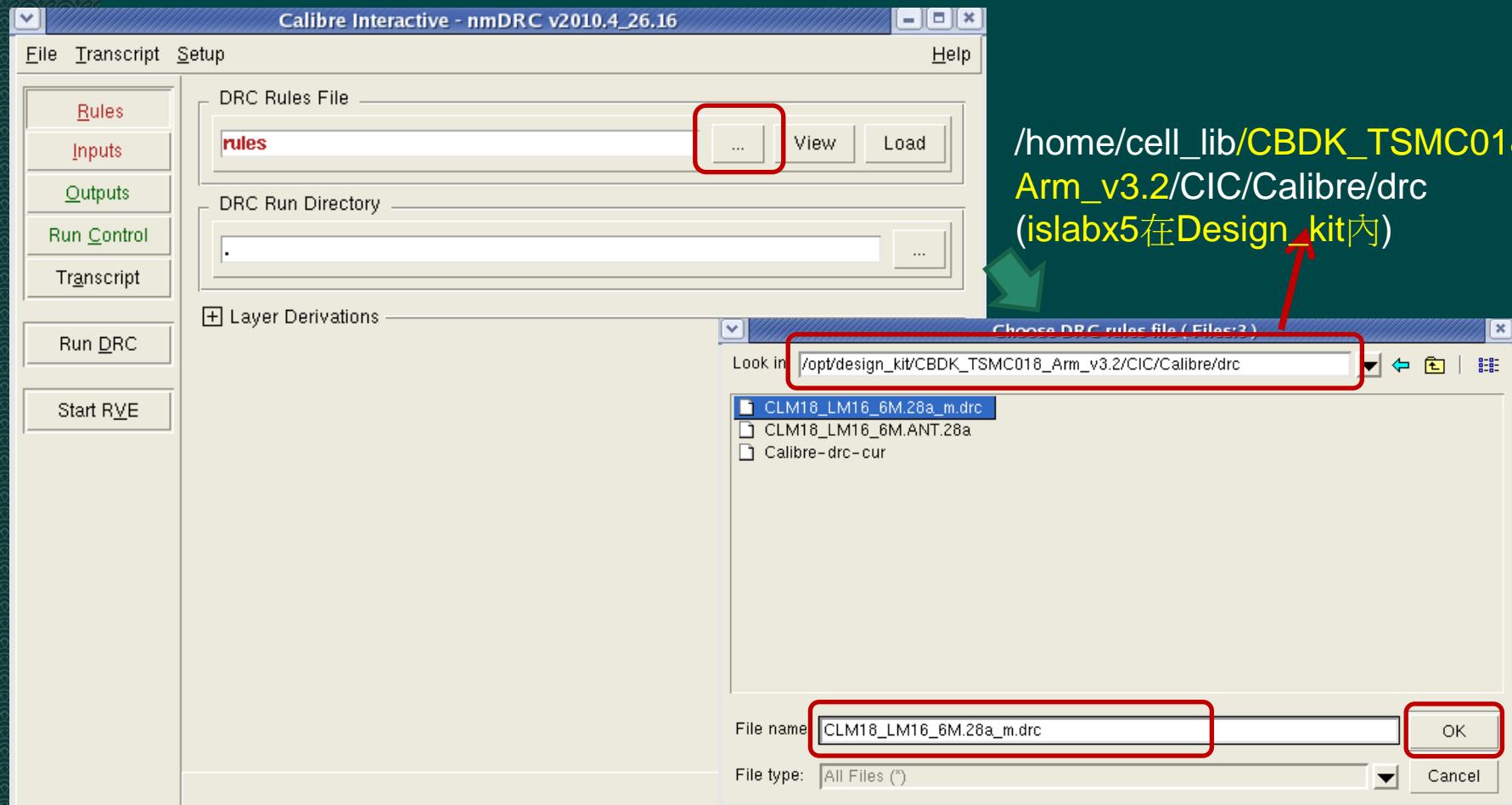
- ◆ 進入DRC的工作資料夾
- ◆ 鍵入 `calibre -gui` 開啟驗證的gui介面

```
t108368062@islabx7:DRC
檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)
-- Now source Cadence NC-Verilog --
-- Now source Synopsys Design Compiler --
Platform = amd64
-- Now source Synopsys Formality --
-- Now source Mentor MBISTArchitect --
-- Now source Synopsys TetraMAX --
-- Now source Cadence INNOVUS --
-- Now source Mentor Calibre --
-- Now source Synopsys PrimeTime --
Platform = amd64
-- Now source Synopsys Nanosim --
-- Now source Synopsys Verdi --
Platform = LINUX
#####
#      32BIT is the default mode
#      If you want to run 64BIT mode,
#      please set the LD_LIBRARY_PATH and SHLIB_PATH
#      to path of 64BIT by yourself.
#####
[t108368062@islabx7 ~] cd SOC/DRC/
[t108368062@islabx7 DRC]$ calibre -gui
```

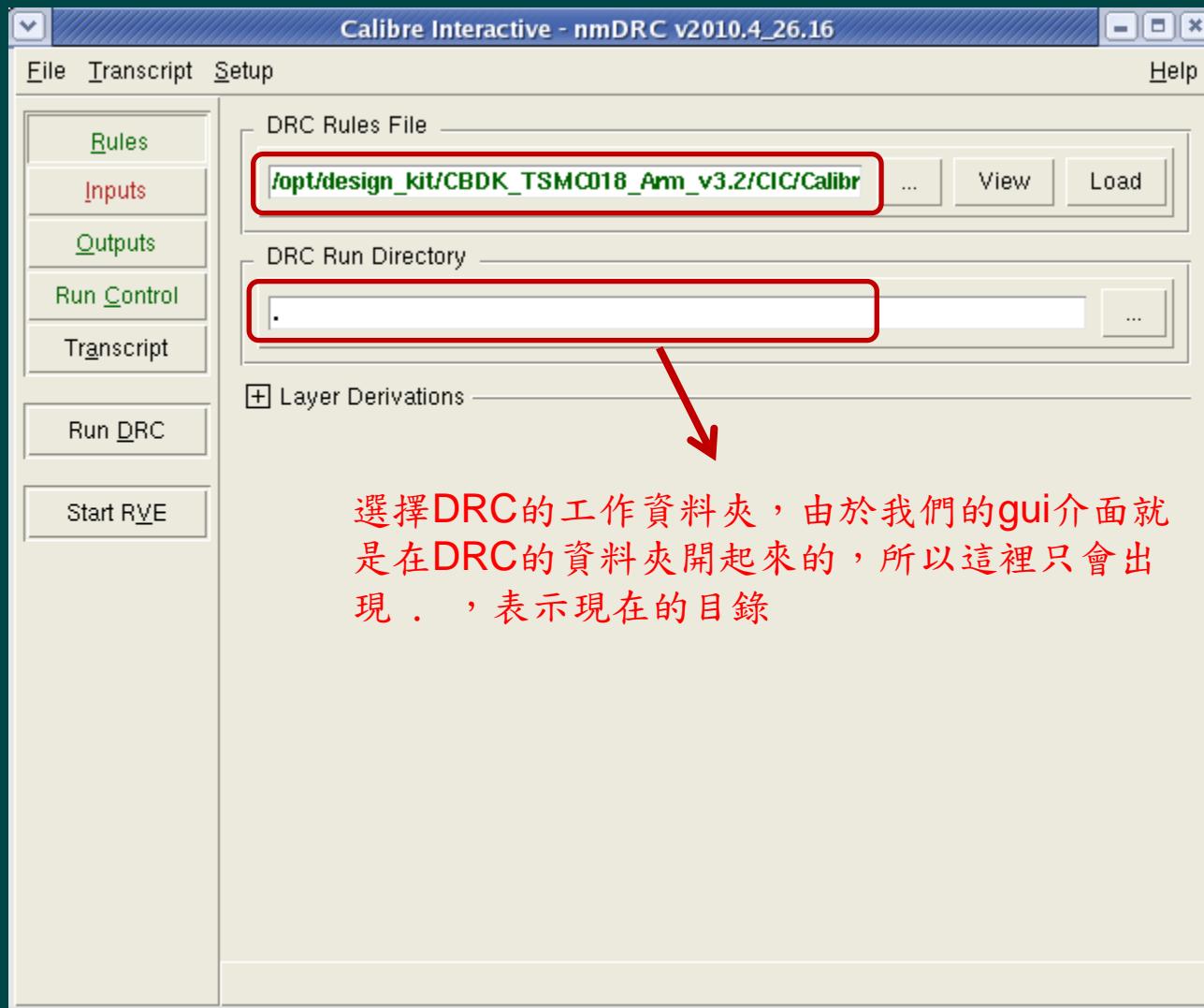




# DRC

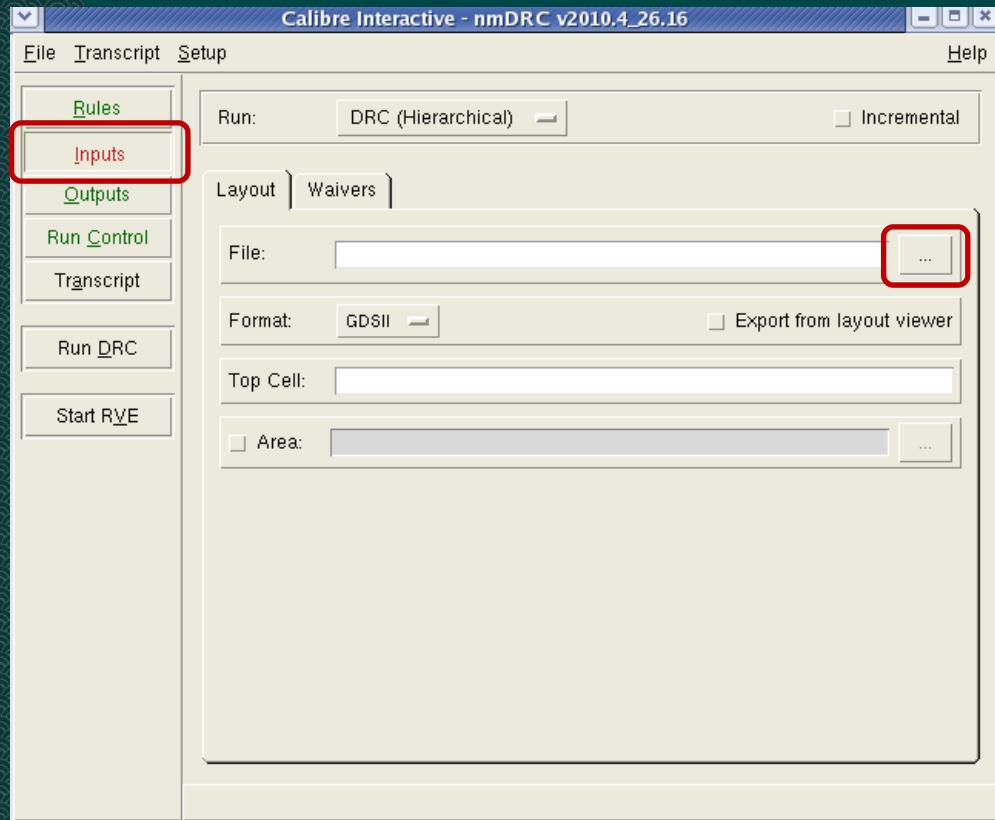


# DRC



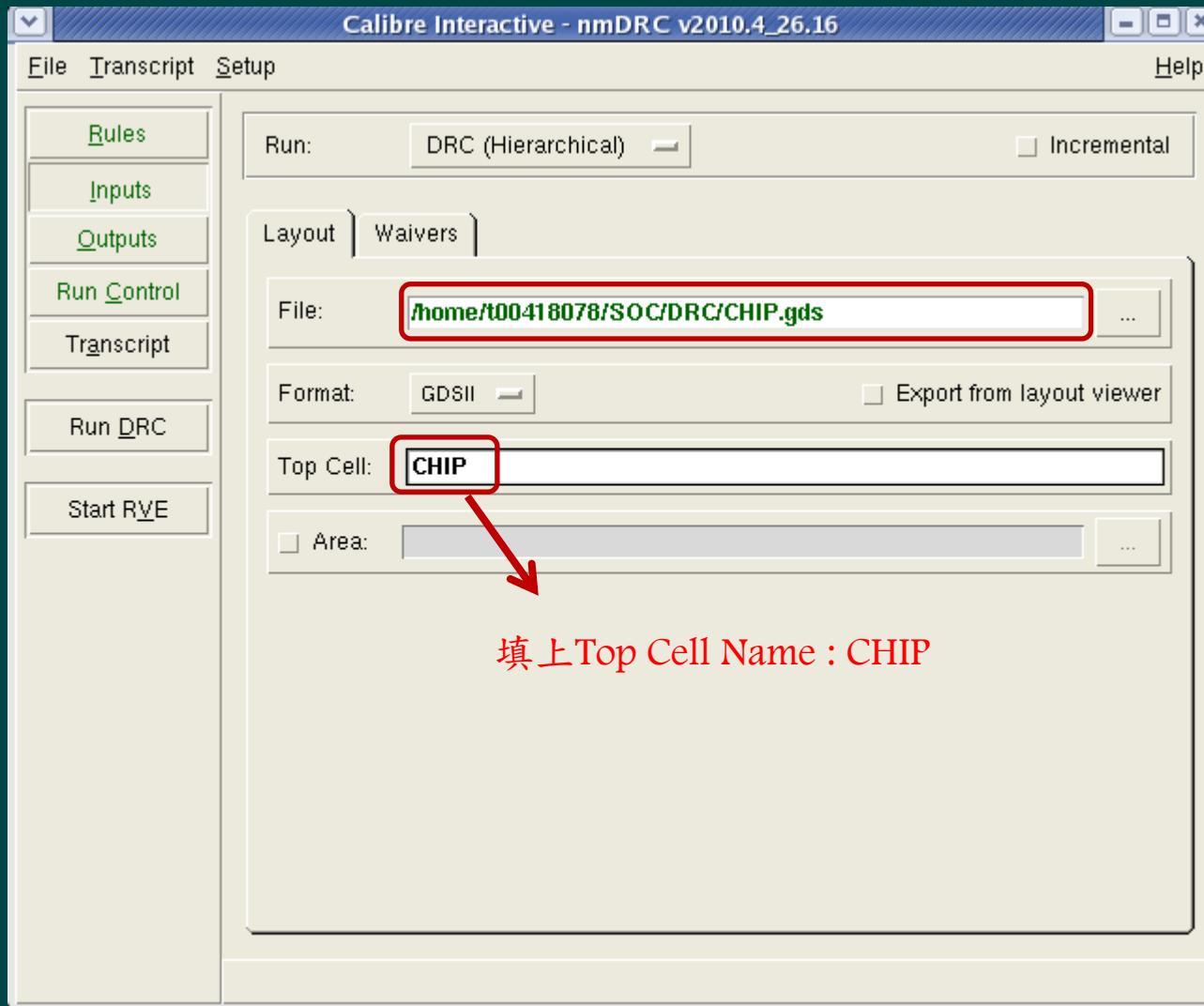
選擇DRC的工作資料夾，由於我們的gui介面就是在DRC的資料夾開起來的，所以這裡只會出現 . ，表示現在的目錄

# DRC

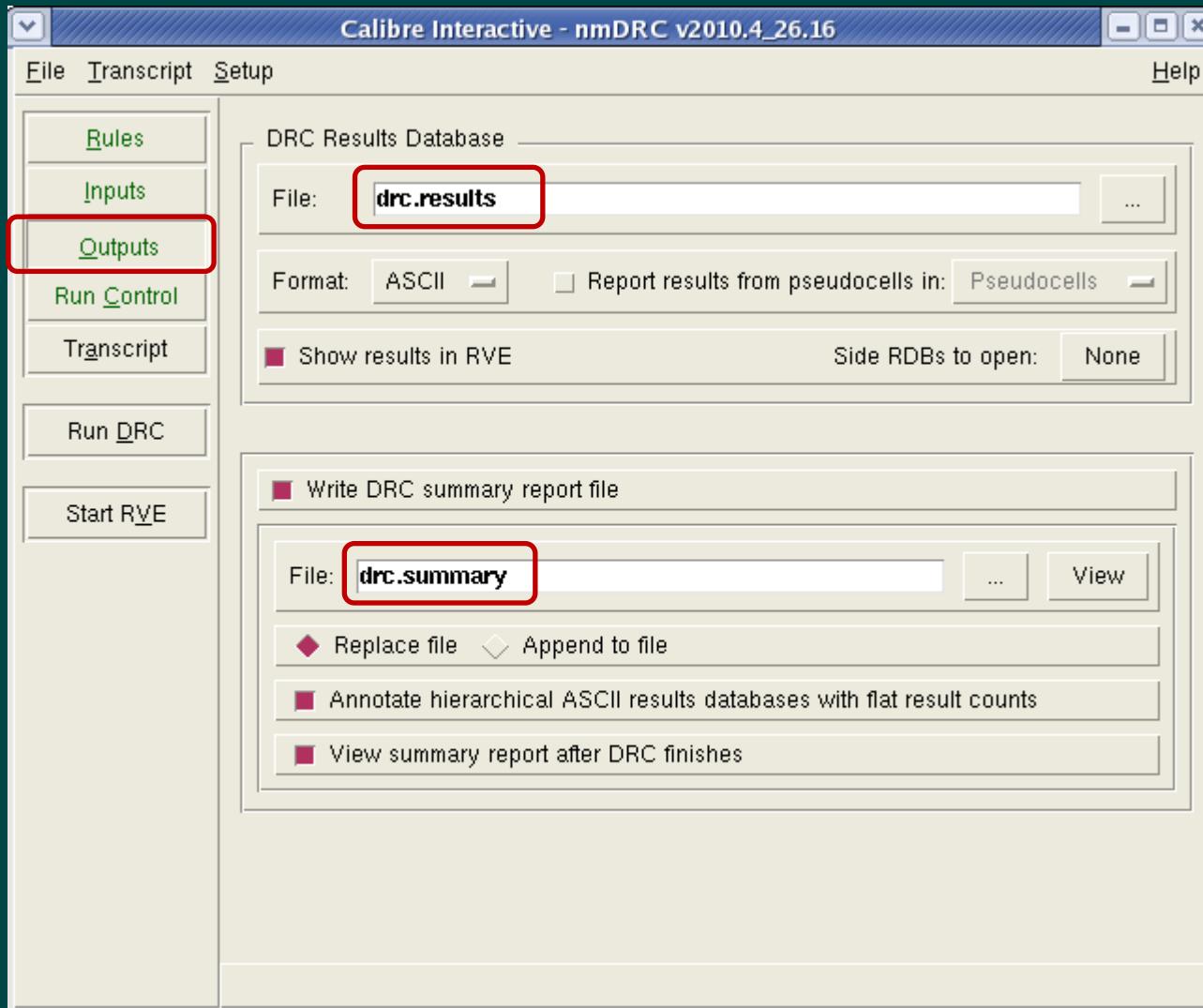


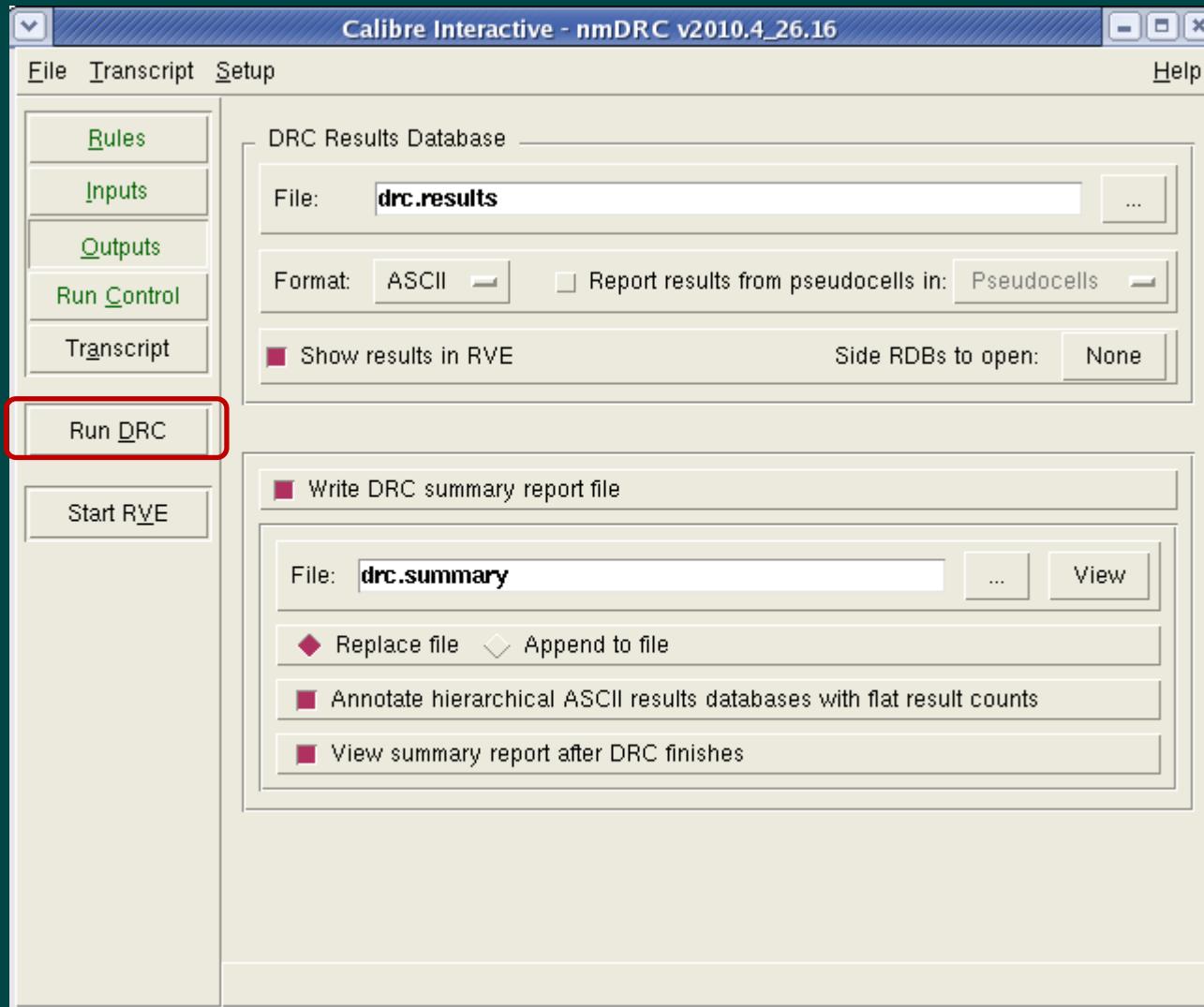
選擇gds檔

# DRC



填上Top Cell Name : CHIP





# DRC



◆ 應該可以看到7個DRC error，這幾個DRC error是指metal及poly的density不足，可以不必理會，如果結果是七個個錯誤就算是DRC驗證成功，到這裡結束DRC的驗證

Calibre - RVE v2010.4\_26.16 : drc.results

File View Highlight Tools Window Setup Help

Topcell CHIP, 6 Results (in 6 of 368 Checks) Find:

Check / Cell

- ⊕ **Check NO.IND.PO.R.3** ✘
- ⊕ Check NO.IND.M1.R
- ⊕ Check NO.IND.M2.R
- ⊕ Check NO.IND.M3.R
- ⊕ Check NO.IND.M4.R
- ⊕ Check UTM20K.R.1

NO. IND.PO.R.3 { @ Min. density of POLY area >= 14% (exclude application for inductor)  
ALL POLY\_NIND = POLYI OR DPO  
POLYT\_NIND = ALL POLY\_NIND NOT INDDMY  
CHIP\_NIND = CHIP NOT INDDMY  
DENSTY POLYT\_NIND CHIP\_NIND < 0.14 PRINT POLYT\_DENSITY.log  
! AREA1/DOI\_VTP\_MTMN1/Area1/CHTD\_MTMN1

Check NO.IND.PO.R.3, Cell CHIP: 1 Result

DRC Summary Report - drc.summary

File Edit Options Windows

RULECHECK SBD. S. 1 ..... TOTAL Result Count = 0 (0)  
RULECHECK SBD. E. 1 ..... TOTAL Result Count = 0 (0)  
RULECHECK SBD. E. 2 ..... TOTAL Result Count = 0 (0)  
RULECHECK SBD. O. 1 ..... TOTAL Result Count = 0 (0)  
RULECHECK SBD. E. 1. 1 ..... TOTAL Result Count = 0 (0)  
RULECHECK SBD. E. 3 ..... TOTAL Result Count = 0 (0)  
RULECHECK SBD. R. 2 ..... TOTAL Result Count = 0 (0)  
RULECHECK SBD. R. 3 ..... TOTAL Result Count = 0 (0)  
RULECHECK SBD. R. 4 ..... TOTAL Result Count = 0 (0)  
RULECHECK SBD. R. 5 ..... TOTAL Result Count = 0 (0)

--- RULECHECK RESULTS STATISTICS (BY CELL)

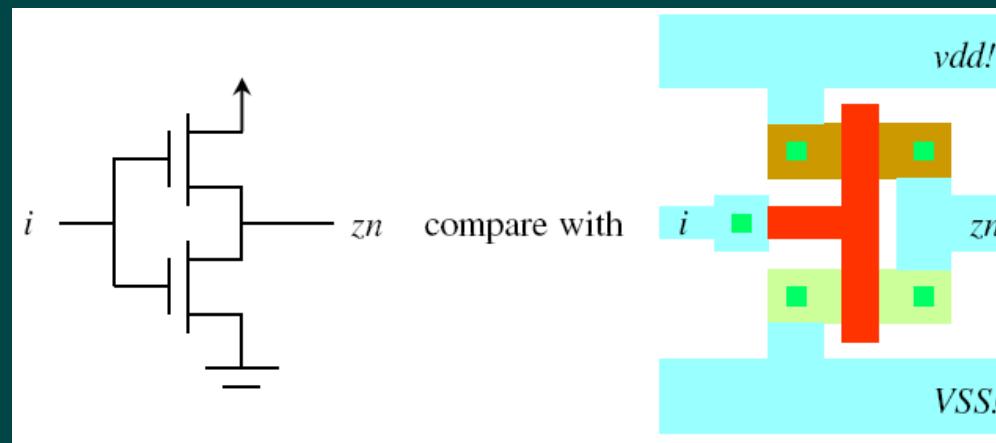
CELL CHIP ..... TOTAL Result Count = 6 (6)  
RULECHECK NO. IND. PO. R. 3 ... TOTAL Result Count = 1 (1)  
RULECHECK NO. IND. M1. R. 1 ... TOTAL Result Count = 1 (1)  
RULECHECK NO. IND. M2. R. 1 ... TOTAL Result Count = 1 (1)  
RULECHECK NO. IND. M3. R. 1 ... TOTAL Result Count = 1 (1)  
RULECHECK NO. IND. M4. R. 1 ... TOTAL Result Count = 1 (1)  
RULECHECK UTM20K. R. 1 ..... TOTAL Result Count = 1 (1)

--- SUMMARY

TOTAL CPU Time: 2  
TOTAL REAL Time: 3  
TOTAL Original Layer Geometries: 26990 (193785)  
TOTAL DRC RuleChecks Executed: 366  
TOTAL DRC Results Generated: 6 (6)



# Post-Layout Verification LVS

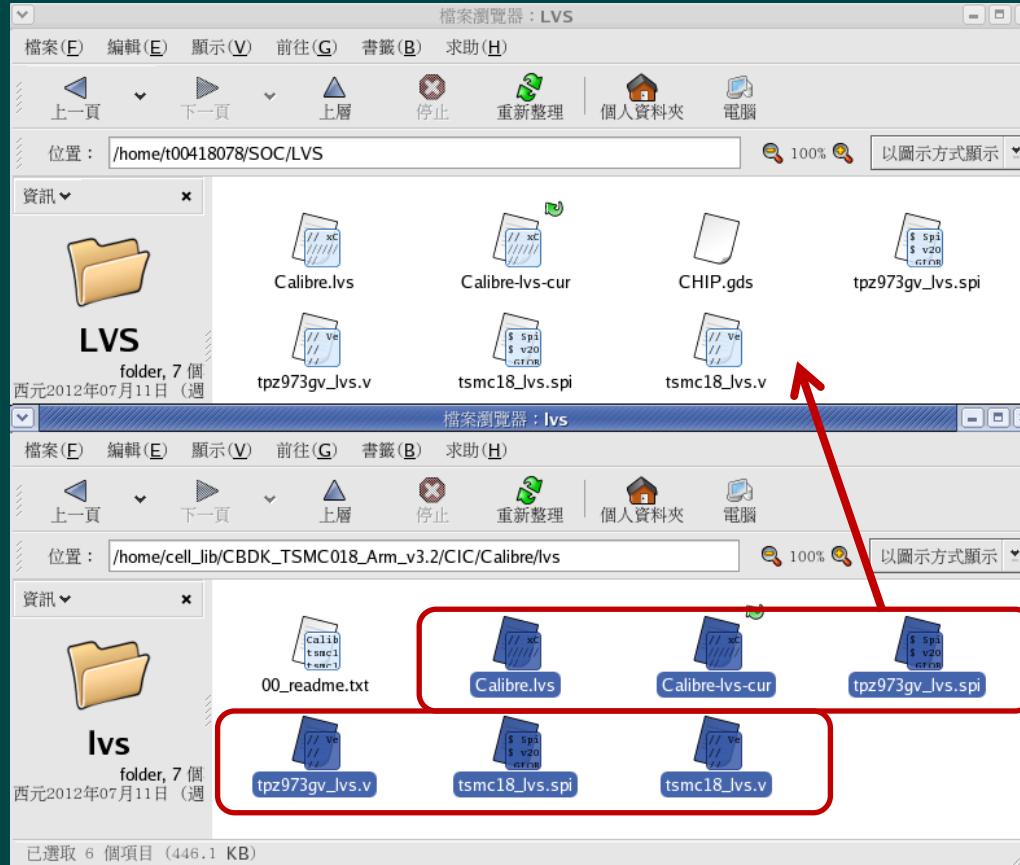




# Prepared Files

- ◆ .gds file
- ◆ .v file
- ◆ Calibre.lvs
- ◆ tsmc18\_lvs.spi
  - ~~ The core blackbox SPICE netlist for Calibre LVS
- ◆ tpz973gv\_lvs.spi
  - ~~ The io blackbox SPICE netlist for Calibre LVS
- ◆ tsmc18\_lvs.v
  - ~~ The core verilog library for Calibre LVS
- ◆ tpz973gv\_lvs.v
  - ~~ The io verilog library for Calibre LVS
- ◆ Calibre-lvs-cur
  - ~~Calibre lvs rule file

# Prepared Files



複製 CHIP.gds 和這六個檔案至創建的 LVS 資料夾

路徑：

/opt/Design\_kit/CBDK\_TSMC018\_Arm\_v3.2/  
CIC/Calibre/lvs



# v2lvs

- ◆ 進入LVS的工作資料夾
- ◆ 鍵入 v2lvs -v ../CHIP.v -l tsmc18\_lvs.v -l tpz973gv\_lvs.v -s tsmc18\_lvs.spi -s tpz973gv\_lvs.spi -o source.spi -s1 VDD -s0 VSS

終端機

檔案(E) 編輯(E) 顯示(V) 終端機(I) 分頁(B) 求助(H)

```
Platform = amd64
-- Now source Synopsys Tmax
-- Now source Synopsys Nanosim
-- Now source Synopsys Formality
-- Now source Spring soft nWave(Verdi) --
Platform = LINUX
#####
#      32BIT is the default mode
#      If you want to run 64BIT mode,
#      please set the LD_LIBRARY_PATH and SHLIB_PATH
#      to path of 64BIT by yourself.
#####
-- Now source Spring soft Debussy --
Platform = LINUX
#####
#      32BIT is the default mode
#      If you want to run 64BIT mode,
#      please set the LD_LIBRARY_PATH and SHLIB_PATH
#      to path of 64BIT by yourself.
#####
-- Now Plug-in Calibre for Laker --
[t00418078@islabx3 ~]$ cd SOC/LVS/
[t00418078@islabx3 LVS]$ v2lvs -v ../CHIP.v -l tsmc18_lvs.v -l tpz973gv_lvs.v -s
tsmc18_lvs.spi -s tpz973gv_lvs.spi -o source.spi -s1 VDD -s0 VSS
```

做LVS驗證的時候，我們的netlist檔必須是SPICE格式，所以我們先將.v檔轉成SPICE的格式，鍵入指令後應該會產生spi檔



# LVS



- ◆ 開啟Calibre.lvs的檔案，更改Layout和Source的設定

The screenshot shows a gedit window with the title bar reading "/home/t00418078/SOC/LVS/Calibre.lvs - gedit". The menu bar includes 檔案(E), 編輯(E), 顯示(V), 搜尋(S), 工具(T), 文件(D), and 求助(H). The toolbar contains icons for 新增 (New), 開啓 (Open), 儲存 (Save), 列印 (Print), 復原 (Undo), 取消復原 (Redo), 剪下 (Cut), 複製 (Copy), 貼上 (Paste), 搜尋 (Search), and 取代 (Replace). A single tab labeled "Calibre.lvs" is open. The code content is as follows:

```
#IFDEF RC_DECK
#define ACCURACY
#endif

LAYOUT PRIMARY "CHIP"
LAYOUT PATH "CHIP.gds"
LAYOUT SYSTEM GDSII
LAYOUT CASE YES
//LAYOUT PATH "layout.net"
//LAYOUT SYSTEM SPICE

SOURCE PRIMARY "CHIP"
SOURCE PATH "source.spi"
SOURCE SYSTEM SPICE
SOURCE CASE YES

DRC RESULTS DATABASE "calibre_drc.db" ASCII // ASCII or GDSII
DRC SUMMARY REPORT "calibre_drc.sum"

ERC RESULTS DATABASE "calibre_erc.db" ASCII
ERC SUMMARY REPORT "calibre_erc.sum"
```

Two sections of the code are highlighted with red boxes: the LAYOUT block and the SOURCE block.

# LVS



/home/t00418078/SOC/LVS/Calibre.lvs - gedit

檔案(E) 編輯(E) 顯示(V) 搜尋(S) 工具(T) 文件(D) 求助(H)

新增 開啓 儲存 列印 復原 取消復原

Calibre.lvs

```
LVS BOX PRU12DGZ
LVS BOX PRU12SDGZ
LVS BOX PRU16DGZ
LVS BOX PRU16SDGZ
LVS BOX PRU24DGZ
LVS BOX PRU24SDGZ
LVS BOX PRUW08DGZ
LVS BOX PRUW12DGZ
LVS BOX PRUW16DGZ
LVS BOX PRUW24DGZ
//LVS BOX PVDD1ANA
//LVS BOX PVDD1DGZ
//LVS BOX PVDD2ANA
//LVS BOX PVDD2DGZ
//LVS BOX PVDD2POC
//LVS BOX PVSS1ANA
//LVS BOX PVSS1DGZ
//LVS BOX PVSS2ANA
//LVS BOX PVSS2DGZ
//LVS BOX PVSS3DGZ
```

移除掉的原因是因為我們的 verilog netlist 沒有這些 cell，但是我們的 layout 上面有，所以希望 calibre 不要把這些 cell 當 black box 看待



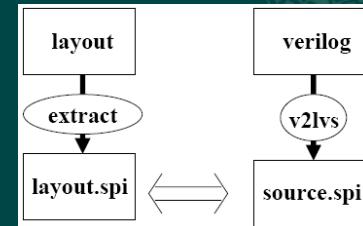
◆ 在 Calibre.lvs 最後面的地方，註解下列各個 LVS BOX，如圖所示。

```
// LVS BOX FILL1           //LVS BOX PVDD1ANA
// LVS BOX FILL16          //LVS BOX PVDD1DGZ
// LVS BOX FILL2           //LVS BOX PVDD2ANA
// LVS BOX FILL32          //LVS BOX PVDD2DGZ
// LVS BOX FILL4           //LVS BOX PVDD2POC
// LVS BOX FILL64          //LVS BOX PVSS1ANA
// LVS BOX FILL8           //LVS BOX PVSS1DGZ
// LVS BOX PAD50ARU        //LVS BOX PVSS2ANA
// LVS BOX PAD60NU         //LVS BOX PVSS2DGZ
// LVS BOX PAD70NU         //LVS BOX PVSS3DGZ
// LVS BOX PAD80NU

//LVS BOX PCORNER
//LVS BOX PFILLER0005
//LVS BOX PFILLER05
//LVS BOX PFILLER10
//LVS BOX PFILLER1
//LVS BOX PFILLER20
//LVS BOX PFILLER5
```

# LVS

- ◆ 鍵入calibre -lvs -spice layout.spi -hier -auto Calibre.lvs



The screenshot shows a terminal window titled '終端機' (Terminal) with the following text:

```
AP = 4/25/26  MALLOC = 43/43/43  ELAPSED TIME = 4

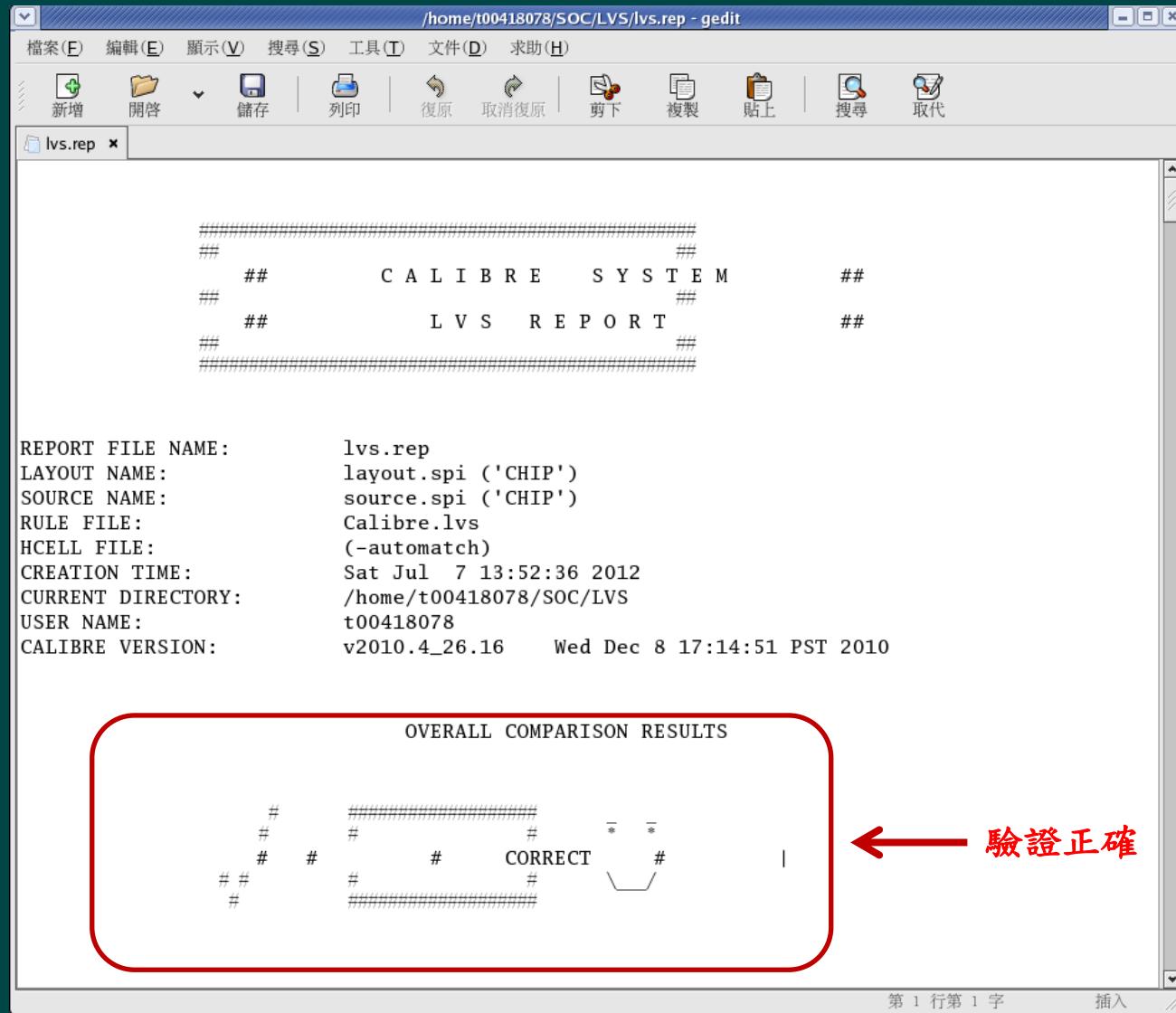
--- CALIBRE::LVS/xRC COMPLETED - Wed Jul 11 12:30:53 2012
--- TOTAL CPU TIME = 0  REAL TIME = 0  LVHEAP = 4/25/26  MALLOC = 43/43/43  ELAPSED
TIME = 4
--- XDB CROSS REFERENCE DATABASE = svdb/CHIP.xdb
--- ERC PATHCHK RESULTS DATABASE = svdb/CHIP.pathchk.erc
--- ERC PATHCHK REPORT = svdb/CHIP.pathchk.rep

--- SPICE NETLIST FILE = layout.spi
--- CIRCUIT EXTRACTION REPORT FILE = lvs.rep.ext
--- ERC PATHCHK RESULTS DATABASE = svdb/CHIP.pathchk.erc
--- ERC PATHCHK REPORT = svdb/CHIP.pathchk.rep
--- PERSISTENT HIERARCHICAL DATABASE(PHDB) = svdb/CHIP.phdb
--- QUERY DATABASE = svdb  TOP CELL = CHIP
--- TOTAL RULECHECKS EXECUTED = 9
--- TOTAL RESULTS GENERATED = 1 (1)
--- ERC RESULTS DATABASE FILE = calibre_erc.db (ASCII)
--- ERC SUMMARY REPORT FILE = calibre_erc.sum

--- GRAND TOTAL CPU TIME = 2  REAL TIME = 4  LVHEAP = 3/25/26  MALLOC = 43/43/43  E
LAPSED TIME = 4
```

[t00418078@is1abx3 LVS]\$ calibre -lvs -spice layout.spi -hier -auto Calibre.lvs

LVS





Thanks for your attention.