Matthew French

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Education

University of Michigan – Ann Arbor, MI

- M.S.E. Electrical and Computer Engineering – Embedded Systems (4.00/4.00) **Anticipated Dec 2021**
- B.S.E. Computer Engineering, Minor Mathematics, Summa Cum Laude (3.84/4.00) **Dec 2020**
- Engineering Honors Program, James B. Angell Scholar, University Honors, Dean's List
- Coursework: Advanced Embedded Systems (EECS 473), Autonomous Robotics (EECS 467), Computer Architecture (EECS 470), Embedded Control Systems (EECS 461), Computer Vision (EECS 442), Intro to Logic Design (EECS 270), Embedded Systems Research (EECS 507)

Work Experience

SpaceX – FPGA & ASIC RTL Design Intern **May 2020 – Present**

- Parameterized existing RTL to efficiently instantiate RAM within a block, thereby reducing space and complexity throughout the top level
- Proposed two novel packet generation and checker blocks after drawing block diagrams, writing documentation in reStructuredText, creating register files using SystemRDL, and receiving feedback from other team members
- Developed efficient RTL in Verilog to implement proposed designs and further optimized design to close timing with a 500 MHz clock
- Performed full FPGA build with integrated blocks to validate design on real hardware

SpaceX – FPGA & ASIC Design Verification Intern **May 2020 – Jul 2020**

- Architected block-level UVM testbench in SystemVerilog to verify SpaceX IP block with 100% functional and code coverage
- Diagnosed several issues during design verification process and worked closely alongside designer to resolve them before ASIC tape-out
- Supplemented components to existing system-level UVM testbench to further verify untested functionality
- Initialized foundations for testbench to verify RISC-V core implementation using random assembly instruction generation

DCS Corporation – Computer Engineering Intern in US Army Ground Vehicle Systems Center **May 2019 – Sep 2019**

- Independently researched, designed, implemented, and tested standalone camera streaming server plugin for Unreal Engine 4 which provides high quality (1080p), low latency (8-10ms) video feeds of in-game imagery via RTSP to local network clients
- Leveraged Nvidia's GPU accelerated NVENC encoder by means of a hardware accelerator API to compress video feeds into h.264 format for efficient streaming thereby removing significant dependency on CPU

Technical Projects

EECS 470, Computer Architecture – Out-of-order, N-Way-Parameterized Superscalar RISC-V Core **Jan 2021 – May 2021**

- Implemented RTL of MIPS R10000-based CPU core suited for unprivileged RISC-V base and multiply instructions; synthesizable at 60 MHz
- Parameterized superscalar ways and other parameters; analyzed and selected parameter values to achieve 1.692 CPI on average

EECS 473, Advanced Embedded Systems – Contact Tracing BLE Smartwatch Prototype **Sep 2020 – Dec 2020**

- Prototyped smart watch which can detect potential disease transmission to users by contract tracing over Bluetooth Low Energy
- Designed and printed compact PCB which deployed STM32 microcontroller and various supporting components including antenna, OLED screen, temperature sensor, buttons, LEDs, USB charging circuit, and power supply

M-Fly Student Project Team – Hardware Systems Lead Engineer **Sep 2018 – May 2020**

- Coordinated team of 10 engineers in iterative development of autonomous RC plane embedded system
- Surveyed and procured system components to enable payload drop of unmanned ground vehicle, autonomous waypoint navigation, imaging object recognition, obstacle avoidance, and multiple communication links
- Reduced battery weight by 12% by building custom monitoring hardware and logging power usage to determine optimal specification
- Illustrated line diagram and soldered efficient wiring harness for plug-and-play modular design and minimization of weight
- Implemented safety workaround for flying manually by routing flight servo controls into custom switching mechanism PCB

EECS 507, Embedded Systems Research – Efficient Wildfire Detection for Embedded Platforms **Jan 2021 – May 2021**

- Developed novel horizon detection and color space heuristics to limit portions of input images from running on full fire detection CNN
- Integrated heuristics into image pre-processing pipeline to reduce overall power consumption by 40% while preserving 99% accuracy

EECS 467, Autonomous Robotics – CHESSBOT (Chess-Playing Autonomous Robot) **Jan 2018 – Apr 2018**

- Moved chess pieces with robotic SCARA robotic arm based on interpretation of chess board from computer vision solution
- Leveraged open stockfish chess solver software to play optimal moves and scale game difficulty for a variety of human skill levels
- Pivoted from physical device to Unreal Engine 4 simulation to validate prototype and software during COVID-19 complications

Additional

Theta Tau Professional Engineering Fraternity – Academic/Philanthropy/Social Chairs **Sep 2017 – Present**

Programming Languages: C/C++, Verilog, SystemVerilog, UVM, Bash, Python, MATLAB, Arduino

Platforms & Software: Linux, BLE, Quartus, Vivado, Synopsis, STM32, Arduino, RaspberryPi, Unreal Engine 4, Git, Visual Studio Code