EE 660 – Computer Architecture **(UH Manoa, Spring 2021)**

Homework 1

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Problem B.1

a) $AMAT = cache_{hit} + cache_{miss} = 97\% * 1 + 3\% * 110 = 4.27$ cycles.

b) $Hit_{rate} = \frac{64KB}{1GB} = 0.000064$
$AMAT = cache_{hit} + cache_{miss} = 0.000064 * 1 + (1 - 0.000064) * 110 = 109.99$ cycles.

c) The cache memory would be of not use as when the cache is disabled the cycles are 105 which is lower than 109.99 (from problem b).

d) Let Memory Access Time with no cache be, T_{off}; with cache, T_{on}; miss rate, m_{rate}.

Therefore,
$T_{on} = (1 - miss_{rate})(T_{off} - G) + miss_{rate}(T_{off+L})$.

We also know that cache is not useful when,
$T_{off} \leq (1 - miss_{rate})(T_{off} - G) + miss_{rate}(T_{off+L})$.
$miss_{rate} \geq \frac{G}{G+L} \geq \frac{104}{109} \approx 0.95$
Therefore, the highest miss rate after the cache use would be disadvantageous is 95%.

Problem B.8

a) Assuming the misses are not overlapped in memory, this imply that their effects will be accumulated. Therefore, it will take $4 * 100 = 400$ cycles.

b) Since the cache line size is 16 bytes, then every 4 iteration will mess elements a,b,c, and d. Thus, in average number of cycles an average iteration will take is $\frac{400}{4} = 100$ cycles.

c) Same as b), instead it will be every 16 iteration. Thus, in average number of cycles an average iteration will take is $\frac{400}{16} = 25$ cycles.

d) If the cache is direct-mapped and its size is reduced to 2048 bytes. It will make every array access to be a miss. This is true because for each a_i, b_i, c_i and d_i will map to the same cache line. This implies that every iteration will have 3 read misses (a_i, b_i, c_i) and 1 write miss (d_i). Beside this, we know that there will be a cost of a write back for d_i that goes from iteration 1 through 511.
Therefore, the average number of cycles is $(4 + \frac{511}{512}) * 100$

Problem B.12

a) Let $AMAT_{direct}$ be the direct-mapped cache; $\text{AMAT}_{associative}$ the 4-way associative cache; and, m_i the miss rate of a cache. Therefore, if the miss penalty is $100ns$ we can conclude the following.
$\text{AMAT}_{direct} = 0.22 + 100 * m_1$
$\text{AMAT}_{associative} = 0.52 + 100 * m_2$

Thus, it will be advantageous to use the smaller cache when:
$\text{AMAT}_{direct} \leq \text{AMAT}_{associative}$
$0.22 + 100 * m_1 \leq 0.52 + 100 * m_2$
$m_1 \leq 0.003 + m_2$

b) We know that AMAT = Hit time = Miss Rate $*$ Miss Penalty, where
Miss Penalty = Hit Time * Cycles. Therefore,
Miss penalty of 10: $m_1 \leq 0.136 + 2.364m_2$
Miss penalty of 1000: $m_1 \leq 0.0136 + 2.364m_2$

Thus, you should use a smaller cache when the data being cache is small.

Problem C.1

a)

Register	Line #s of the instructions	Type of data dependencies, e.g., RAW, WAR, WAW
x1	1,2	RAW
x1	1,2	WAW
x2	4,5	RAW
x4	5, 6	RAW

b)

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Loop: ld x1,0(x2)	F	D	X	M	W													
addi x1,x1,1		F	s	s	D	X	M	W										
sd x1,0(x2)					F	s	s	D	X	M	W							
addi x2,x2,4								F	D	X	M	W						
sub x4,x3,x2									F	s	s	D	X	M	W			
bnez x4,Loop												F	s	S	D	X	M	W

The loop takes 1586 cycles.
We know that $x_3 = x_2 + 396$ which implies that the loop will run $\frac{396}{4} = 99$ times. We also know that due to flushing, the loop will take 16 cycles. We also know that the last loop will run 18 cycles. Therefore, the total of cycles is $98 * 16 + 18 = 1586$.

Problem C.3

a) We know that MEM stage is the slowest, $2ns$ and the pipeline register delay is $0.1ns$. Therefore the clock cycle time is $2.1ns$.

b) We know that the ideal CPI is 1. Since there is a stall every 4 instruction.
CPI $= 1 + \frac{1}{4} = 1.25$

c)
Speedup $= \frac{I*1*7}{I*1.25*2.1} = 2.67$.

d)
The speedup would be equal to the number of tasks/instruction

Problem C.7

a)
Execution time of 5-stage $= I * (1 + \frac{1}{5}) * 1 = 1.20I$
Execution time of 12-stage $= I * (1 + \frac{3}{8}) * 0.6 = 0.825I$
Speedup $= \frac{1.25}{0.825} = 1.45$

b)
$CPI_{5-stages} = \frac{6}{5} + 0.20 * 0.05 * 2 = 1.22$
$CPI_{12-stages} = \frac{11}{8} + 0.20 * 0.05 * 5 = 1.425$