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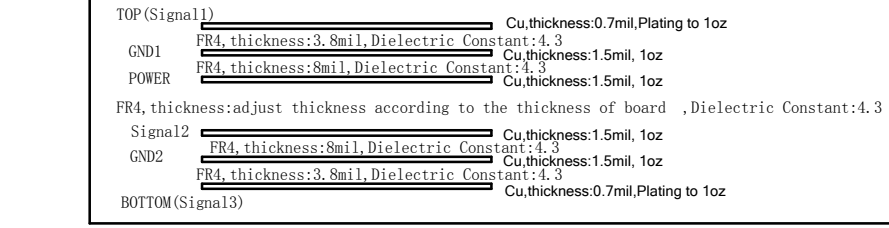
6 LAYERS PCB STACK



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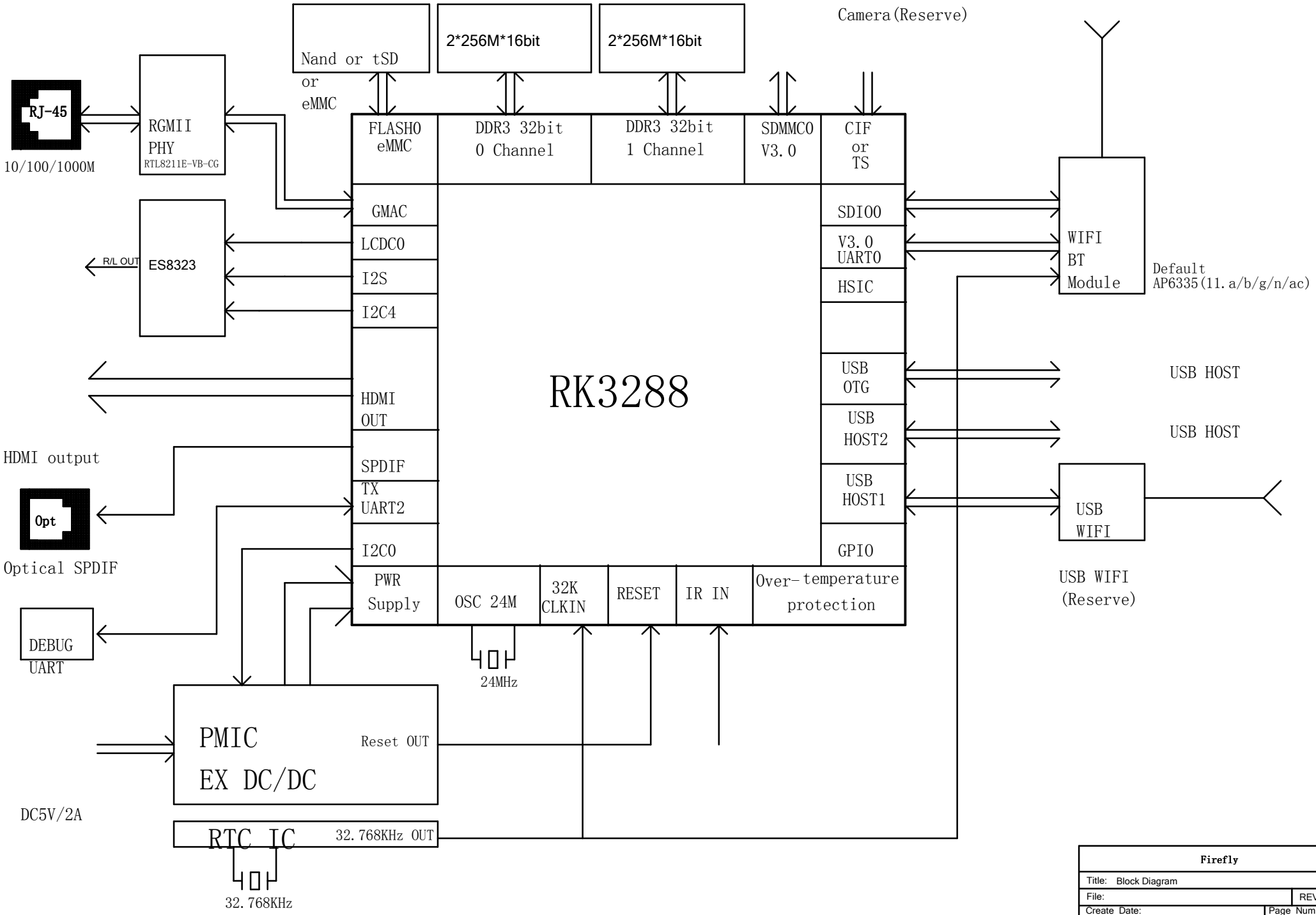
Create Date:	Page Num: 1
Modify Date: Wednesday, June 18, 2014	Page Total: 21



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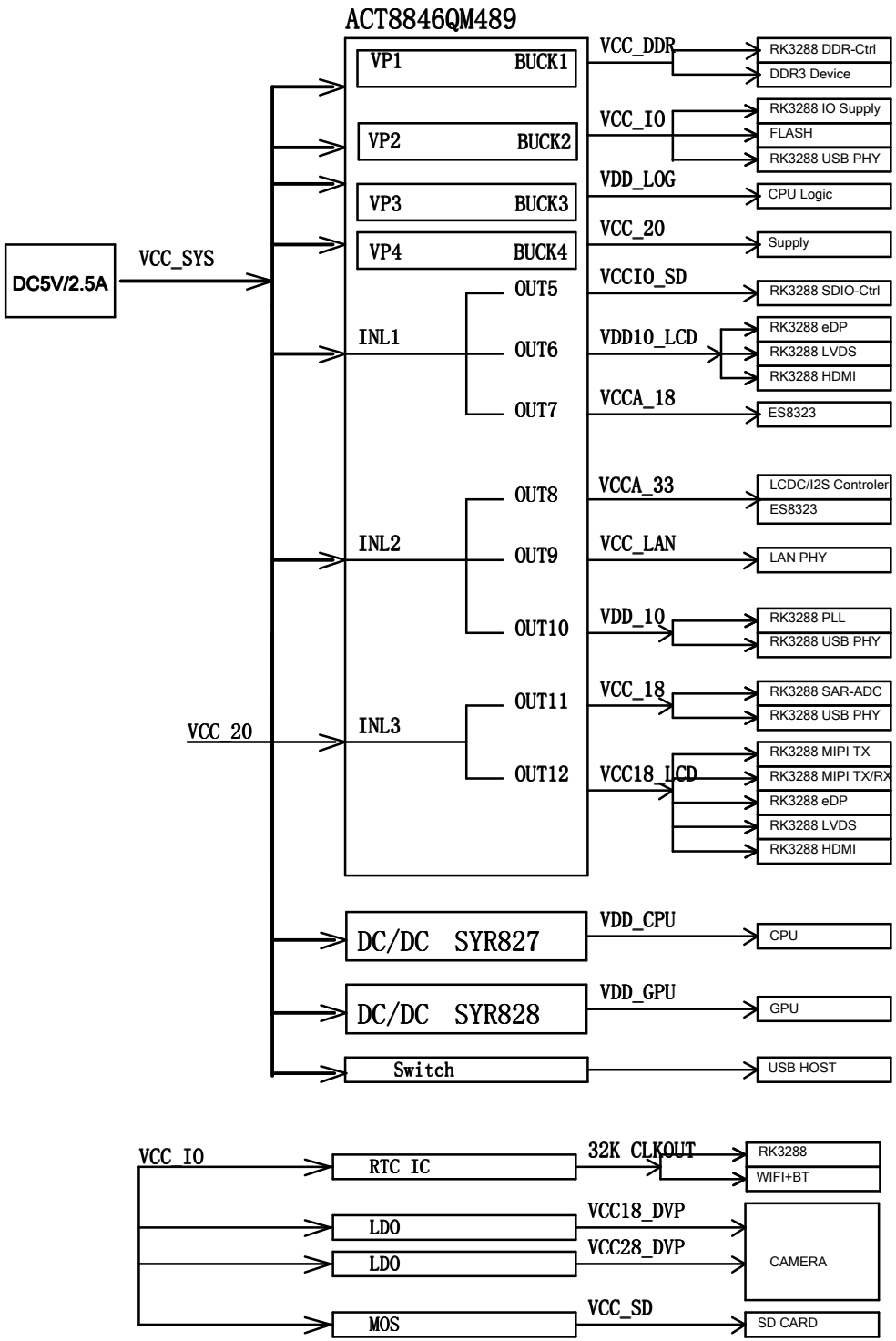
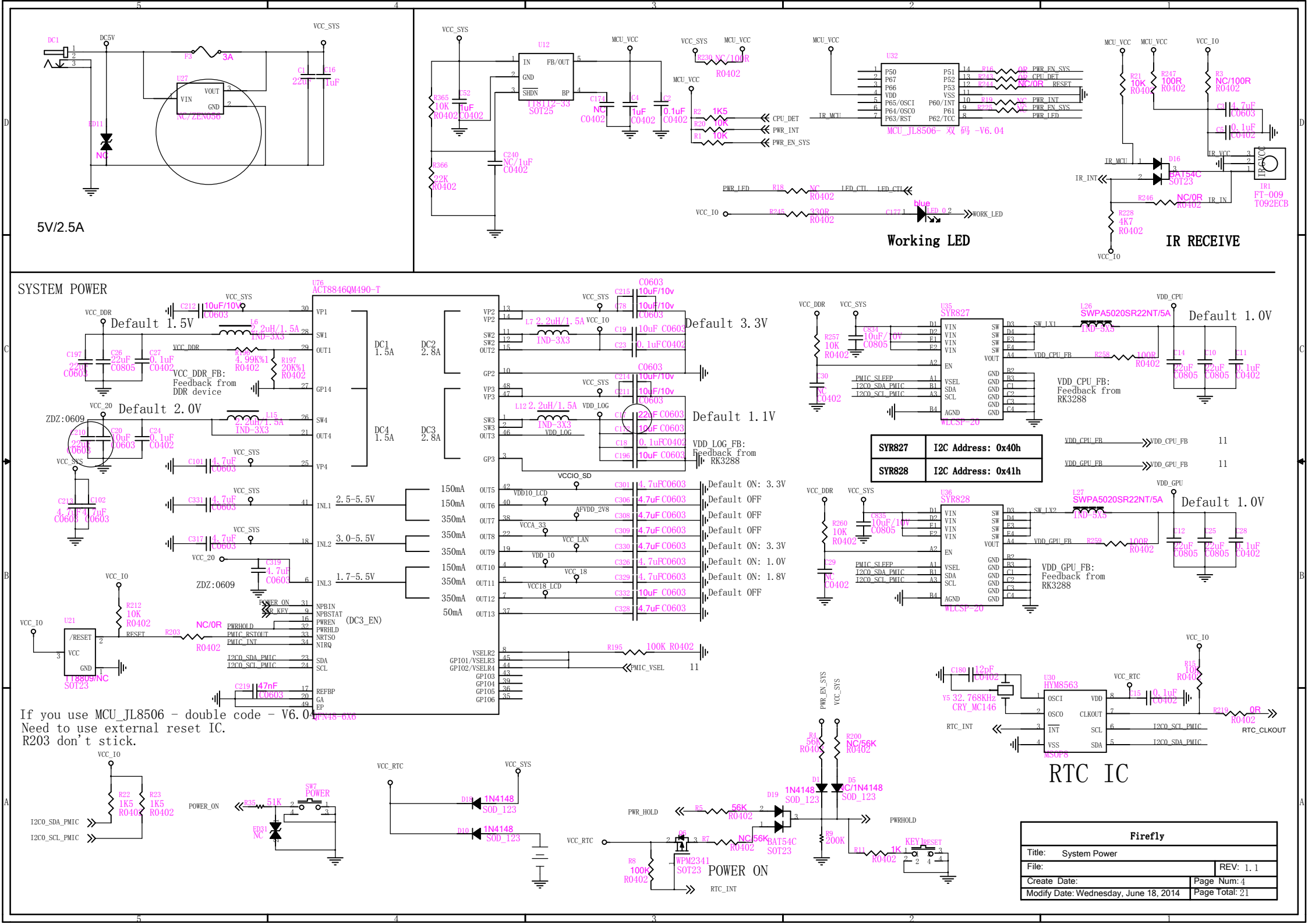
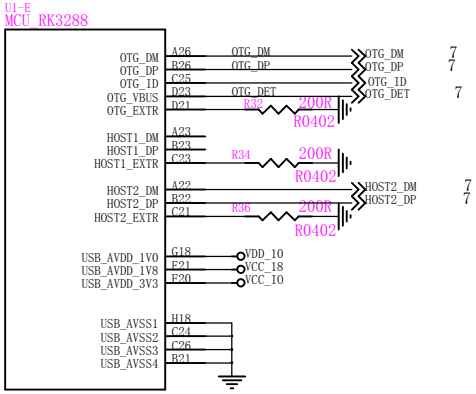


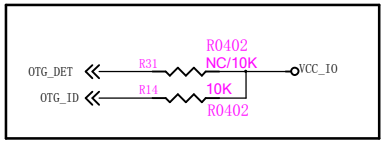
PowerName	PMIC Channel	timer(2mS)	Default	Working
VCC_20	DCDC4	Solt:0	voltage 2.0V	voltage 2.0V
VDD_10	OUT10	Solt:1	1.0V	1.0V
VCC_DDR	DCDC1	Solt:2	1.5V	1.5V(DDR3)
VDD_CPU	EX DCDC	Solt:2A	(FB=1.2V) 1.0V	DVFS
VDD_GPU	EX DCDC	Solt:2B	1.0V	DVFS
VDD_LOG	DCDC3	Solt:3	1.1V	DVFS
VCC_18	OUT11	Solt:4	1.8V	1.8V
VCC_LAN	OUT9	Solt:5	3.3V	3.3V
VCC_IO	DCDC2	Solt:6	3.3V	3.3V
VCCIO_SD	OUT5	Solt:6	3.3V	SD2.0:3.3V
VCCA_33	OUT8	OFF	OFF	SD3.0:1.8V 3.3V
VCCA_18	OUT7	OFF	OFF	1.8V
VDD10_LCD	OUT6	OFF	OFF	1.0V
VCC18_LCD	OUT12	OFF	OFF	1.8V

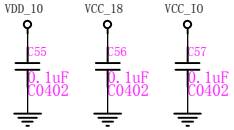
Firefly	
Title: Power Tree	
File:	REV: 1.1
Create Date:	Page Num: 3
Modify Date: Wednesday, June 18, 2014	Page Total: 21

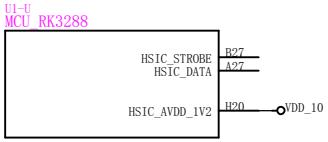

5V/2.5A
Working LED
IR RECEIVE
SYSTEM POWER
Default 1.5V
Default 2.0V
Default 3.3V
Default 1.1V
Default 1.0V
VCC_DDR_FB: Feedback from DDR device
VDD_LOG_FB: Feedback from RK3288
VDD_CPU_FB: Feedback from RK3288
VDD_GPU_FB: Feedback from RK3288
SYR827 I2C Address: 0x40h
SYR828 I2C Address: 0x41h
If you use MCU_JL8506 - double code - V6.04
Need to use external reset IC.
R203 don't stick.
POWER ON
RTC IC
Firefly
Title: System Power
File:
REV: 1.1
Create Date:
Page Num: 4
Modify Date: Wednesday, June 18, 2014
Page Total: 21



RK3288_E







RK3288_U

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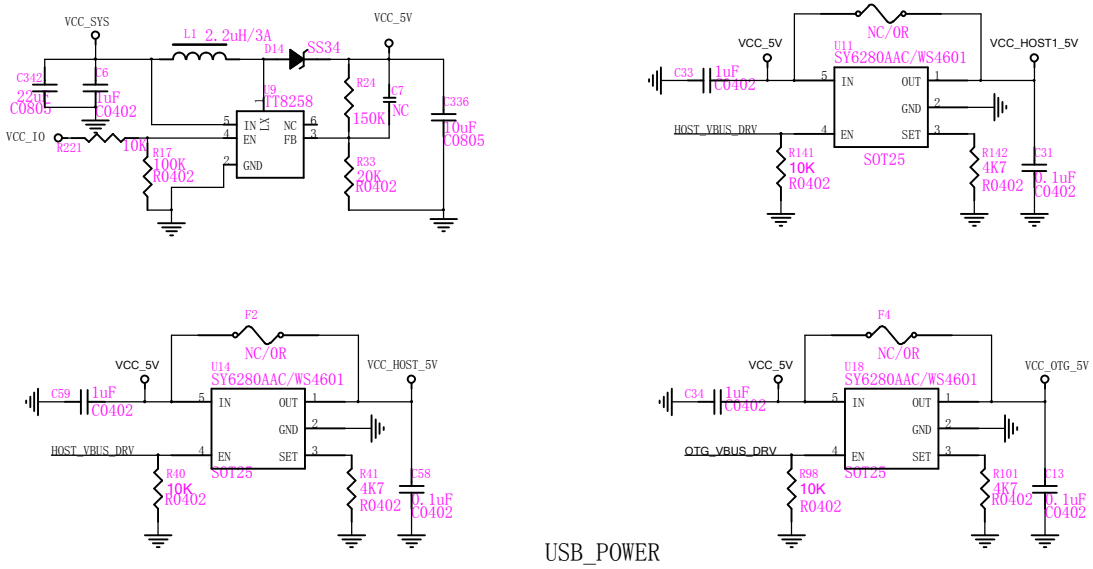
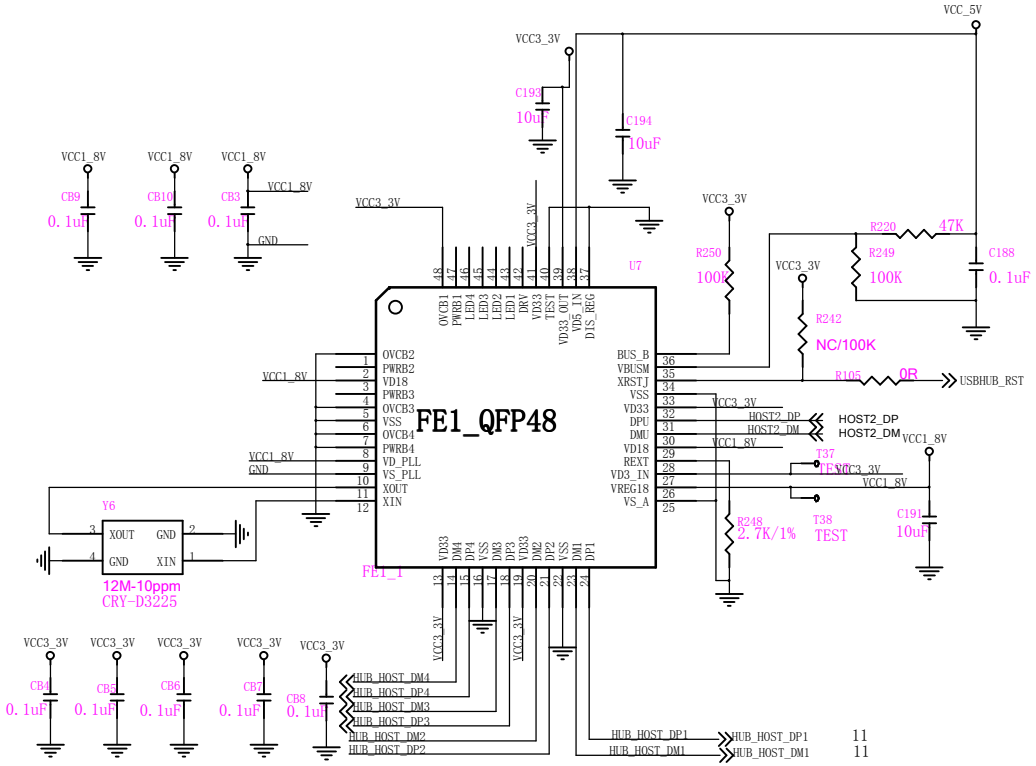
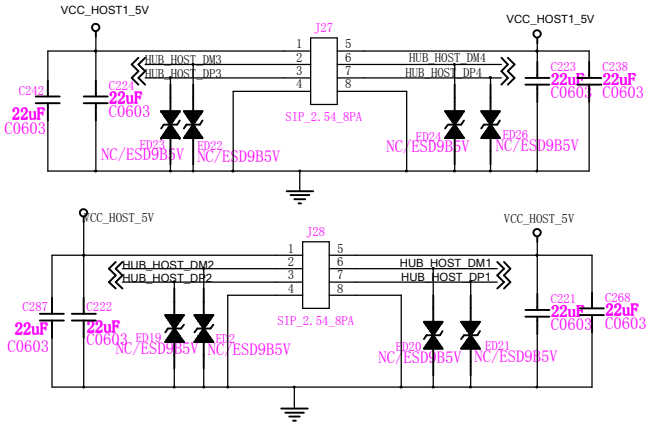
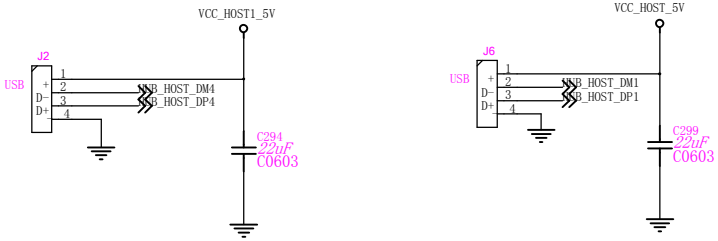


USB_POWER

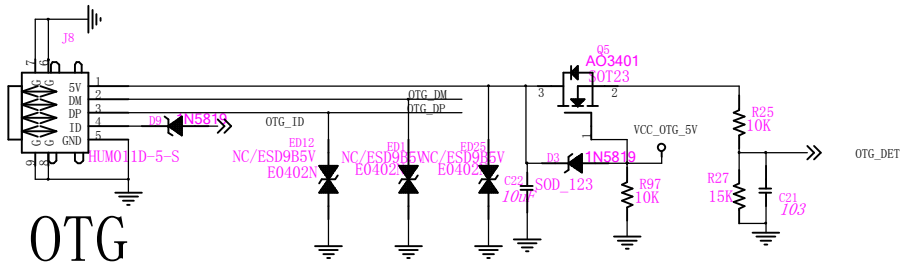


HUB CHIP





HOST



OTG

Firefly	
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File:	REV: 1.1
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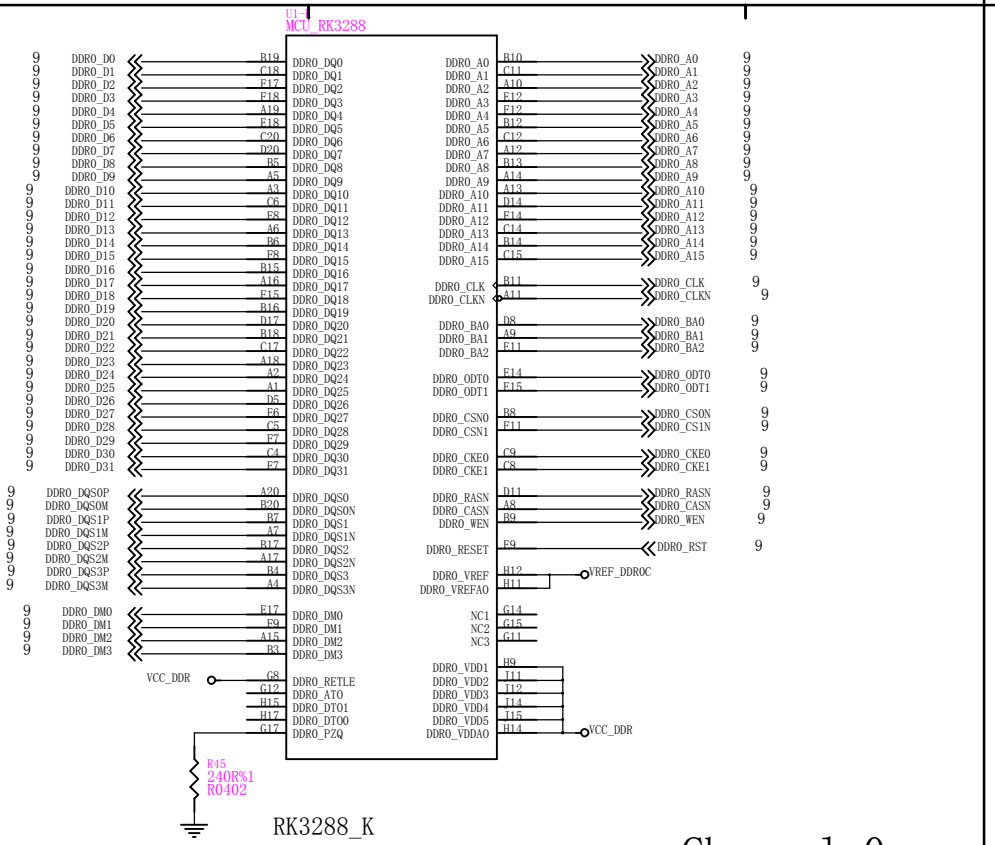
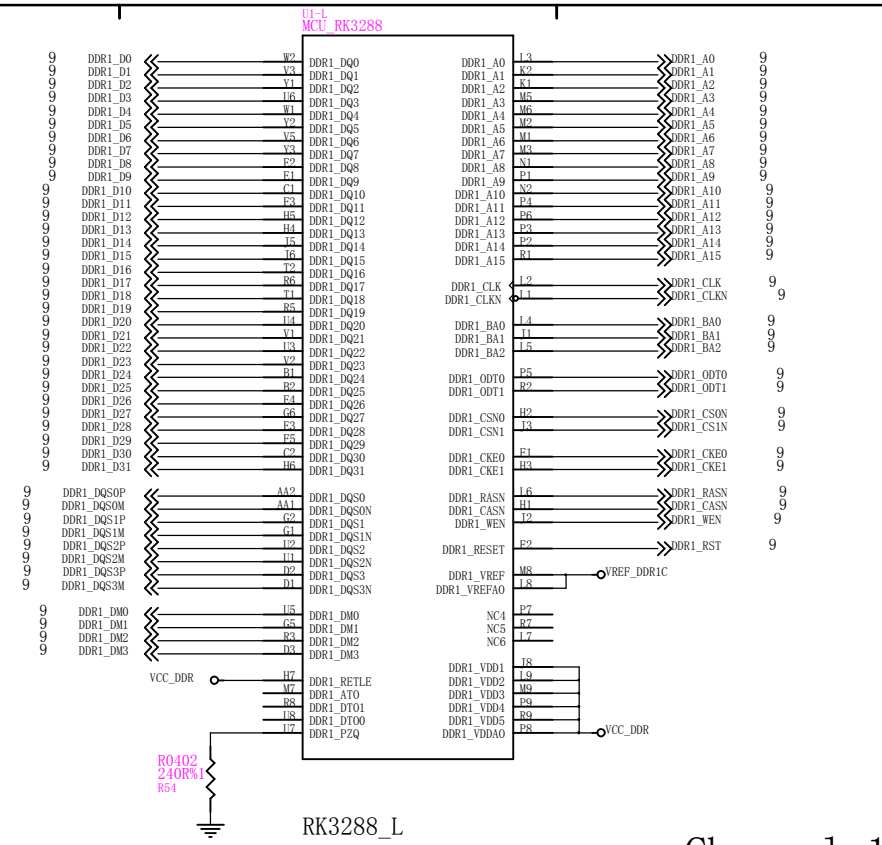
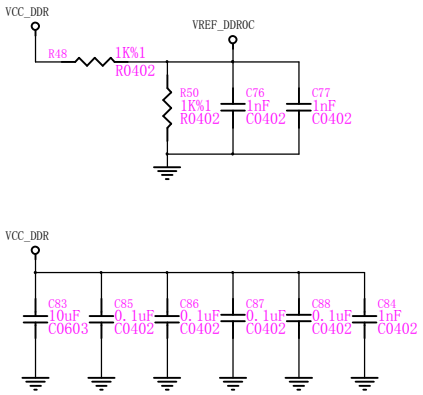
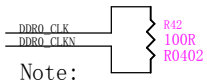


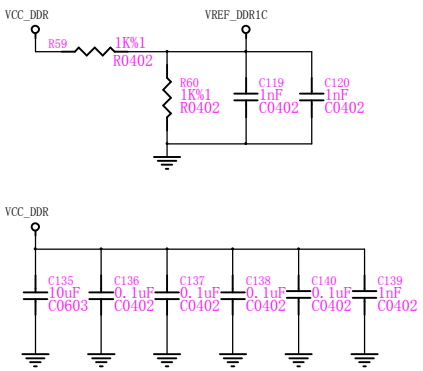




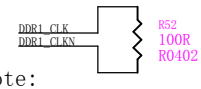
DDR0 FILTER



Note:
These termination resistors must be placed
in the middle of trace, and the termination resistor of CLK must be placed in thebifurcation point.



DDR1 FILTER



Note:
These termination resistors must be placed
in the middle of trace, and the termination resistor of CLK must be placed in thebifurcation point.

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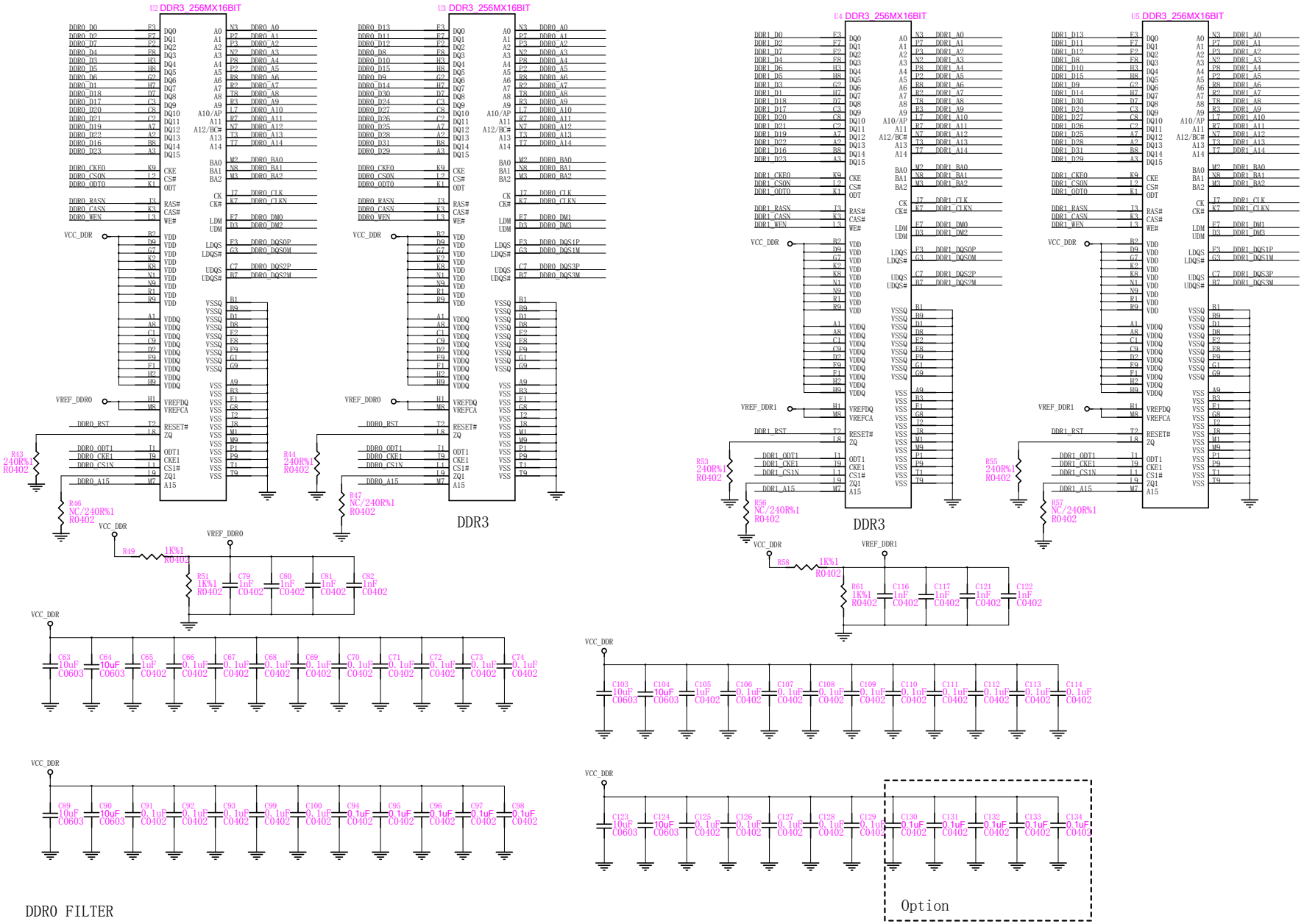

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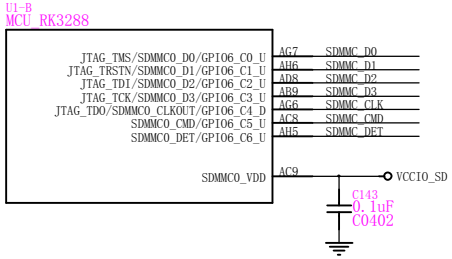
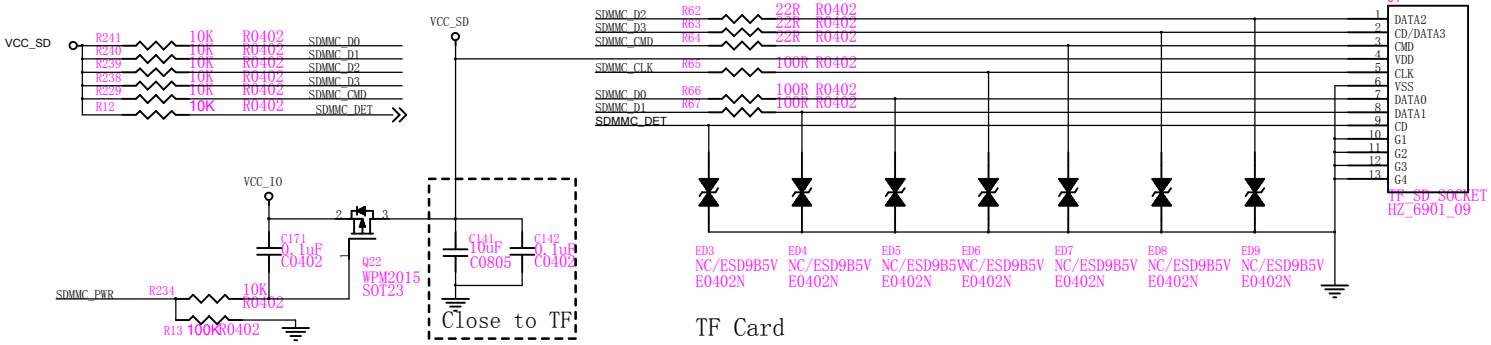
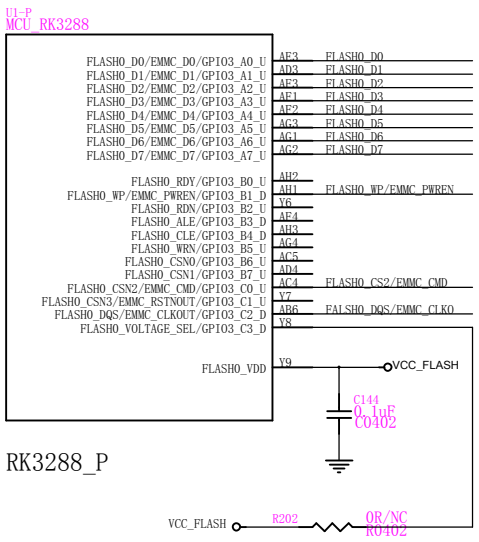
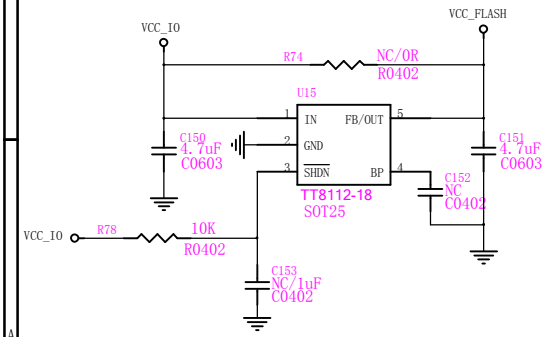
Modify Date: Wednesday, June 18, 2014	Page Total: 21

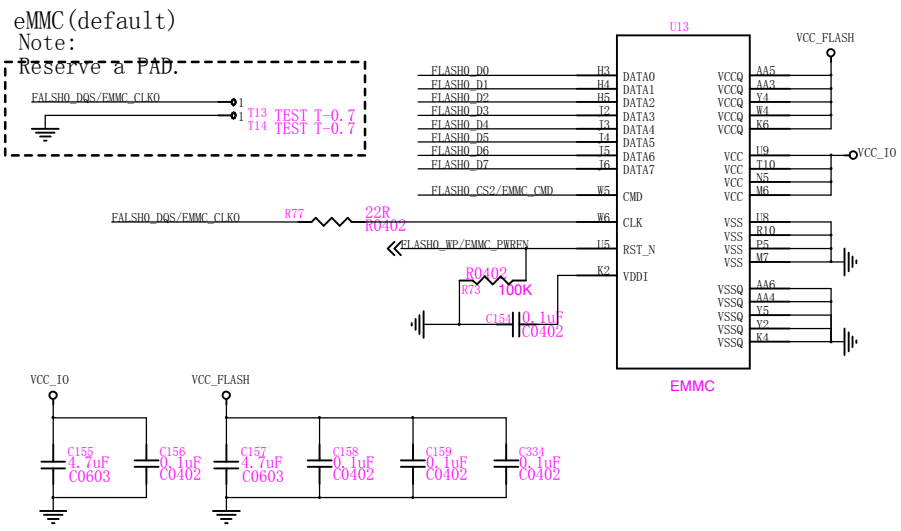


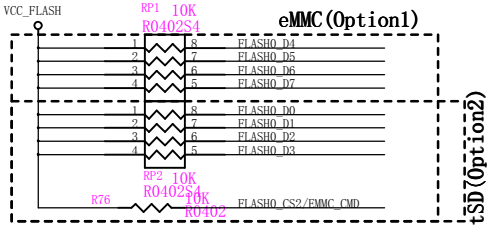






Flash Power





Pull-up select

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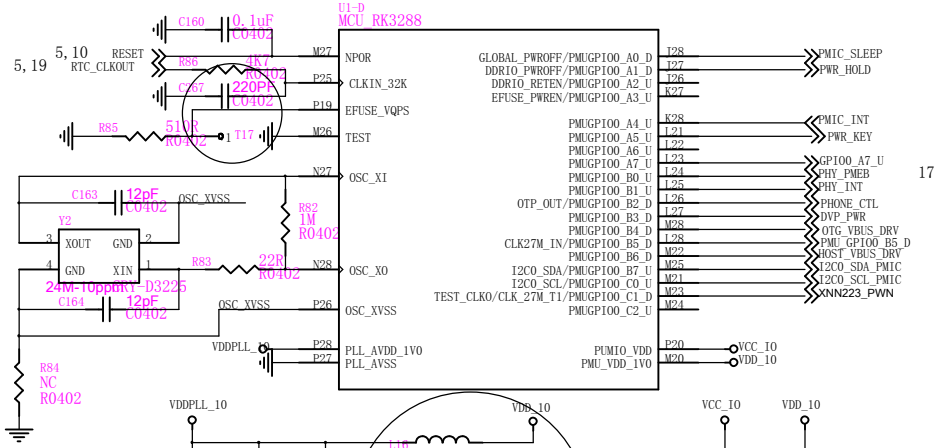
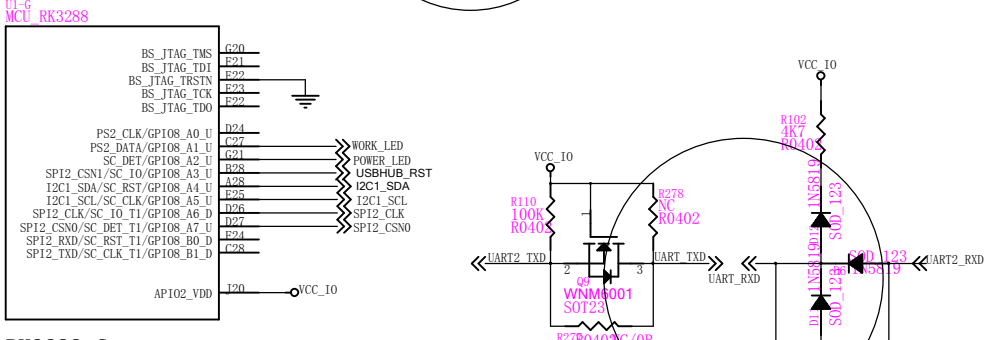
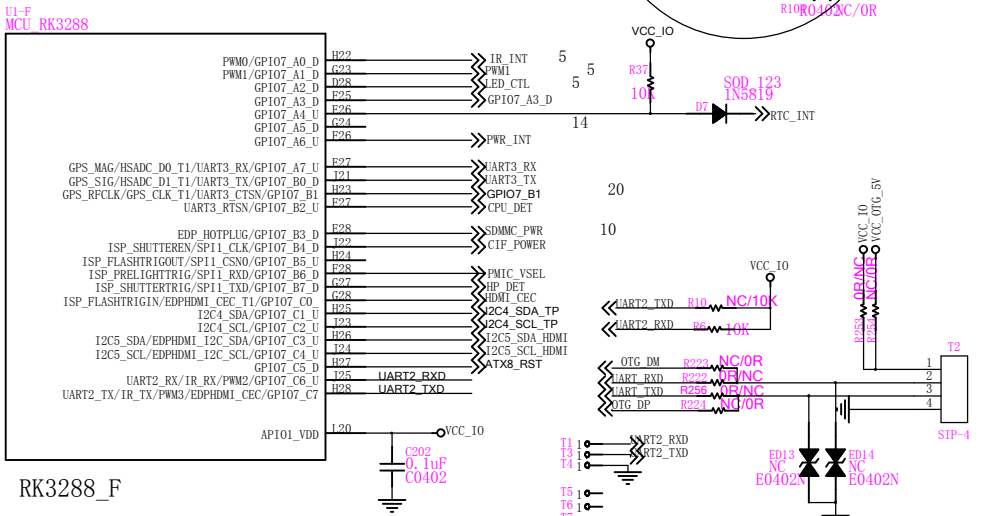
File:	REV: 1.1
Create Date:	Page Num: 9
Modify Date: Wednesday, June 18, 2014	Page Total: 21



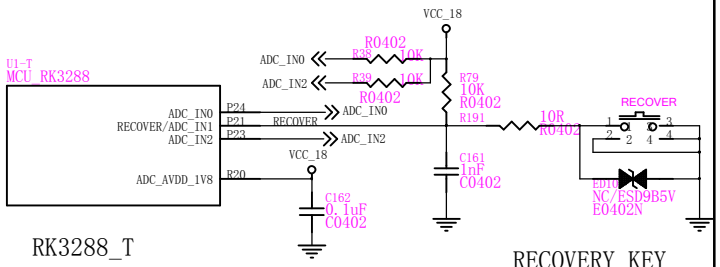
RK3288_D



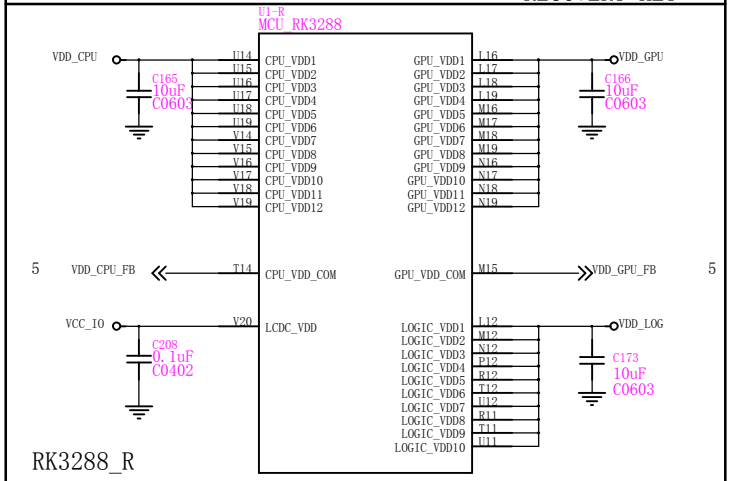
RK3288_G



RK3288_F



RK3288_T RECOVERY KEY



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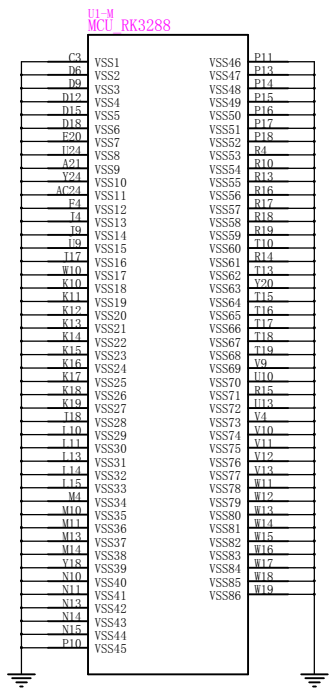
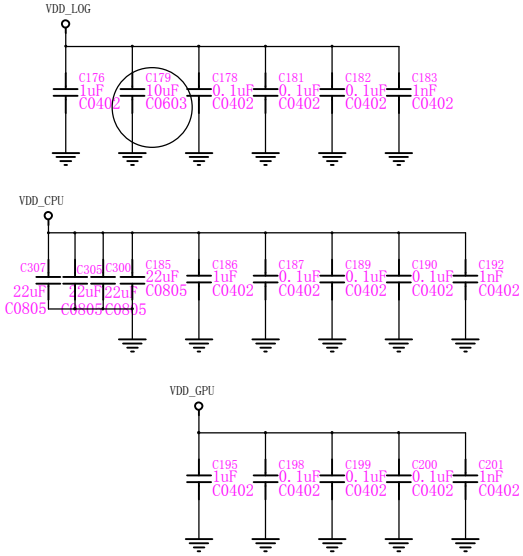
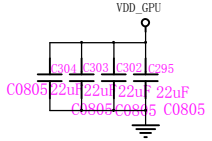


RK3288_M

RK3288 FILTER



Place the Component
if need to write eFUSE



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Title: RK3288 GPIO/POWER	
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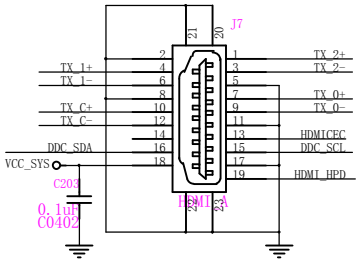
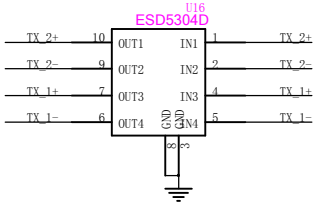
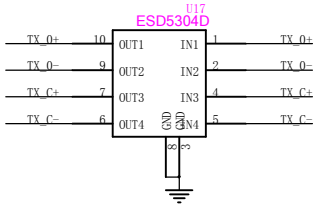
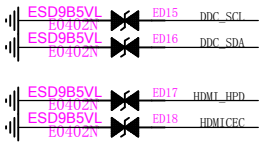
Modify Date: Wednesday, June 18, 2014	Page Total: 21

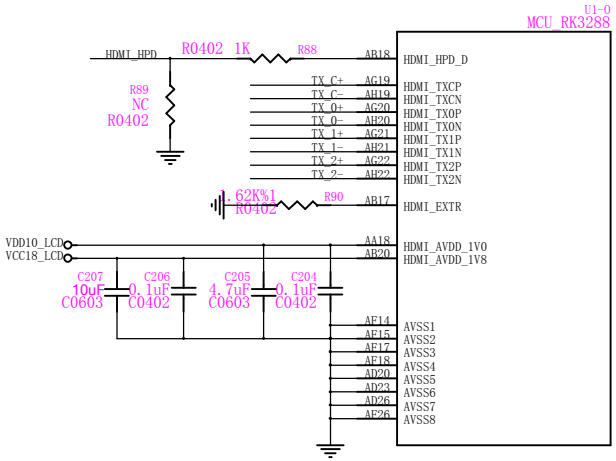


HDMI OUT

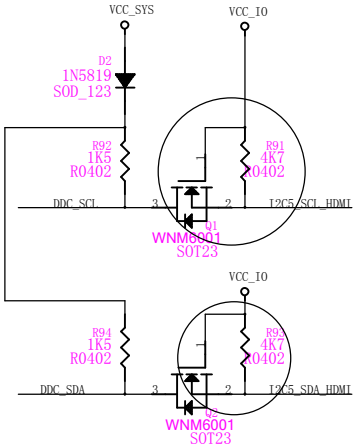


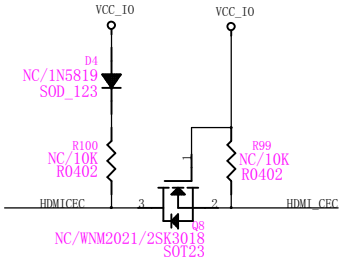






RK3288_0





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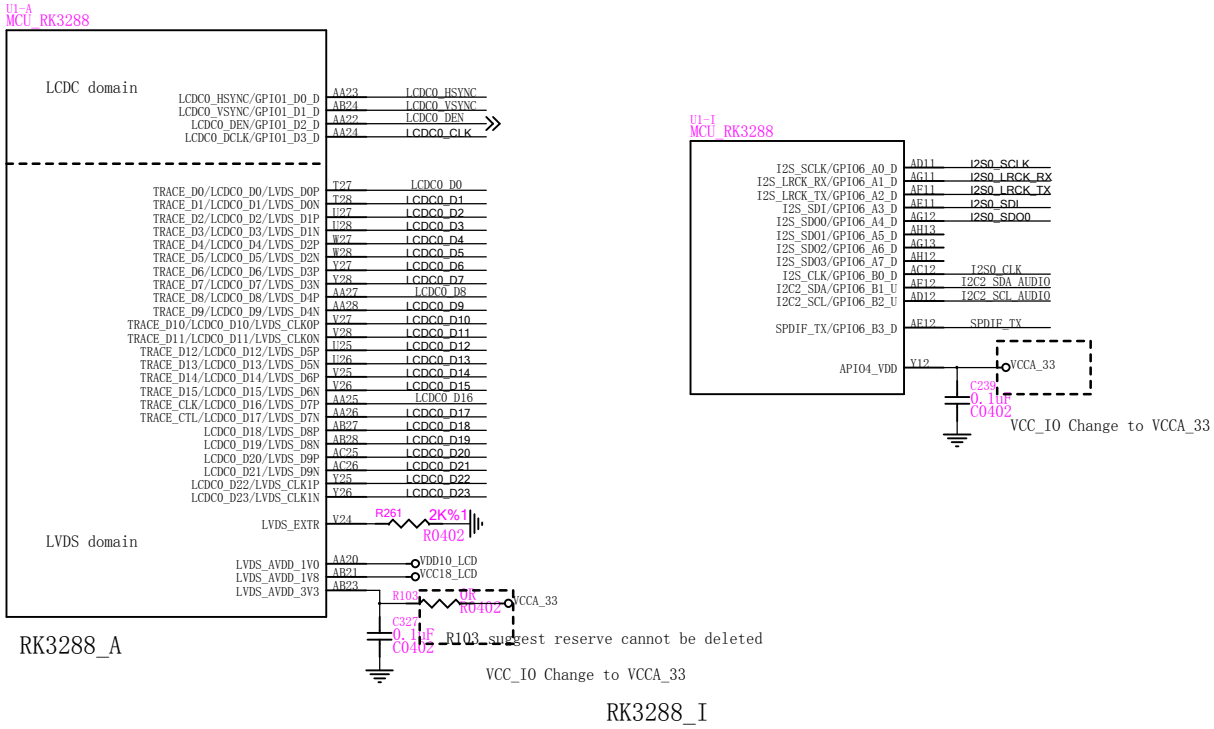
Page Total:21	Modify Date: Wednesday, June 18, 2014



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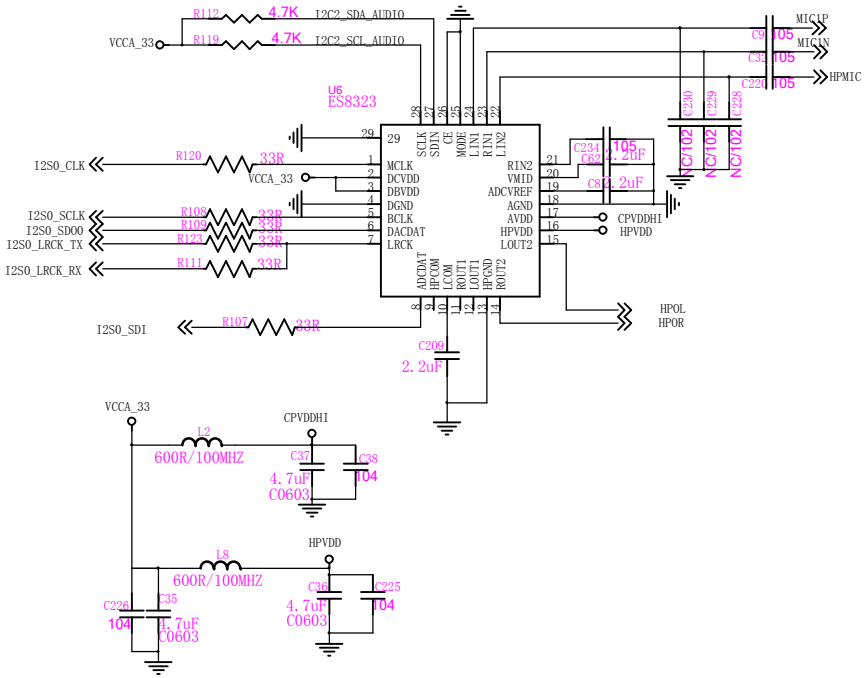
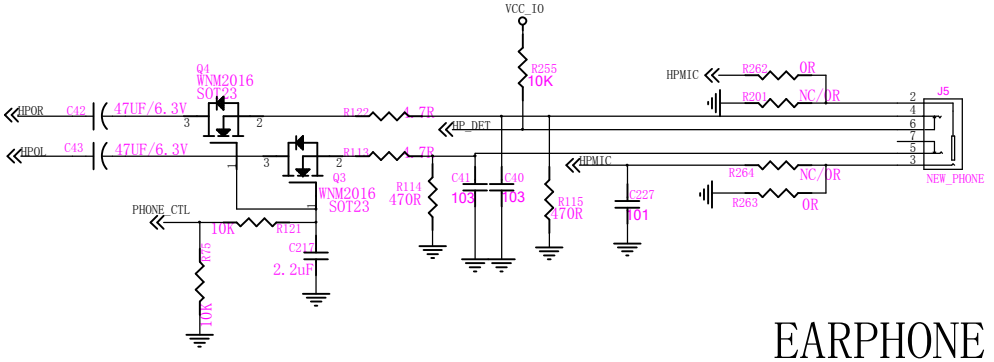
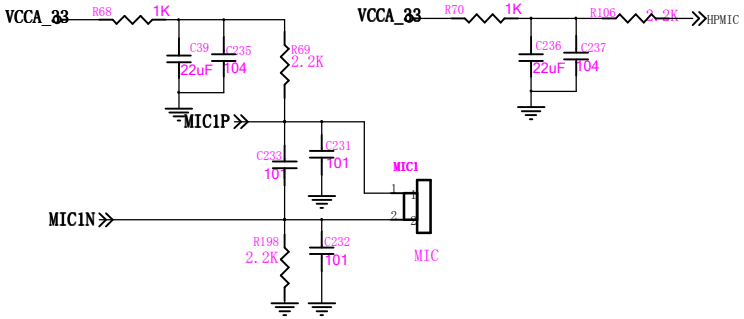
File:		REV: 1.1
Create Date:		Page Num: 12
Modify Date: Wednesday, June 18, 2014		Page Total: 21



ES8323



EARPHONE

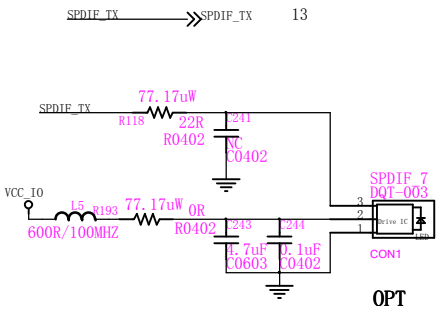


MIC

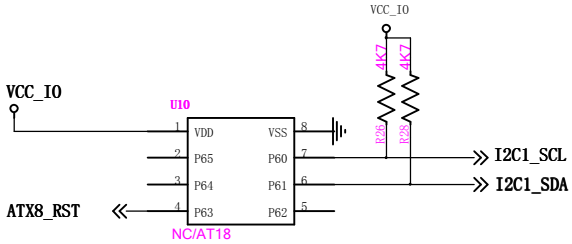
If the connection to the international standard, R262 R263 don't pick up

If the connection is millet, R201 R264 don't pick up

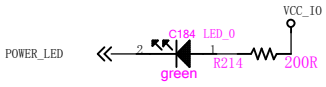
Firefly	
Title: ES8323	
File:	REV:1.1
Create Date:	Page Num: 13
Modify Date: Wednesday, June 18, 2014	Page Total: 21



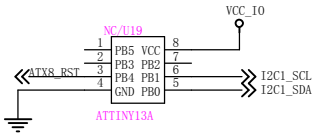
Optical S/PDIF OUT



AT18



WORKING_LED



ATTINY13A

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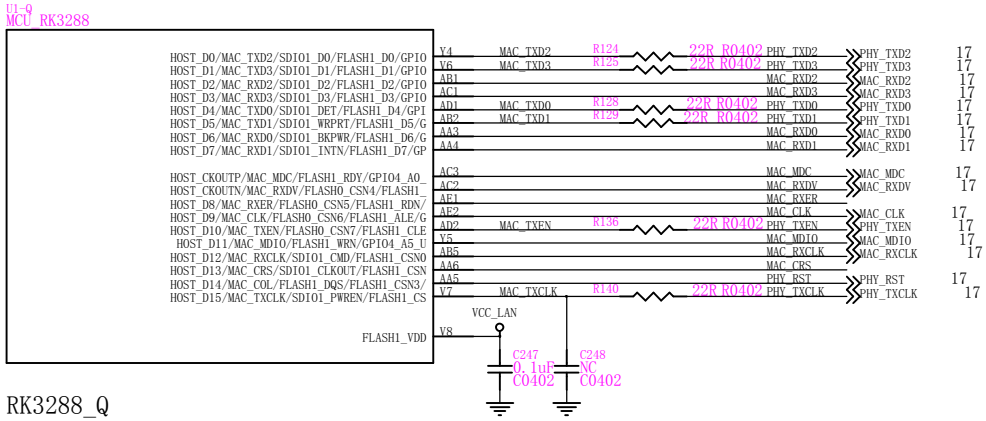
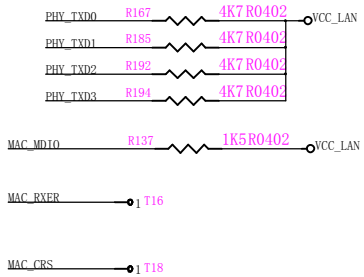
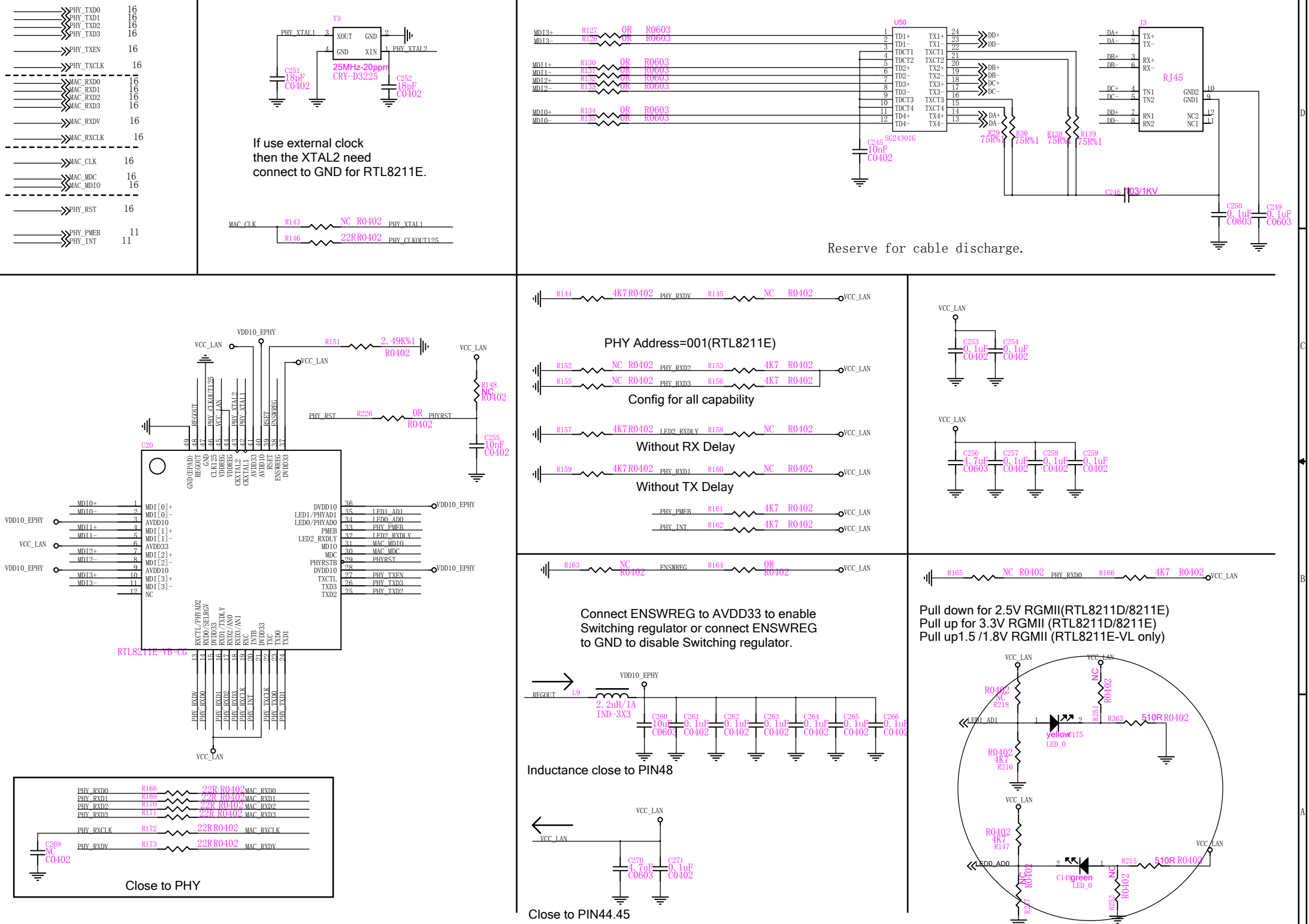
File:	REV:1.1	
Create Date:	Page Num: 14	
Modify Date: Wednesday, June 18, 2014	Page Total: 21	

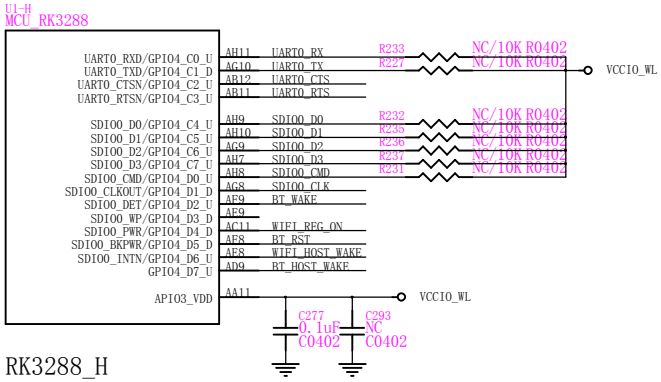


RK3288_Q



Firefly	
Title: RK3288 EthernetMAC Controler	
File:	REV:1.1
Create Date:	Page Num: 15
Modify Date: Wednesday, June 18, 2014	Page Total: 21


PHY_TXD0 16
PHY_TXD1 16
PHY_TXD2 16
PHY_TXD3 16
PHY_TXEN 16
PHY_TXCLK 16
MAC_RXD0 16
MAC_RXD1 16
MAC_RXD2 16
MAC_RXD3 16
MAC_RXDV 16
MAC_RXCLK 16
MAC_CLK 16
MAC_MDC 16
MAC_MDIO 16
PHY_RST 16
PHY_PMEB 11
PHY_INT 11
Y3
PHY_XTAL1
PHY_XTAL2
XOUT GND
GND XIN
25MHz-20ppm
CRY-D3225
C251 18pF C0402
C252 18pF C0402
If use external clock
then the XTAL2 need
connect to GND for RTL8211E.
MAC_CLK R143 NC R0402 PHY_XTAL1
R146 22R R0402 PHY_CLKOUT125
MDI3+ MDI3- MDI1+ MDI1- MDI2+ MDI2- MDI0+ MDI0-
R127 R128 R130 R131 R133 R135 R134 R136 0R R0603
U50
TD1+ TD1- TDCT1 TDCT2 TD2+ TD2- TD3+ TD3- TDCT3 TDCT4 TD4+ TD4-
TX1+ TX1- TXCT1 TXCT2 TX2+ TX2- TX3+ TX3- TXCT3 TXCT4 TX4+ TX4-
DD+ DD- DB+ DB- DC+ DC- DA+ DA-
SG24301G
C245 10nF C0402
R29 75R%1 R30 75R%1 R138 75R%1 R139 75R%1
J3
RJ45
TX+ TX- RX+ RX-
TN1 TN2 RN1 RN2
GND2 GND1 NC2 NC1
C246 103/1KV
C250 0.1uF C0603
C249 0.1uF C0603
Reserve for cable discharge.
VDD10_EPHY
VCC_LAN
R151 2.49K%1 R0402
R148 NC R0402
PHY_RST R226 0R R0402 PHYRST
C255 10nF C0402
U20
REGOUT PHY_CLKOUT125 VCC_LAN PHY_XTAL2 PHY_XTAL1 RSETT ENSWREG
GND(EPAD) REGOUT GND CLK125 VDDREG CKXTAL2 CKXTAL1 AVDD33 AVDD10 RSET ENSWREG DVDD33
MDI0+ MDI0- MDI1+ MDI1- AVDD33 MDI2+ MDI2- AVDD10 MDI3+ MDI3- NC
MDI[0]+ MDI[0]- AVDD10 MDI[1]+ MDI[1]- AVDD33 MDI[2]+ MDI[2]- AVDD10 MDI[3]+ MDI[3]-
DVDD10 LED1/PHYAD1 LED0/PHYAD0 PMEB LED2_RXDLY MDIO MDC PHYRSTB DVDD10 TXCTL TXD3 TXD2
LED1_AD1 LED0_AD0 PHY_PMEB LED2_RXDLY MAC_MDIO MAC_MDC PHYRST PHY_TXEN PHY_TXD3 PHY_TXD2
RXCTL/PHYAD2 RXD0/SELRGV DVDD33 RXD1/TXDLY RXD2/AN0 RXD3/AN1 RXC INTB DVDD33 TXC TXD0 TXD1
PHY_RXDV PHY_RXD0 PHY_RXD1 PHY_RXD2 PHY_RXD3 PHY_RXCLK PHY_INT PHY_TXCLK PHY_TXD0 PHY_TXD1
RTL8211E-VB-CG
VCC_LAN
R168 R169 R170 R171 R172 R173 22R R0402
PHY_RXD0 PHY_RXD1 PHY_RXD2 PHY_RXD3 PHY_RXCLK PHY_RXDV
MAC_RXD0 MAC_RXD1 MAC_RXD2 MAC_RXD3 MAC_RXCLK MAC_RXDV
C269 NC C0402
Close to PHY
R144 4K7 R0402 PHY_RXDV R145 NC R0402 VCC_LAN
PHY Address=001(RTL8211E)
R152 R155 NC R0402 PHY_RXD2 PHY_RXD3 R153 R156 4K7 R0402
Config for all capability
R157 4K7 R0402 LED2_RXDLY R158 NC R0402
Without RX Delay
R159 4K7 R0402 PHY_RXD1 R160 NC R0402
Without TX Delay
PHY_PMEB R161 4K7 R0402
PHY_INT R162 4K7 R0402
R163 NC R0402 ENSWREG R164 0R R0402
Connect ENSWREG to AVDD33 to enable
Switching regulator or connect ENSWREG
to GND to disable Switching regulator.
REGOUT L9 VDD10_EPHY
2.2uH/1A IND-3X3
C260 10uF C0603 C261 0.1uF C0402 C262 0.1uF C0402 C263 0.1uF C0402 C264 0.1uF C0402 C265 0.1uF C0402 C266 0.1uF C0402
Inductance close to PIN48
VCC_LAN
C270 4.7uF C0603 C271 0.1uF C0402
Close to PIN44.45
C253 0.1uF C0402 C254 0.1uF C0402
C256 4.7uF C0603 C257 0.1uF C0402 C258 0.1uF C0402 C259 0.1uF C0402
R165 NC R0402 PHY_RXD0 R166 4K7 R0402 VCC_LAN
Pull down for 2.5V RGMII(RTL8211D/8211E)
Pull up for 3.3V RGMII (RTL8211D/8211E)
Pull up1.5 /1.8V RGMII (RTL8211E-VL only)
R0402 NC R218
R0402 4K7 R216
R0402 4K7 R147
LED1_AD1 LED0_AD0
yellow 175 LED_0
green LED_0
R363 510R R0402
R215 510R R0402
R251 R252 NC R0402



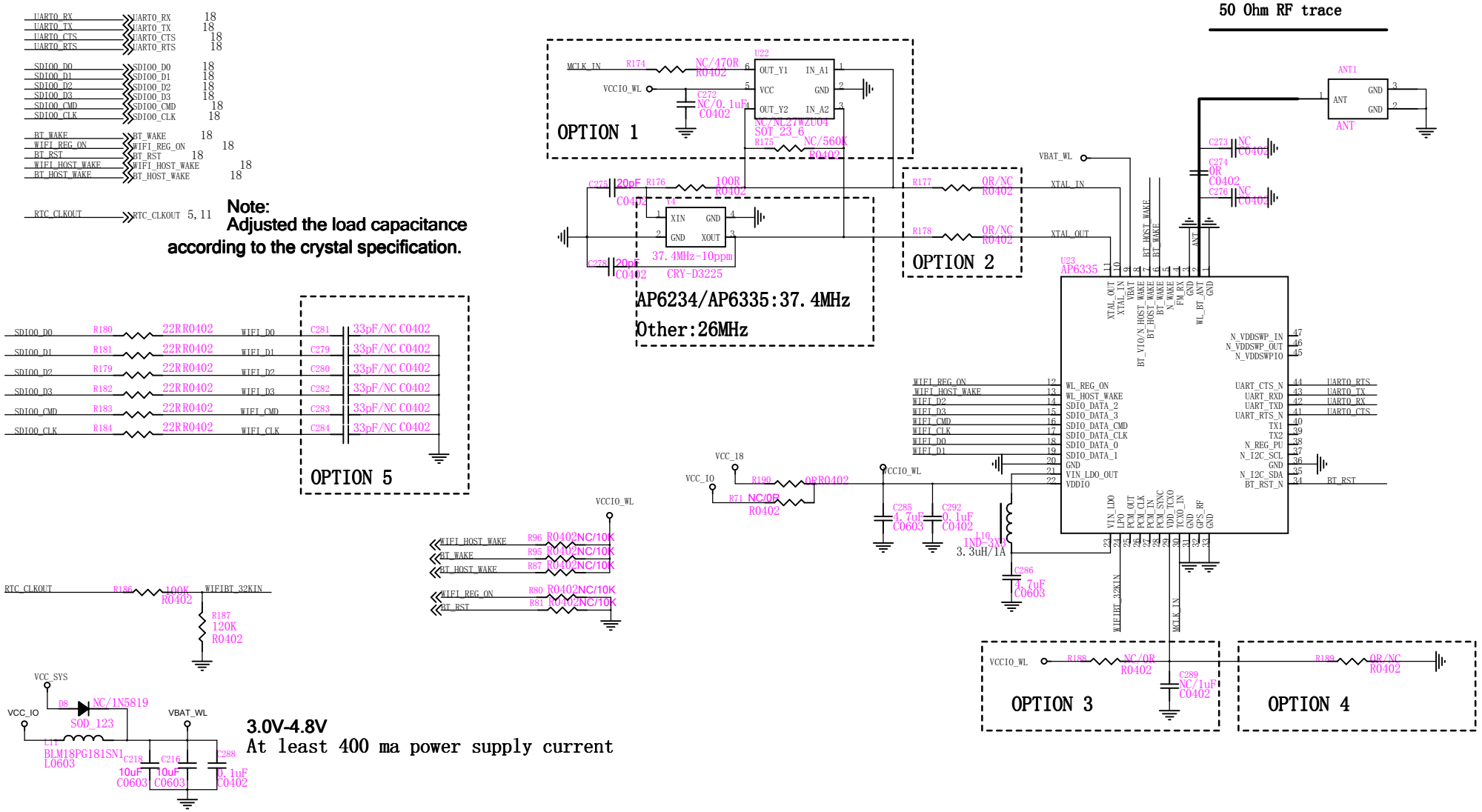
RK3288_H

UART0_RX — UART0_RX 19
UART0_TX — UART0_TX 19
UART0_CTS — UART0_CTS 19
UART0_RTS — UART0_RTS 19

SDIO0_D0 — SDIO0_D0 19
SDIO0_D1 — SDIO0_D1 19
SDIO0_D2 — SDIO0_D2 19
SDIO0_D3 — SDIO0_D3 19
SDIO0_CMD — SDIO0_CMD 19
SDIO0_CLK — SDIO0_CLK 19

BT_WAKE — BT_WAKE 19
WIFI_REG_ON — WIFI_REG_ON 19
BT_RST — BT_RST 19
WIFI_HOST_WAKE — WIFI_HOST_WAKE 19
BT_HOST_WAKE — BT_HOST_WAKE 19

Firefly	
Title: RK3288 SDIO0 Controler	
File:	REV:1.1
Create Date:	Page Num: 17
Modify Date: Wednesday, June 18, 2014	Page Total: 21



OPTION	WIFI				BT4.0	Crystals	VDDIO
	a	b/g/n	ac	5GHz			
AP6181		Yes				26MHz	1.71-3.6V
AP6210		Yes			Yes	26MHz	1.71-3.6V
AP6234	Yes	Yes		Yes	Yes	37.4MHz	1.6-3.4V
AP6330	Yes	Yes		Yes	Yes	26MHz	1.2-2.9V
AP6335	Yes	Yes	Yes	Yes	Yes	37.4MHz	1.71-3.63V

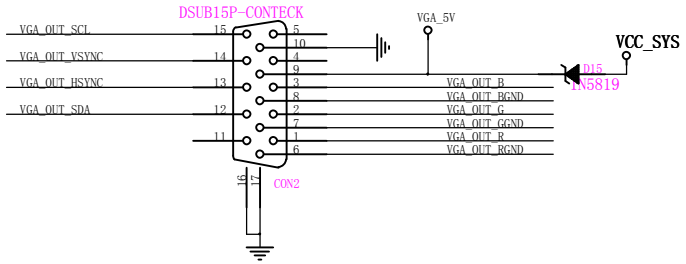
(Default)

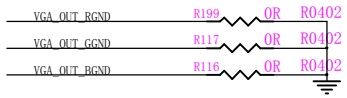
OPTION	1	2	3	4	5
AP6181	No	Yes	No	No	No
AP6210	Yes	No	Yes	No	No
AP6234	No	Yes	No	No	No
AP6330	No	Yes	No	No	No
AP6335	No	Yes	No	Yes	Yes

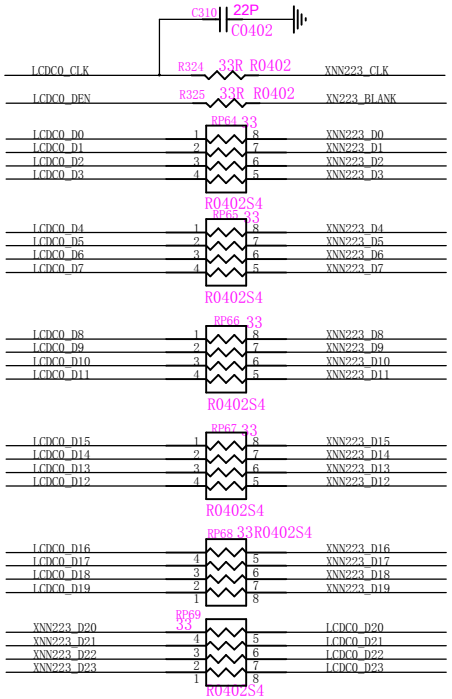
(Default)

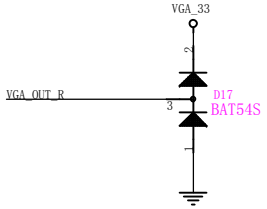
Note:
Yes:Inside the box to
No:The box is not posted

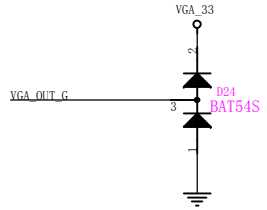
Firefly	
Title: AP6XXX-WIFI/BT	
File:	REV:1.1
Create Date:	Page Num: 18
Modify Date: Wednesday, June 18, 2014	Page Total: 21

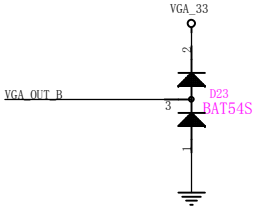


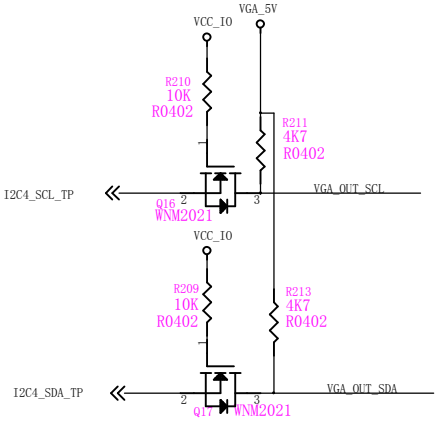


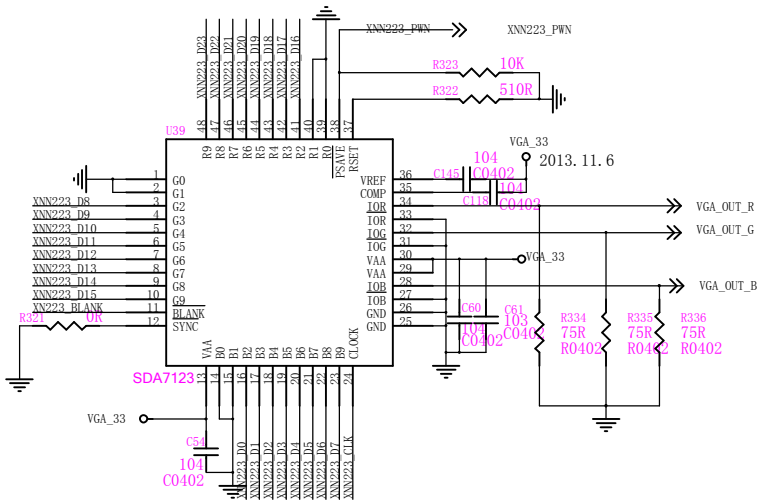




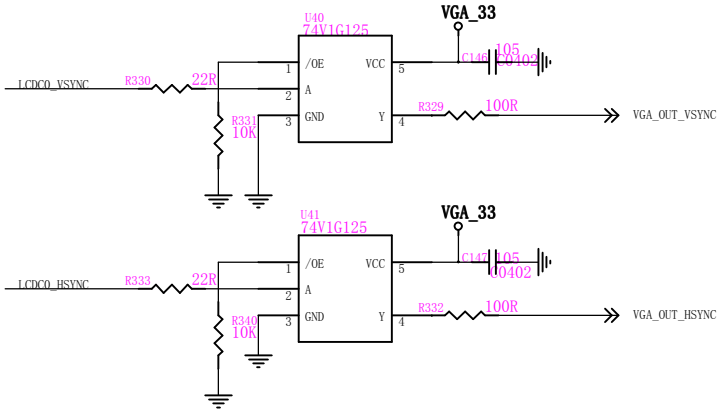


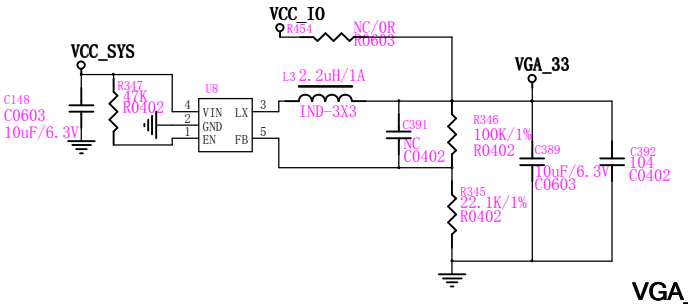






SDA7123





VGA_POWER

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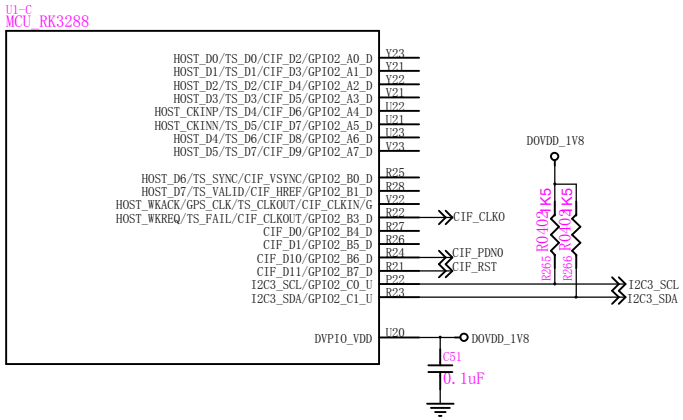
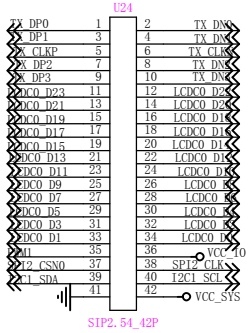
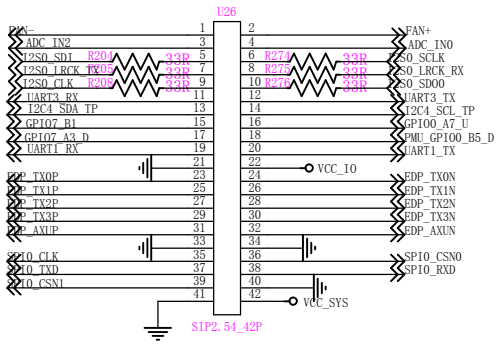
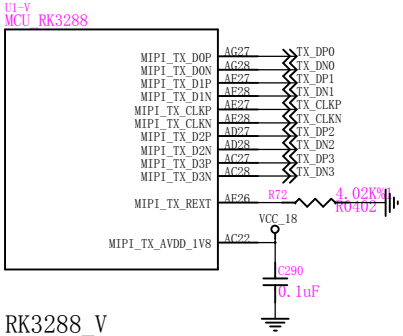
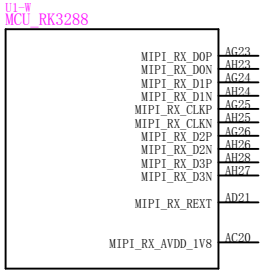
File:	REV:1.1
Create Date:	Page Num: 19
Modify Date: Wednesday, June 18, 2014	Page Total: 21

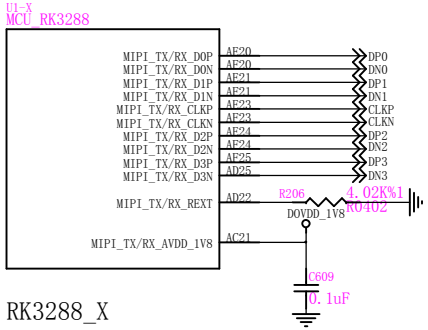


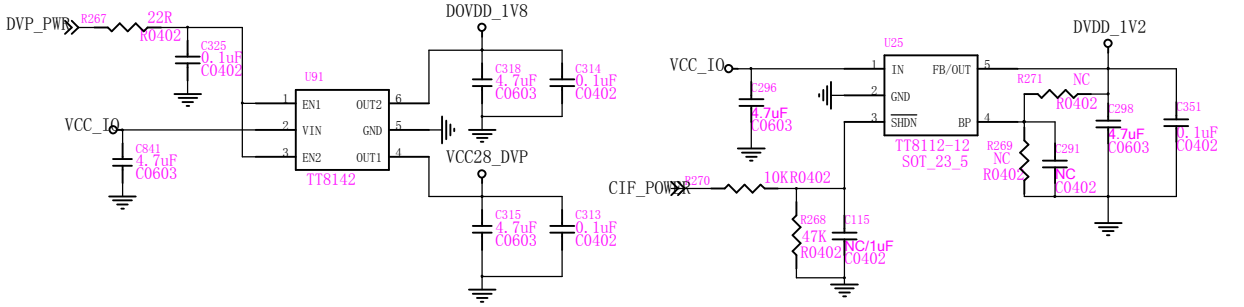


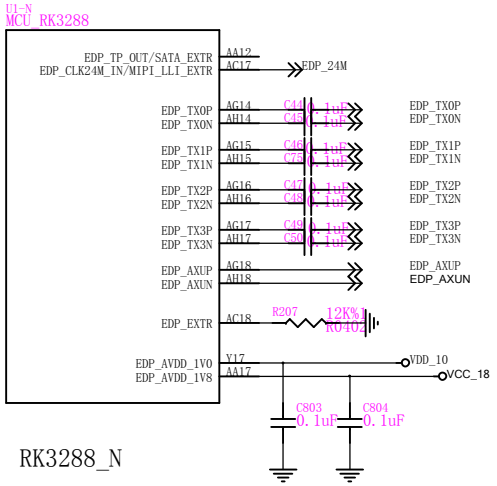


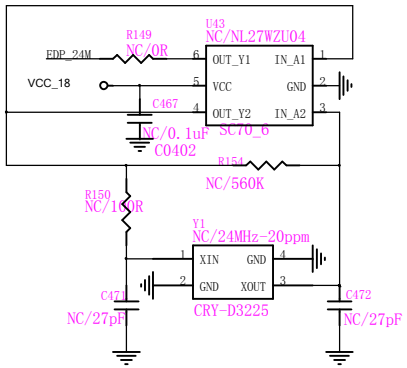


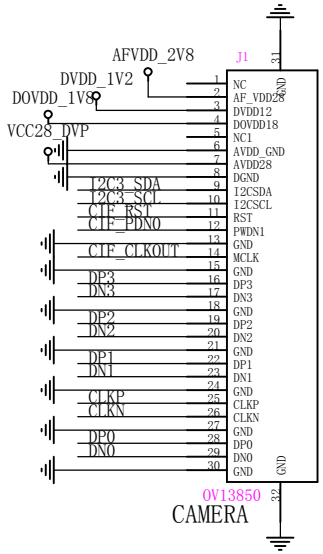


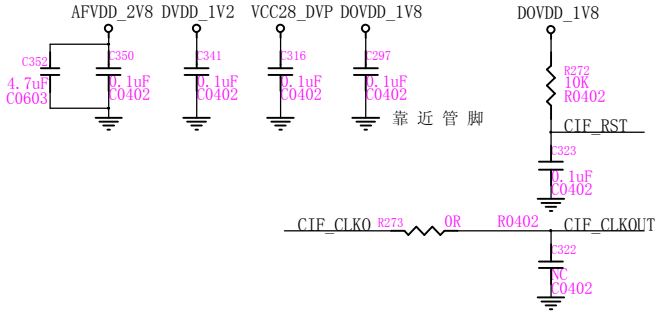












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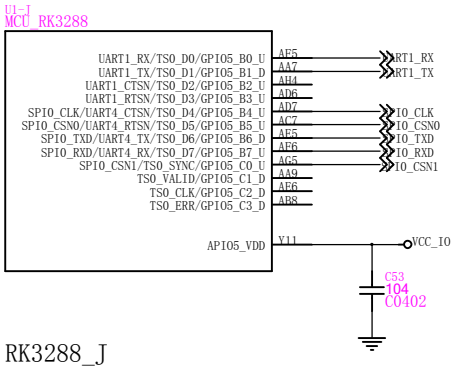
File:	REV:1.1
Create Date:	Page Num: 20
Modify Date: Wednesday, June 18, 2014	Page Total: 21



RK3288_J

Firefly	
Title: DTV-(Reserve)	
File:	REV:1.1
Create Date:	Page Num: 21
Modify Date: Wednesday, June 18, 2014	Page Total: 21