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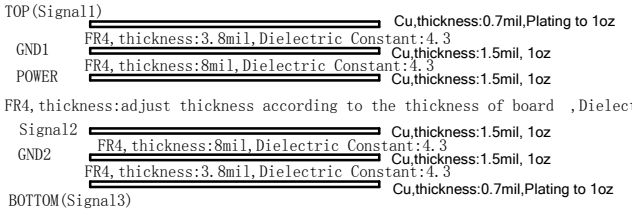
6 LAYERS PCB STACK



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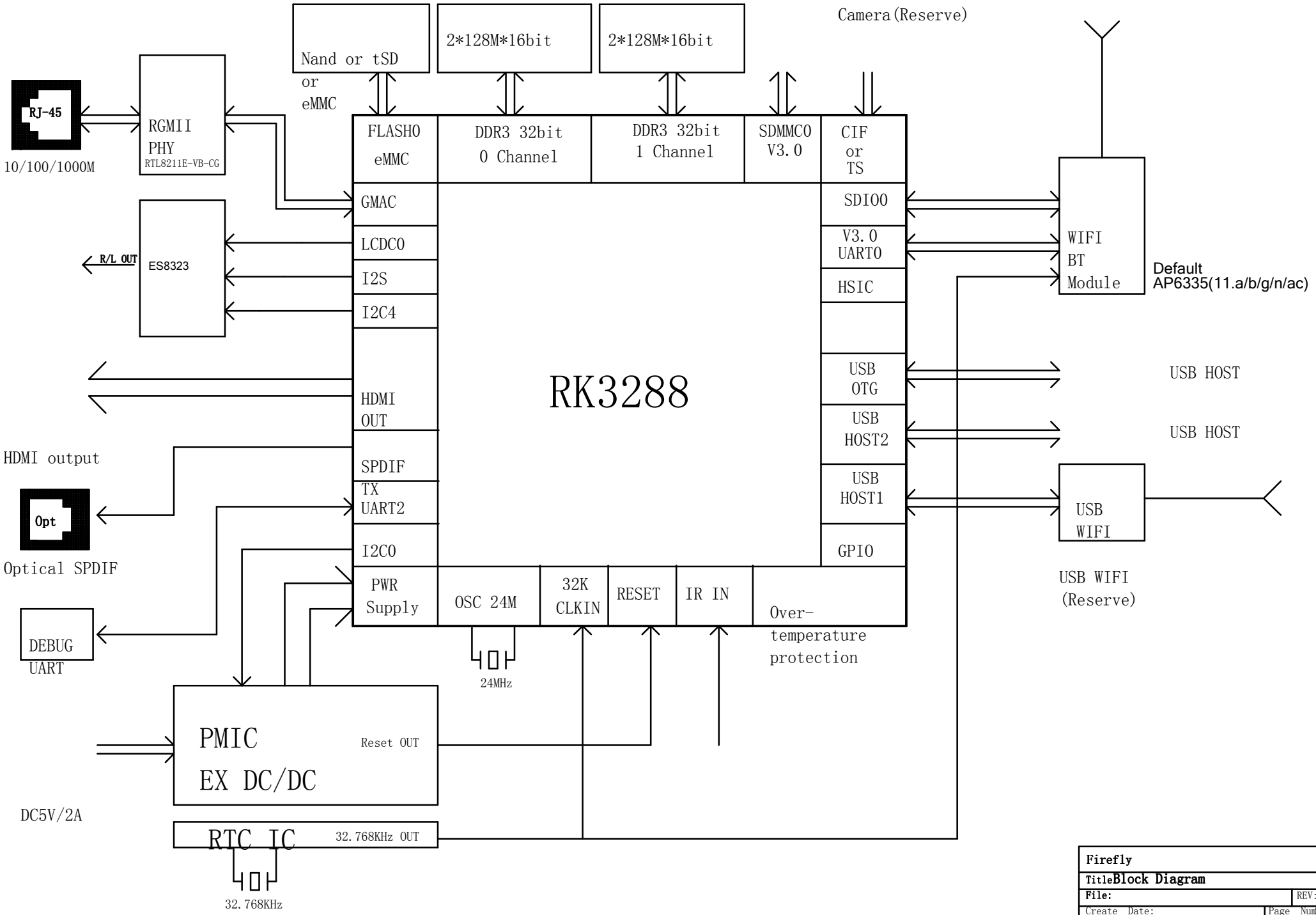
Create Date:	Page Num: 1
Modify Date: Wednesday, June 18, 2014	Page Total: 21



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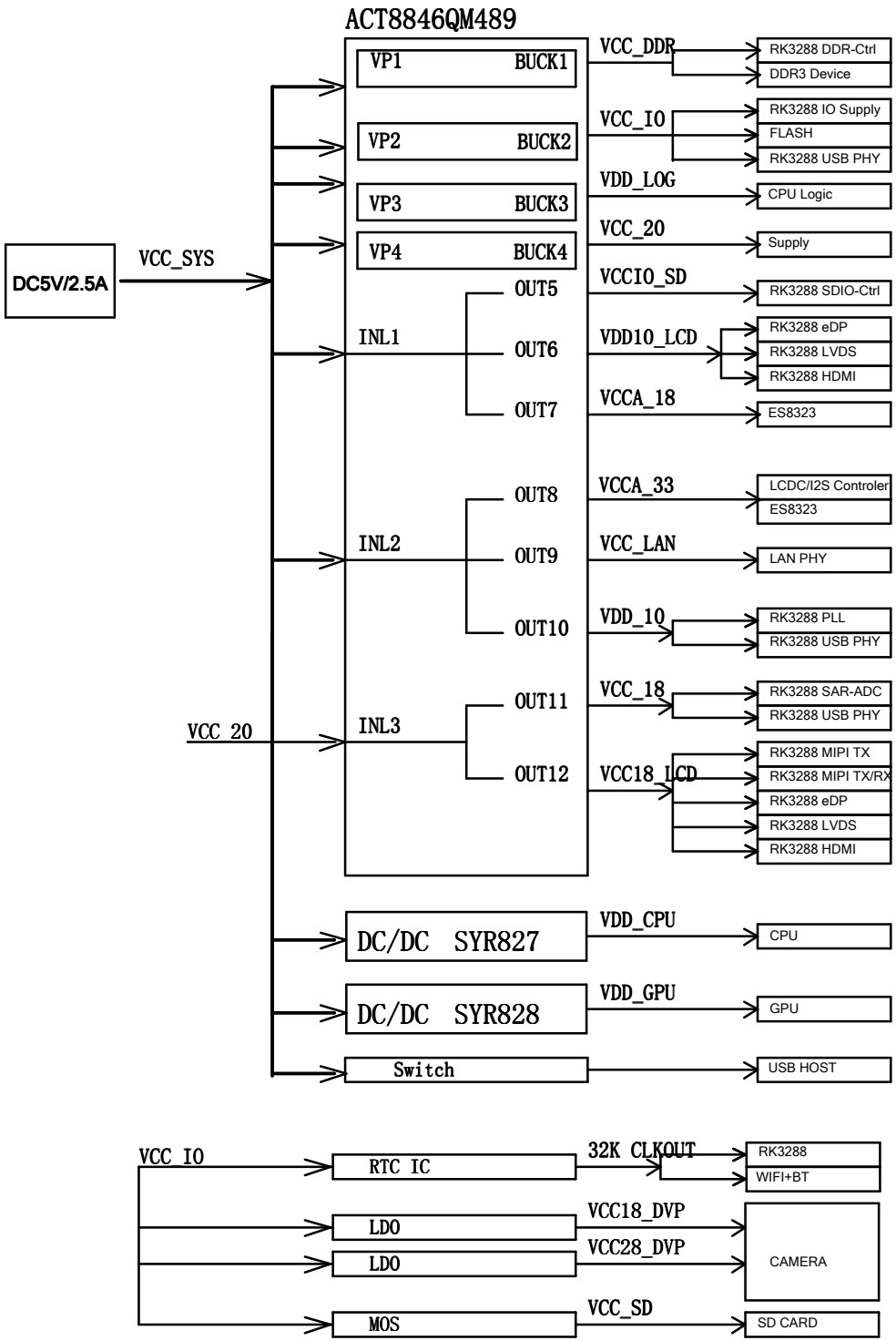
Modify Date: Wednesday, June 18, 2014	Page Total 21



PowerName	PMIC Channel	timer(2mS)	Default	Working
VCC_20	DCDC4	Solt:0	voltage 2.0V	voltage 2.0V
VDD_10	OUT10	Solt:1	1.0V	1.0V
VCC_DDR	DCDC1	Solt:2	1.5V	1.5V(DDR3)
VDD_CPU	EX DCDC	Solt:2A	(FB=1.2V) 1.0V	DVFS
VDD_GPU	EX DCDC	Solt:2B	1.0V	DVFS
VDD_LOG	DCDC3	Solt:3	1.1V	DVFS
VCC_18	OUT11	Solt:4	1.8V	1.8V
VCC_LAN	OUT9	Solt:5	3.3V	3.3V
VCC_IO	DCDC2	Solt:6	3.3V	3.3V
VCCIO_SD	OUT5	Solt:6	3.3V	SD2.0:3.3V
VCCA_33	OUT8	OFF	OFF	SD3.0:1.8V 3.3V
VCCA_18	OUT7	OFF	OFF	1.8V
VDD10_LCD	OUT6	OFF	OFF	1.0V
VCC18_LCD	OUT12	OFF	OFF	1.8V

Firefly	
Title: Power Tree	
File:	REV: 1.1
Create Date:	Page Num: 3
Modify Date: Wednesday, June 18, 2014	Page Total: 21

5V/2A

Working LED

IR RECEIVE

SYSTEM POWER

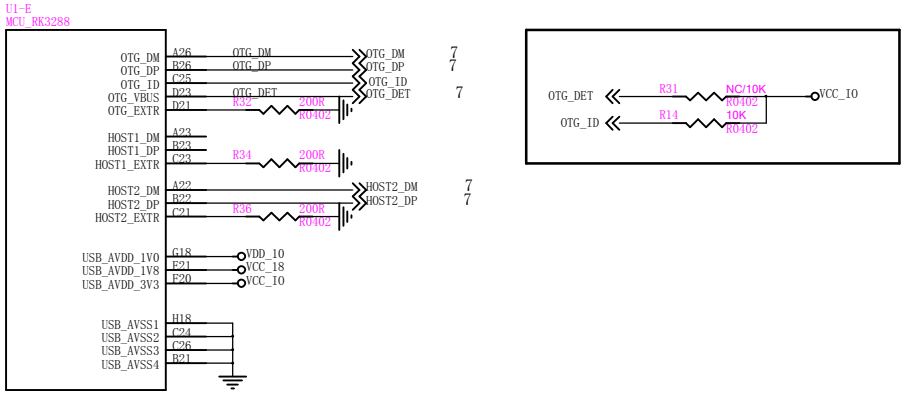
SYR827	I2C Address: 0x40h
SYR828	I2C Address: 0x41h

If you use MCU_JL8506 - double code - V6.04
Need to use external reset IC.
R203 don't stick.

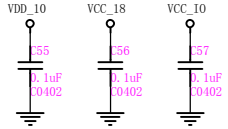
POWER ON

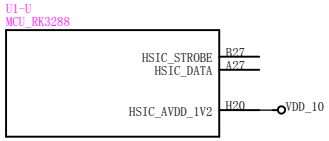
RTC IC

Firefly	
Title: System Power	
File:	REV: 1.1
Create Date:	Page Num: 4
Modify Date: Wednesday, June 18, 2014	Page Total: 21



RK3288_E





RK3288_U

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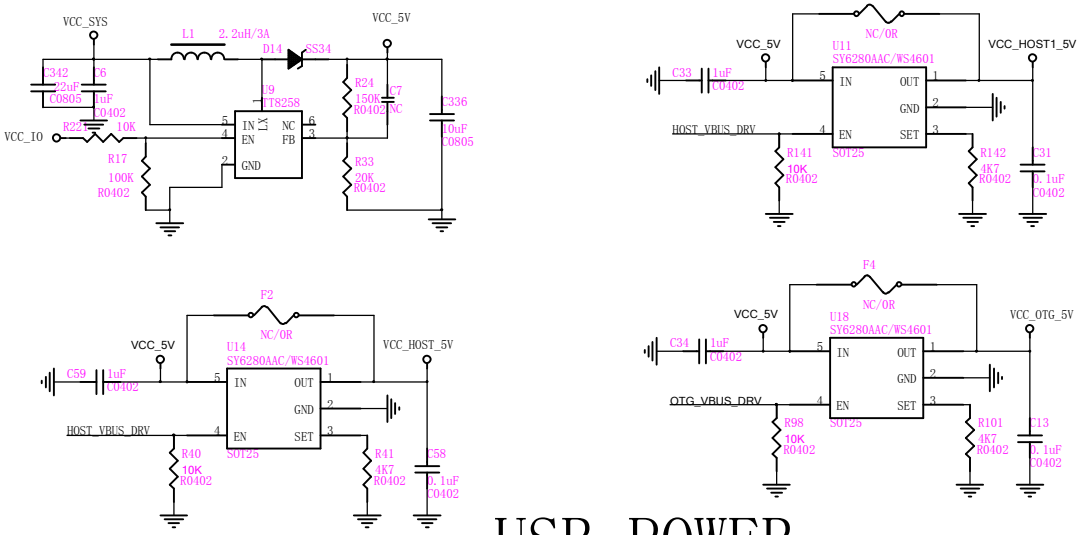
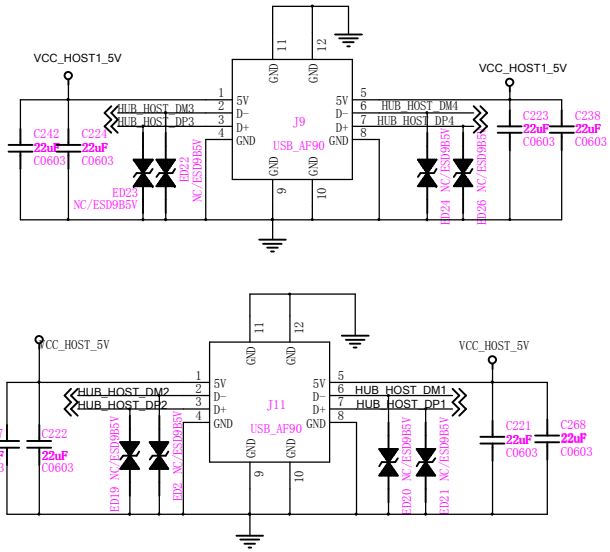
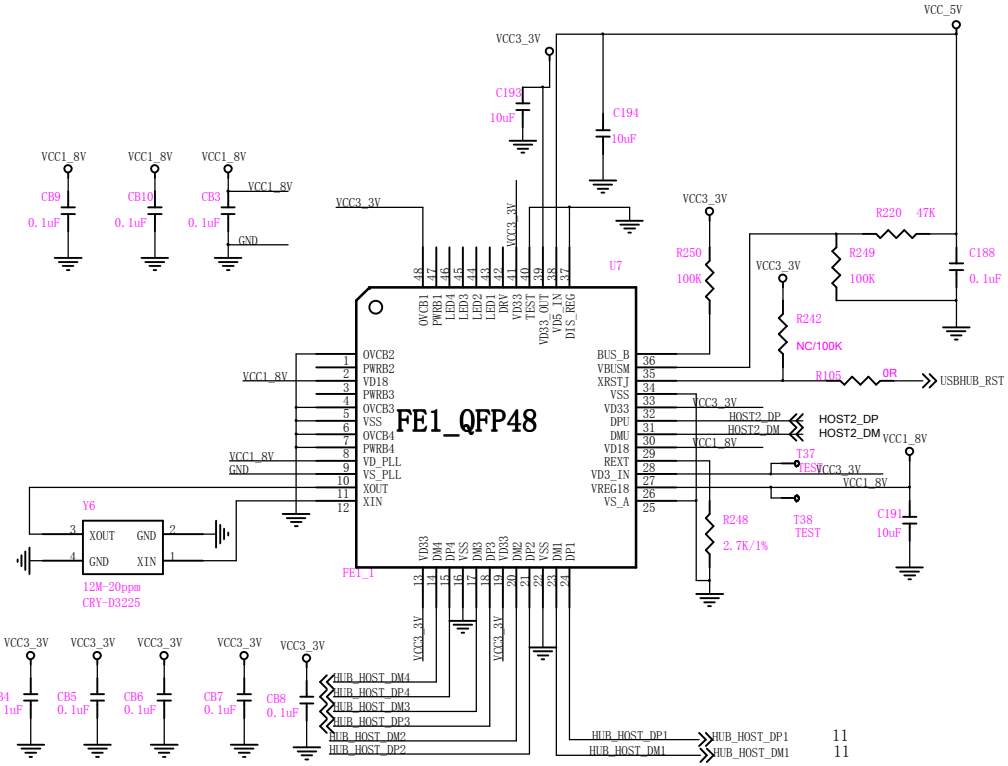
Create Date:	Page Num: 5
Modify Date: Wednesday, June 18, 2014	Page Total: 21



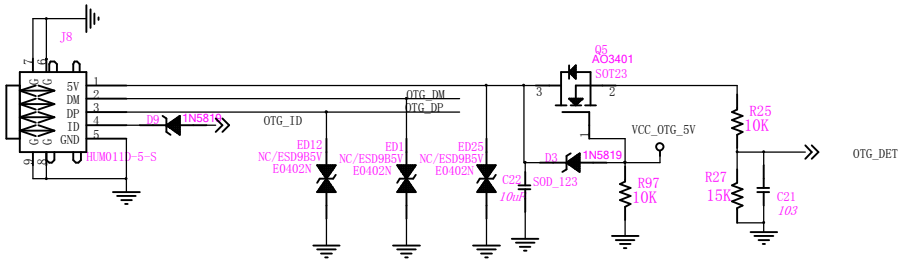
USB_POWER



HOST



HUB CHIP



OTG

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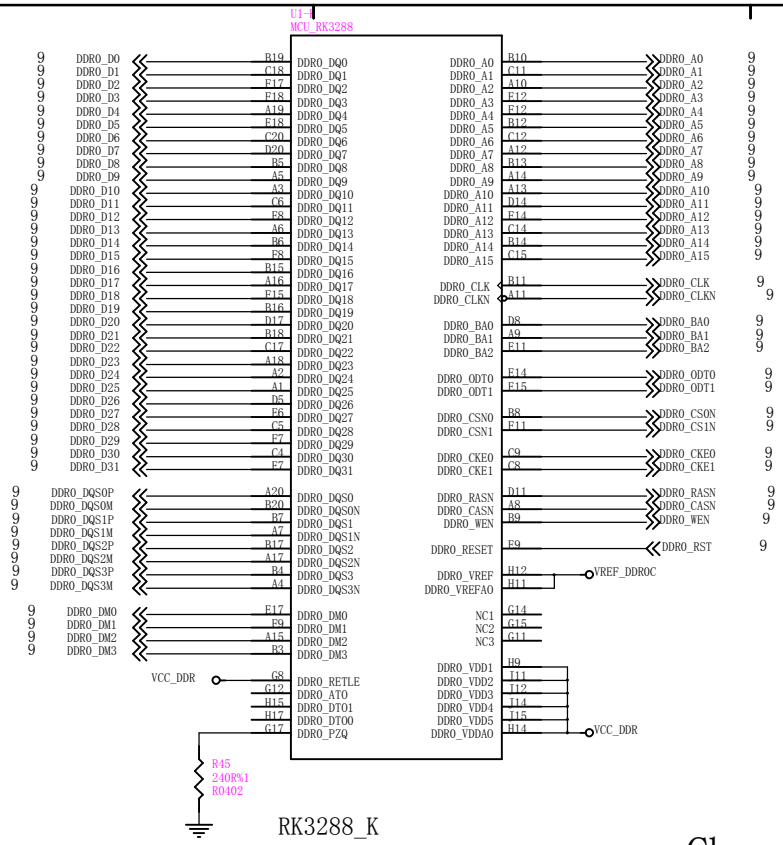
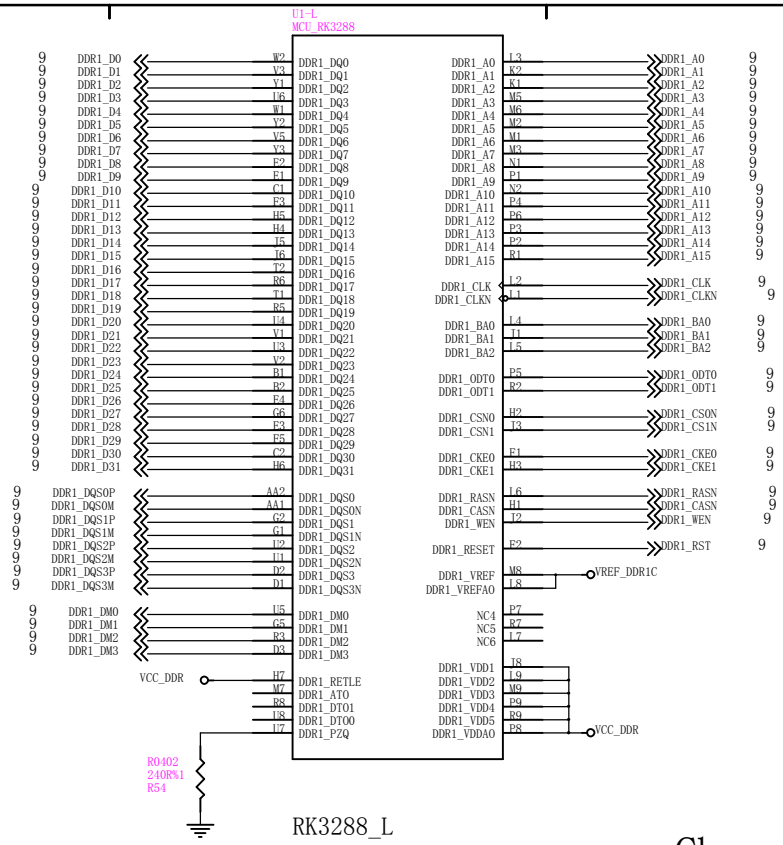
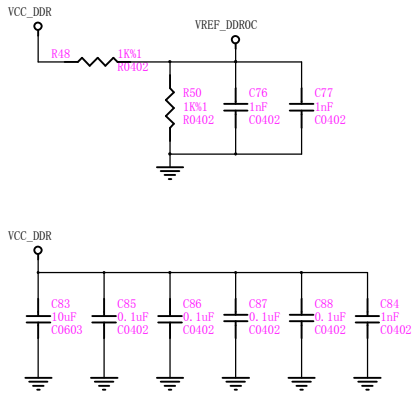


Channel 0

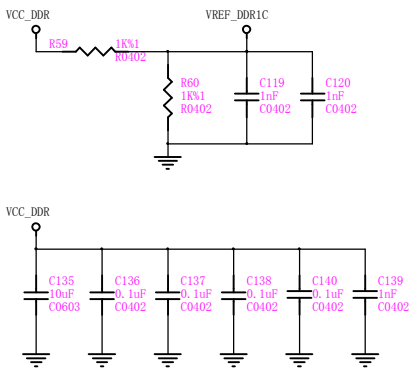


Channel 1

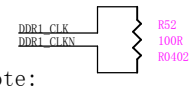


DDR0 FILTER

Note:
These termination resistors must be placed
in the middle of trace, and the termination resistor of CLK must be placed in thebifurcation point.



DDR1 FILTER



Note:
These termination resistors must be placed
in the middle of trace, and the termination resistor of CLK must be placed in thebifurcation point.

Firefly	
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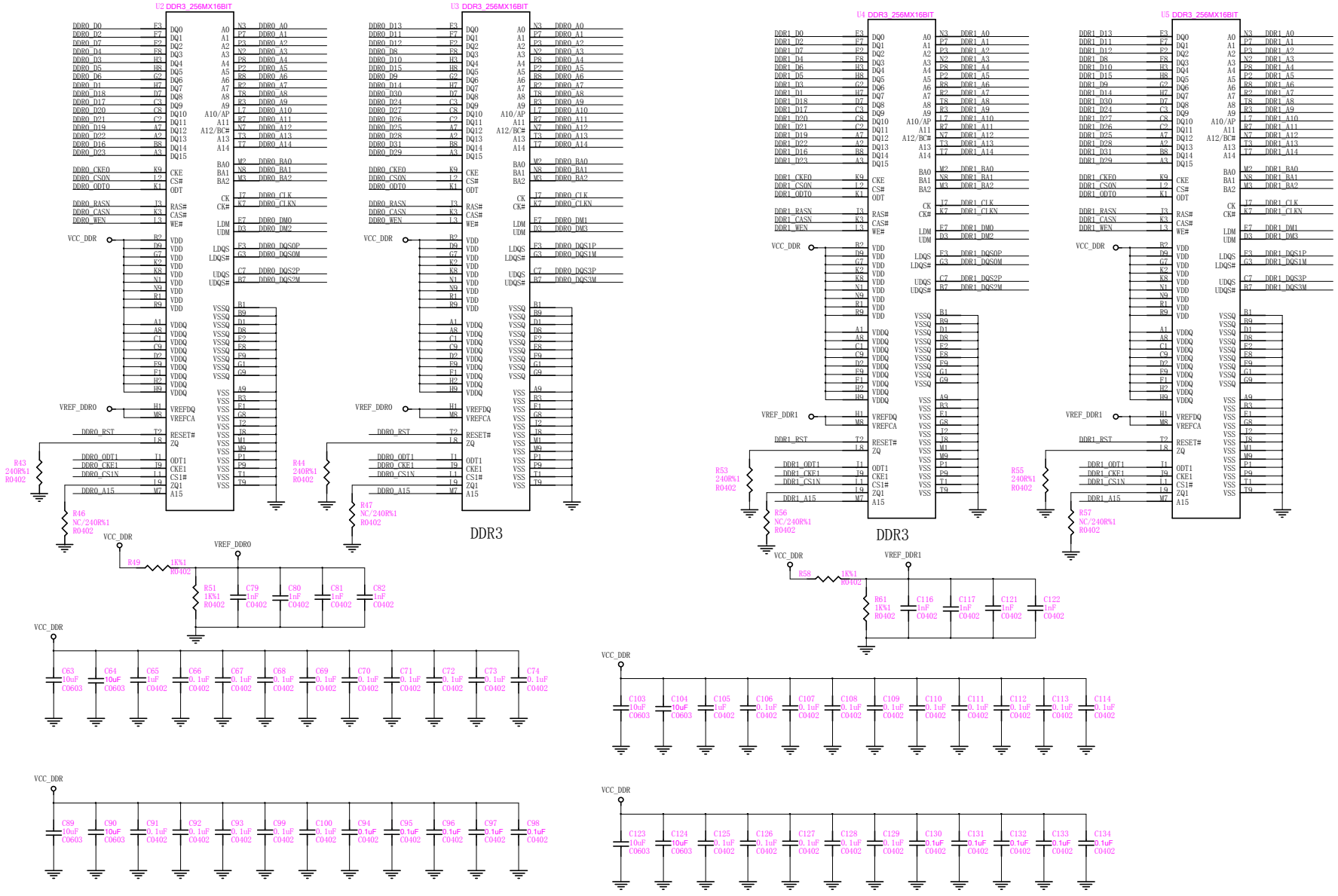
File:	REV: 1.1
Create Date:	Page Num: 7
Modify Date: Wednesday, June 18, 2014	Page Total: 21



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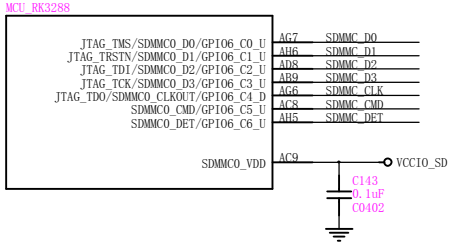
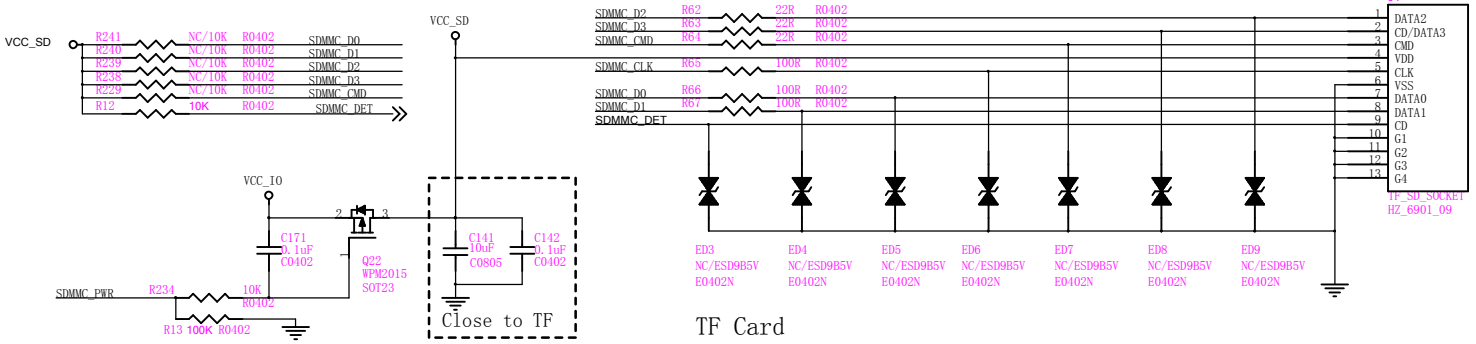
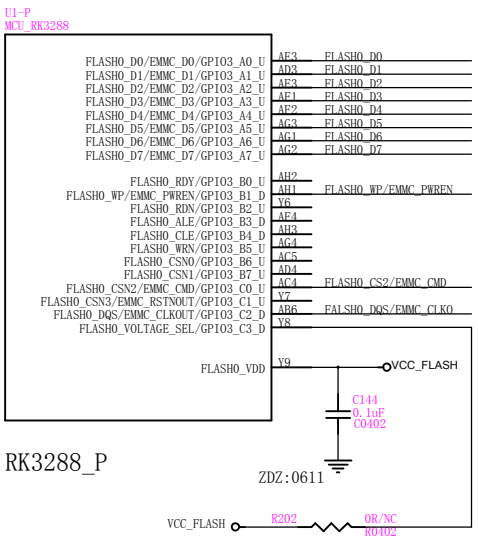
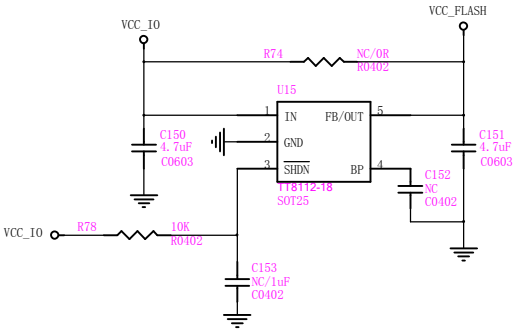
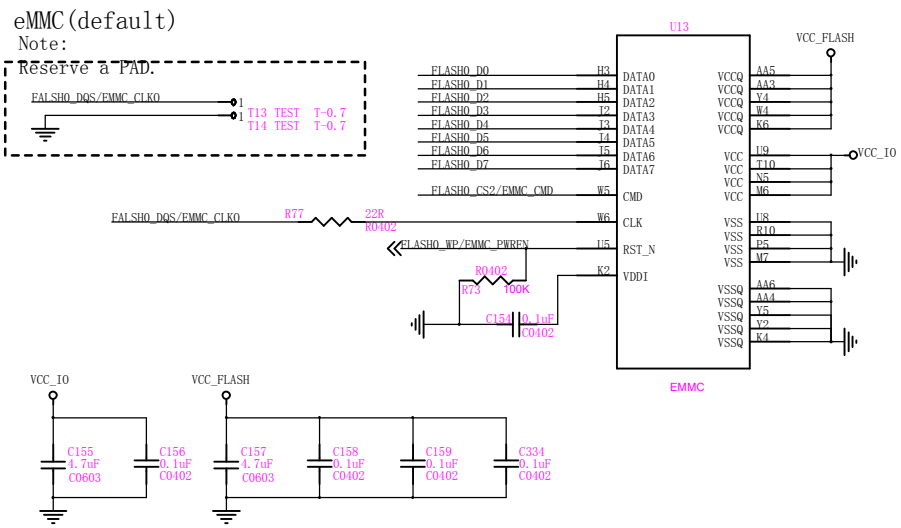
File:	REV: 1.1
Create Date:	Page Num: 8
Modify Date: Wednesday, June 18, 2014	Page Total: 21

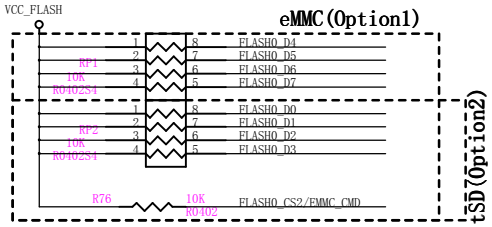












Pull-up select

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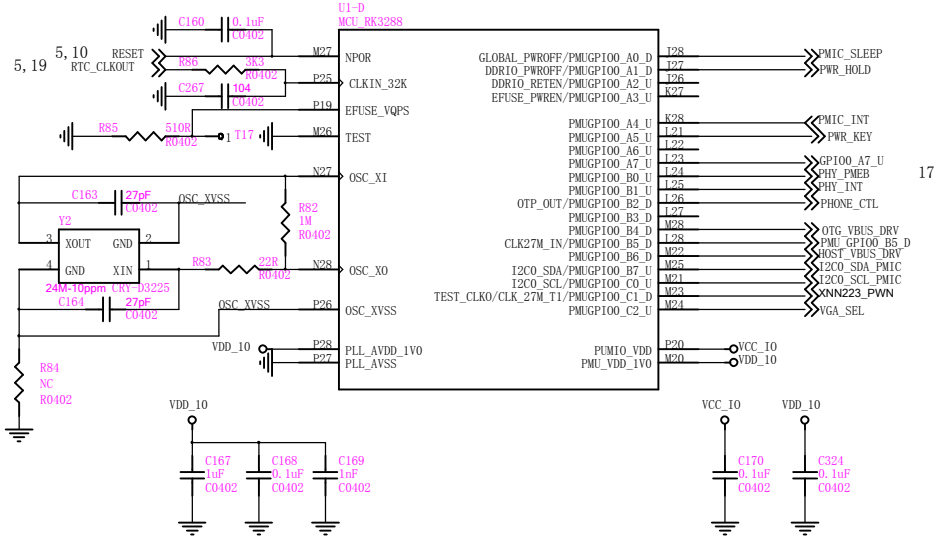
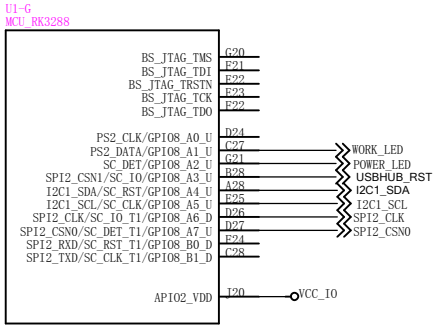
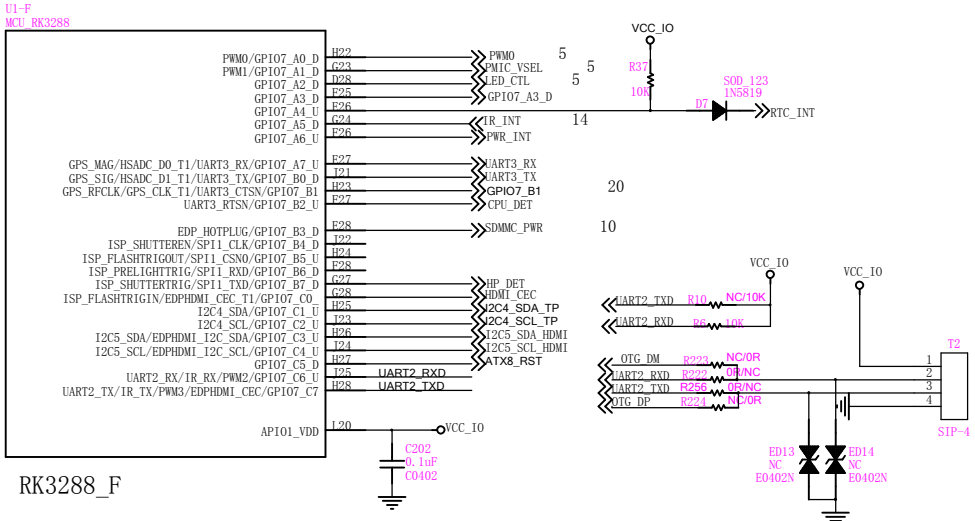
File:	REV: 1.1
Create Date:	Page Num: 9
Modify Date: Wednesday, June 18, 2014	Page Total: 21



RK3288_D

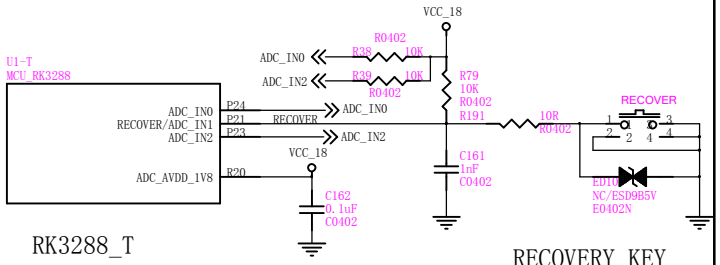


RK3288_G



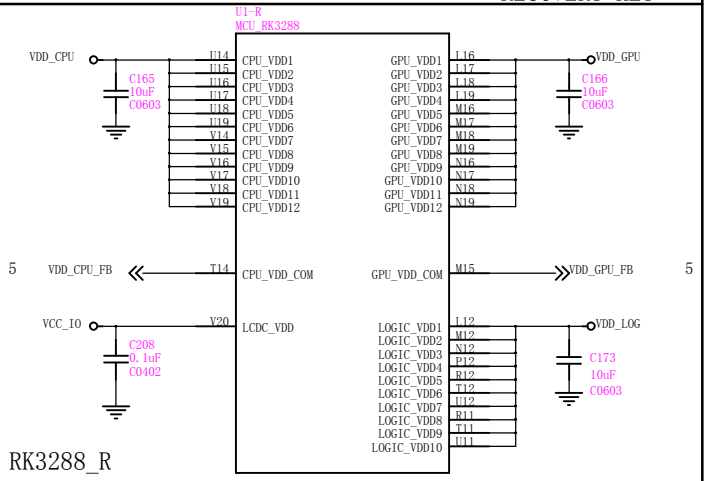
RK3288_F

For debug(Default)

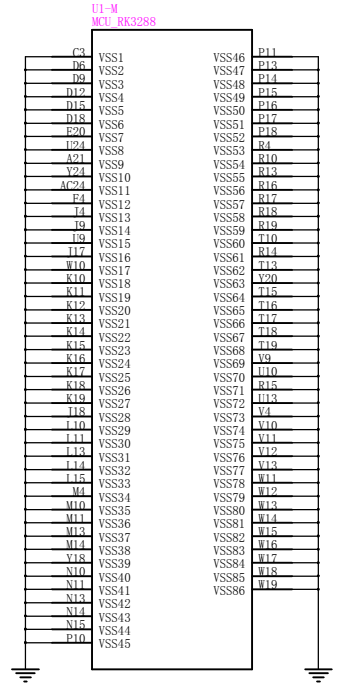


RK3288_T

RECOVERY KEY

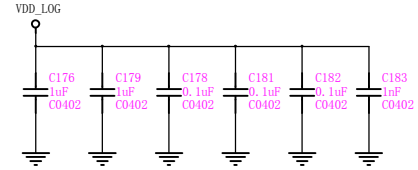


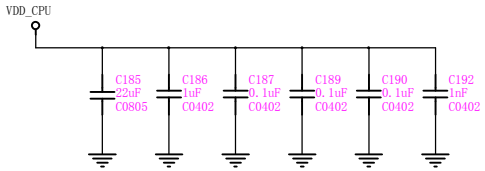
RK3288_R

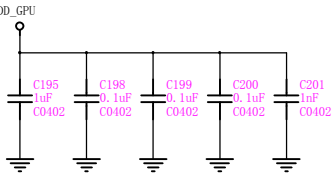


RK3288_M

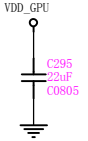
RK3288 FILTER







Place the Component
if need to write eFUSE



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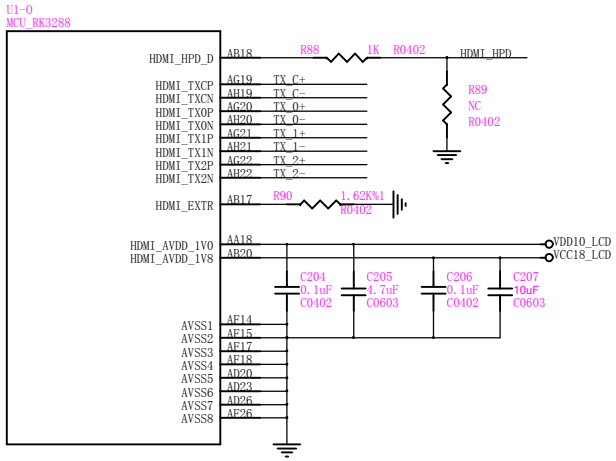
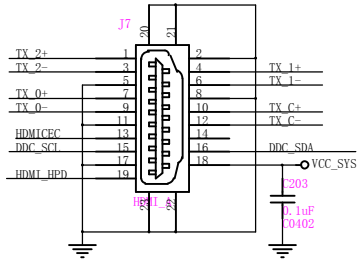
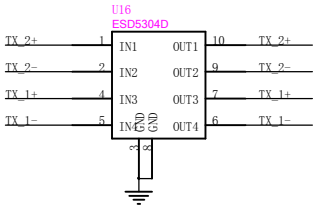
File:	REV: 1.1
Create Date:	Page Num: 10
Modify Date: Wednesday, June 18, 2014	Page Total: 21

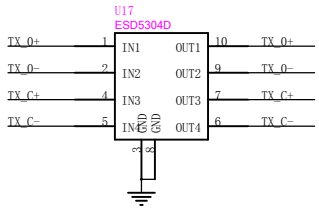


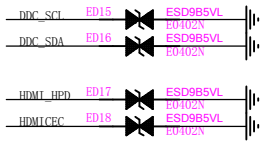
RK3288_0

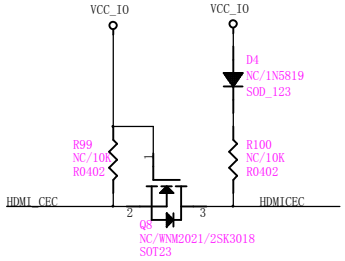


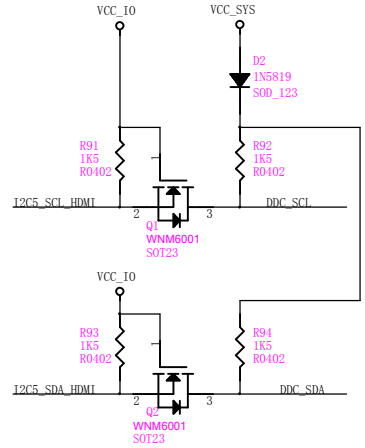
HDMI OUT











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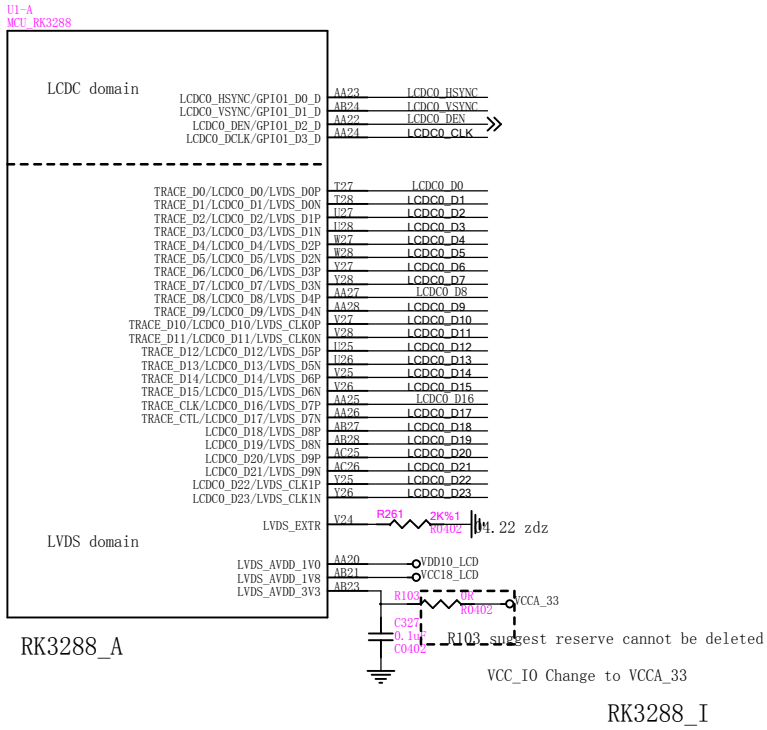
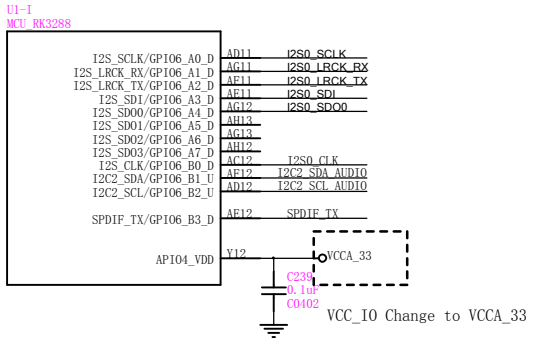
REV: 1.1	File:
Page Num:11	Create Date:
Page Total:21	Modify Date: Wednesday, June 18, 2014





RK3288_I

Firefly		
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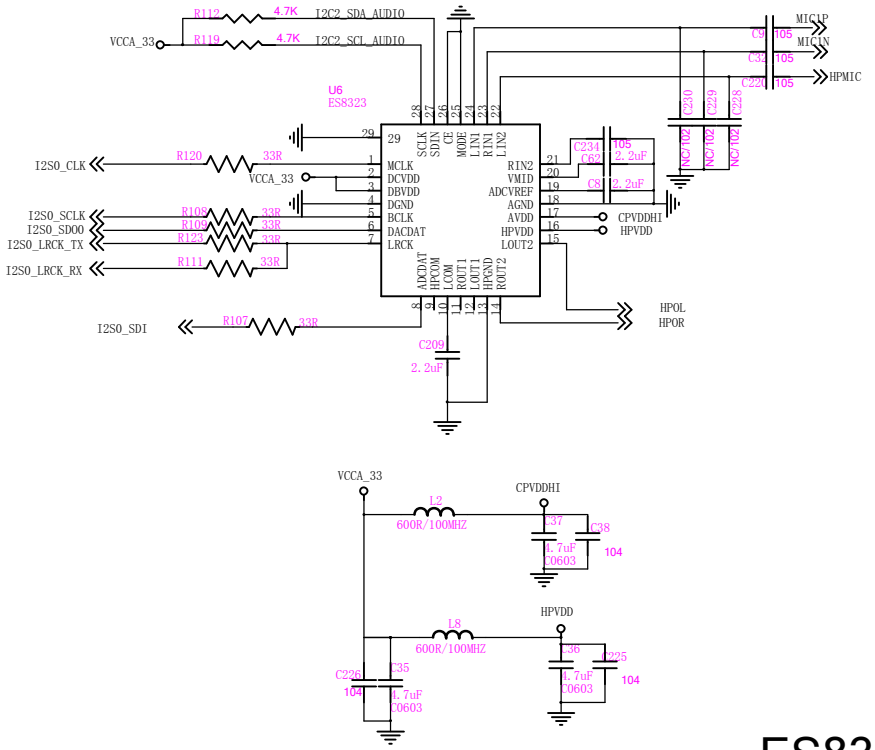
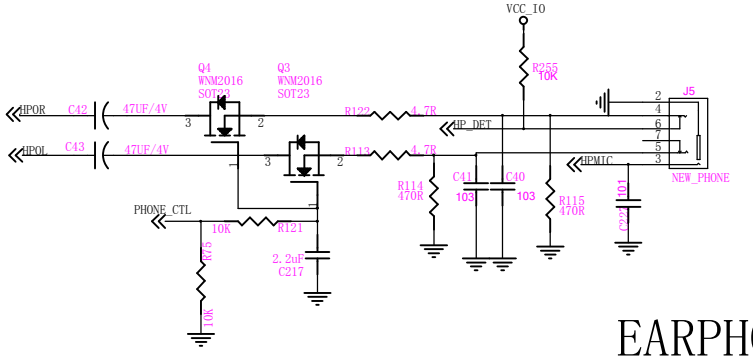
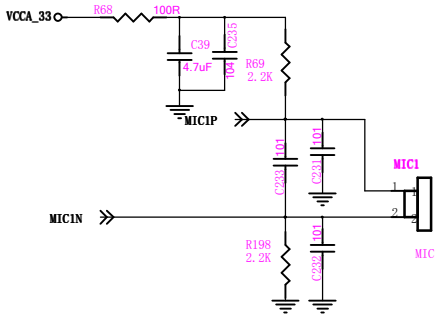
File:		REV: 1.1
Create Date:		Page Num: 12
Modify Date:	Wednesday, June 18, 2014	Page Total: 21

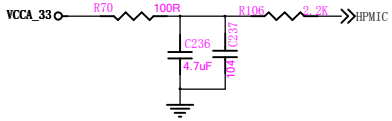


ES8323



EARPHONE





MIC

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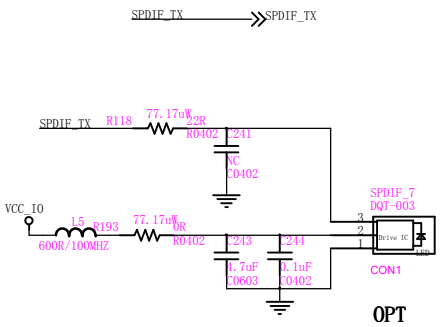
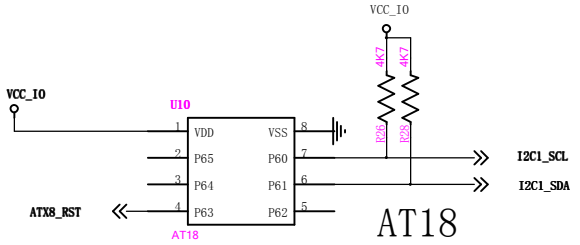
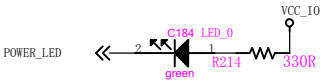
File:	REV:1.1
Create Date:	Page Num: 13
Modify Date: Wednesday, June 18, 2014	Page Total: 21



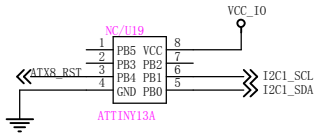
Optical S/PDIF OUT



AT18

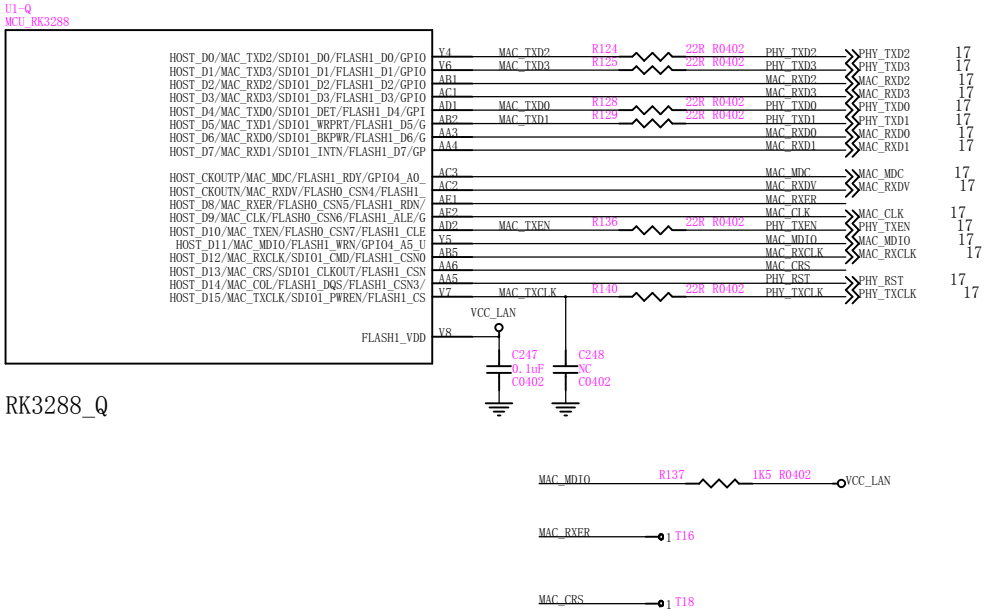


WORKING_LED

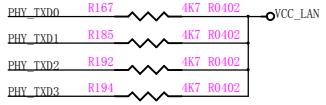


ATTINY13A

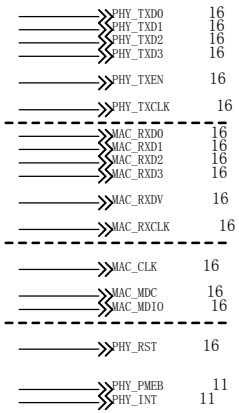
Firefly		A
Title: S/PDIF OUT		
File:	REV:1.1	
Create Date:	Page Num: 14	
Modify Date: Wednesday, June 18, 2014	Page Total: 21	

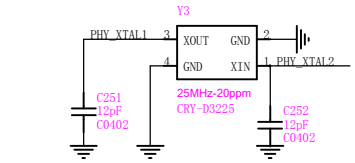


RK3288_Q

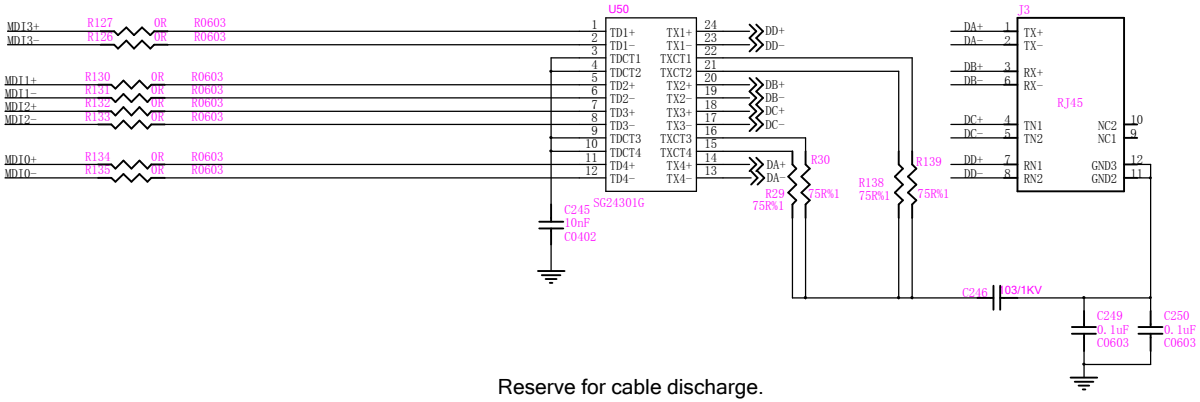


Firefly	
Title: RK3288 EthernetMAC Controler	
File:	REV:1.1
Create Date:	Page Num: 15
Modify Date: Wednesday, June 18, 2014	Page Total: 21

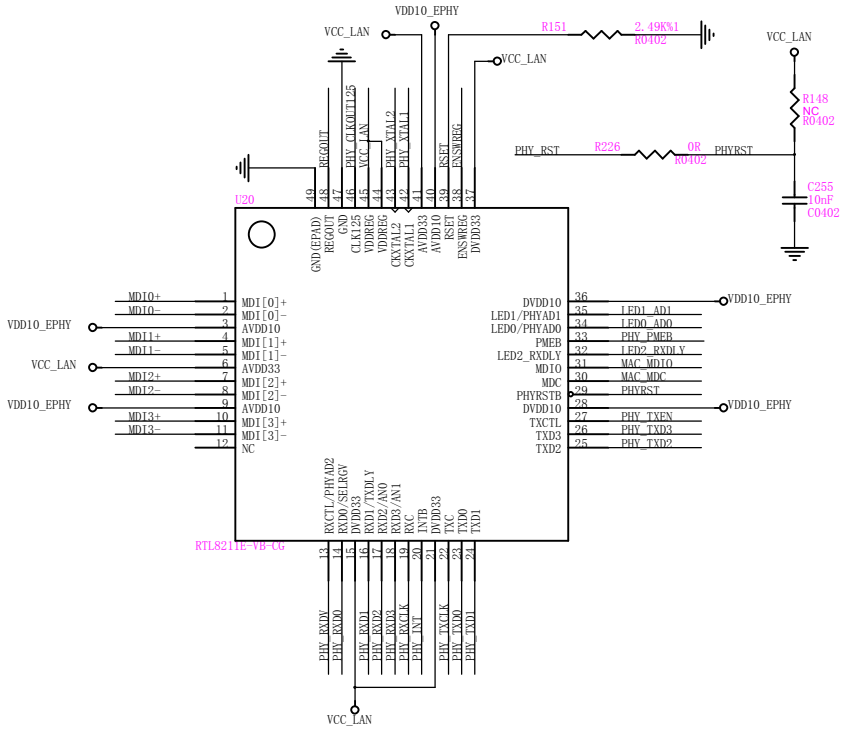


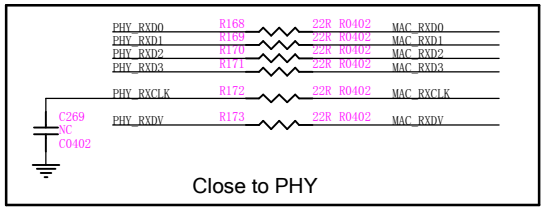


If use external clock
then the XTAL2 need
connect to GND for RTL8211E.

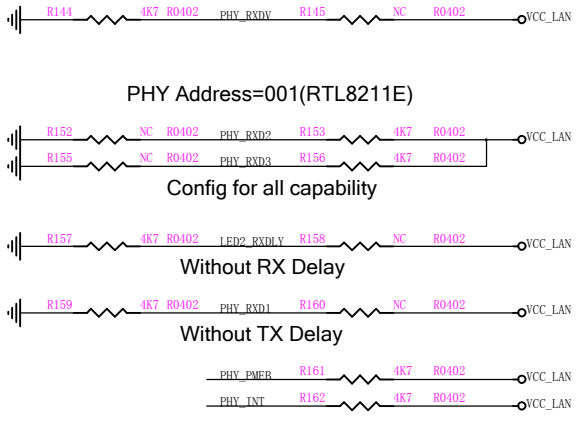


Reserve for cable discharge.





Close to PHY

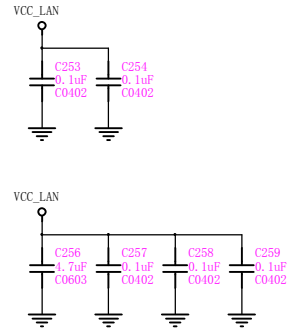


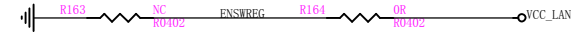
PHY Address=001(RTL8211E)

Config for all capability

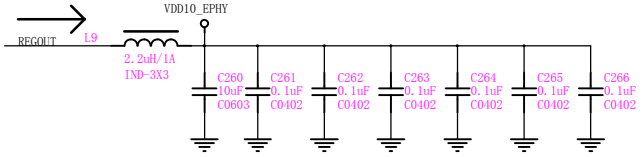
Without RX Delay

Without TX Delay

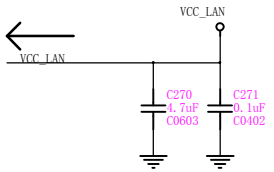




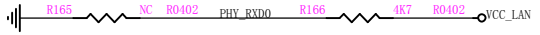
Connect ENSWREG to AVDD33 to enable
Switching regulator or connect ENSWREG
to GND to disable Switching regulator.



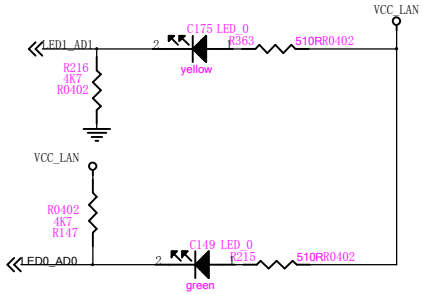
Inductance close to PIN48

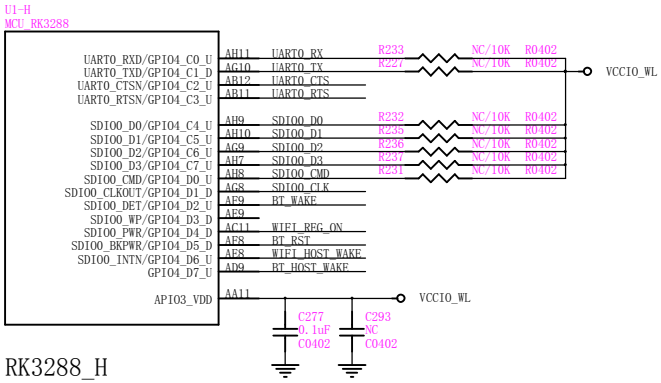


Close to PIN44.45



Pull down for 2.5V RGMII(RTL8211D/8211E)
Pull up for 3.3V RGMII (RTL8211D/8211E)
Pull up1.5 /1.8V RGMII (RTL8211E-VL only)





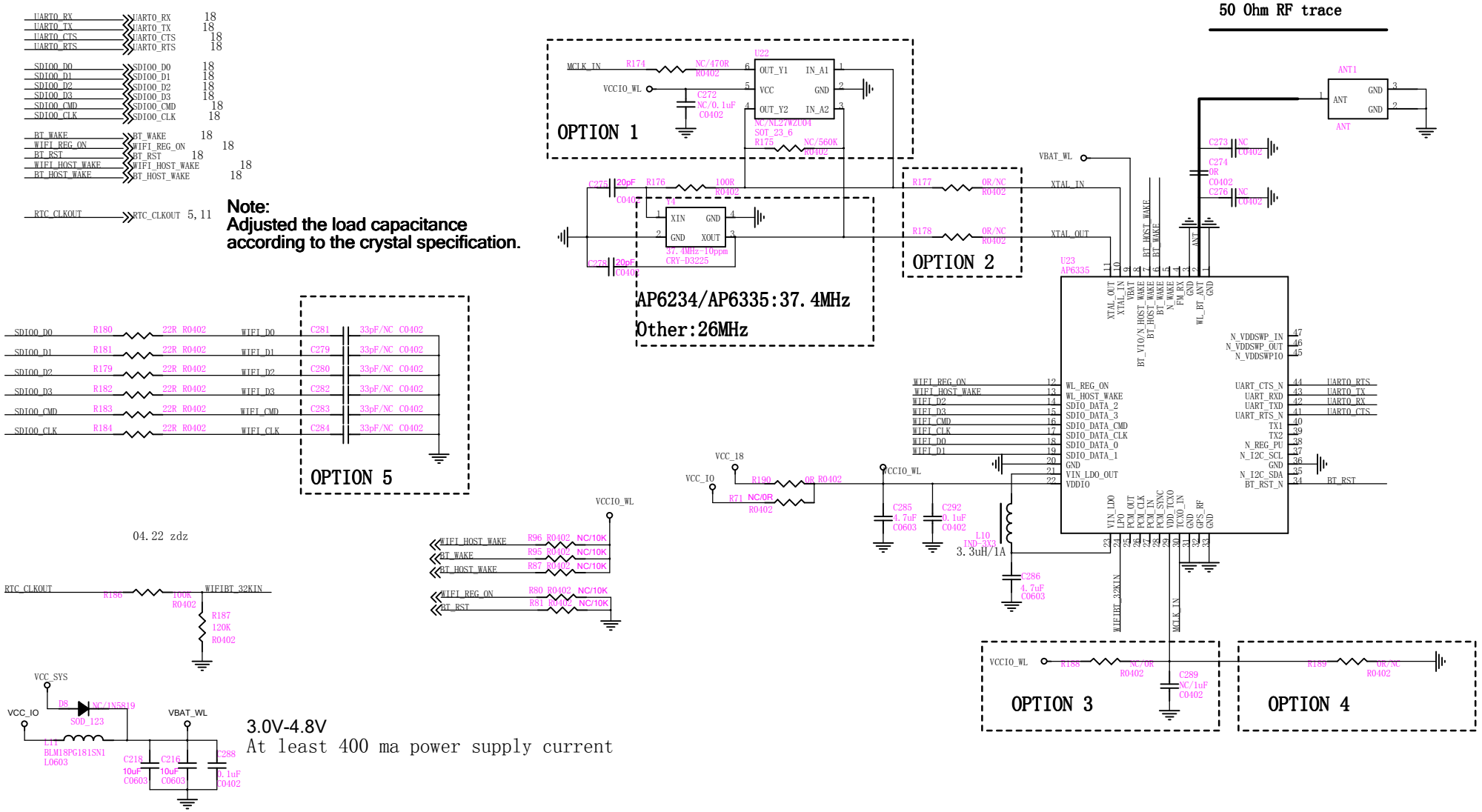
RK3288_H

UART0_RX — UART0_RX 19
UART0_TX — UART0_TX 19
UART0_CTS — UART0_CTS 19
UART0_RTS — UART0_RTS 19

SDIO0_D0 — SDIO0_D0 19
SDIO0_D1 — SDIO0_D1 19
SDIO0_D2 — SDIO0_D2 19
SDIO0_D3 — SDIO0_D3 19
SDIO0_CMD — SDIO0_CMD 19
SDIO0_CLK — SDIO0_CLK 19

BT_WAKE — BT_WAKE 19
WIFI_REG_ON — WIFI_REG_ON 19
BT_RST — BT_RST 19
WIFI_HOST_WAKE — WIFI_HOST_WAKE 19
BT_HOST_WAKE — BT_HOST_WAKE 19

Firefly	
Title: RK3288 SDIO0 Controler	
File:	REV:1.1
Create Date:	Page Num: 17
Modify Date: Wednesday, June 18, 2014	Page Total: 21

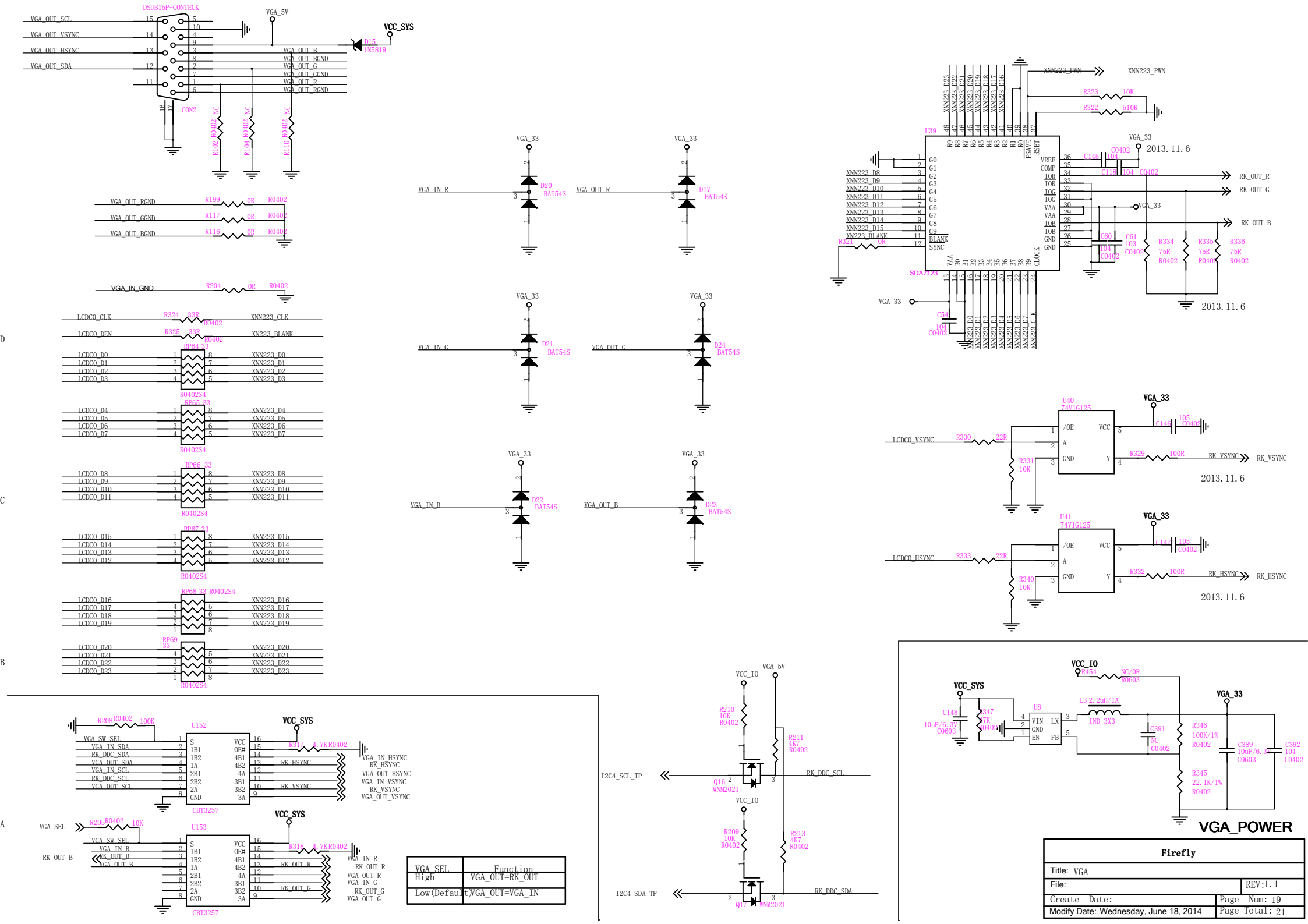


OPTION	WIFI				BT4.0	Crystals	VDDIO
	a	b/g/n	ac	5GHz			
AP6181		Yes				26MHz	1.71-3.6V
AP6210		Yes			Yes	26MHz	1.71-3.6V
AP6234	Yes	Yes		Yes	Yes	37.4MHz	1.6-3.4V
AP6330	Yes	Yes		Yes	Yes	26MHz	1.2-2.9V
AP6335 (Default)	Yes	Yes	Yes	Yes	Yes	37.4MHz	1.71-3.63V

OPTION	1	2	3	4	5
AP6181	No	Yes	No	No	No
AP6210	Yes	No	Yes	No	No
AP6234	No	Yes	No	No	No
AP6330	No	Yes	No	No	No
AP6335 (Default)	No	Yes	No	Yes	Yes

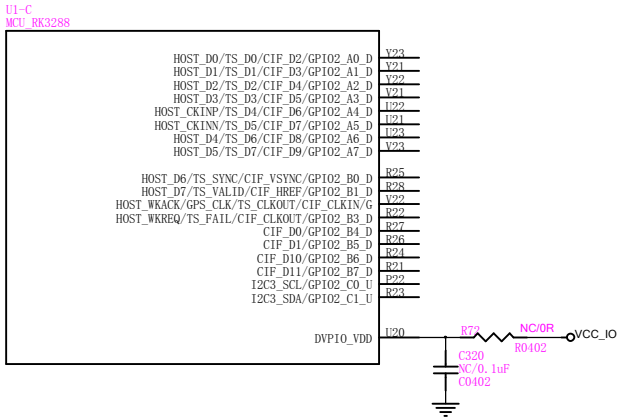
Note:
Yes:Inside the box to
No:The box is not posted

Firefly	
Title: AP6XXX-WIFI/BT	
File:	REV:1.1
Create Date:	Page Num: 18
Modify Date: Wednesday, June 18, 2014	Page Total: 21

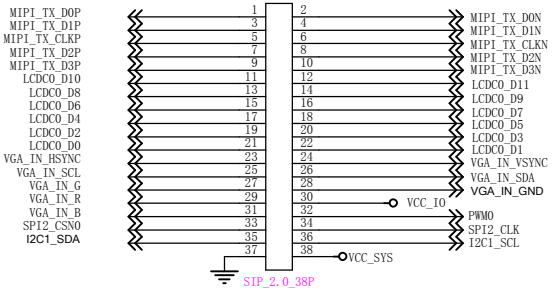


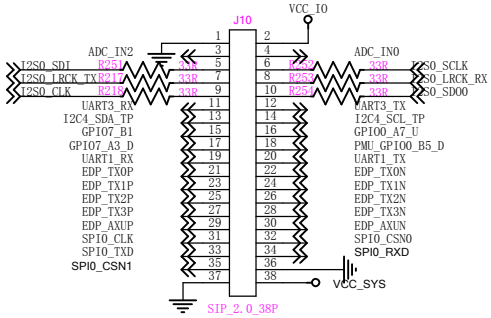
VGA_SEL	Function
High	VGA_OUT=RK_OUT
Low(Default)	VGA_OUT=VGA_IN

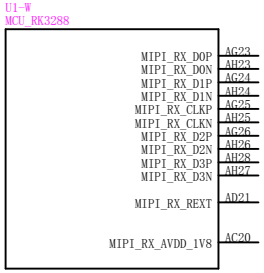
Firefly	
Title: VGA	
File:	REV:1.1
Create Date:	Page Num: 19
Modify Date: Wednesday, June 18, 2014	Page Total: 21



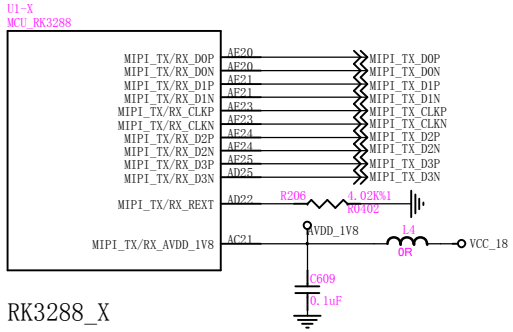
RK3288_C



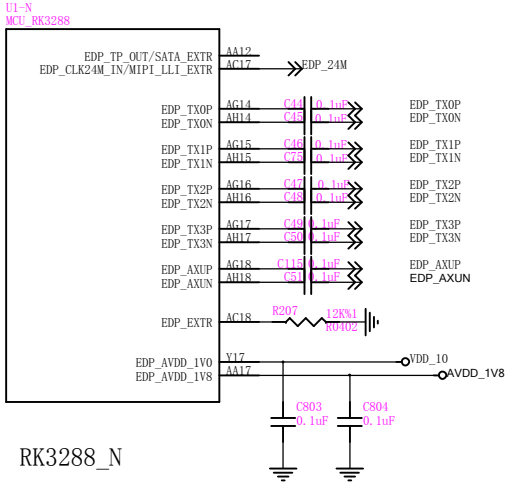




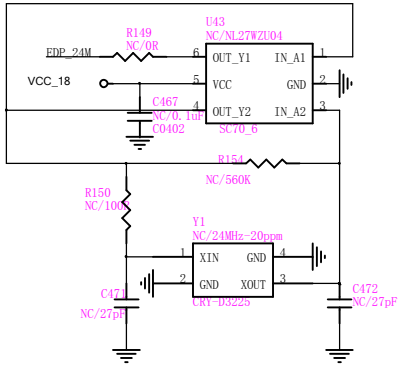
RK3288_W

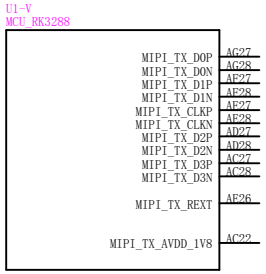


RK3288_X



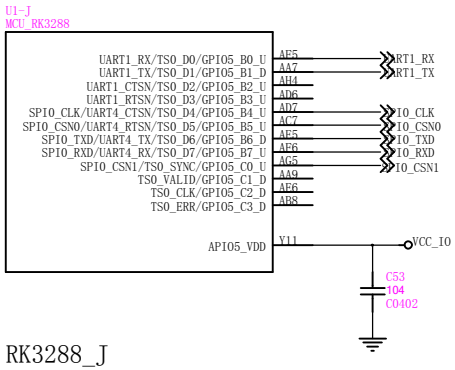
RK3288_N





RK3288_V

Firefly	
Title: Camera Interface	
File:	REV:1.1
Create Date:	Page Num: 20
Modify Date: Wednesday, June 18, 2014	Page Total: 21



RK3288_J

Firefly	
Title: DTV-(Reserve)	
File:	REV:1.1
Create Date:	Page Num:21
Modify Date: Wednesday, June 18, 2014	Page Total:21