

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Layer 1 - Top Layer	Copper	2.80mil		
	Dielectric 1	FR-4 High Tg	6.00mil	4.2	
2	Layer 2 - GND	Copper	1.40mil		
	Dielectric 2	FR-4 High Tg	41.00mil	4.2	
3	Layer 3 - Signal	Copper	1.40mil		
	Dielectric 3	FR-4 High Tg	6.00mil	4.2	
4	Layer 4 - Bottom Layer	Copper	2.80mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8_ML

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 20_ML

MINIMUM ANNULAR RING 0.05mm (2ML) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5_MIL, HOLES +/- 3_MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3_MIL

MATERIAL:

☐ FR-408

☒ FR-4 High Tg

☐ OTHER

THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER

TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2

☐ OTHER +/-

BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2

☐ OTHER +/-

DRILLING:

REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILESPTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER

BOARD FINISH:

SILKSCREEN: ☒ TOP ☒ BOTTOMSILKSCREEN COLOR: ☒ WHITE ☐ OTHERSOLDER RESIST COLOR: ☒ GREEN ☐ OTHER☒ MATTE ☐ SEMI-GLOSSSURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENIEPG☐ IMM. TIN/SILVER OR EQUIV ☐ OTHERARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: ☐ YESBARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

PROJECT TITLE:
BQ76952EVM

DESIGNED FOR:
Public Release

FILE NAME:
BMS029B.PcbDoc

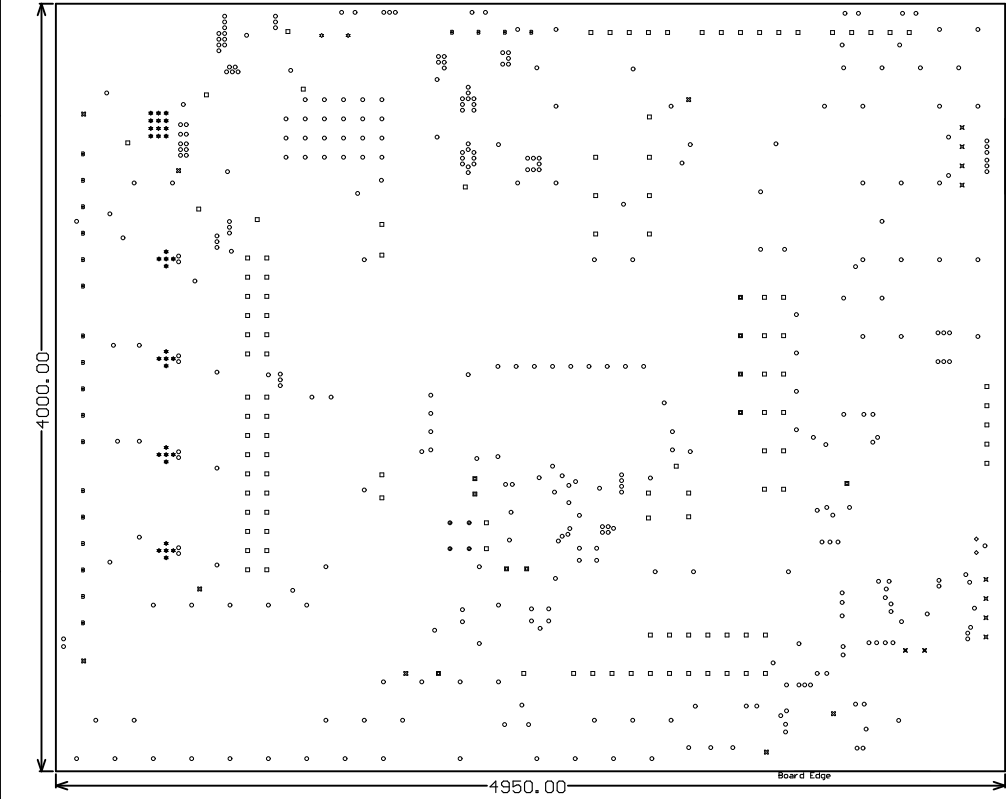
ENGINEER:
M. Sunna

LAYOUT BY:
JMM

SCALE: 1.00

ALTUM DESIGNER VERSION:
19.1.9.167

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape
◇	2	31.50mil (0.800mm)	NPTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	Pad	Rounded
✕	2	45.28mil (1.150mm)	PTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	Pad	(Mixed)
⊙	2	50.00mil (1.270mm)	PTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	Pad	(Mixed)
⊗	4	35.00mil (0.889mm)	PTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	Pad	(Mixed)
✕	8	40.16mil (1.020mm)	PTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	Pad	(Mixed)
⊗	8	63.00mil (1.600mm)	PTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	Pad	Rounded
■	10	25.00mil (0.635mm)	PTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	Pad	Rounded
B	21	43.31mil (1.100mm)	PTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	Pad	(Mixed)
✱	32	7.87mil (0.200mm)	PTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	Via	Rounded
□	109	40.00mil (1.016mm)	PTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	Pad	(Mixed)
○	376	10.00mil (0.254mm)	PTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	Via	Rounded
	574 Total						



ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = ~~BMS029B.PcbDoc~~

PLOT NAME = Fabrication Drawing

BOARD #: BMS029

TID #: N/A

GENERATED : 6/30/2020 3:04:14 PM

REV: B

SUN REV: Not In VersionControl

TEXAS INSTRUMENTS

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.