BL602/604

Datasheet

Version：1.6

www.bouffalolab.com

Contents

List of Figures

List of Tables

1 Overview

BL602/BL604 is Wi-Fi + BLE combo chipset for ultra-low-cost and low-power application. Wireless subsystem contains 2.4G radio, Wi-Fi 802.11b/g/n and BLE 5.0 baseband/MAC designs. Microcontroller subsystem contains a low-power 32-bit RISC CPU, high-speed cache and memories. Power Management Unit controls low-power modes. Moreover, variety of security features are supported.

Peripheral interfaces include SDIO, SPI, UART, I2C, IR remote, PWM, ADC, DAC, PIR, and GPIOs.

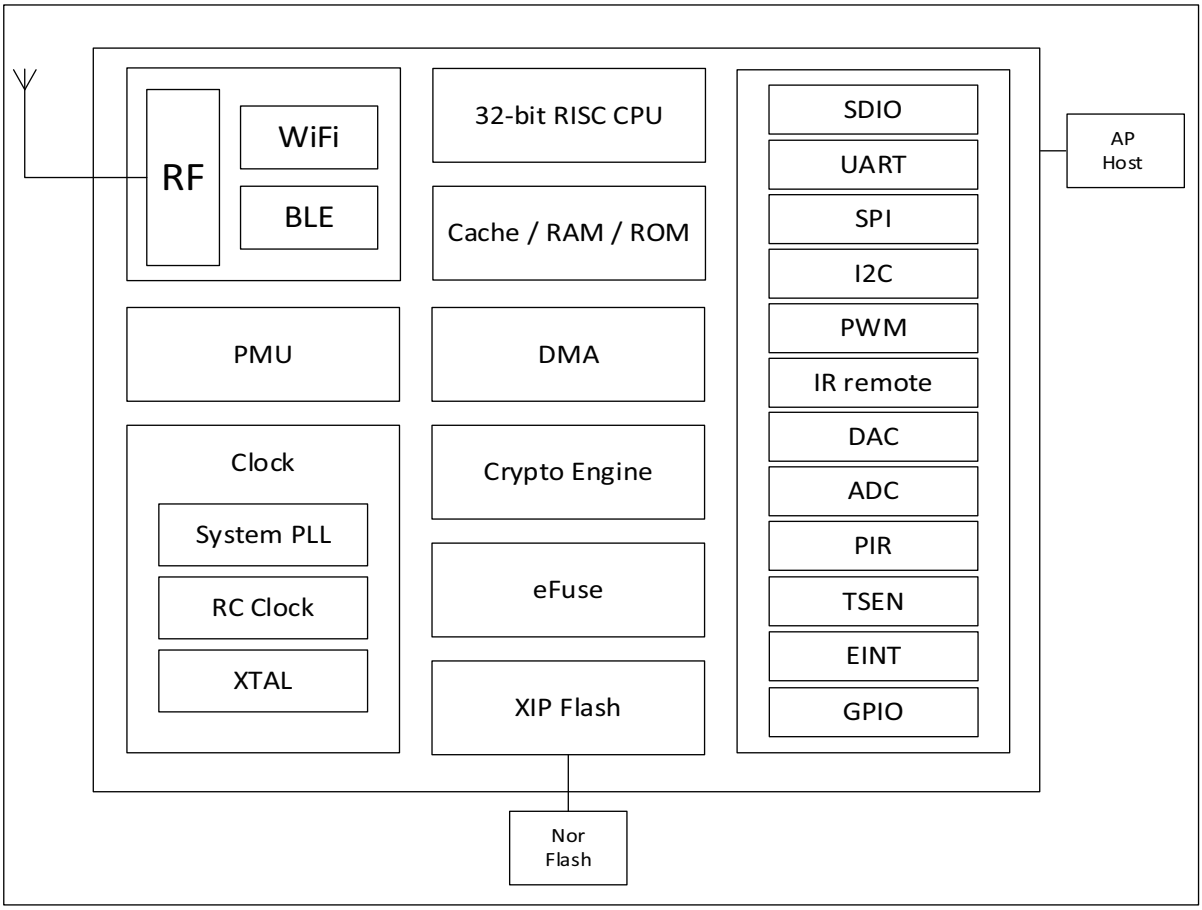

Figure 1.1: Functional Block Diagram

1.1 Wireless

- Support IEEE 802.11 b/g/n protocol
- 2.4 GHz band 1T1R mode, support 20 MHz, data rate up to 72.2 Mbps
- Wi-Fi security WPS/WEP/WPA/WPA2 Personal/WPA2 Enterprise/WPA3
- Wireless Multimedia (WMM)
- Frame aggregation (AMPDU, AMSDU)
- Immediate Block ACK
- Fragmentation and defragmentation
- Beacon automatic reception (hardware TSF)
- Hardware support 6 × virtual Wi-Fi interface
- Support Station mode, SoftAP mode, Station + SoftAP mode, Sniffer mode
- Support multiple cloud access at the same time
- Integrated balun, PA/LNA
- Bluetooth® Low Energy 5.0, Bluetooth Mesh
- BLE assists in achieving fast Wi-Fi connection
- Wi-Fi and BLE coexist
- Support BLE 5.0 channel selection #2
- 2M PHY / Coded PHY / ADV extension is not supported

1.2 MCU Subsystem

- 32-bit RISC CPU with FPU (floating point unit)
- Level-1 cache
- One RTC timer update to one year
- Two 32-bit general purpose timers
- Four DMA channels
- DFS (Dynamic Frequency Scaling) from 1MHz to 192MHz
- JTAG development support
- XIP QSPI/SPI Flash with hardware decryption support

1.3 Memory

- 276KB RAM
- 128KB ROM
- 1Kb eFuse
- Embedded Flash (Optional)

1.4 Security

- Secure boot,support ECC-256 signed image
- Secure debug ports
- QSPI/SPI Flash On-The-Fly AES Decryption (OTFAD),support AES-128 CTR mode
- AES 128/192/256 bits
- SHA-1/224/256
- TRNG (True Random Number Generator)
- PKA (Public Key Accelerator),support big number operation,software support sign/verify API

1.5 Peripheral

- One SDIO 2.0 slave
- One SPI master/slave with max clock 40Mbps
- Two UART with max baudrate 10Mbps,support RTS/CTS flow control
- One I2C master with max clock 3Mbps
- Five PWM channels with max output frequency 40MHz
- Two 10-bit general DAC channels with max conversion rate 512Ksps
- Twelve 12-bit general ADC channels with max conversion rate 2Msps
- Two general analog comparators (ACOMP),can be CPU wake up source
- One PIR (Passive Infra-Red) detection,can be CPU wake up source
- One infrared remote controller(IR),support NEC RC5 protocol
- 16 or 23 GPIOs

1.6 Power Management

- Off
- Hibernate (flexible modes)
- Power Down Sleep (flexible modes)
- Active

1.7 Clock

- Support XTAL 24/32/38.4/40MHz
- Internal RC 32kHz oscillator
- Internal RC 32MHz oscillator
- Internal System PLL
- XTAL 32kHz

2 Functional Description

BL602/BL604 main functions described as follows：

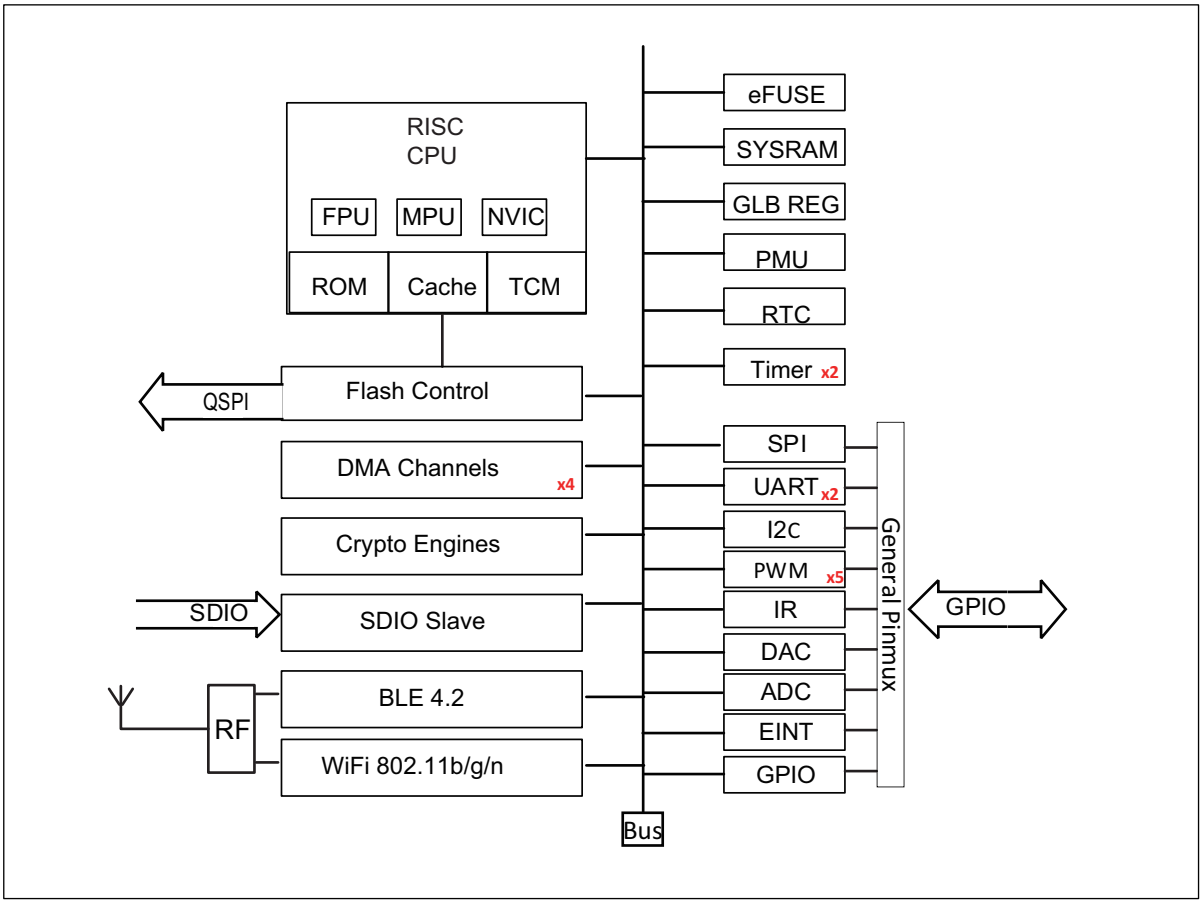

Figure 2.1: System Architecture

2.1 CPU

BL602/BL604 32-bit RISC CPU contains FPU (floating-point unit) for 32-bit single-precision arithmetic, three-stage pipelined (IF, EXE, WB), compressed 16 and 32-bit instruction set, standard JTAG debugger port including 4 hardware-

programmable breakpoints, interrupt controller including 64 interrupts and 16 interrupt levels/priorities for low latency interrupt processing. Up to 192MHz clock frequency, can be dynamically configured to change clock frequency, enter the power saving mode to achieve low power consumption.

Both WiFi/BLE stack and application run on single 32-bit RISC CPU for simple and ultra-low power applications. CPU performance ~1.46 DMIPS/MHz. ~3.1 CoreMark/MHz.

2.2 Cache

BL602/BL604 cache improves CPU performance to access external memory. Cache memories can be partially or fully configured as TCM (tightly coupled memory).

2.3 Memory

BL602/BL604 memories include: on-chip zero-delay SRAM memories, read-only memories, write-once memories, embedded flash memory (optional).

2.4 DMA

BL602/BL604 DMA (direct memory access) controller has four dedicated channels that manage data transfer between peripherals and memories to improve cpu/bus efficiency. There are three main types of transfers including memory to memory, memory to peripheral, and peripheral to memory. DMA also supports LLI (link list item) that multiple transfers are pre-defined by a series of linked lists, then hardware automatically complete all transfers according to each LLI size and address. DMA supports peripheral UART, I2C, SPI, ADC and DAC.

2.5 Bus

BL602/BL604 bus fabric connection and memory-map summarized as follows:

Table 2.1: Bus Connection

Slave/ Master	CPU	SDIO	DMA	Crypto Engine	Debug
SRAM	V	V	V	V	V
Peripheral	V	V	V	-	V
WiFi/BLE	V	V	V	-	V

Table 2.2: Memory Map

Module	Base Address	Size	Description
WRAM	0x42030000	112KB	Wireless SRAM memory
RETRAM	0x40010000	4KB	Deep sleep memory (Retention RAM)

Table 2.2: Memory Map

Module	Base Address	Size	Description
HBN	0x4000F000	4KB	Deep sleep control (Hibernate)
PDS	0x4000E000	4KB	Sleep control (Power Down Sleep)
SDU	0x4000D000	4KB	SDIO control
DMA	0x4000C000	4KB	DMA control
QSPI	0x4000B000	4KB	Flash control
IRR	0x4000A600	256B	IR Remote control
TIMER	0x4000A500	256B	Timer control
PWM	0x4000A400	256B	Pulse Width Modulation *5 control
I2C	0x4000A300	256B	I2C control
SPI	0x4000A200	256B	SPI master/slave control
UART1	0x4000A100	256B	UART control
UART0	0x4000A000	256B	UART control
L1C	0x40009000	4KB	Cache control
eFuse	0x40007000	4KB	eFuse memory control
TZ2	0x40006000	4KB	Trust isolation
TZ1	0x40005000	4KB	Trust isolation
SEC	0x40004000	4KB	Security engine
GPIP	0x40002000	4KB	General purpose DAC/ADC/ACOMP interface control
MIX	0x40001000	4KB	Mixed signal register
GLB	0x40000000	4KB	Global control register
RAM	0x22020000 /0x42020000	64KB	On-chip memory.If used as data memory, use address 0x42020000 for access; if used as program memory, use address 0x22020000 for access
XIP	0x23000000	16MB	XIP Flash memory
TCM1	0x22014000 /0x42014000	48KB	Cache memory.If used as data memory, use address 0x42014000 for access; if used as program memory, use address 0x22014000 for access
TCM0	0x22008000 /0x42008000	48KB	Cache memory.If used as data memory, use address 0x42008000 for access; if used as program memory, use address 0x22008000 for access
ROM	0x21000000	128KB	Read-only memory

2.6 Interrupt

BL602/BL604 supports internal RTC wake-up and external interrupts wake-up.

CPU interrupt controller supports stack/nesting, level/pulse, and high/low active.

2.7 Boot

BL602/BL604 supports multiple boot options: UART, SDIO, and Flash.

2.8 Power

PMU (power management unit) manages the power of the entire chip and is divided into active, idle, sleep, and hibernate power modes. The software can be configured to enter sleep mode and wake-up via RTC timer or EINT to achieve low-power sleep and accurate wake-up management.

Power down sleep modes are flexible for applications to configure as the lowest power consumption.

2.9 Clock

Clock control unit generates clocks to the core MCU and the peripheral SOC devices. The root clock source can be XTAL, PLL or RC oscillator. Dynamic power-saved by proper configurations such as sel, div, en, etc. PMU runs at 32kHz clock to keep system low-power in sleep mode.

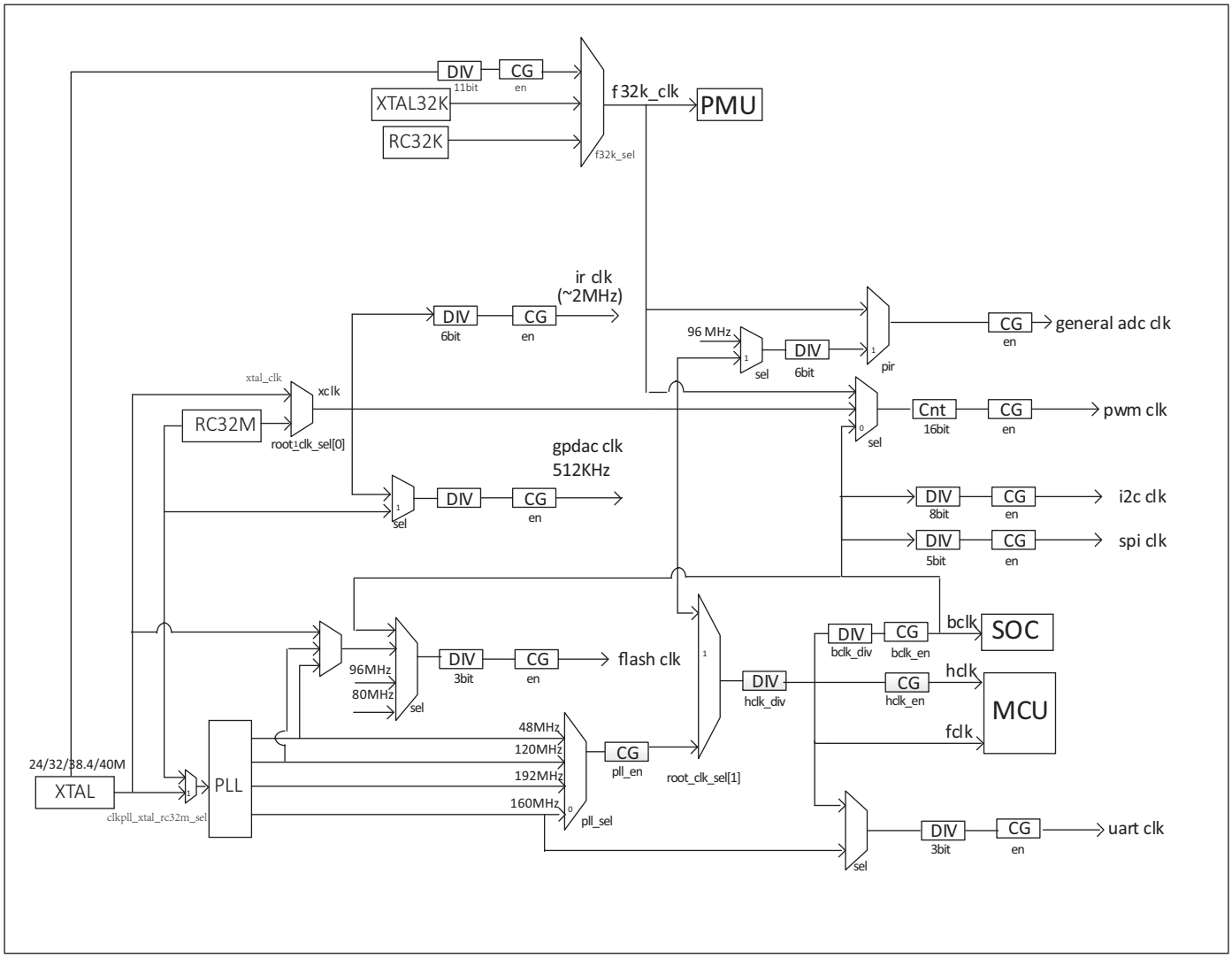

Figure 2.2: Clock Architecture

2.10 Peripherals

Peripherals include SDIO, SPI, UART, I2C, IR remote, PWM, ADC, DAC, PIR.

Each peripheral can be assigned to different groups of GPIOs through flexible configurations.

Each GPIO can be used as a general-purpose input and output function.

3 Pin Definition

BL602 32-pin package includes 10 power pins, 6 analog pins, and 16 flexible GPIO pins.

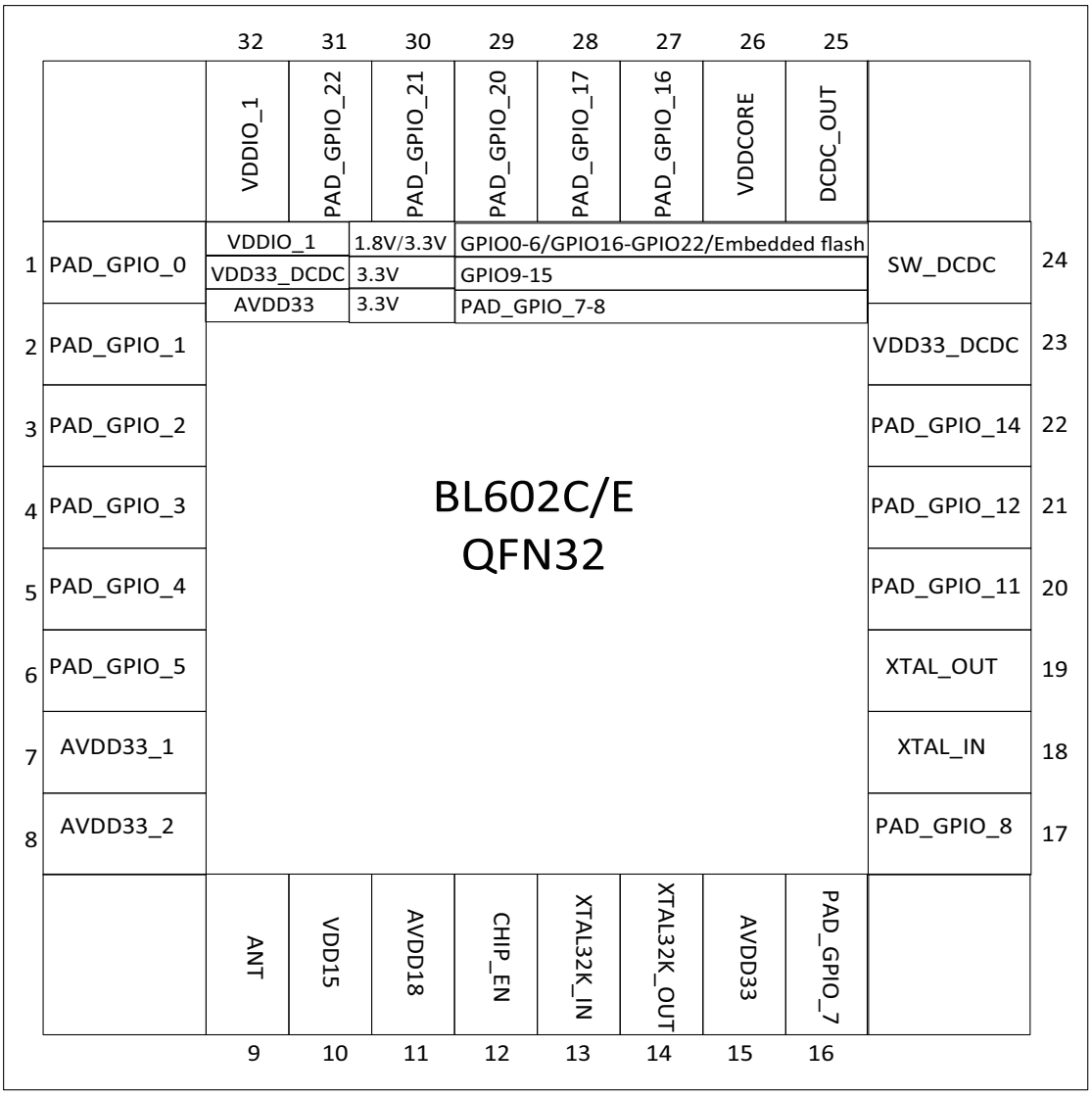

Figure 3.1: BL602 pin layout

BL604 40-pin package includes 10 power pins, 6 analog pins, 1 reset pin, and 23 flexible GPIO pins.

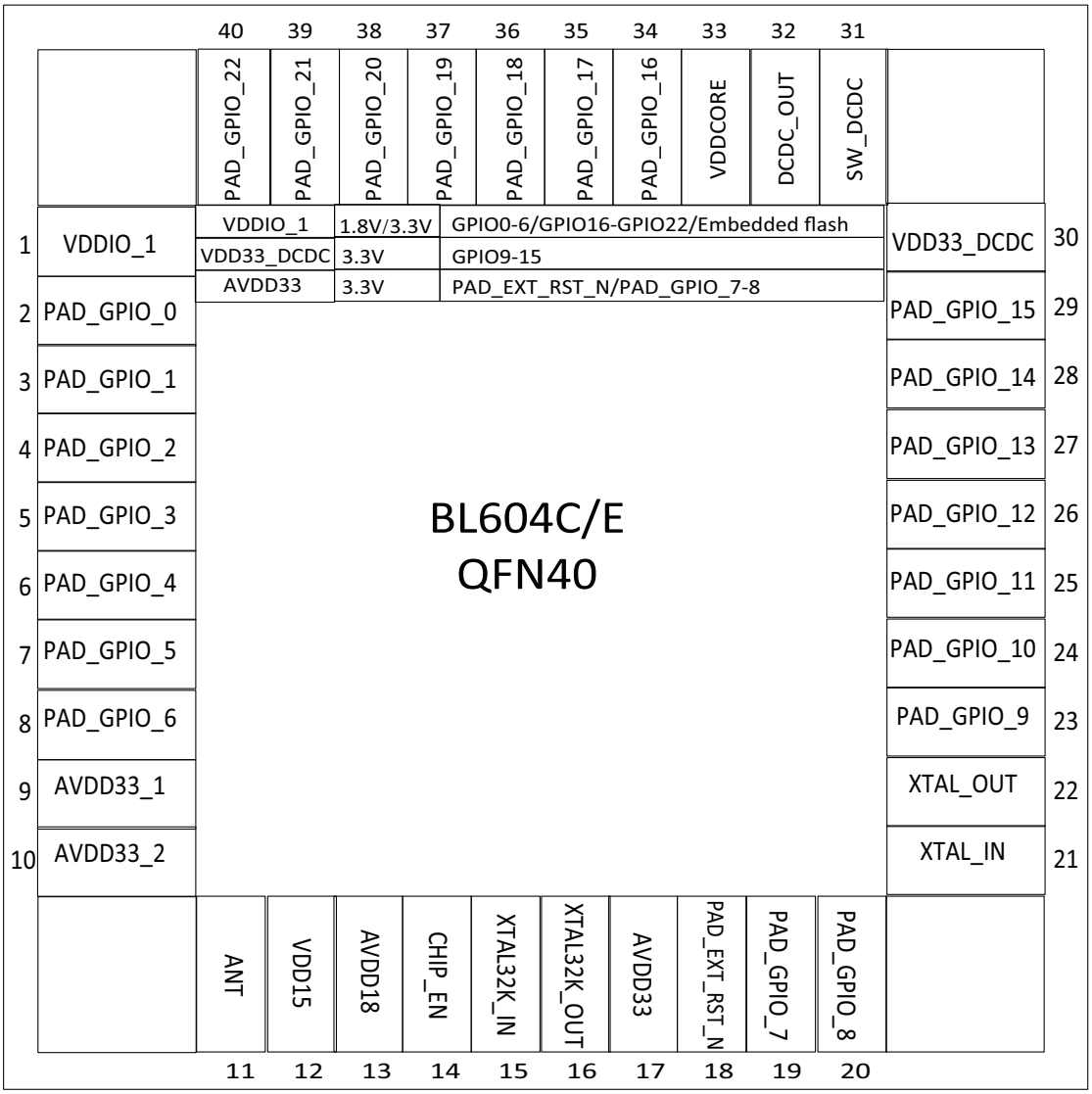

Figure 3.2: BL604 pin layout

Table 3.1: Pin description

No	Voltage Domain	BL602	BL604	I/O Type	Pin Name	Description
1	VDDIO_1	1	2	DI/DO	PAD_GPIO_0	-
2	VDDIO_1	2	3	DI/DO	PAD_GPIO_1	-
3	VDDIO_1	3	4	DI/DO	PAD_GPIO_2	-
4	VDDIO_1	4	5	DI/DO	PAD_GPIO_3	-
5	VDDIO_1	5	6	DI/DO	PAD_GPIO_4	-
6	VDDIO_1	6	7	DI/DO	PAD_GPIO_5	-
7	VDDIO_1	-	8	DI/DO	PAD_GPIO_6	-
8	AVDD33	16	19	DI/DO	PAD_GPIO_7	-
9	AVDD33	17	20	DI/DO	PAD_GPIO_8	-
10	VDD33_DCDC	-	23	DI/DO	PAD_GPIO_9	-
11	VDD33_DCDC	-	24	DI/DO	PAD_GPIO_10	-
12	VDD33_DCDC	20	25	DI/DO	PAD_GPIO_11	-
13	VDD33_DCDC	21	26	DI/DO	PAD_GPIO_12	-
14	VDD33_DCDC	-	27	DI/DO	PAD_GPIO_13	-
15	VDD33_DCDC	22	28	DI/DO	PAD_GPIO_14	-
16	VDD33_DCDC	-	29	DI/DO	PAD_GPIO_15	-
17	VDDIO_1	27	34	DI/DO	PAD_GPIO_16	-
18	VDDIO_1	28	35	DI/DO	PAD_GPIO_17	-
19	VDDIO_1	-	36	DI/DO	PAD_GPIO_18	-
20	VDDIO_1	-	37	DI/DO	PAD_GPIO_19	-
21	VDDIO_1	29	38	DI/DO	PAD_GPIO_20	-
22	VDDIO_1	30	39	DI/DO	PAD_GPIO_21	-
23	VDDIO_1	31	40	DI/DO	PAD_GPIO_22	-
24	VDDIO_1	-	-	DI/DO	PAD_GPIO_23	-
25	VDDIO_1	-	-	DI/DO	PAD_GPIO_24	-
26	VDDIO_1	-	-	DI/DO	PAD_GPIO_25	-

BL602/604 Datasheet

Table 3.1: Pin description

No	Voltage Domain	BL602	BL604	I/O Type	Pin Name	Description
27	VDDIO_1	-	-	DI/DO	PAD_GPIO_26	-
28	VDDIO_1	-	-	DI/DO	PAD_GPIO_27	-
29	VDDIO_1	-	-	DI/DO	PAD_GPIO_28	-
30	AVDD33	12	14	Analog	CHIP_EN	Chip enable
31	AVDD33	-	18	DI	PAD_EXT_RST_N	External reset
32	AVDD33	13	15	Analog	XTAL32K_IN	Crystal oscillator 32.768kHz input
33	AVDD33	14	16	Analog	XTAL32K_OUT	Crystal oscillator 32.768kHz output
34	AVDD33	18	21	Analog	XTAL_IN	External crystal input, support 24/32/38.4/40MHz
35	AVDD33	19	22	Analog	XTAL_OUT	External crystal output, support 24/32/38.4/40MHz
36	VDD15	9	11	Analog	ANT	RF input and output (single pin)
37	-	32	1	Power	VDDIO_1	Externally powered 3.3V or 1.8V
38	-	23	30	Power	VDD33_DCDC	DCDC
39	-	24	31	Power	SW_DCDC	DCDC
40	-	25	32	Power	DCDC_OUT	DCDC
41	-	7	9	Power	AVDD33_1	Externally powered 3.3V
42	-	8	10	Power	AVDD33_2	Externally powered 3.3V
43	-	15	17	Power	AVDD33	Externally powered 3.3V
44	-	10	12	Power	VDD15	Power 1.5V
45	-	11	13	Power	AVDD18	Power 1.8V
46	-	26	33	Power	VDDCORE	Core power

BL602/604 Datasheet

Table 3.2: GPIO Muxed Pins

Pin Name	Flash[1]	SDIO	SPI	UART[2](Default /SWAP=1)	I2C Master	PWM	Analog	External_PA	JTAG (Default /SWAP=1)	IR
PAD_GPIO_0	SF2_D1	CLK	MIS0 /MOSI	SIG0 /SIG4	SCL	PWM_CH0	-	FEM0	TMS/TCK	-
PAD_GPIO_1	SF2_D2	CMD	MOSI /MISO	SIG1/SIG5	SDA	PWM_CH1	-	FEM1	TDI/TDO	-
PAD_GPIO_2	SF2_D3	DAT0	SS	SIG2/SIG6	SCL	PWM_CH2	-	FEM2	TCK/TMS	-
PAD_GPIO_3	-	DAT1	SCLK	SIG3/SIG7	SDA	PWM_CH3	-	FEM3	TDO/TDI	-
PAD_GPIO_4	-	DAT2	MISO /MOSI	SIG4/SIG0	SCL	PWM_CH4	ADC_CH1	FEM0	TMS/TCK	-
PAD_GPIO_5	-	DAT3	MOSI /MISO	SIG5/SIG1	SDA	PWM_CH0	ADC_CH4	FEM1	TDI/TDO	-
PAD_GPIO_6	-	-	SS	SIG6/SIG2	SCL	PWM_CH1	ADC_CH5	FEM2	TCK/TMS	-
PAD_GPIO_7	-	-	SCLK	SIG7/SIG3	SDA	PWM_CH2	-	FEM3	TDO/TDI	-
PAD_GPIO_8	-	-	MISO /MOSI	SIG0/SIG4	SCL	PWM_CH3	-	FEM0	TMS/TCK	-
PAD_GPIO_9	-	-	MOSI /MISO	SIG1/SIG5	SDA	PWM_CH4	ADC_CH6/7	FEM1	TDI/TDO	-
PAD_GPIO_10	-	-	SS	SIG2/SIG6	SCL	PWM_CH0	MICBIAS /ADC_CH8/9	FEM2	TCK/TMS	-
PAD_GPIO_11	-	-	SCLK	SIG3/SIG7	SDA	PWM_CH1	ADC_CH10 /IRTX	FEM3	TDO/TDI	IRRX (ir_rx_gpio_sel=1)
PAD_GPIO_12	-	-	MISO /MOSI	SIG4/SIG0	SCL	PWM_CH2	ADC_CH0	FEM0	TMS/TCK	IRRX (ir_rx_gpio_sel=2)
PAD_GPIO_13	-	-	MOSI /MISO	SIG5/SIG1	SDA	PWM_CH3	ADC_CH3 /DAC_A	FEM1	TDI/TDO	IRRX (ir_rx_gpio_sel=3)
PAD_GPIO_14	-	-	SS	SIG6/SIG2	SCL	PWM_CH4	ADC_CH2 /DAC_B	FEM2	TCK/TMS	-
PAD_GPIO_15	-	-	SCLK	SIG7/SIG3	SDA	PWM_CH0	psw_irrcv_out /ADC_CH11	FEM3	TDO/TDI	-

Table 3.2: GPIO Muxed Pins

Pin Name	Flash[1]	SDIO	SPI	UART[2](Default /SWAP=1)	I2C Master	PWM	Analog	External_PA	JTAG (Default /SWAP=1)	IR
PAD_GPIO_16	-	-	MISO /MOSI	SIG0/SIG4	SCL	PWM_CH1	-	FEM0	TMS/TCK	-
PAD_GPIO_17	SF1_D3	-	MOSI /MISO	SIG1/SIG5	SDA	PWM_CH2	-	FEM1	TDI/TDO	-
PAD_GPIO_18	SF1_D2	-	SS	SIG2/SIG6	SCL	PWM_CH3	-	FEM2	TCK/TMS	-
PAD_GPIO_19	SF1_D1	-	SCLK	SIG3/SIG7	SDA	PWM_CH4	-	FEM3	TDO/TDI	-
PAD_GPIO_20	SF1_D0 /SF2_D0	-	MISO /MOSI	SIG4/SIG0	SCL	PWM_CH0	-	FEM0	TMS/TCK	-
PAD_GPIO_21	SF1_CS /SF2_CS	-	MOSI /MISO	SIG5/SIG1	SDA	PWM_CH1	-	FEM1	TDI/TDO	-
PAD_GPIO_22	SF1_CLK /SF2_CLK	-	SS	SIG6/SIG2	SCL	PWM_CH2	-	FEM2	TCK/TMS	-
PAD_GPIO_23	SF0_CLK	-	-	-	-	-	-	-	-	-
PAD_GPIO_24	SF0_CS	-	-	-	-	-	-	-	-	-
PAD_GPIO_25	SF0_D0	-	-	-	-	-	-	-	-	-
PAD_GPIO_26	SF0_D1	-	-	-	-	-	-	-	-	-
PAD_GPIO_27	SF0_D2	-	-	-	-	-	-	-	-	-
PAD_GPIO_28	SF0_D3	-	-	-	-	-	-	-	-	-

[1] There are 3 groups of Flash, and the smallest selection unit is group, which is configured according to group when used.

[2] The default UART signal mapping table is shown below.

BL602/604 Datasheet

Table 3.3: UART Signal Mapping(Default)

UART Signal	uart_sig_x_sel	Mapping Signal
UART_SIG0	uart_sig_0_sel=0	UART0_RTS
UART_SIG1	uart_sig_1_sel=1	UART0_CTS
UART_SIG2	uart_sig_2_sel=2	UART0_TXD
UART_SIG3	uart_sig_3_sel=3	UART0_RXD
UART_SIG4	uart_sig_4_sel=4	UART1_RTS
UART_SIG5	uart_sig_5_sel=5	UART1_CTS
UART_SIG6	uart_sig_6_sel=6	UART1_TXD
UART_SIG7	uart_sig_7_sel=7	UART1_RXD

Note: UART_SIG0-UART_SIG7 can be configured as any of 8 Mapping Signals. For example: UART_SIG0 can also be configured as UART_RXD. The specific signal mapping example is shown in the table below.

Table 3.4: UART Signal Mapping(Example)

UART Signal	uart_sig_x_sel	Mapping Signal
UART_SIG0	uart_sig_0_sel=7	UART1_RXD
UART_SIG1	uart_sig_1_sel=6	UART1_TXD
UART_SIG2	uart_sig_2_sel=5	UART1_CTS
UART_SIG3	uart_sig_3_sel=4	UART1_RTS
UART_SIG4	uart_sig_4_sel=3	UART0_RXD
UART_SIG5	uart_sig_5_sel=2	UART0_TXD
UART_SIG6	uart_sig_6_sel=1	UART0_CTS
UART_SIG7	uart_sig_7_sel=0	UART0_RTS

4 Electrical Specifications

4.1 Absolute Maximum Rating

Table 4.1: Absolute Maximum Rating

Pin Name	Min.	Max.	Unit
AVDD33_1	-0.3	3.63	V
AVDD33_2	-0.3	3.63	V
AVDD33	-0.3	3.63	V
DVDD33_DCDC	-0.3	3.63	V
DVDDIO_1	-0.3	3.63	V
ESD Protection (HBM)		2000	V
Storage Temperature	-45	135	°C

4.2 Operating Condition

Table 4.2: Recommended Power Operating Range

Pin Name	Min.	Typ	Max.	Unit
AVDD33_1	2.1	3.3	3.63	V
AVDD33_2	2.1	3.3	3.63	V
AVDD33	2.1	3.3	3.63	V
DVDD33_DCDC	2.1	3.3	3.63	V
DVDDIO_1	2.1 / 1.62	3.3 / 1.8	3.63 / 1.98	V

Table 4.3: Recommended Temperature Operating Range

Item		Min.	Max.	Unit
Temperature	Main Die	-30	105	°C
	Multi-Die SiP	-30	85	°C

Table 4.4: General Operating Conditions

Item	Description	Min.	Typ	Max.	Unit
FCPU	CPU/TCM/Cache clock frequency	1	160	192	MHz
FSYS	System clock frequency	1	80	96	MHz

5 Reference Design (simplified)

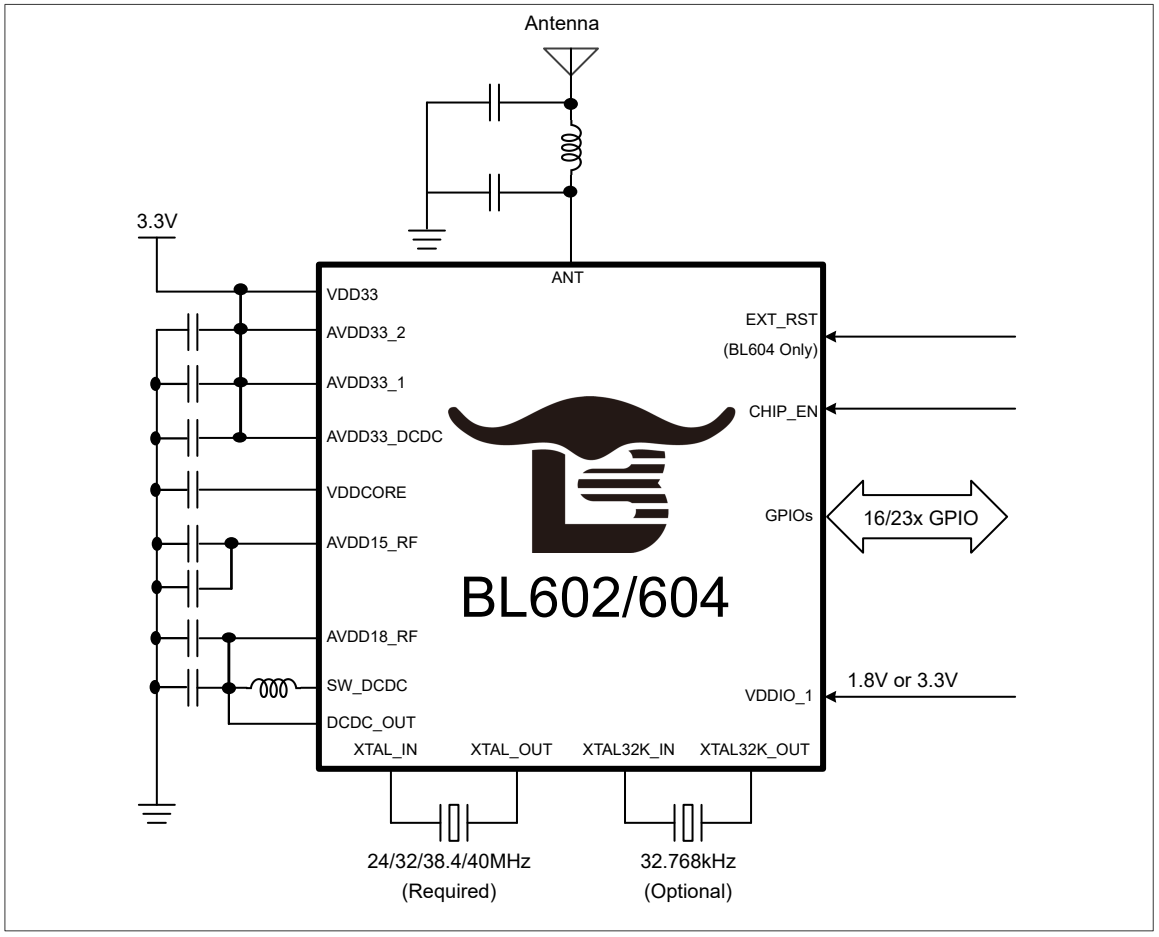

Figure 5.1: Reference Design

6 Package Information(QFN32)

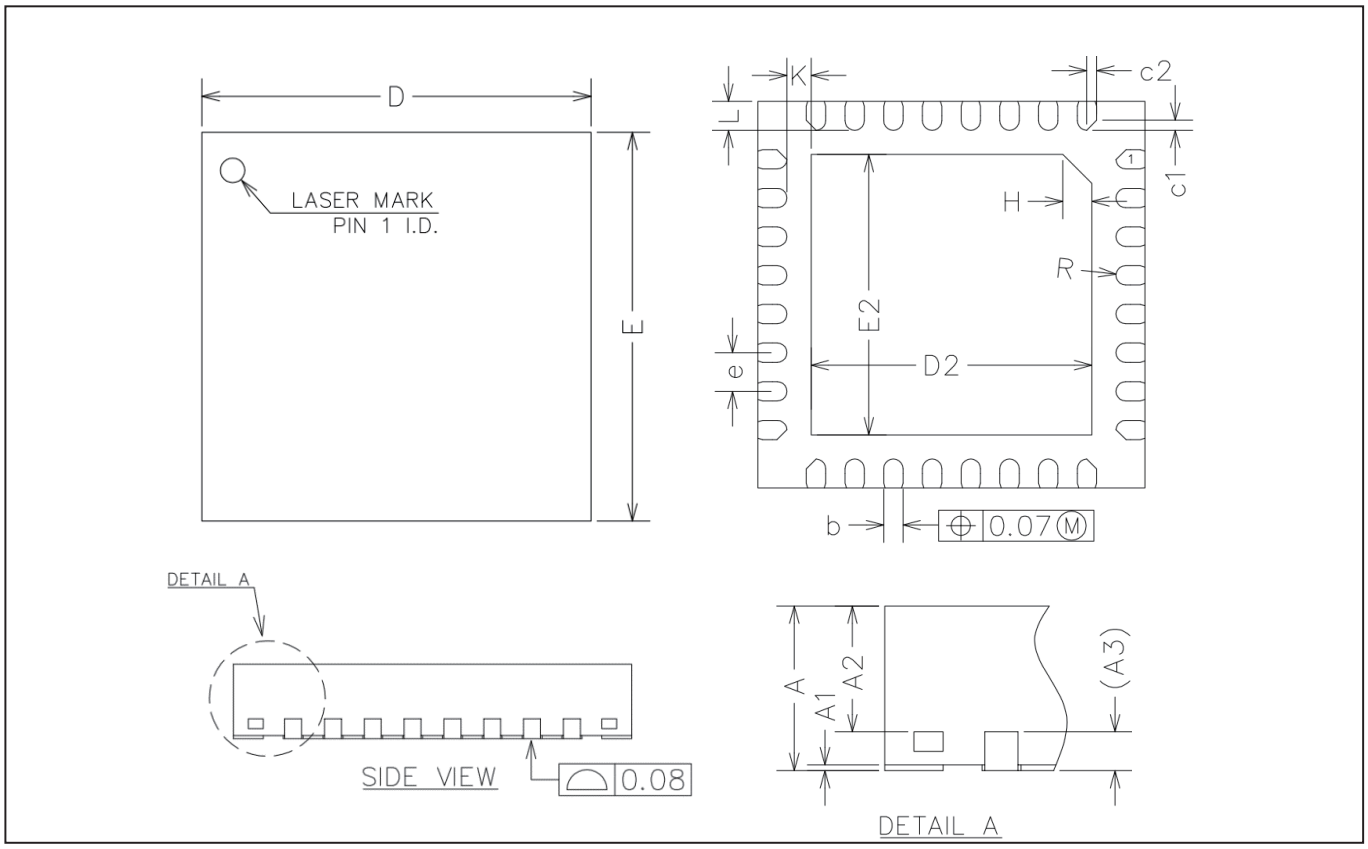

Figure 6.1: QFN32 Package drawing

Table 6.1: QFN32 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05

Table 6.1: QFN32 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A2	0.50	0.55	0.60
A3	0.20REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.80	2.90	3.00
E2	2.80	2.90	3.00
e	0.30	0.40	0.50
H	0.30REF		
K	0.25REF		
L	0.25	0.30	0.35
R	0.09	-	-
c1	-	0.10	-
c2	-	0.10	-

7 Package Information(QFN40)

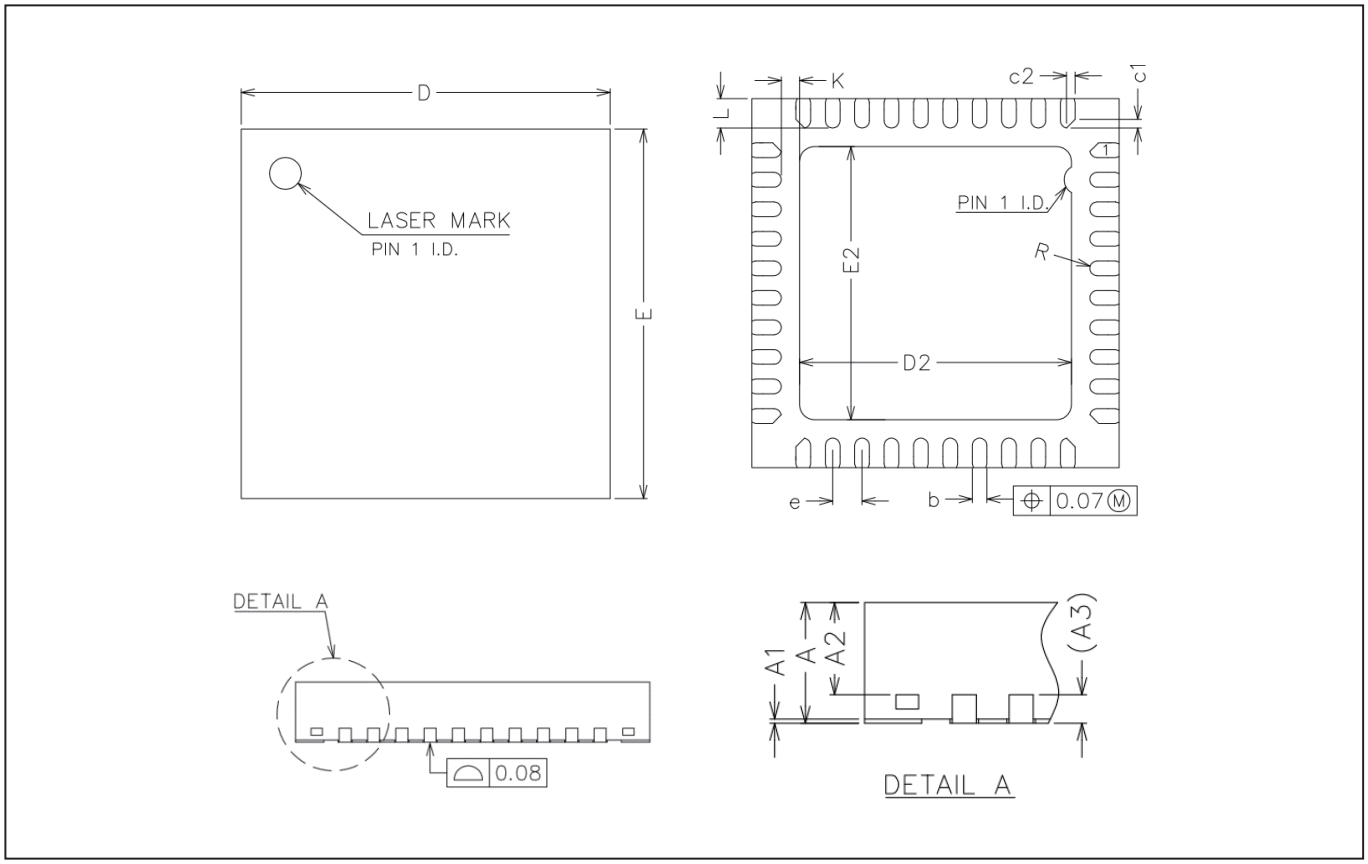

Figure 7.1: QFN40 Package drawing

Table 7.1: QFN40 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05

Table 7.1: QFN40 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A2	0.60	0.65	0.70
A3	0.20REF		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.35	0.40	0.45
K	0.20	-	-
L	0.35	0.40	0.45
R	0.075	-	-
C1	-	0.12	-
C2	-	0.12	-

8 Top Marking Definition

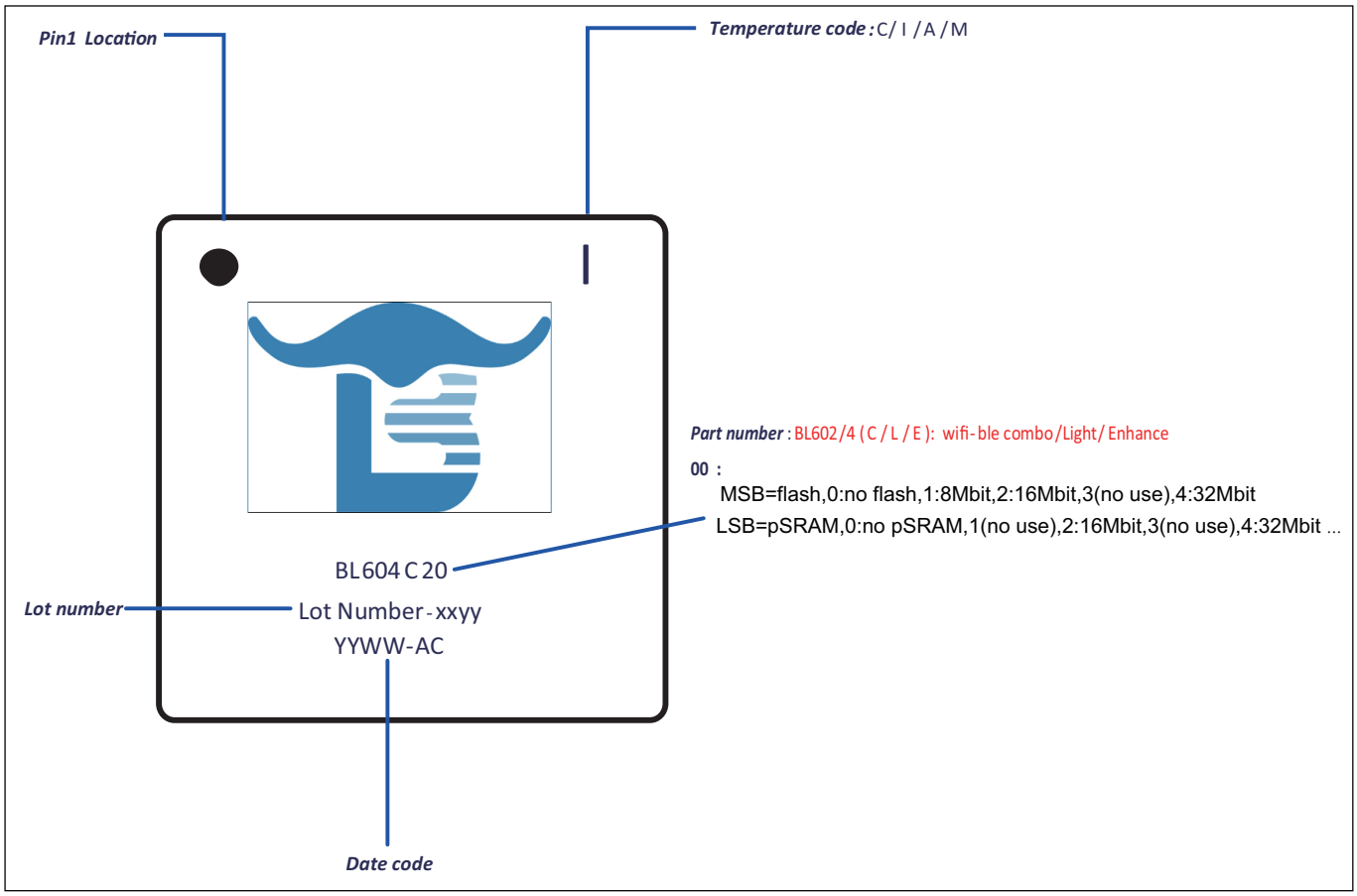

Figure 8.1: Top Marking Definition

9 Ordering Information

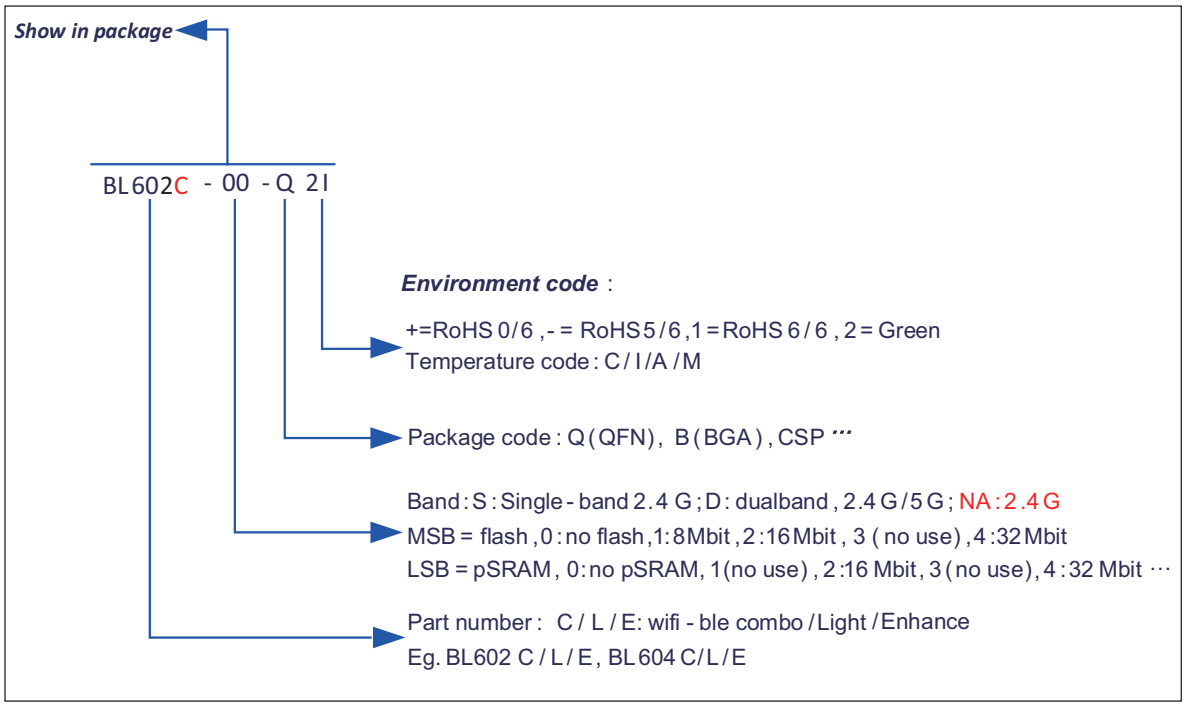

Figure 9.1: Part Number

Table 9.1: Part Order Options

Product No.	Description
BL602C-00-Q2I	WiFi/BLE Combo, QFN32
BL602C-20-Q2I	WiFi/BLE Combo, QFN32, flash 16Mb
BL604E-20-Q2I	WiFi/BLE Enhance, QFN40, flash 16Mb

10 Revision history

Table 10.1: Document revision history

Date	Revision	Changes
2020/2/13	0.9	Initial release
2020/4/20	1.0	Add Marking Definition
2020/5/28	1.1	Modify clock frequency
2020/7/28	1.2	Modify Product Number
2020/12/15	1.4	Modify peripheral characteristics
2020/12/31	1.5	Modify function description
2020/1/13	1.6	Update reference design