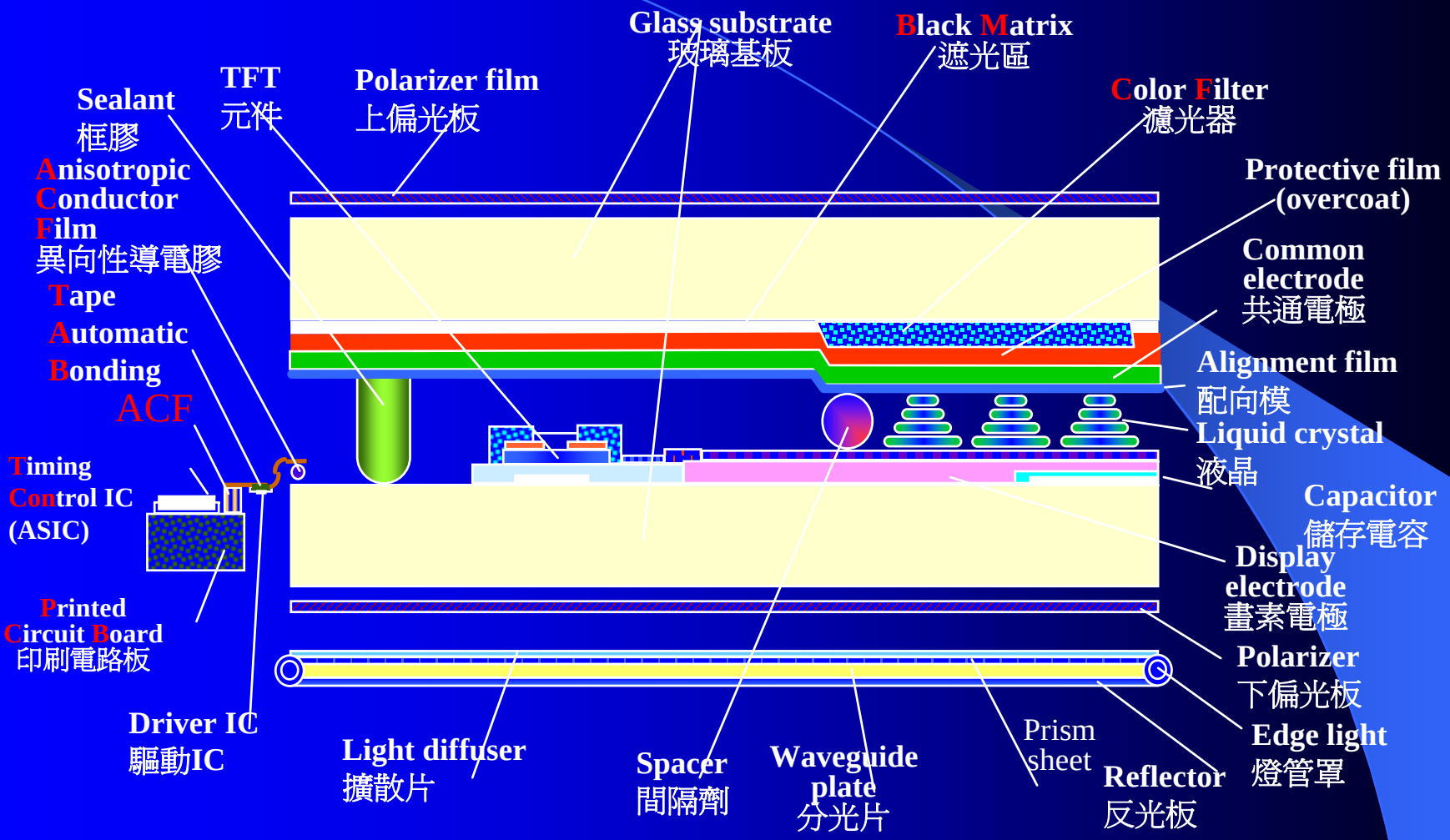
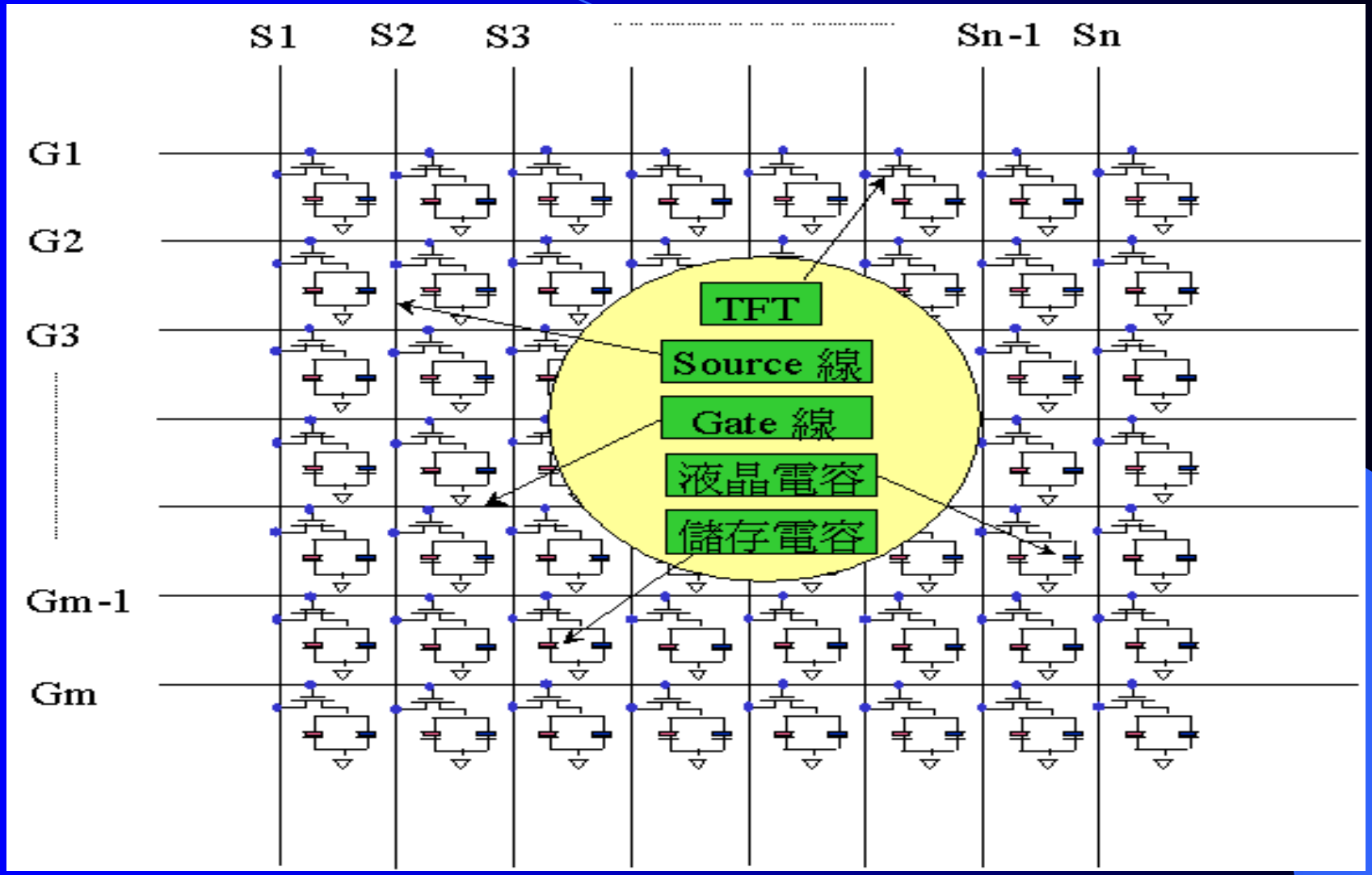
模組迴路解析簡介

清情电子科技有限公司

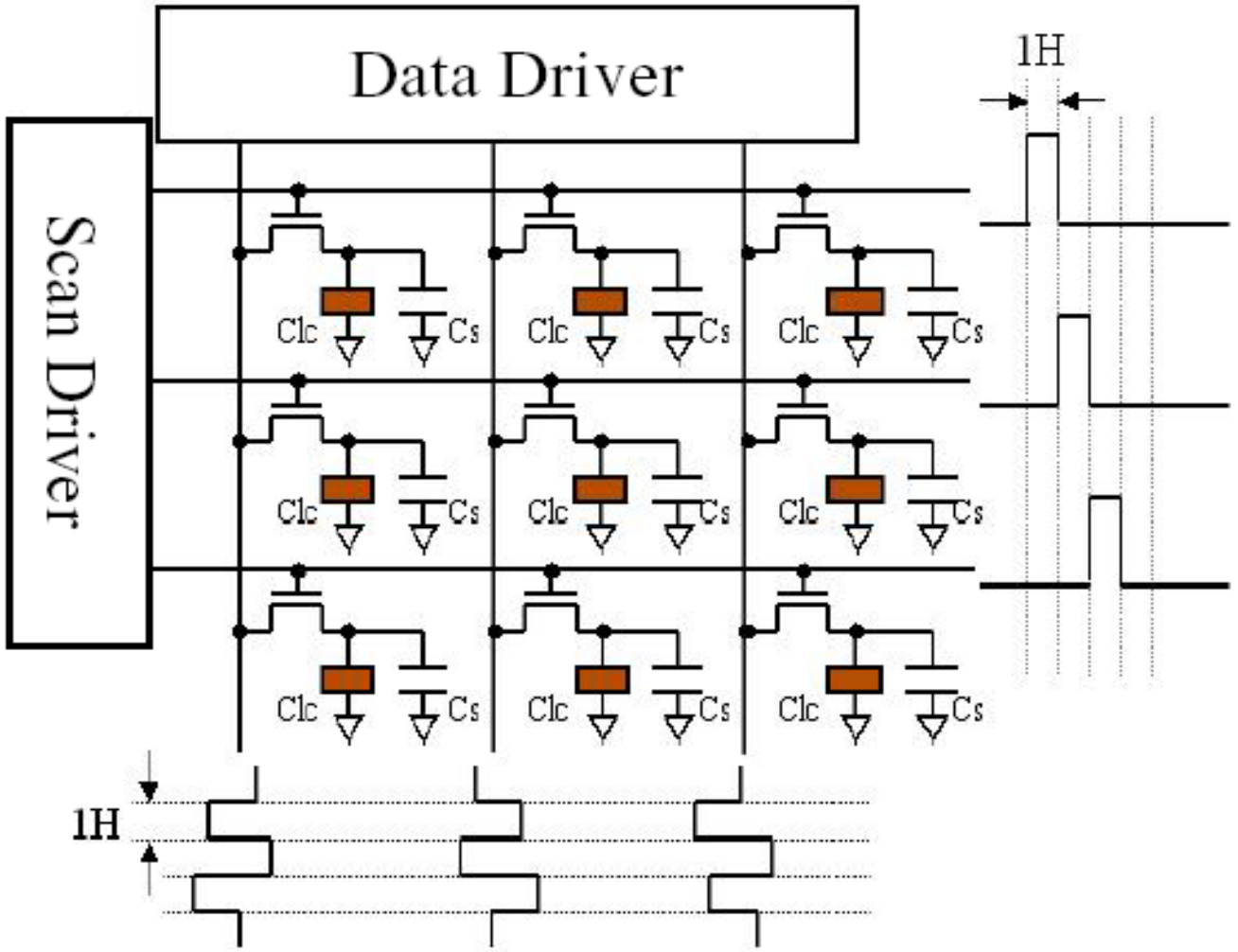
面內構造


Glass substrate
玻璃基板
Black Matrix
遮光區
TFT
元件
Polarizer film
上偏光板
Color Filter
濾光器
Sealant
框膠
Anisotropic Conductor Film
異向性導電膠
Tape
Automatic Bonding
ACF
Protective film (overcoat)
Common electrode
共通電極
Alignment film
配向模
Liquid crystal
液晶
Capacitor
儲存電容
Timing Control IC (ASIC)
Display electrode
畫素電極
Printed Circuit Board
印刷電路板
Polarizer
下偏光板
Edge light
燈管罩
Driver IC
驅動IC
Light diffuser
擴散片
Spacer
間隔劑
Waveguide plate
分光片
Prism sheet
Reflector
反光板

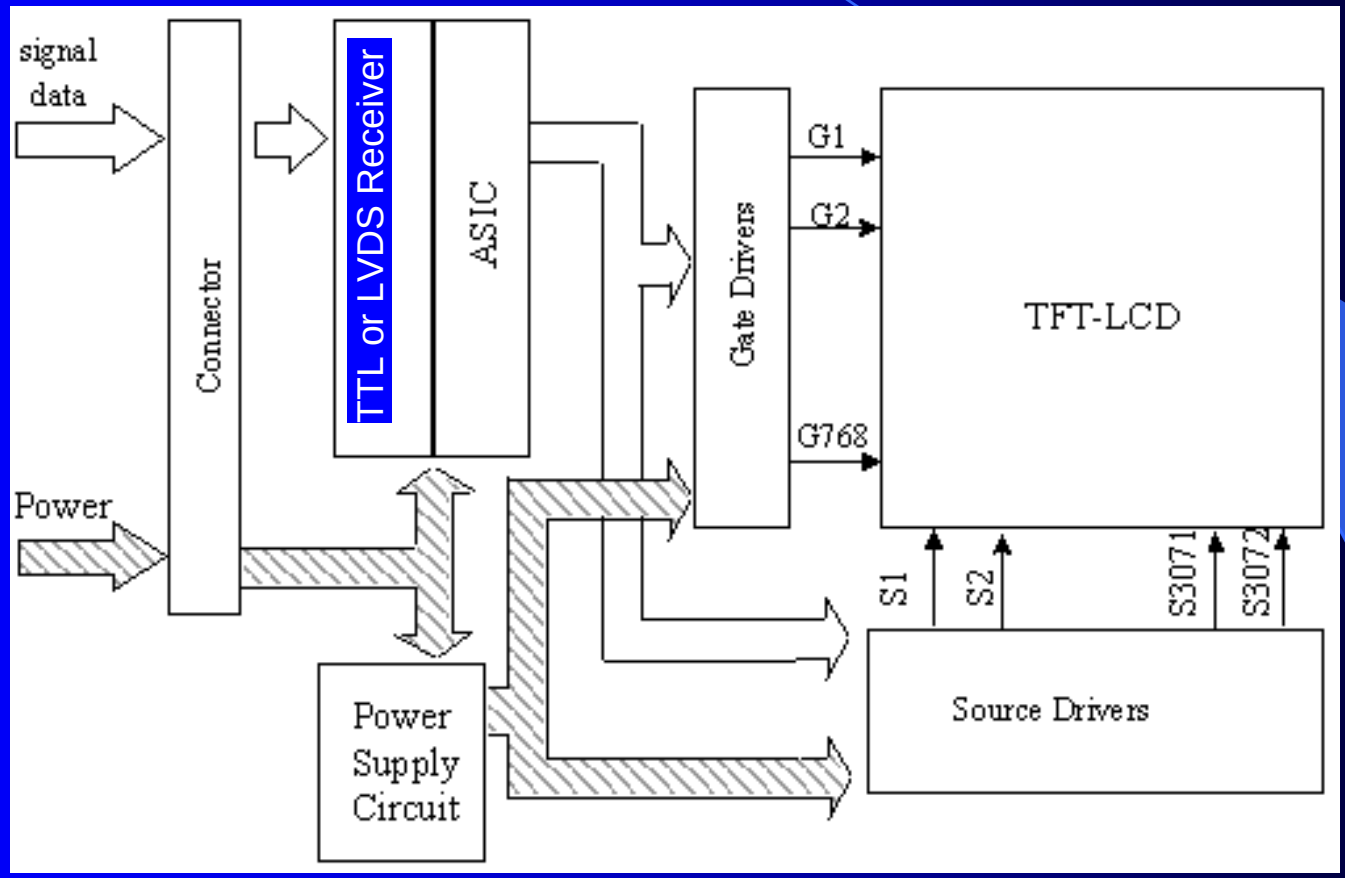
面内構造



訊號驅動原理



模組架構


signal
data
Connector
TTL or LVDS Receiver
ASIC
Gate Drivers
G1
G2
G768
TFT-LCD
Power
Power
Supply
Circuit
S1
S2
S3071
S3072
Source Drivers

專有名詞

What is *EMI/RFI*

ElectroMagnetic Interference

Radio Frequency Interference

電磁波向外輻射干擾(電磁干擾)/(微波干擾)

What is *EMC*

ElectroMagnetic Compatibility

外界電磁波向內輻射干擾(電磁相容)

傳統訊號格式

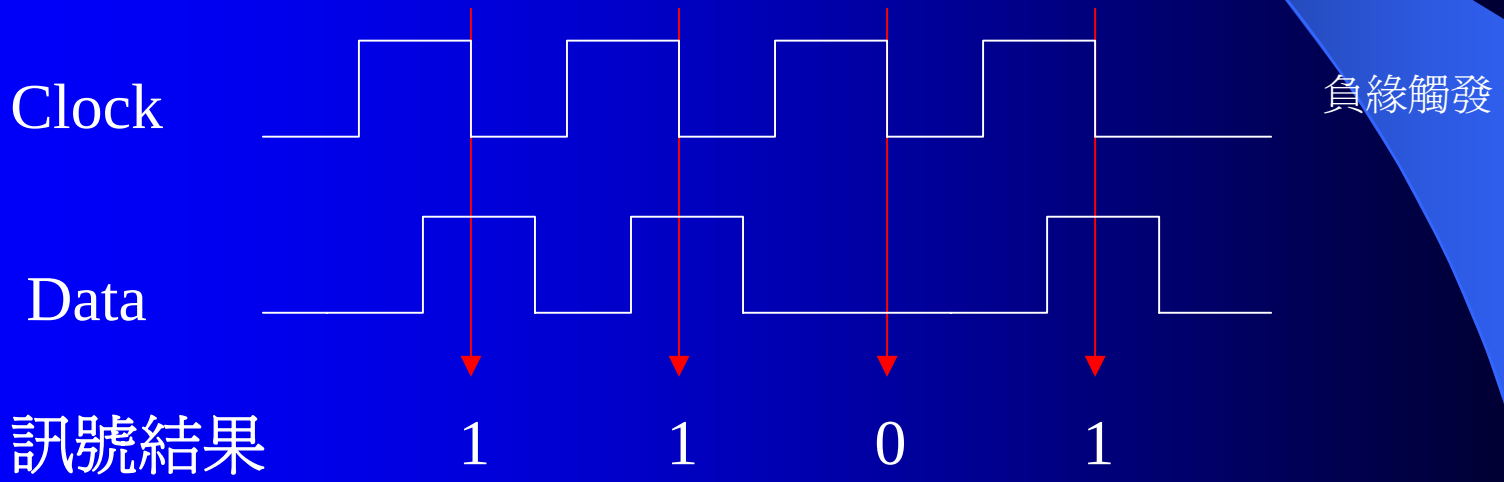
- TTL: ***T**ransistor-**T**ransistor **L**ogic*

  最基本的數位訊號, 低電位代表0,高電位代表1

  優點: 最直接的訊號, 可直接量測

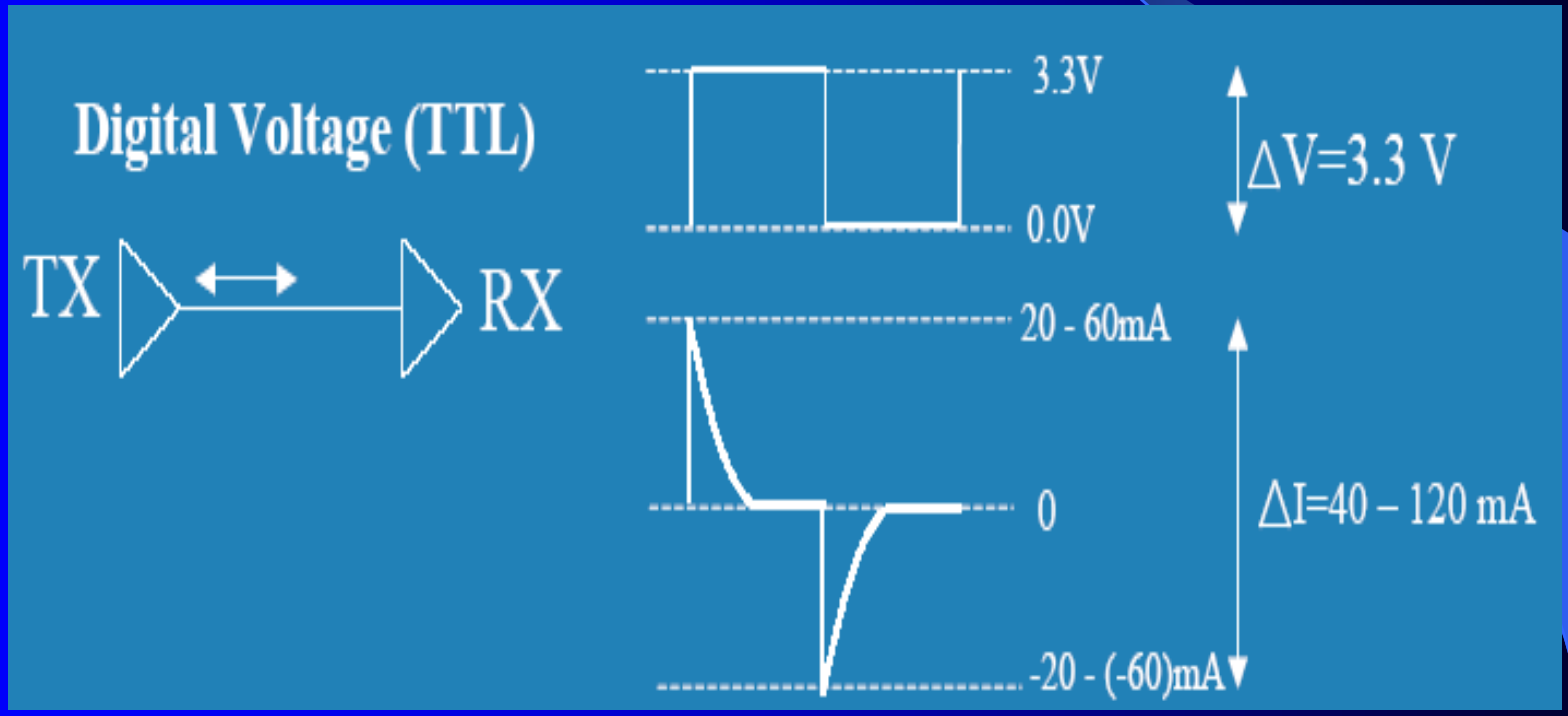
  缺點: 1. 易受外界干擾, 消耗功率大

  2. 易向外界干擾，發射EMI.



TTL 電氣規格

TTL 特性

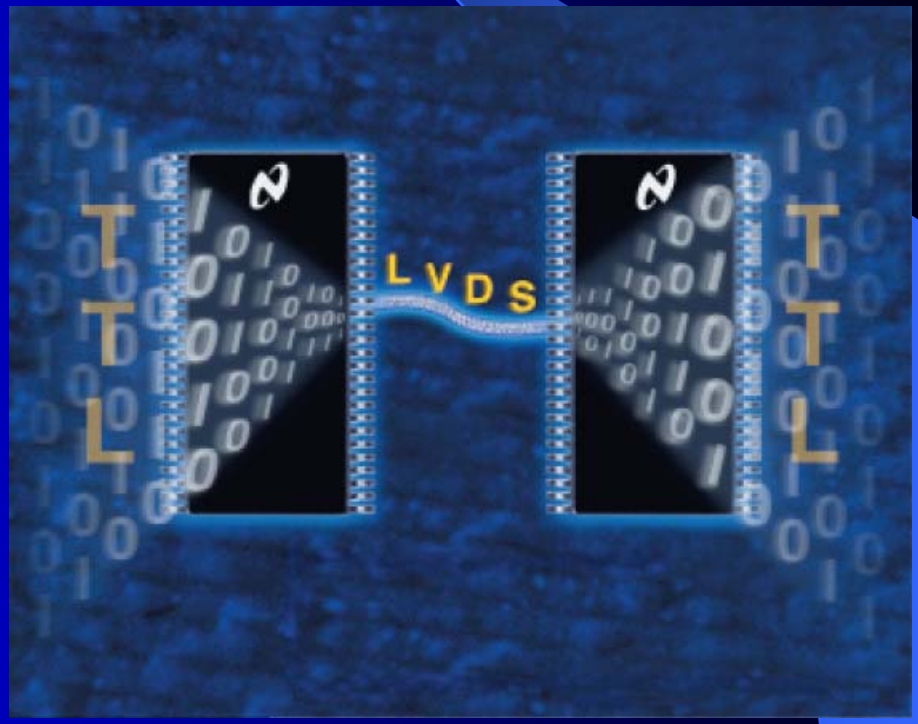


外部訊號

LVDS：*Low Voltage Differential Signaling*

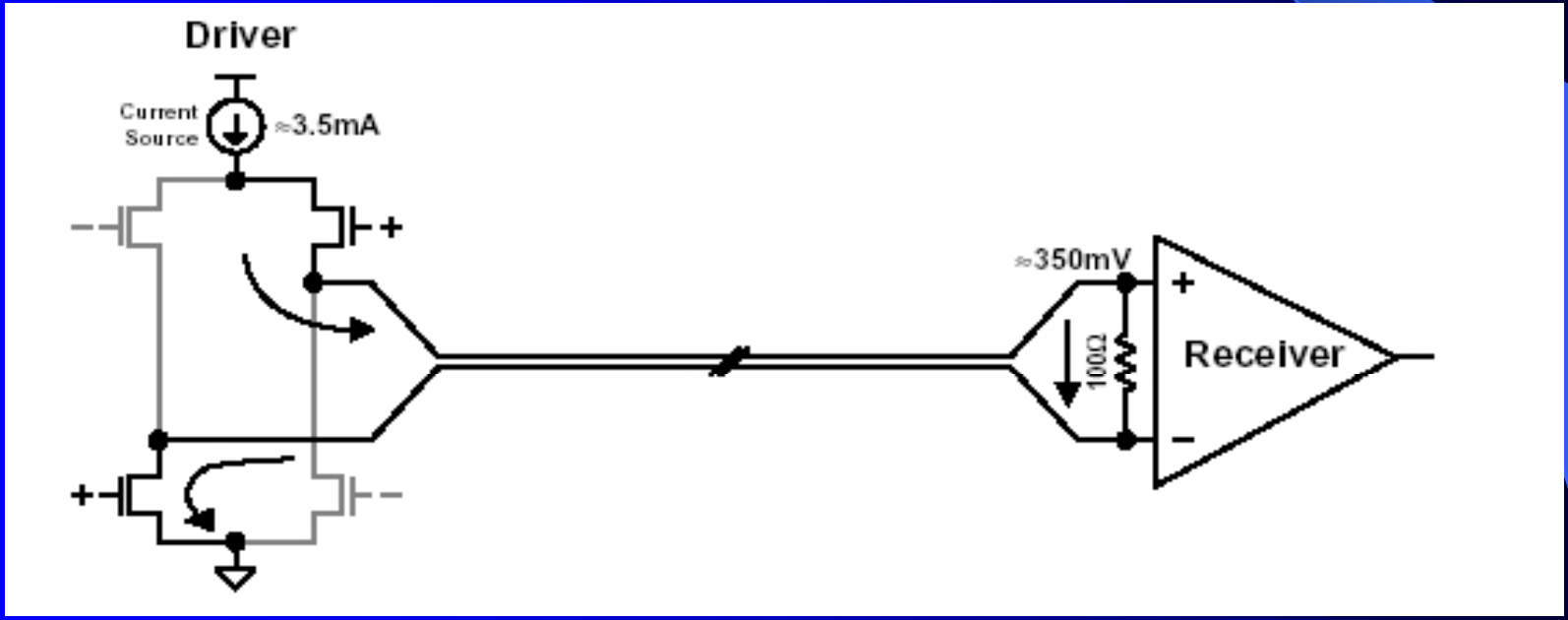
A low noise, low power, low amplitude method for high-speed (gigabits per second) data transmission over copper wire.

使用非常低的電壓擺幅大約350mV，使用這種方式可以減少功率消耗及減低EMI，更能達到降低成本之目的。



LVDS工作方式

差動輸入信號經由兩顆對應MOS gate端輸入，因爲電流源使用3.5mA因此接收器(Receiver)差動接收端可獲取3.5mA電流但是接收器差動輸入端直流阻抗非常大，爲了使電流通過以產生350mV，故在接收器差動輸入端要接上100歐姆的電阻，以滿足LVDS電壓擺幅350mV。



LVDS電性規格

LVDS is currently standardized by two different standards:

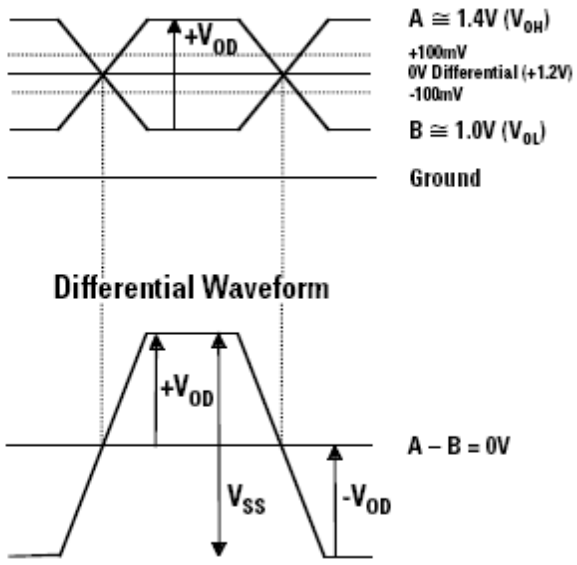
TIA/EIA (Telecommunications Industry Association/Electronic Industries Association)
- ANSI/TIA/EIA-644 (LVDS) Standard

IEEE (Institute for Electrical and Electronics Engineering)
- IEEE 1596.3

ANSI/TIA/EIA-644 (LVDS) Standard
Note: Actual datasheet specifications may be significantly better.

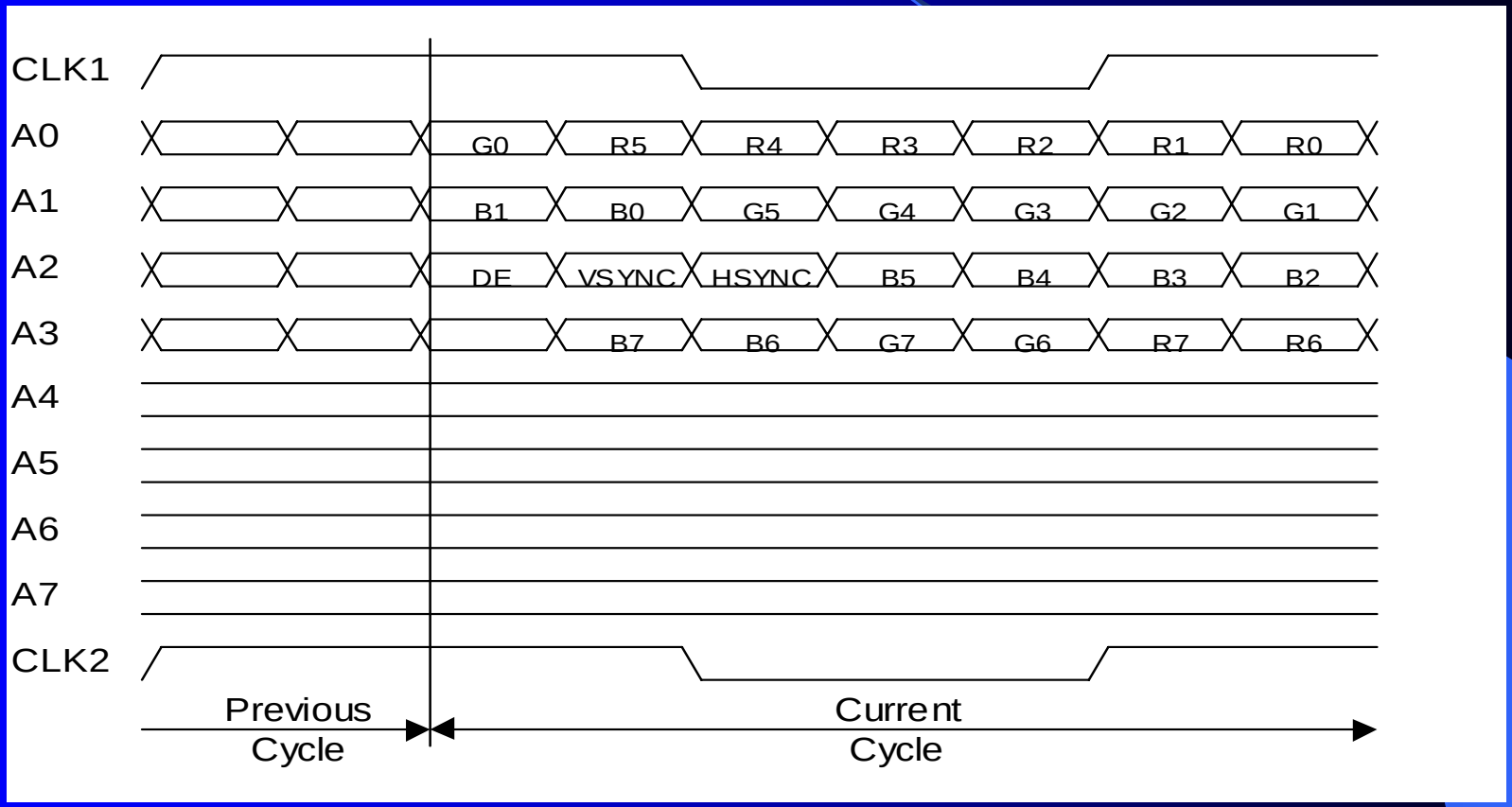
Parameter	Description	Min	Max	Units
V_{OD}	Differential Output Voltage	247	454	mV
V_{OS}	Offset Voltage	1.125	1.375	V
ΔV_{OD}	|Change to V_{OD}|		50	|mV|
ΔV_{OS}	|Change to V_{OS}|		50	|mV|
I_{SA}, I_{SB}	Short Circuit Current		24	|mA|
t_r/t_f	Output Rise/Fall Times (≥200Mbps)	0.26	1.5	ns
	Output Rise/Fall Times (<200Mbps)	0.26	30% of t_{ui}†	ns
I_{IN}	Input Current		20	|µA|
V_{TH}	|Threshold Voltage|		±100	mV
V_{IN}	Input Voltage Range	0	2.4	V

† t_{ui} is unit interval (i.e. bit width).



Single-Ended & Differential Waveforms

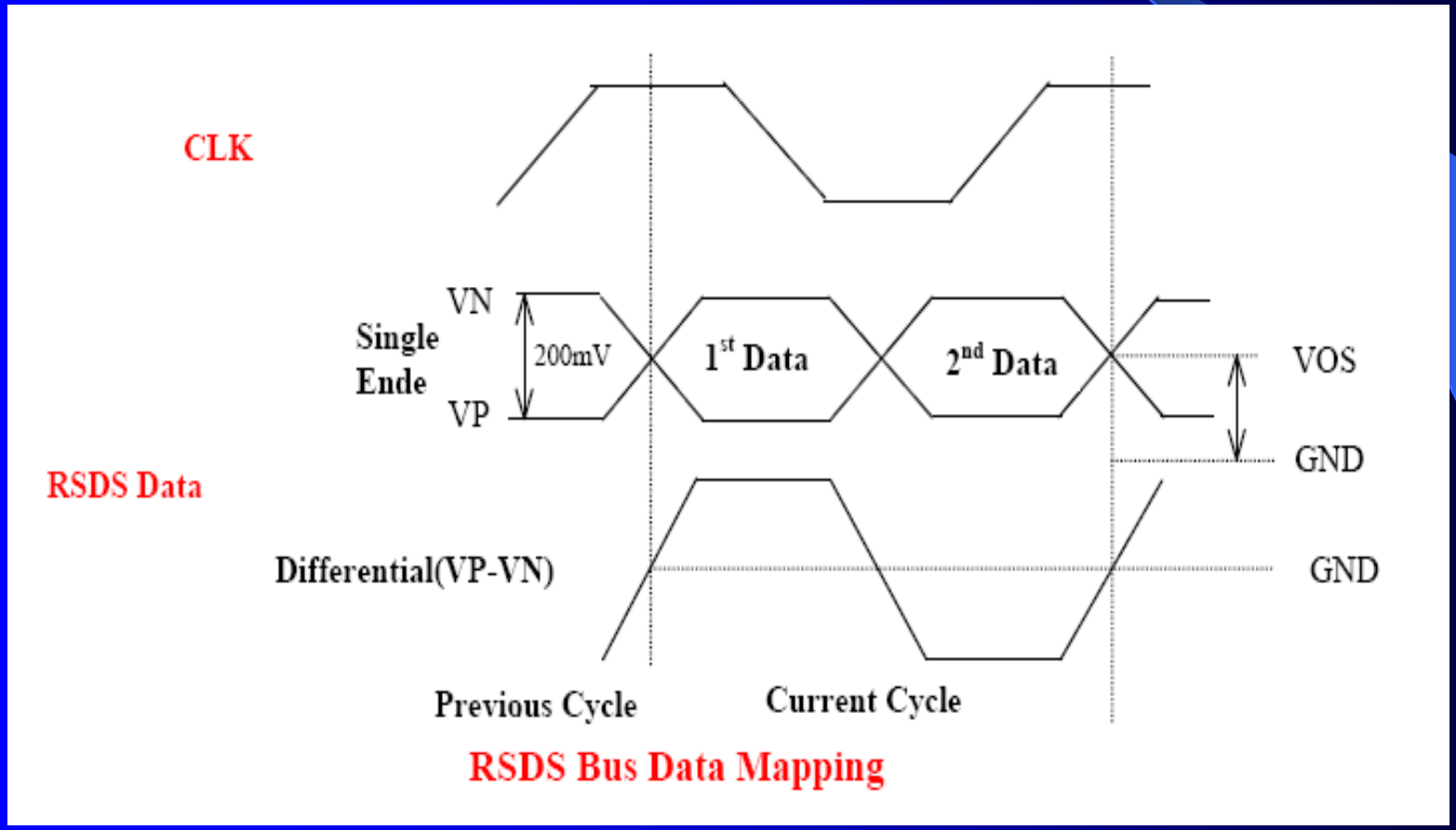
LVDS編碼


CLK1
A0
A1
A2
A3
A4
A5
A6
A7
CLK2
G0
R5
R4
R3
R2
R1
R0
B1
B0
G5
G4
G3
G2
G1
DE
VSYNC
HSYNC
B5
B4
B3
B2
B7
B6
G7
G6
R7
R6
Previous Cycle
Current Cycle

內部訊號格式

RSDS：*Reduced Swing Differentisl Signaling*

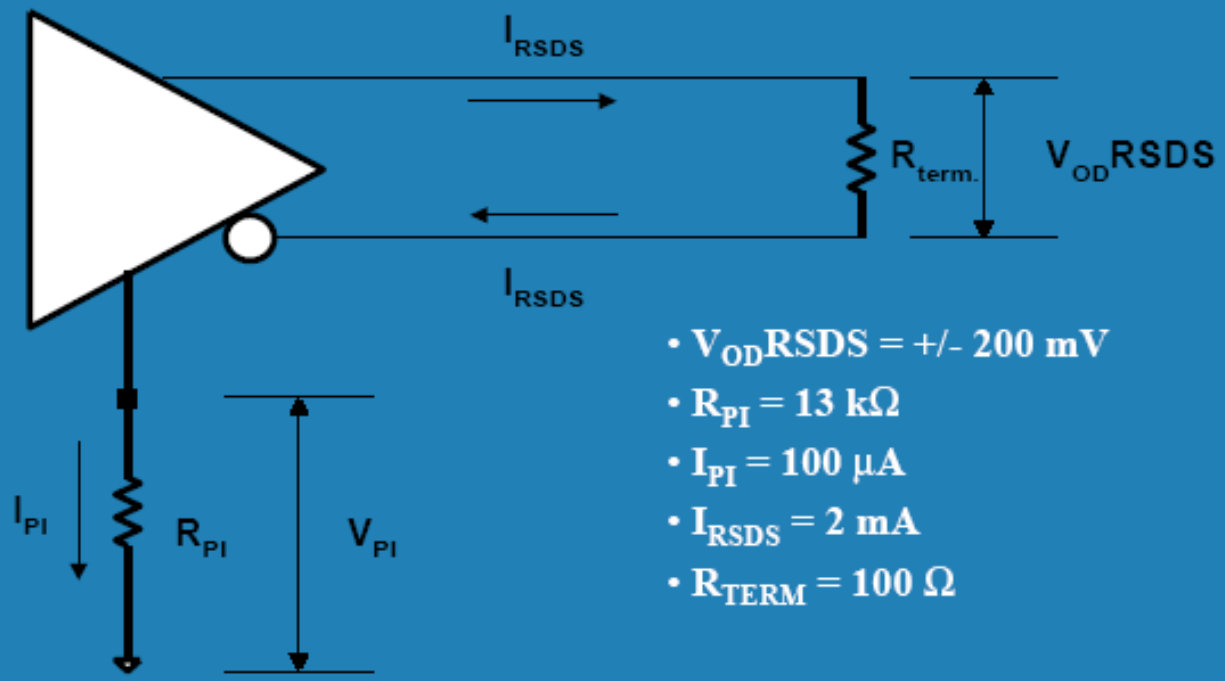
差動訊號與TTL相比具有低EMI與功率損耗之優點，因爲RSDS的電壓擺幅只有200mV，比LVDS更低。



RSDS Bus Data Mapping

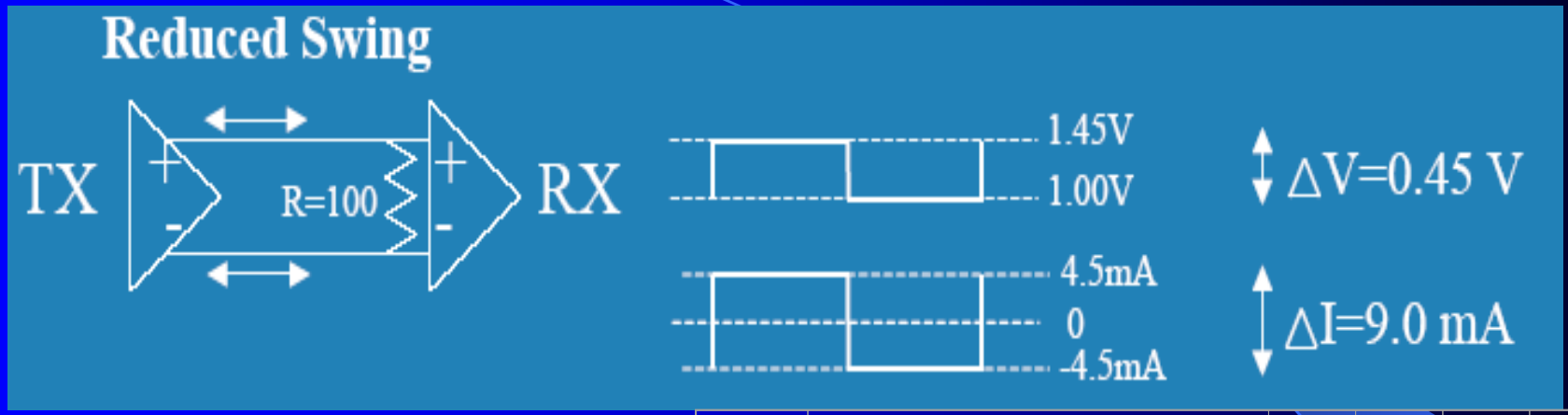
RSDS工作方式

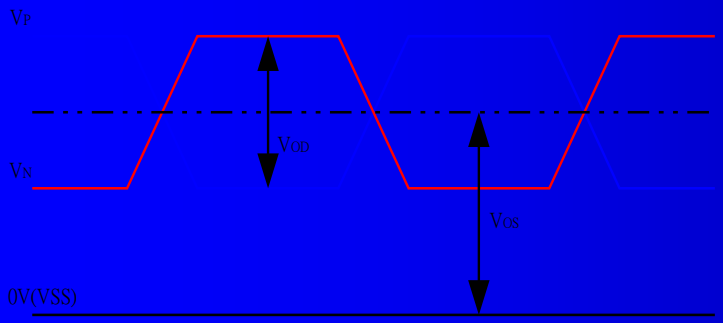
- $I_{RSDS} = 20 \times I_{PI}$ $(I_{PI} = V_{PI} / R_{PI})$
- V_{PI} = 1.3 V +/- 5 % Fixed.



- $V_{OD}RSDS$ = +/- 200 mV
- R_{PI} = 13 kΩ
- I_{PI} = 100 μA
- I_{RSDS} = 2 mA
- R_{TERM} = 100 Ω

RSDS 規格





VP: Positive single end signal of RSDS output buffer.

VN: Negative single end signal of RSDS output buffer.

Symbol	Description	Min	Typ	Max	Units
VDD	Supply Voltage	3.0	3.3	3.6	V
VOD	Differential output voltage (RL = 100 Ohm; Cr 4E [7]=1)	100	200	400	mV
VOS	Common mode Voltage.	1.1	1.3	1.5	V
Trf	Transition time (CL = 5 pF, load between N and P channels)		1		ns
Skew	Skew between different data channels			500	ps

RSDS之優點

RSDS（Reduced swing differential signaling）是由美國國家半導體（National Semiconductor Corp.）推廣的一種平面顯示器的傳輸介面。相較於現在常用的3.3Volt的數位傳輸介面，有著減低EMI（Electro-Magnetic Interference）與降低耗電的優點。

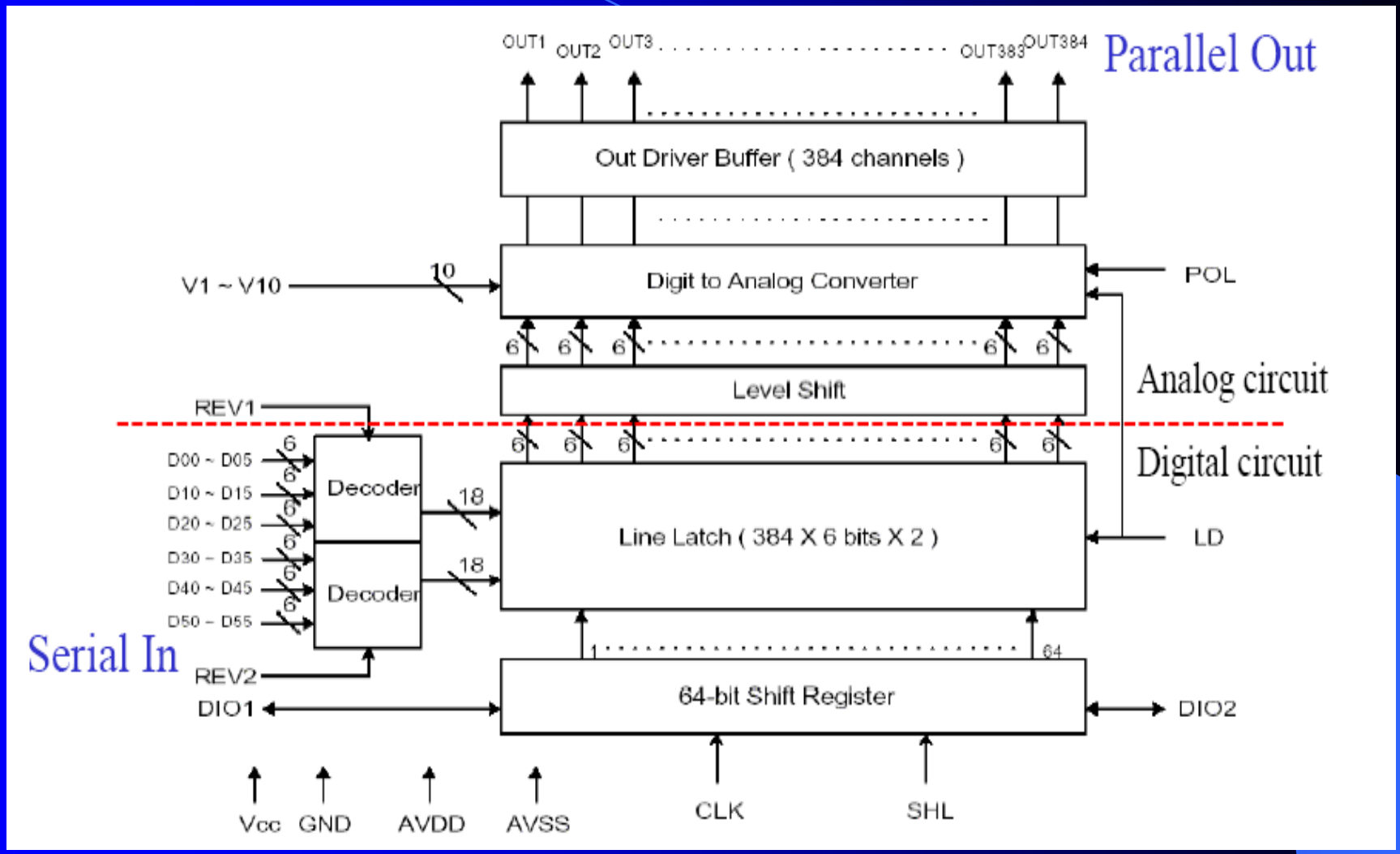
differential pair input降低EMI

跟現在常用的介面比較，爲什麼RSDS可以減低EMI呢？最主要的原因是RSDS介面使用的是differential input，所以輸入介面的信號之電壓振幅比起3.3Volt小很多，最小可到達0.2Volt，如圖5所述。我們知道EMI的發生主要是由於電路中所流動電流大小的變化，所形成的電磁輻射的結果。它會隨著電流變化的大小程度與變化頻率而增加，所以當輸入的電壓振幅變小時，電流的變化幅度也會減少，所以EMI的程度也會減低。

除了由於電流變化幅度降低而減低EMI之外，由於RSDS介面是使用differential pair input，這一對輸入信號線，其輸入信號是反向的。所以信號線上所流通的電流也恰好反向。一般傳統的CMOS輸入信號是一條一條線的，每一條線上流通的電流會各自輻射出EMI來，但是differential pair的兩條線由於電流變化（DI）大小相等且反向，其所輻射出來的EMI會因爲彼此互相作用而抵消掉大部份。請見圖5。因此，從剛才提過的 ，我們可以得知藉由電壓振幅的減小與differential輸入信號的設計，RSDS的傳輸介面可大幅減低EMI的程度。在此同時，由於EMI的降低，也可以節省一般在解EMI時，所需額外多加的零件與電路，如此一來總成本也可以降低。

此外，RSDS除了可以減少EMI外，比起傳統的CMOS輸入介面，RSDS的輸入介面在傳輸過程中所形成的耗電，也能大幅減少。因爲依照功率消耗的公式，功率的消耗正比於電壓的平方，既然電壓振幅由3.3volt降到 0.2volt，稍微計算一下，可得知在信號傳輸的過程中，可節省下接近99.6%的功率消耗。當然，這是依照數學公式最理想的狀況 ，在實際上並不會節省這麼多。

訊號系統


OUT1
OUT2
OUT3
OUT383
OUT384
Parallel Out
Out Driver Buffer (384 channels)
V1 ~ V10
10
Digit to Analog Converter
POL
6
Level Shift
Analog circuit
REV1
Digital circuit
D00 ~ D05
D10 ~ D15
D20 ~ D25
D30 ~ D35
D40 ~ D45
D50 ~ D55
Decoder
Decoder
18
18
Line Latch (384 X 6 bits X 2)
LD
Serial In
REV2
DIO1
1
64
64-bit Shift Register
DIO2
Vcc
GND
AVDD
AVSS
CLK
SHL

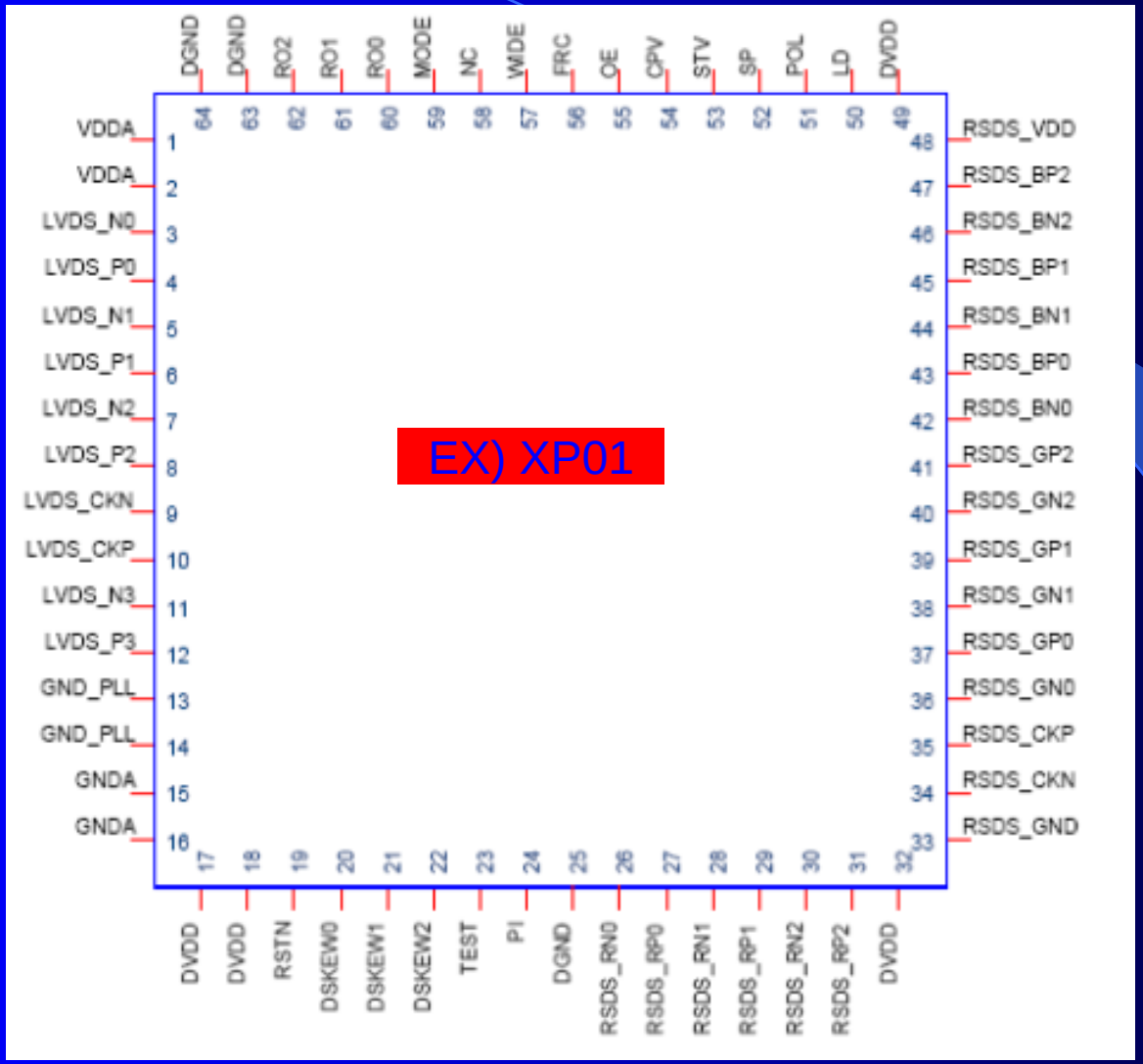
ASIC

Application Specific IC (又稱 T-con Timing controller)

功能

- 接收TTL或LVDS訊號與時脈
- 送出TTL或RSDS訊號與時脈
- 控制各組時序訊號輸出

ASIC


EX) XP01
1 VDDA
2 VDDA
3 LVDS_N0
4 LVDS_P0
5 LVDS_N1
6 LVDS_P1
7 LVDS_N2
8 LVDS_P2
9 LVDS_CKN
10 LVDS_CKP
11 LVDS_N3
12 LVDS_P3
13 GND_PLL
14 GND_PLL
15 GNDA
16 GNDA
17 DVDD
18 DVDD
19 RSTN
20 DSKEW0
21 DSKEW1
22 DSKEW2
23 TEST
24 PI
25 DGND
26 RSDS_RN0
27 RSDS_RP0
28 RSDS_RN1
29 RSDS_RP1
30 RSDS_RN2
31 RSDS_RP2
32 DVDD
33 RSDS_GND
34 RSDS_CKN
35 RSDS_CKP
36 RSDS_GN0
37 RSDS_GP0
38 RSDS_GN1
39 RSDS_GP1
40 RSDS_GN2
41 RSDS_GP2
42 RSDS_BN0
43 RSDS_BP0
44 RSDS_BN1
45 RSDS_BP1
46 RSDS_BN2
47 RSDS_BP2
48 RSDS_VDD
49 DVDD
50 LD
51 POL
52 SP
53 STV
54 CPV
55 OE
56 FRC
57 WIDE
58 NC
59 MODE
60 RO0
61 RO1
62 RO2
63 DGND
64 DGND

ASIC時脈順序

STH出現star pulse，告知Source Driver可以開始接收第一列pixel的資料(RGBP/N)並latch住，之後TP信號上緣讀取RVS(控制極性的變換方式，決定輸出電壓爲正極性或負極性)，下緣將整列之DATA同時寫入面板。同時STV信號也告知Gate Driver可以開始依序啓動每一列所有之TFT。此後則依照CPV信號開啓每一列之TFT。Source Driver則依STH信號、TP信號、RVS信號來給予每列每個像素適當之像素電壓。

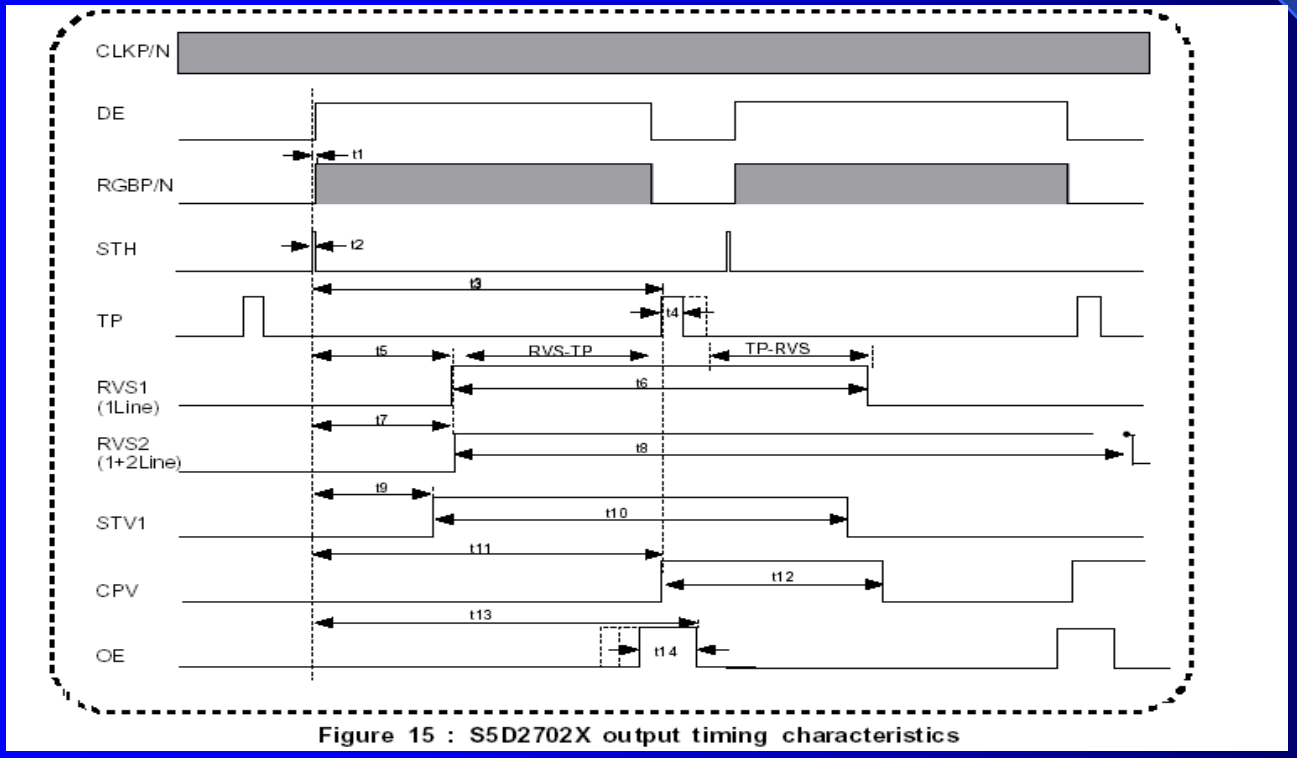


Figure 15 : S5D2702X output timing characteristics

Source Driver IC (S-IC)

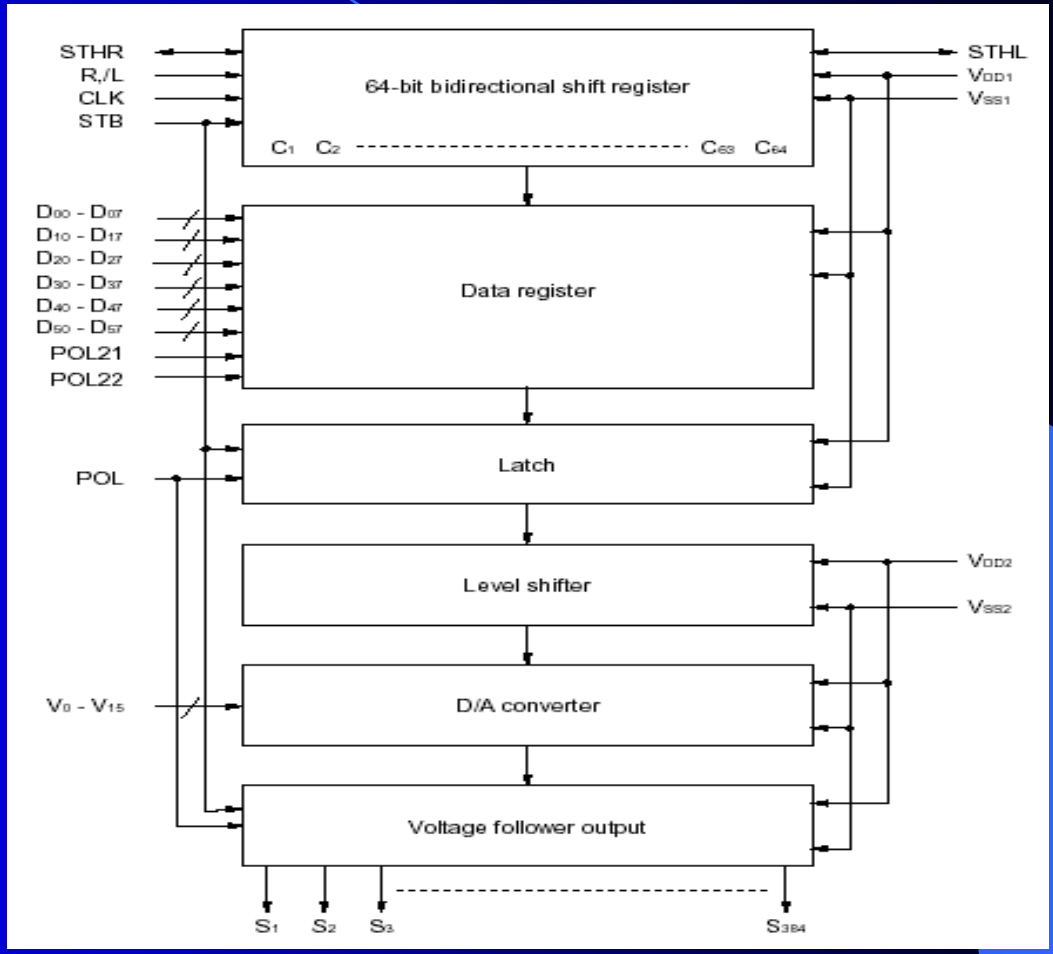
S側驅動IC

- 包裝成Taping，再捲成Reel出貨
- 廠內經金型裁切並本壓於Panel與PWB

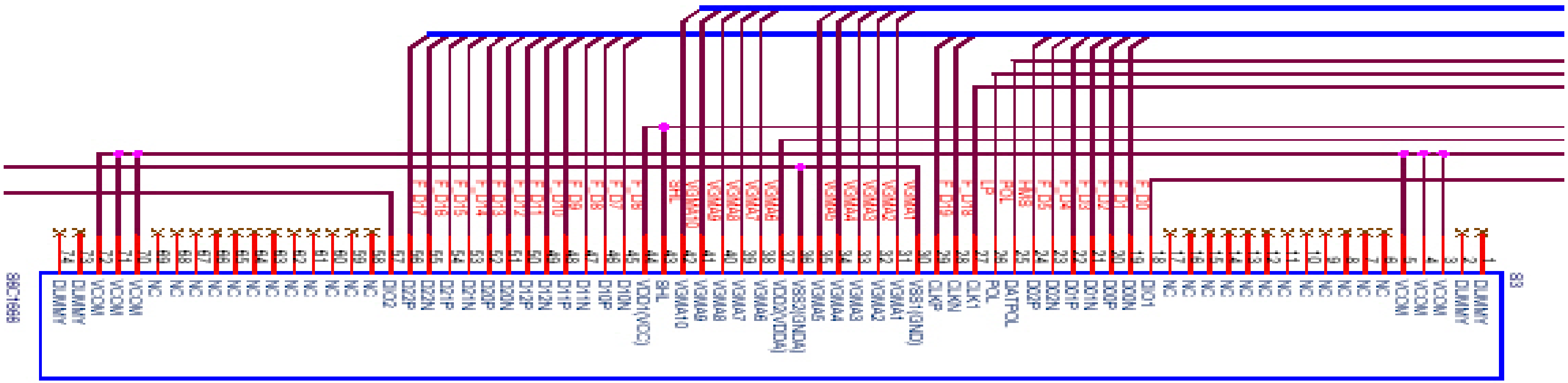
Source Driver部分Pin Assignments

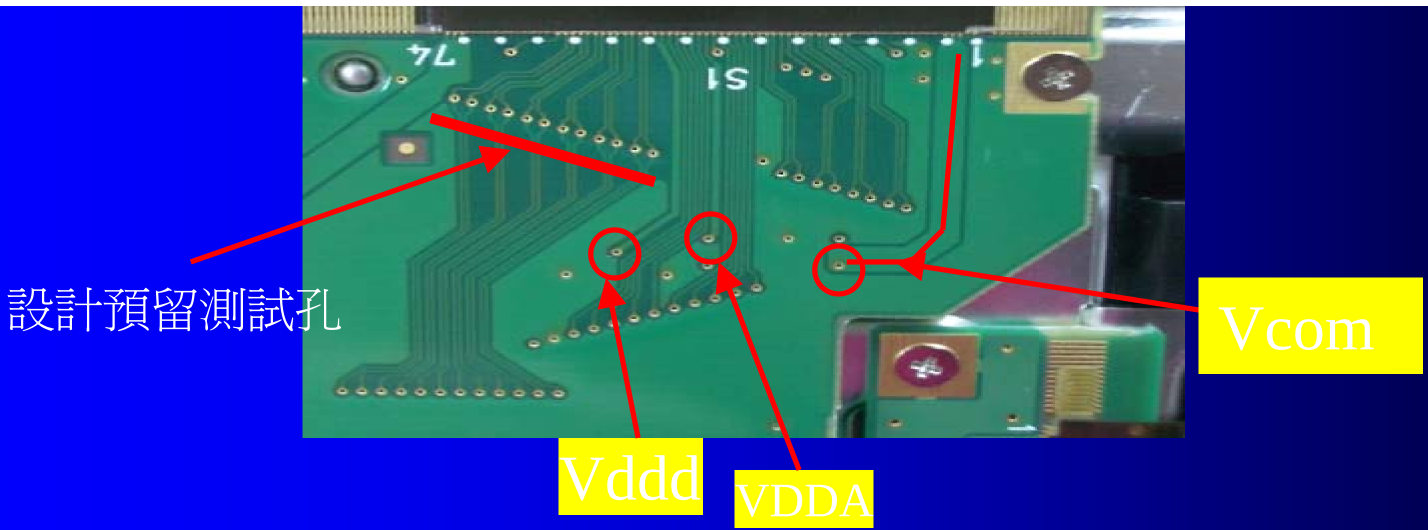
(EX. 17EA)

- STHL/R: 啓動階調訊號接收
- R/L: 控制IC輸出左右順序
- CLK: 時脈
- TP:啓動IC輸出電壓
- RVS to POL: IC輸出之高/低電壓控制---Flicker輸出方式選擇
- VDD1: IC電源
- VSS1, VSS2: GND
- VDD2: 階調電壓最大值
- V0~V15: 階調電壓
- Dx0~Dx7:訊號
- Sx: S-IC輸出



S-IC 對照圖

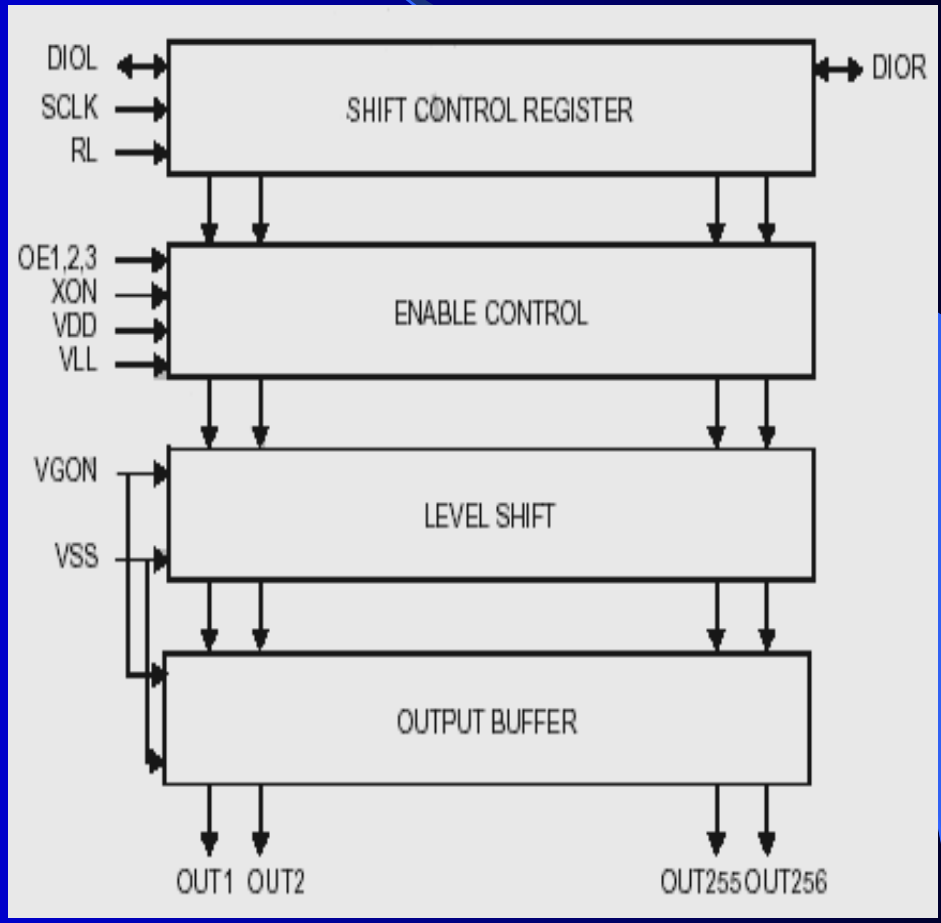




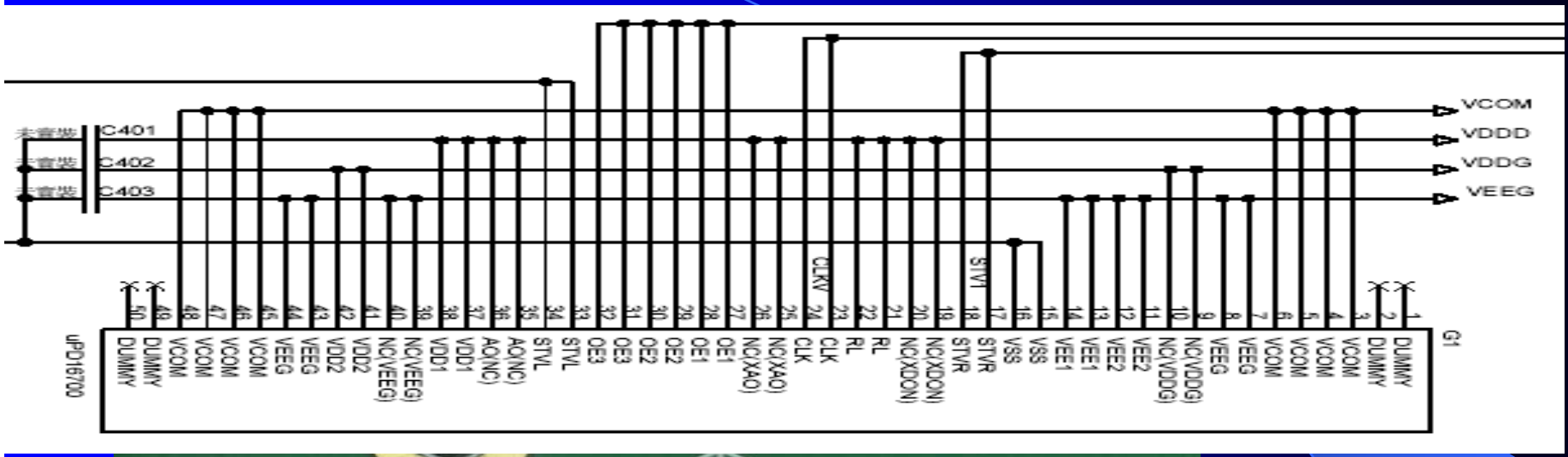
Gate Driver IC (G-IC)

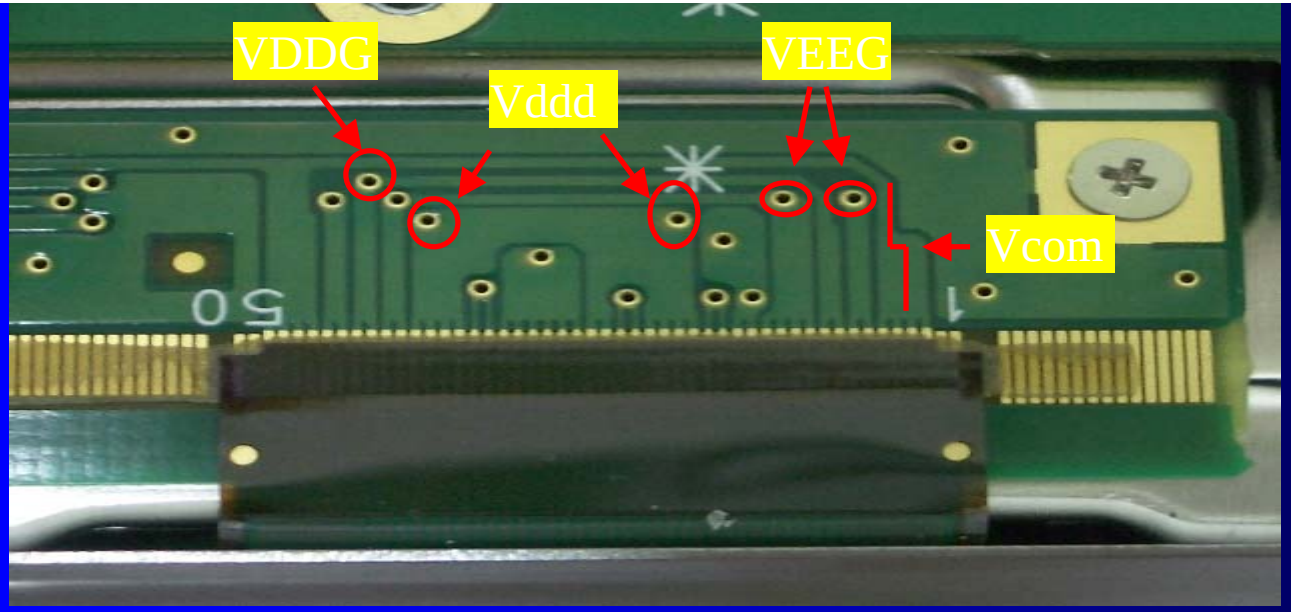
Gate Driver部分Pin Assignments

- DIOL/R: 啓動IC
- R/L: 控制IC輸出左右順序
- SCLK: 時脈
- OE1,2,3: 強迫G-IC輸出VLL
- XON: 強迫G-IC輸出VGON
- VDD: G-IC電源
- VLL: VEEG
- VSS: 接地
- VGON: VDDG
- OUTx: G-IC輸出



G-IC 對照圖


未實裝 C401
未實裝 C402
未實裝 C403
VCOM
VDDD
VDDG
VEEG
uPD16700
DUMMY
DUMMY
VCOM
VCOM
VCOM
VCOM
VEEG
VEEG
VDD2
VDD2
NC(VEEG)
NC(VEEG)
VDD1
VDD1
AO(NC)
AO(NC)
STVL
STVL
OE3
OE3
OE2
OE2
OE1
OE1
NC(XAO)
NC(XAO)
CLK
CLK
RL
RL
NC(XDON)
NC(XDON)
STVR
STVR
VSS
VSS
VEE1
VEE1
VEE2
VEE2
NC(VDDG)
NC(VDDG)
VEEG
VEEG
VCOM
VCOM
VCOM
VCOM
VCOM
DUMMY
DUMMY
G1


VDDG
Vddd
VEEG
Vcom
50
1

PWB

Printed Wire Board

- 將輸入電源轉成所需的電壓〈6項基本電壓〉

  Vin　: 3.3V 、5.0V、12V …基本輸入電源

  VDDD: 3.3V, 各IC所需的電源電壓, S-IC, G-IC, ASIC, 電源IC, …

  VDDG: 18V, 24V …TFT元件打開的Gate電壓, 給G-IC使用

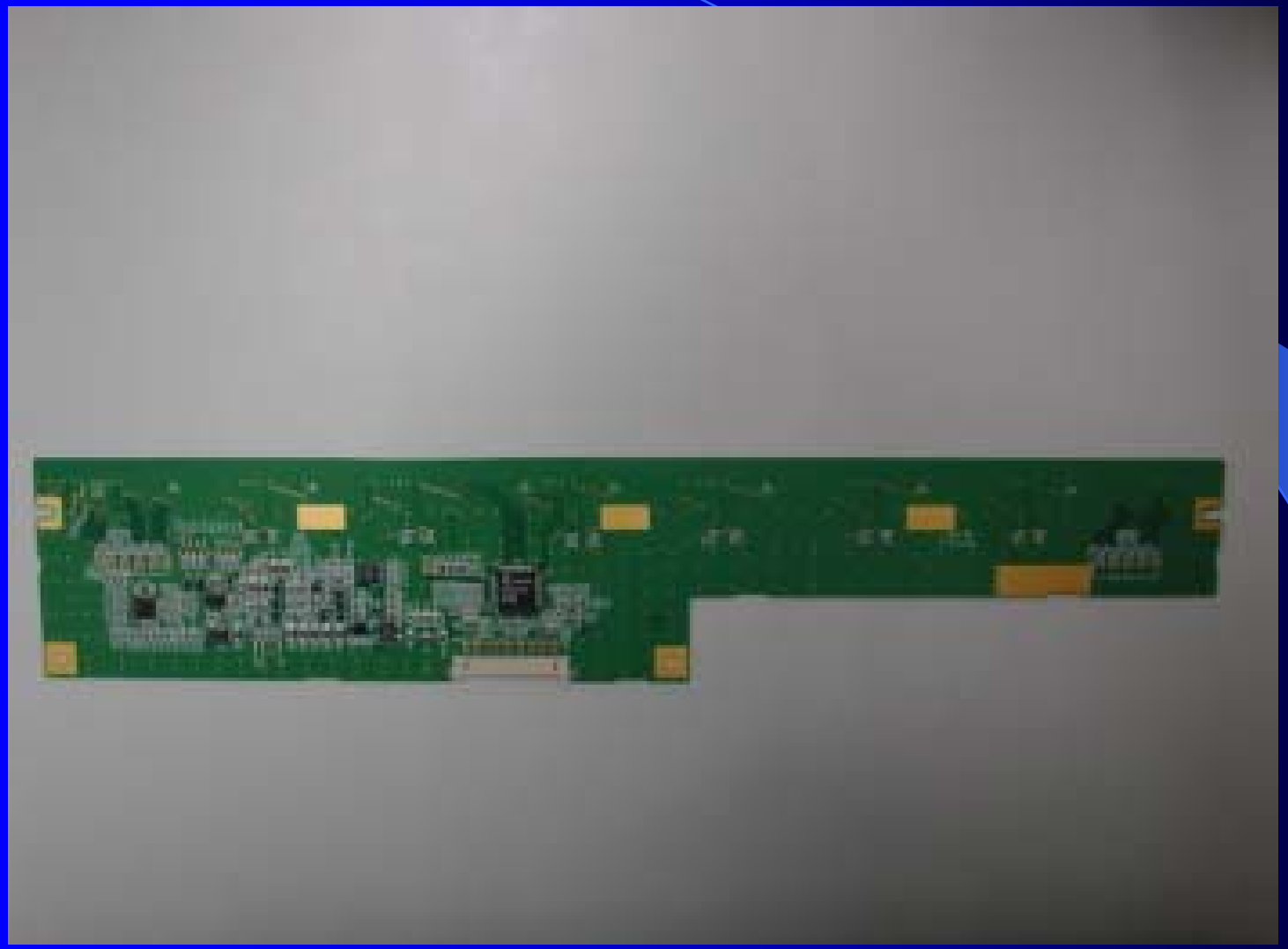
  VEEG: -6V, TFT元件關閉的Gate電壓, 給G-IC使用

  VDDA: 9.2V, 階調電壓最大值, 再轉成各階調所需的電壓, 給S-IC使用

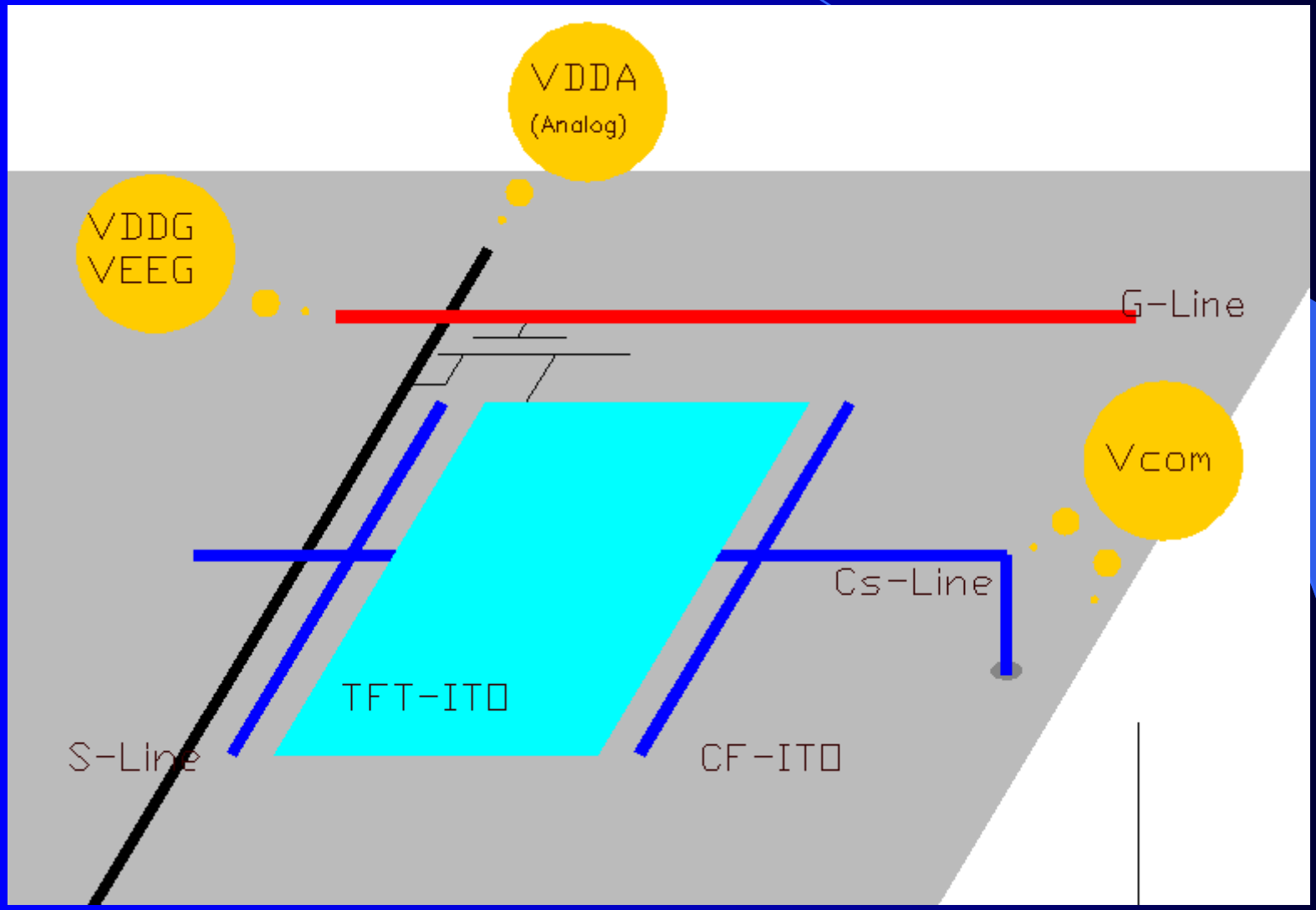
  Vcom: 3.6V, 基準共通電壓, 和階調電壓的差值來驅動液晶, 給面板使用

　　爲了不讓電源瞬間的開與關，而引起內部元件突然承受過大的電流，而破壞IC，因此在Turn_On或Turn_Off時各電壓的啓動順序必須符合先後順序。

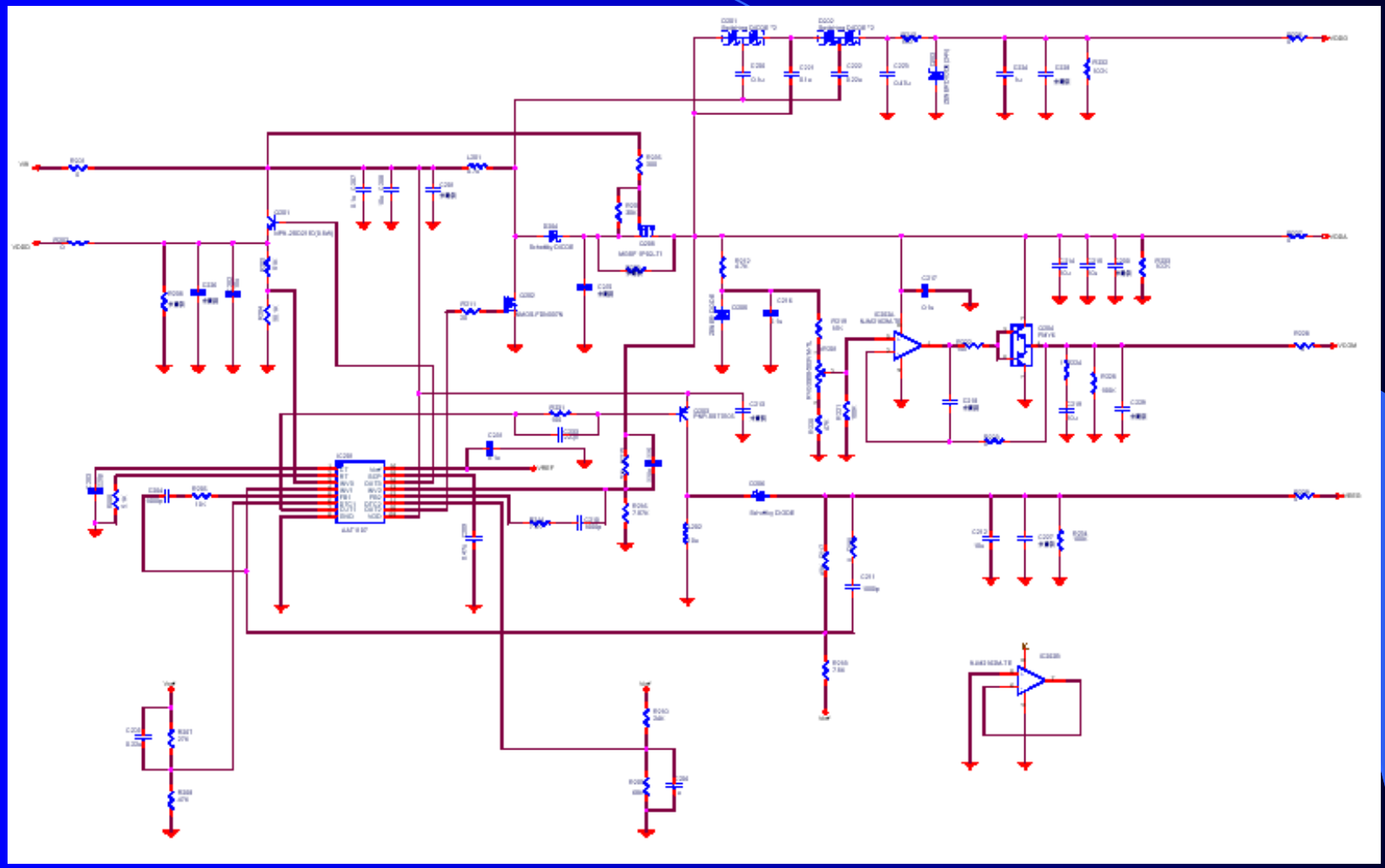
S-PWB 外観



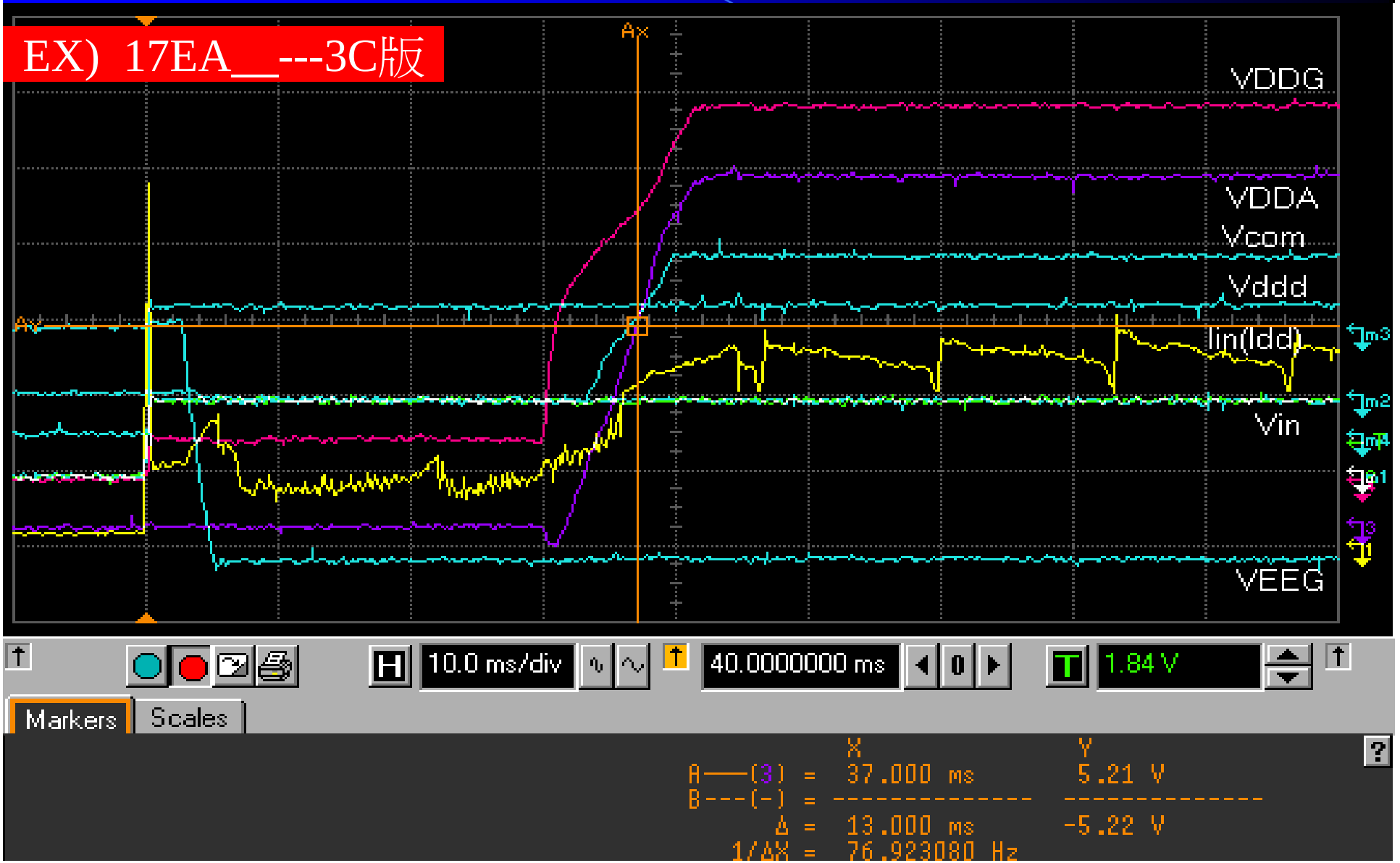
電源示意圖



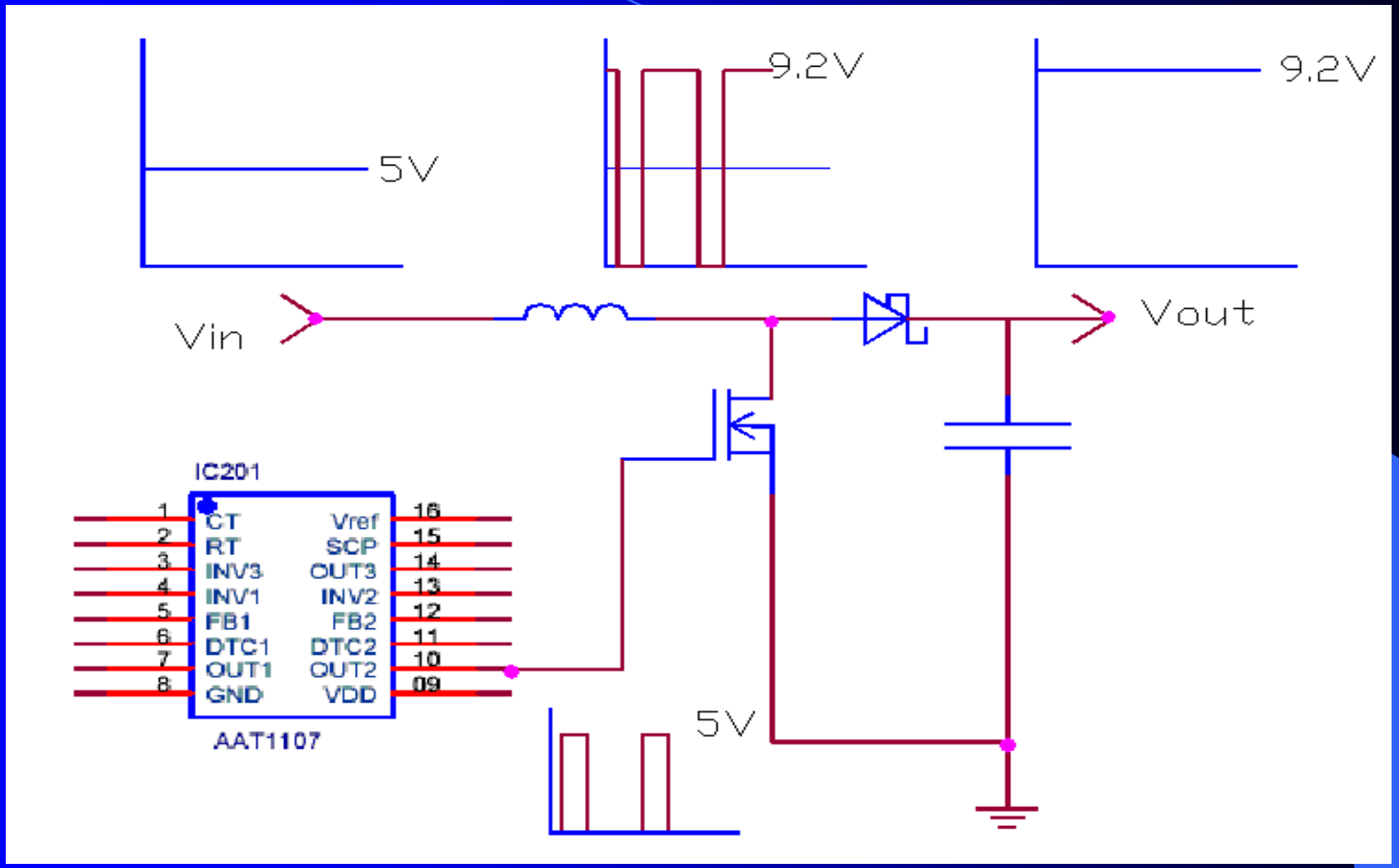
DC-DC 電源電路



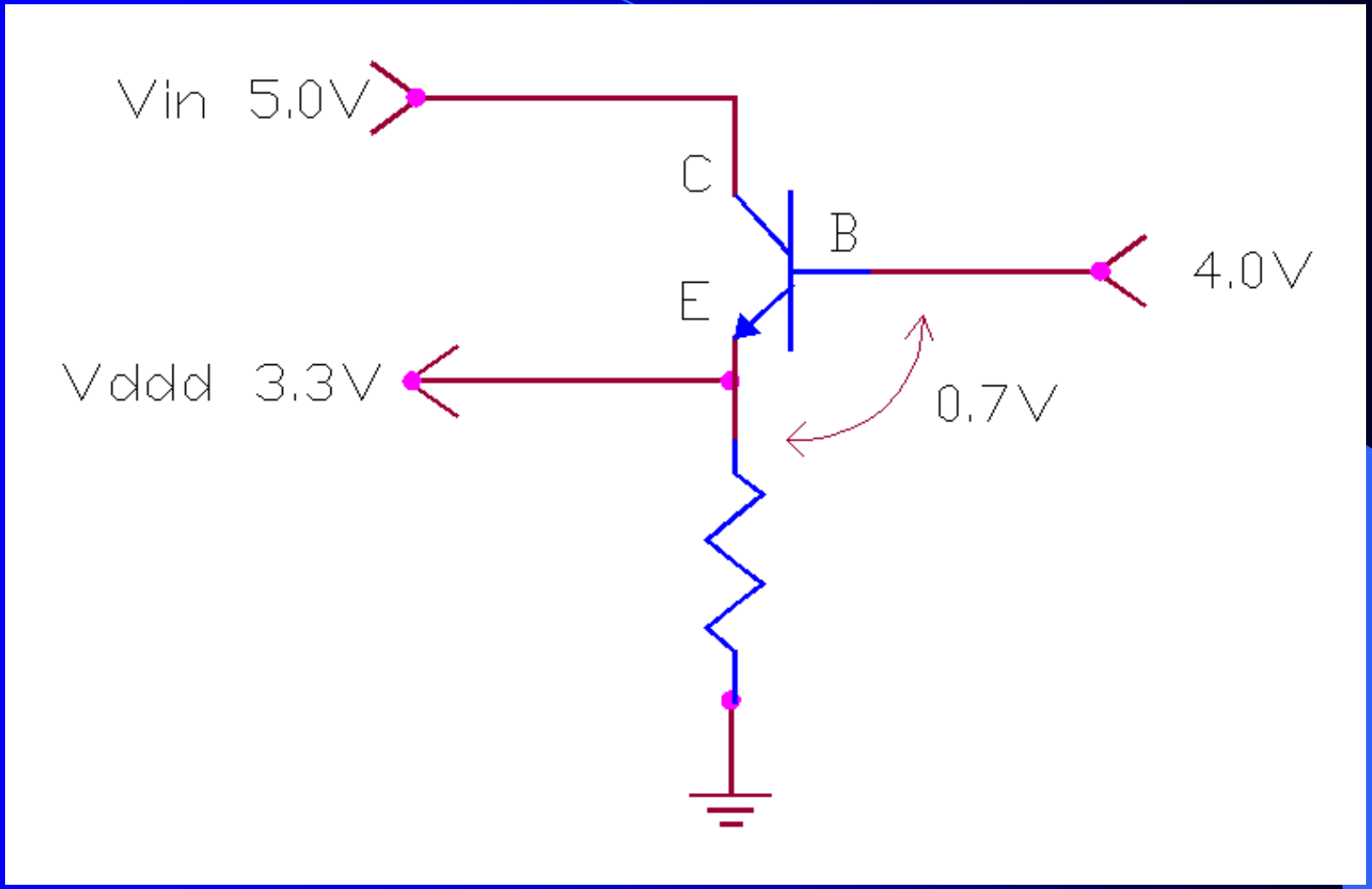
Power On Sequence 開機時序



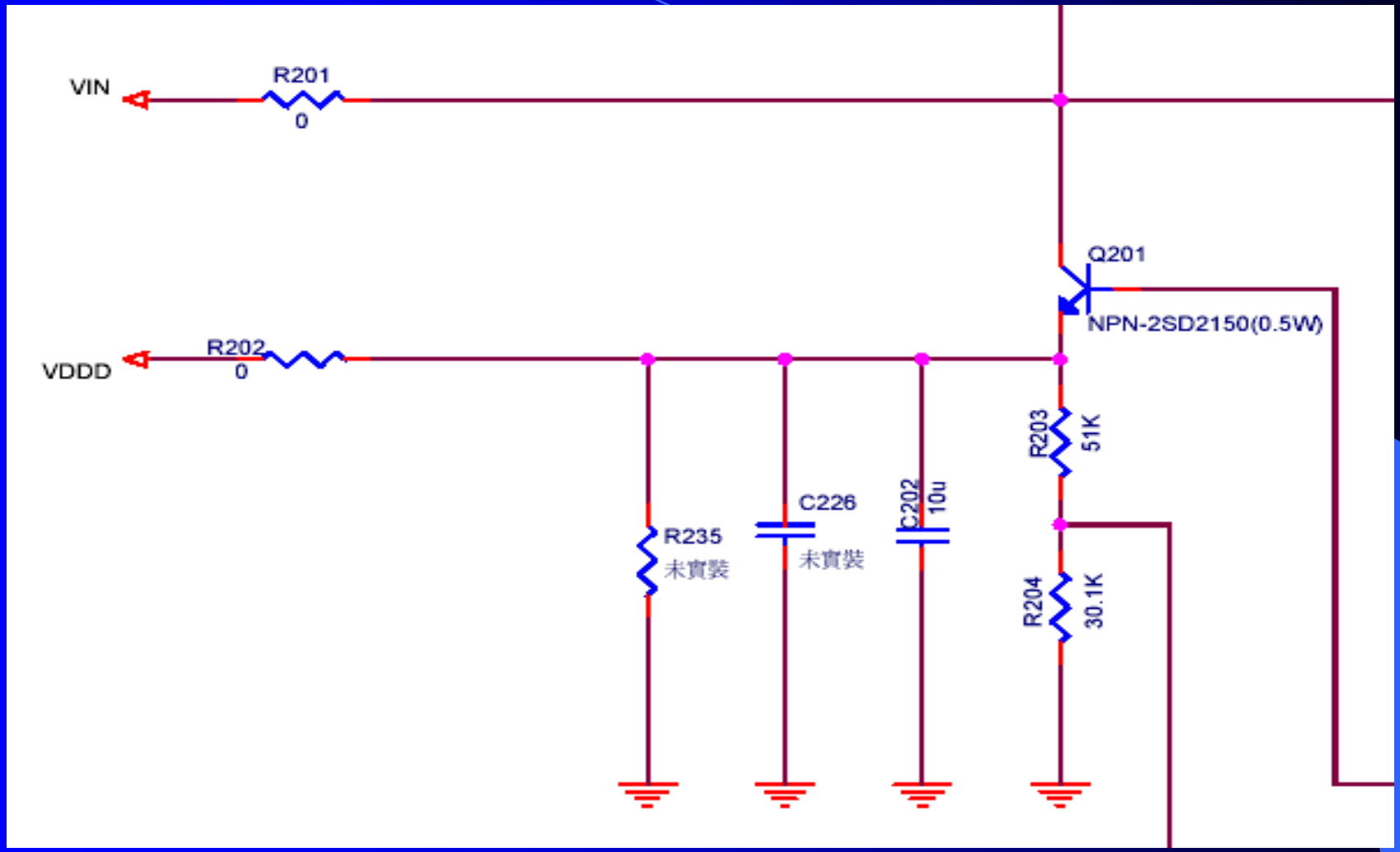
倍壓整流迴路


5V
9.2V
9.2V
Vin
Vout
IC201
1 CT
2 RT
3 INV3
4 INV1
5 FB1
6 DTC1
7 OUT1
8 GND
Vref 16
SCP 15
OUT3 14
INV2 13
FB2 12
DTC2 11
OUT2 10
VDD 09
AAT1107
5V

電晶體偏壓電路

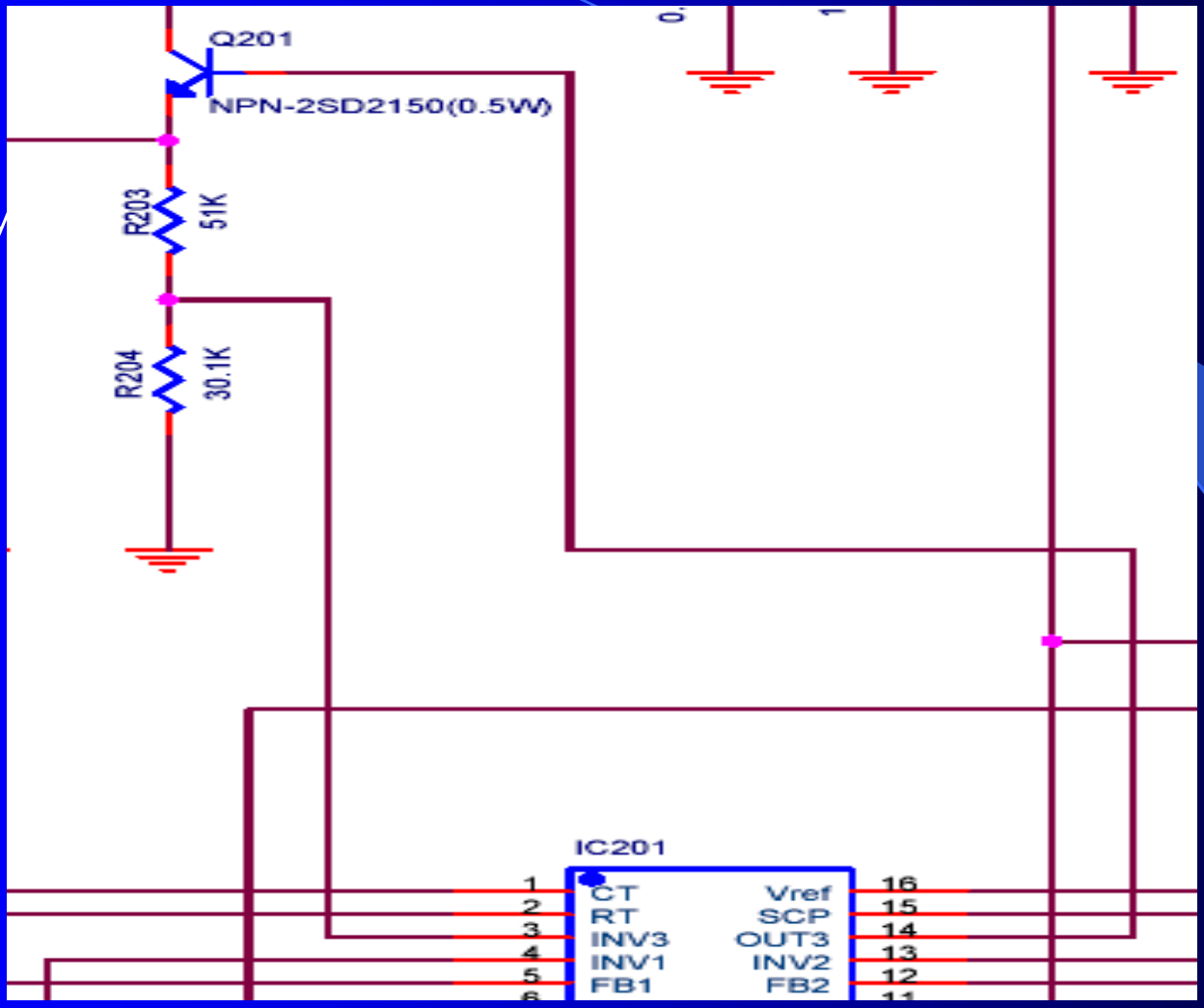


Vddd

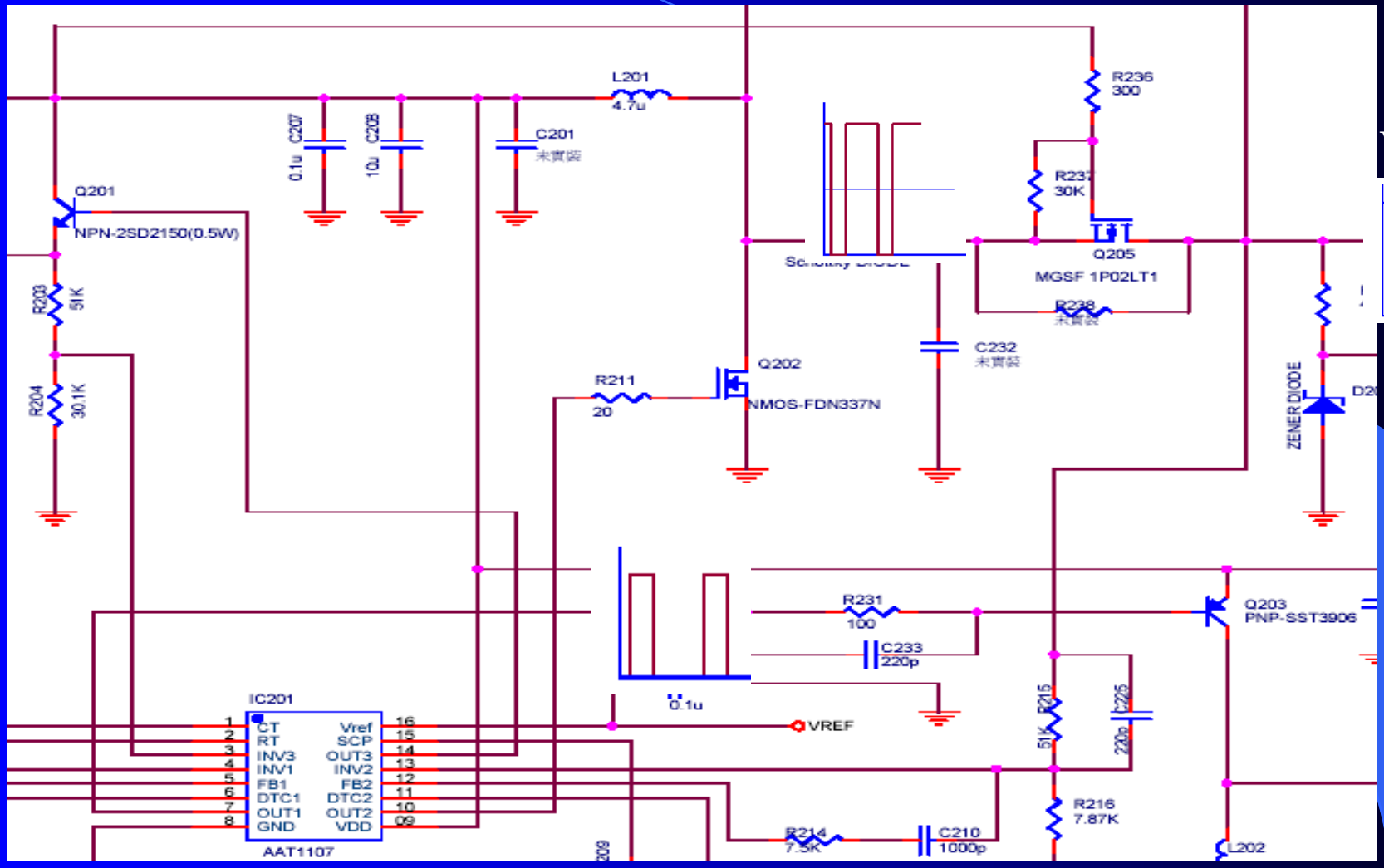

VIN
R201
0
Q201
NPN-2SD2150(0.5W)
VDDD
R202
0
R203
51K
R235
未實裝
C226
未實裝
C202
10u
R204
30.1K

Vddd

3.3V

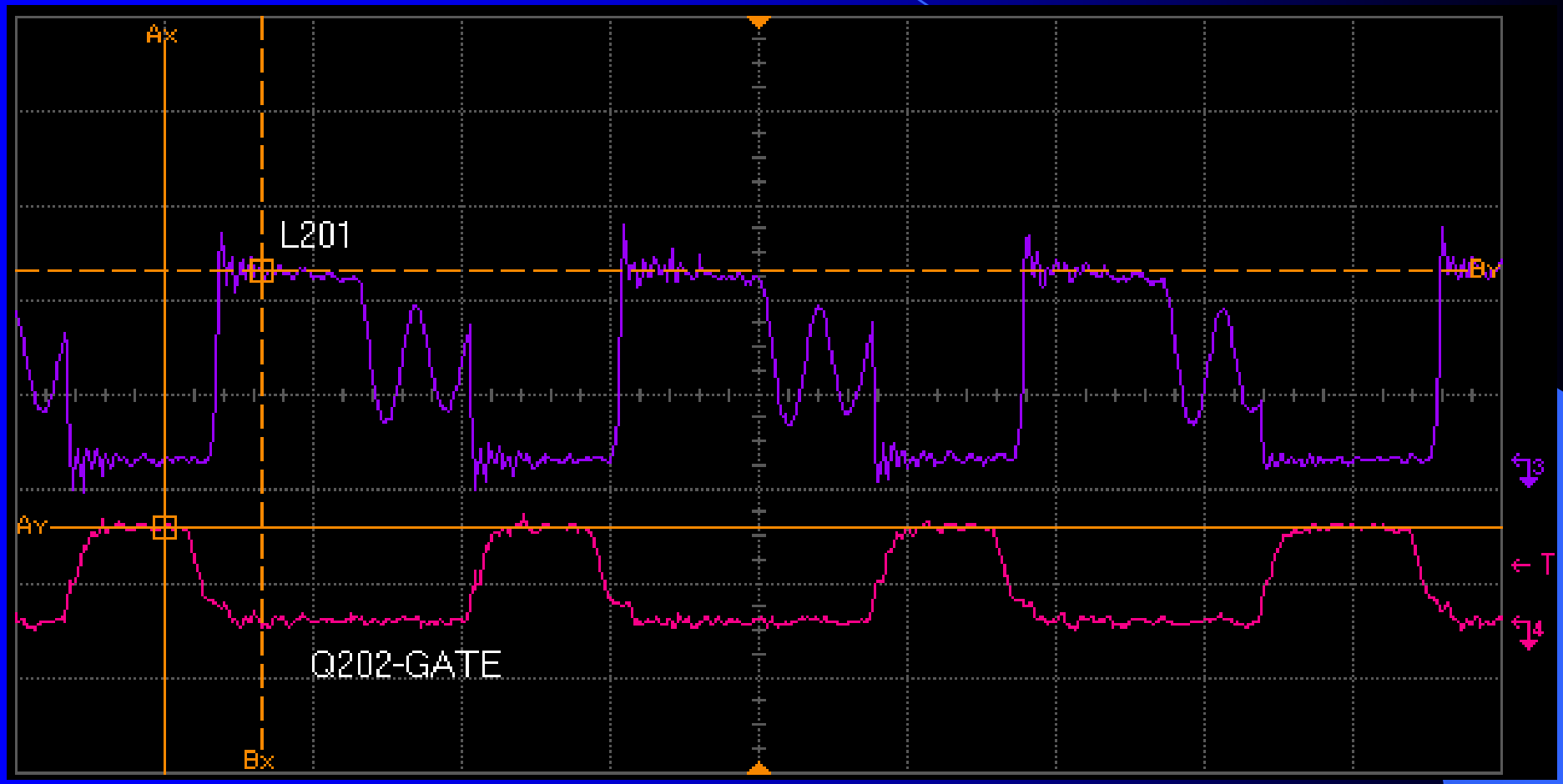

Q201
NPN-2SD2150(0.5W)
R203
51K
R204
30.1K
IC201
1 CT
2 RT
3 INV3
4 INV1
5 FB1
Vref 16
SCP 15
OUT3 14
INV2 13
FB2 12

VDDA

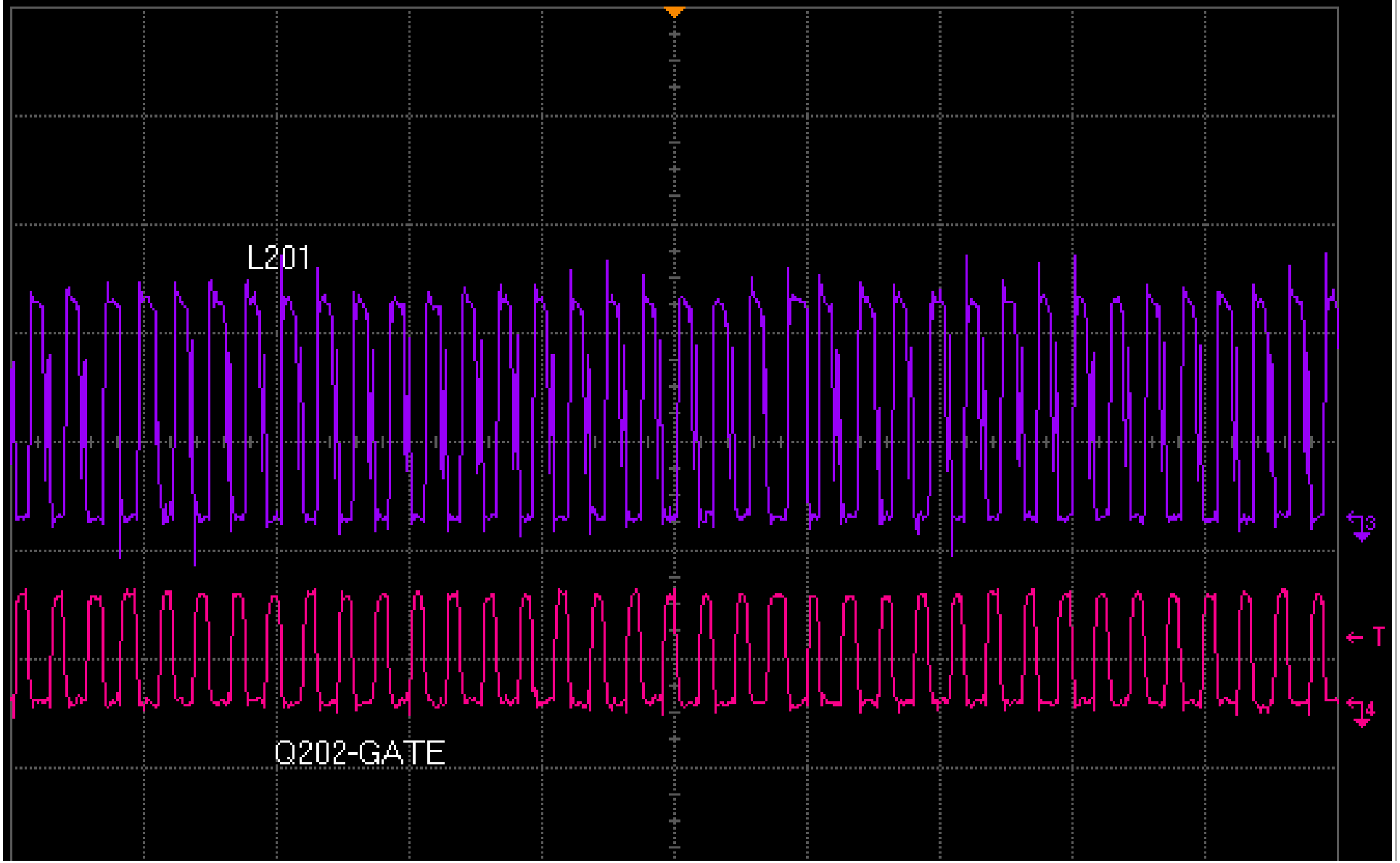

L201
4.7u
C207
0.1u
C206
10u
C201
未實裝
R236
300
R237
30K
Q205
MGSF 1P02LT1
R238
未實裝
C232
未實裝
Q201
NPN-2SD2150(0.5W)
R203
51K
R204
30.1K
R211
20
Q202
NMOS-FDN337N
ZENER DIODE
R231
100
C233
220p
Q203
PNP-SST3906
0.1u
VREF
IC201
CT
RT
INV3
INV1
FB1
DTC1
OUT1
GND
Vref
SCP
OUT3
INV2
FB2
DTC2
OUT2
VDD
AAT1107
R214
7.5K
C210
1000p
R215
51K
C225
220p
R216
7.87K
L202

VDDA

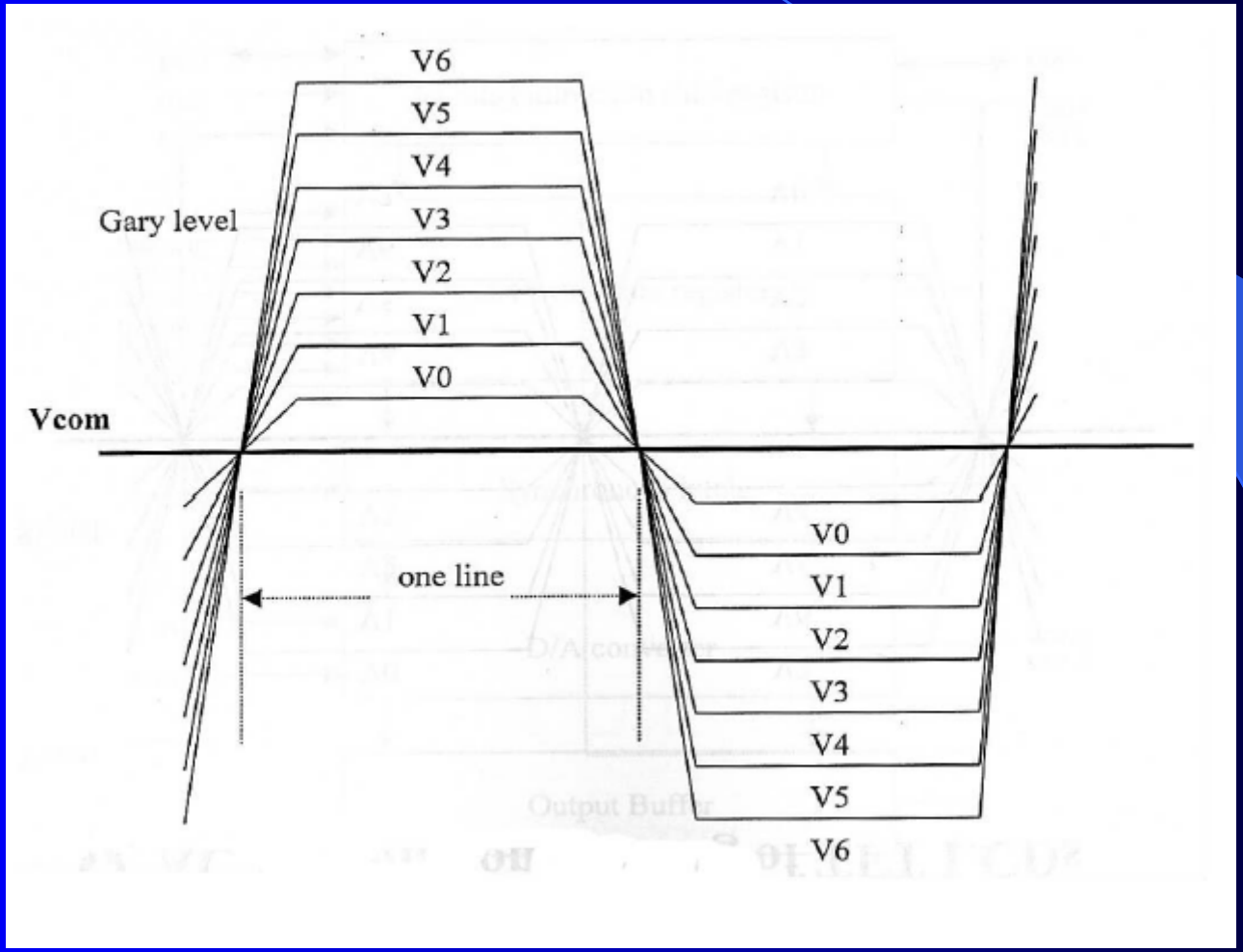
L201 vs Q202 Gate



L201



VDDA轉成階調電壓



階調電壓分壓表

Table 2. Relationship between Input Data and Output Voltage Value

Input Data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output Voltage
00H	0	0	0	0	0	0	VH0	VGMA1
01H	0	0	0	0	0	1	VH1	VGMA1+(VGMA2-VGMA1) × 1000/7000
02H	0	0	0	0	1	0	VH2	VGMA1+(VGMA2-VGMA1) × 1830/7000
03H	0	0	0	0	1	1	VH3	VGMA1+(VGMA2-VGMA1) × 2500/7000
04H	0	0	0	1	0	0	VH4	VGMA1+(VGMA2-VGMA1) × 3170/7000
05H	0	0	0	1	0	1	VH5	VGMA1+(VGMA2-VGMA1) × 3670/7000
06H	0	0	0	1	1	0	VH6	VGMA1+(VGMA2-VGMA1) × 4170/7000
07H	0	0	0	1	1	1	VH7	VGMA1+(VGMA2-VGMA1) × 4670/7000
08H	0	0	1	0	0	0	VH8	VGMA1+(VGMA2-VGMA1) × 5000/7000
09H	0	0	1	0	0	1	VH9	VGMA1+(VGMA2-VGMA1) × 5330/7000
0AH	0	0	1	0	1	0	VH10	VGMA1+(VGMA2-VGMA1) × 5620/7000
0BH	0	0	1	0	1	1	VH11	VGMA1+(VGMA2-VGMA1) × 5910/7000
0CH	0	0	1	1	0	0	VH12	VGMA1+(VGMA2-VGMA1) × 6160/7000
0DH	0	0	1	1	0	1	VH13	VGMA1+(VGMA2-VGMA1) × 6400/7000
0EH	0	0	1	1	1	0	VH14	VGMA1+(VGMA2-VGMA1) × 6600/7000
0FH	0	0	1	1	1	1	VH15	VGMA1+(VGMA2-VGMA1) × 6800/7000
10H	0	1	0	0	0	0	VH16	VGMA2
11H	0	1	0	0	0	1	VH17	VGMA2+(VGMA3-VGMA2) × 170/2315
12H	0	1	0	0	1	0	VH18	VGMA2+(VGMA3-VGMA2) × 340/2315
13H	0	1	0	0	1	1	VH19	VGMA2+(VGMA3-VGMA2) × 510/2315
14H	0	1	0	1	0	0	VH20	VGMA2+(VGMA3-VGMA2) × 680/2315
15H	0	1	0	1	0	1	VH21	VGMA2+(VGMA3-VGMA2) × 820/2315
16H	0	1	0	1	1	0	VH22	VGMA2+(VGMA3-VGMA2) × 960/2315
17H	0	1	0	1	1	1	VH23	VGMA2+(VGMA3-VGMA2) × 1100/2315
18H	0	1	1	0	0	0	VH24	VGMA2+(VGMA3-VGMA2) × 1240/2315
19H	0	1	1	0	0	1	VH25	VGMA2+(VGMA3-VGMA2) × 1380/2315
1AH	0	1	1	0	1	0	VH26	VGMA2+(VGMA3-VGMA2) × 1520/2315
1BH	0	1	1	0	1	1	VH27	VGMA2+(VGMA3-VGMA2) × 1660/2315
1CH	0	1	1	1	0	0	VH28	VGMA2+(VGMA3-VGMA2) × 1800/2315
1DH	0	1	1	1	0	1	VH29	VGMA2+(VGMA3-VGMA2) × 1940/2315
1EH	0	1	1	1	1	0	VH30	VGMA2+(VGMA3-VGMA2) × 2065/2315
1FH	0	1	1	1	1	1	VH31	VGMA2+(VGMA3-VGMA2) × 2190/2315

NOTE: VDD2>VGMA1>VGMA2>VGMA3>VGMA4>VGMA5

階調電壓(Gamma 電壓)

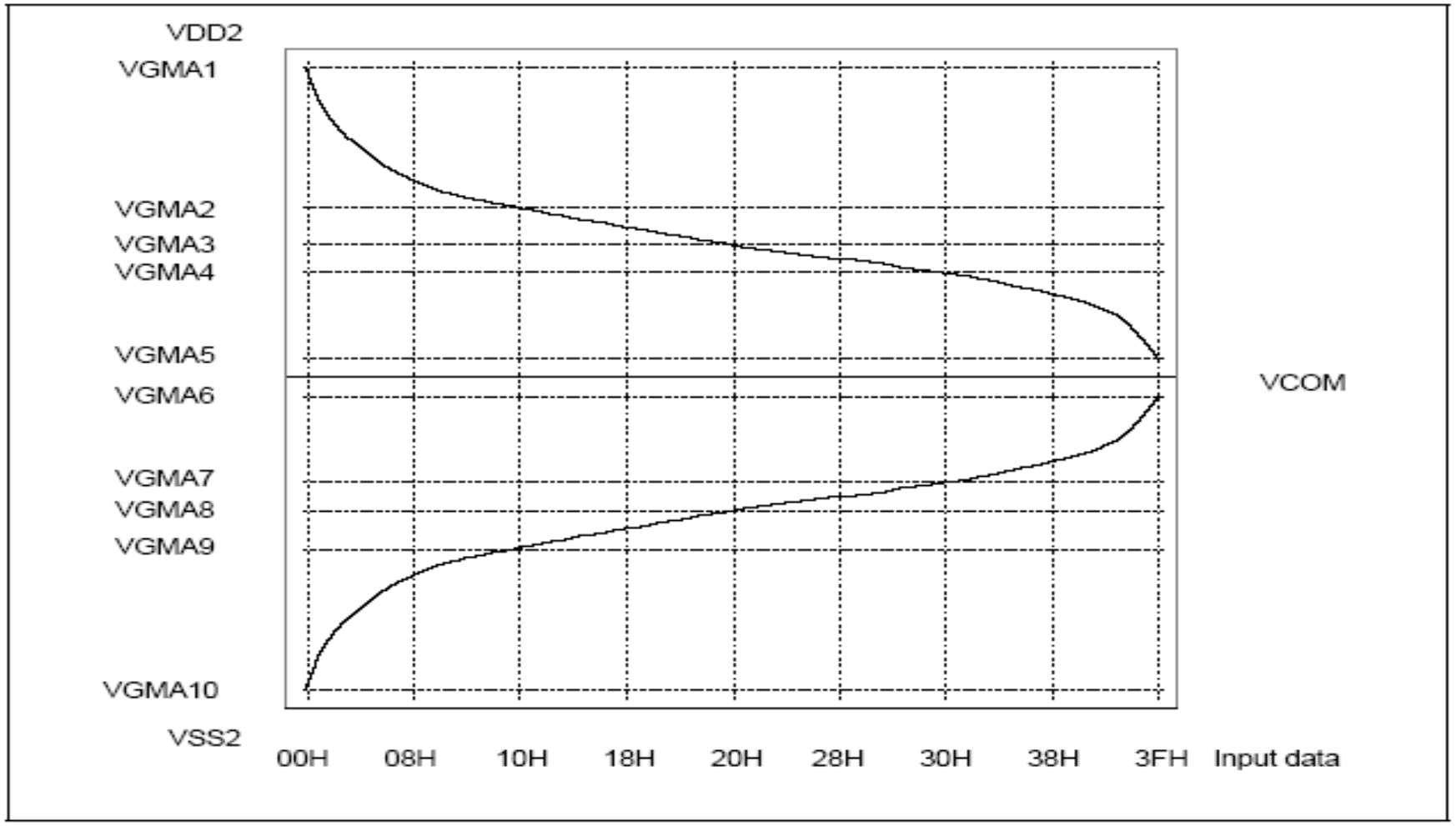
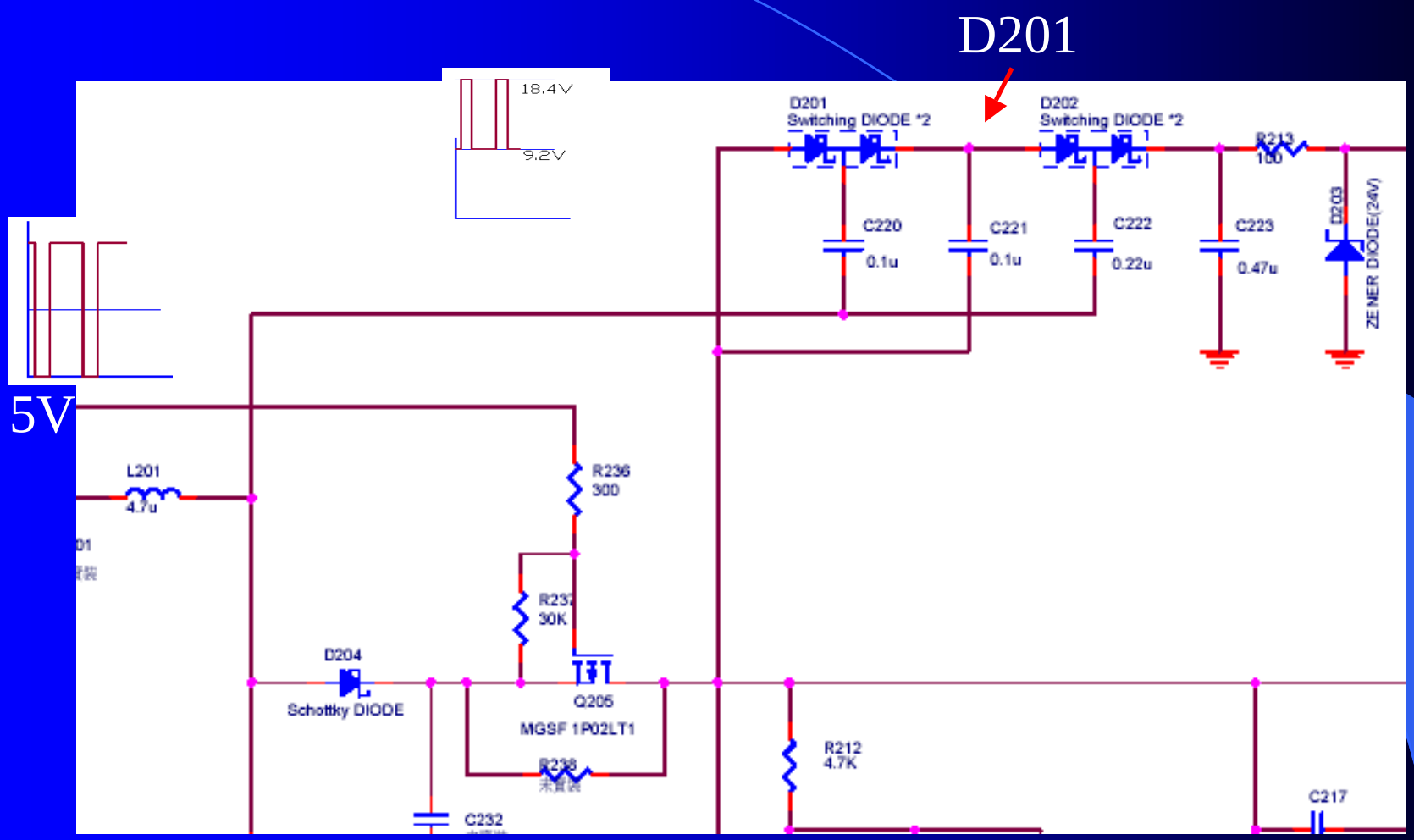
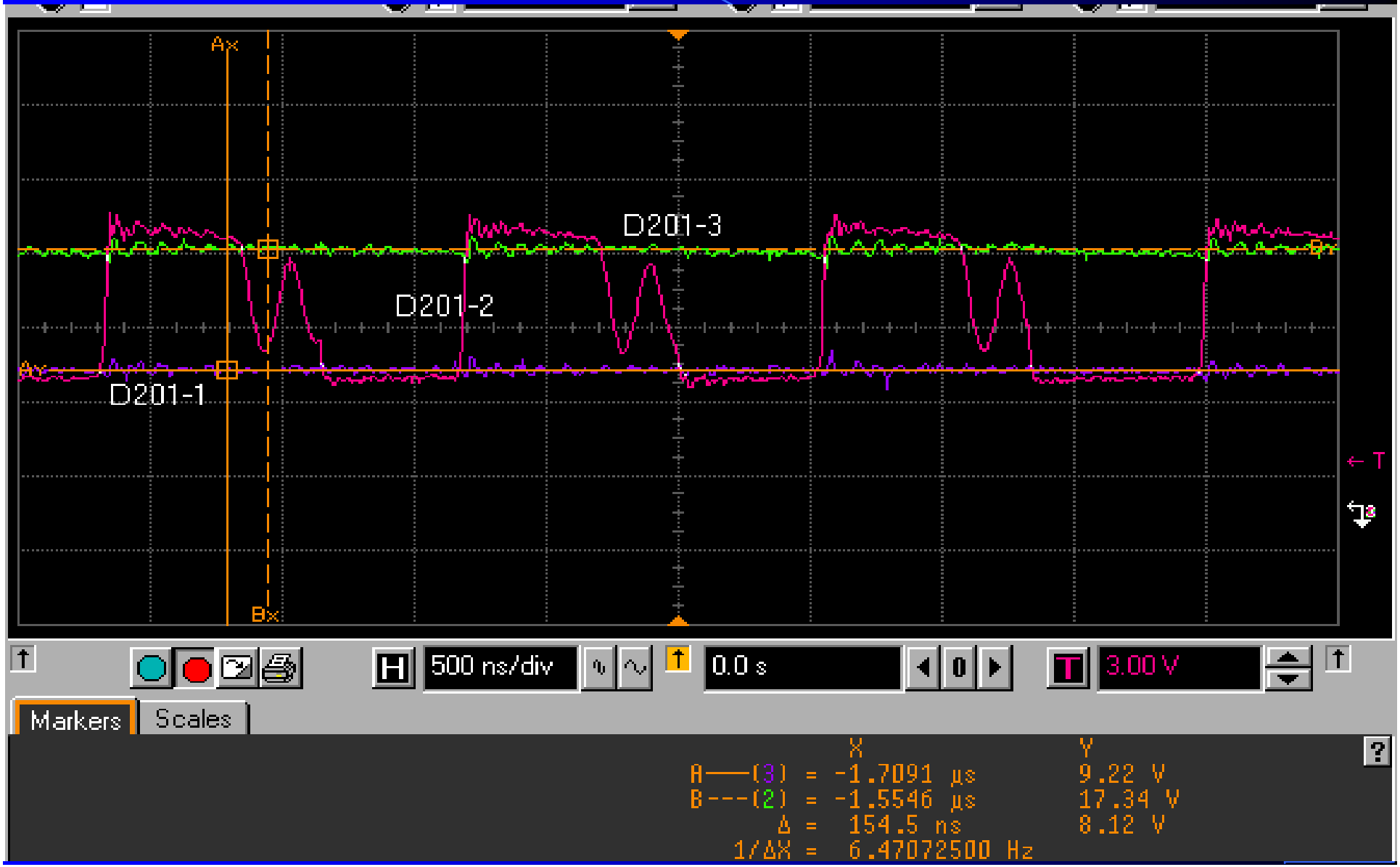


Figure 3. Gamma Correction Curve

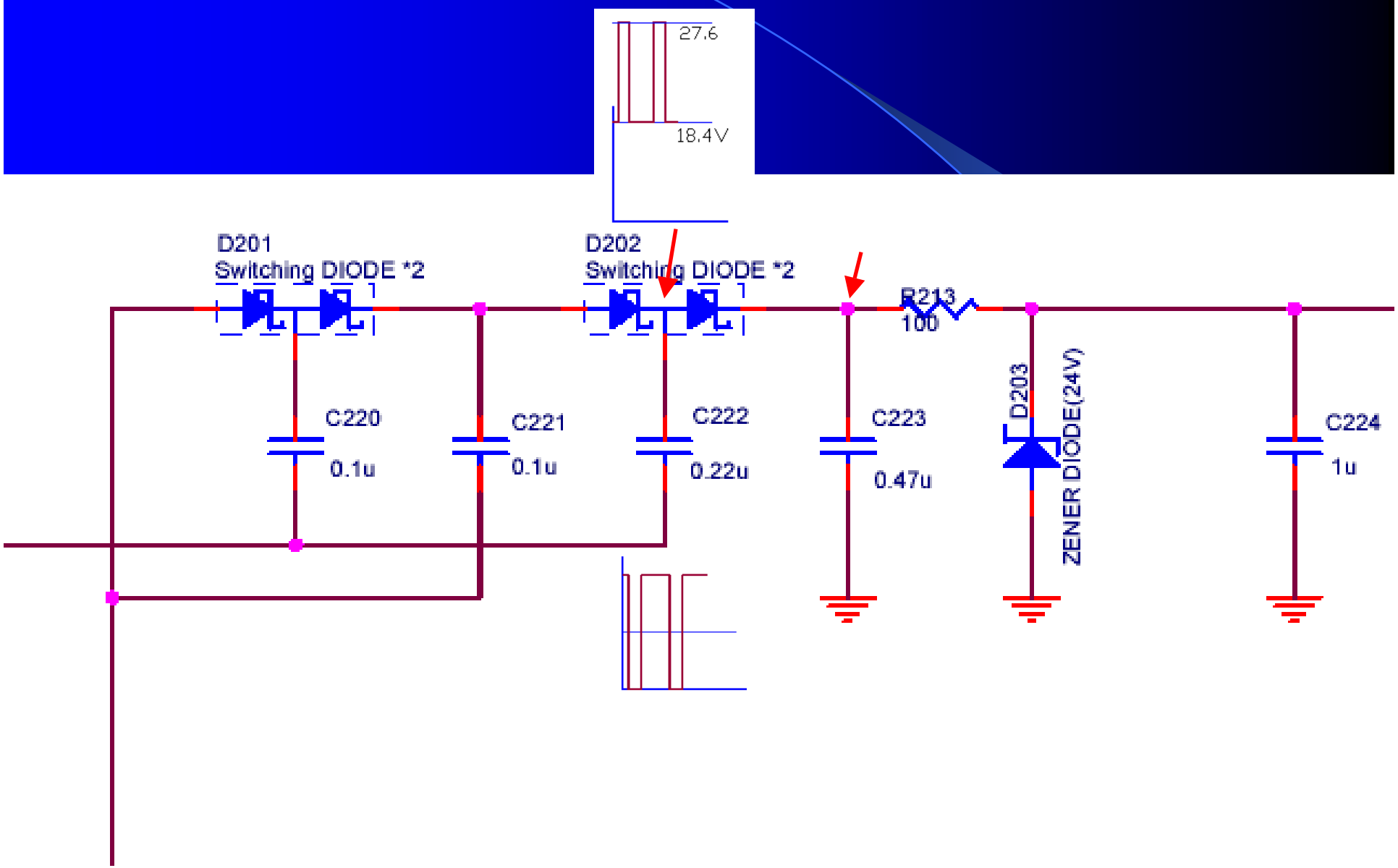
VDDG


D201
18.4V
9.2V
D201
Switching DIODE *2
D202
Switching DIODE *2
R213
100
C220
0.1u
C221
0.1u
C222
0.22u
C223
0.47u
D203
ZENER DIODE(24V)
5V
L201
4.7u
R236
300
R237
30K
D204
Schottky DIODE
Q205
MGSF 1P02LT1
R238
R212
4.7K
C232
C217

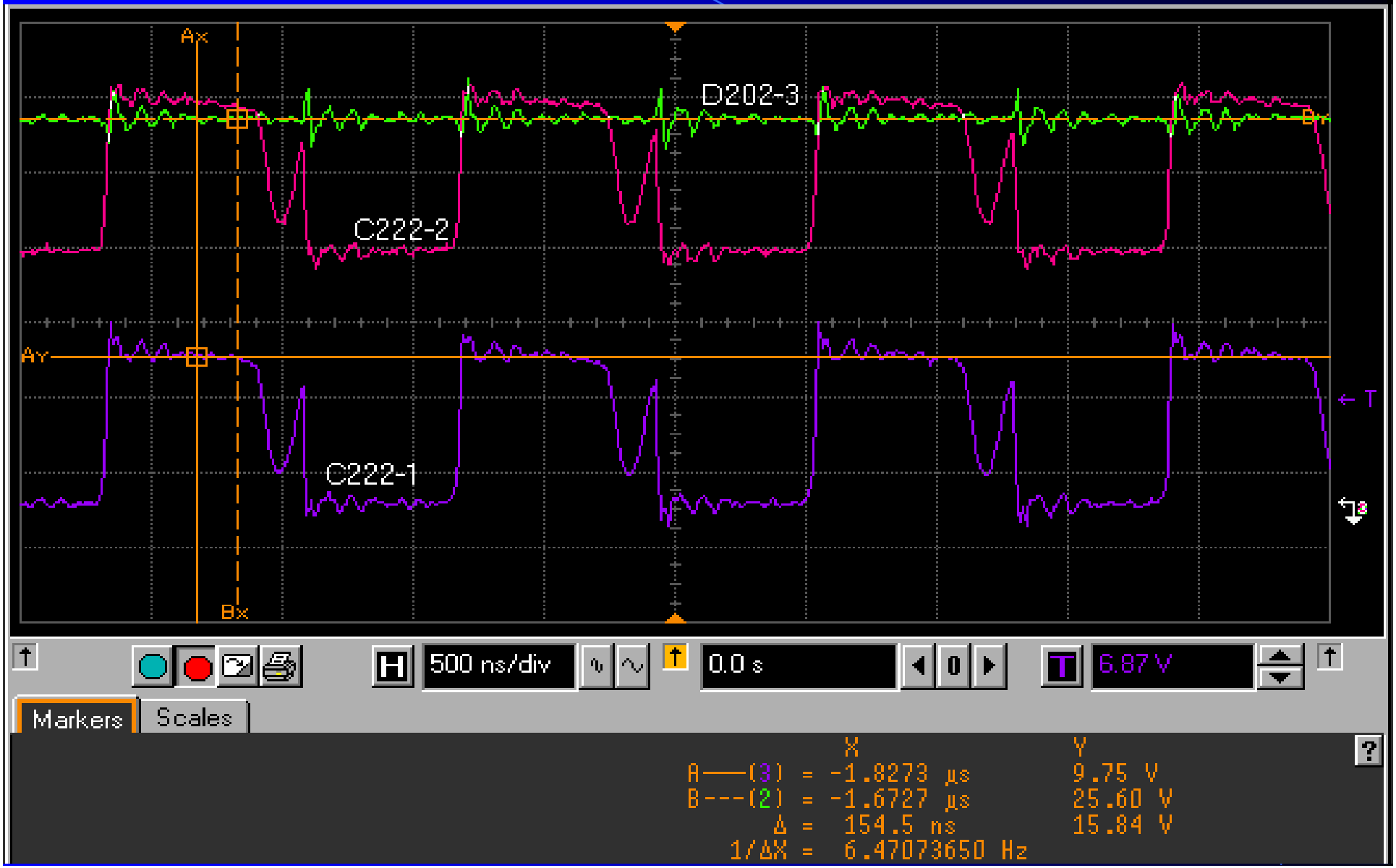
VDDG-D201


Ax
Bx
D201-3
D201-2
D201-1
← T
H
500 ns/div
0.0 s
0
T
3.00 V
Markers
Scales
X
Y
A——(3) = -1.7091 µs 9.22 V
B---(2) = -1.5546 µs 17.34 V
Δ = 154.5 ns 8.12 V
1/ΔX = 6.47072500 Hz

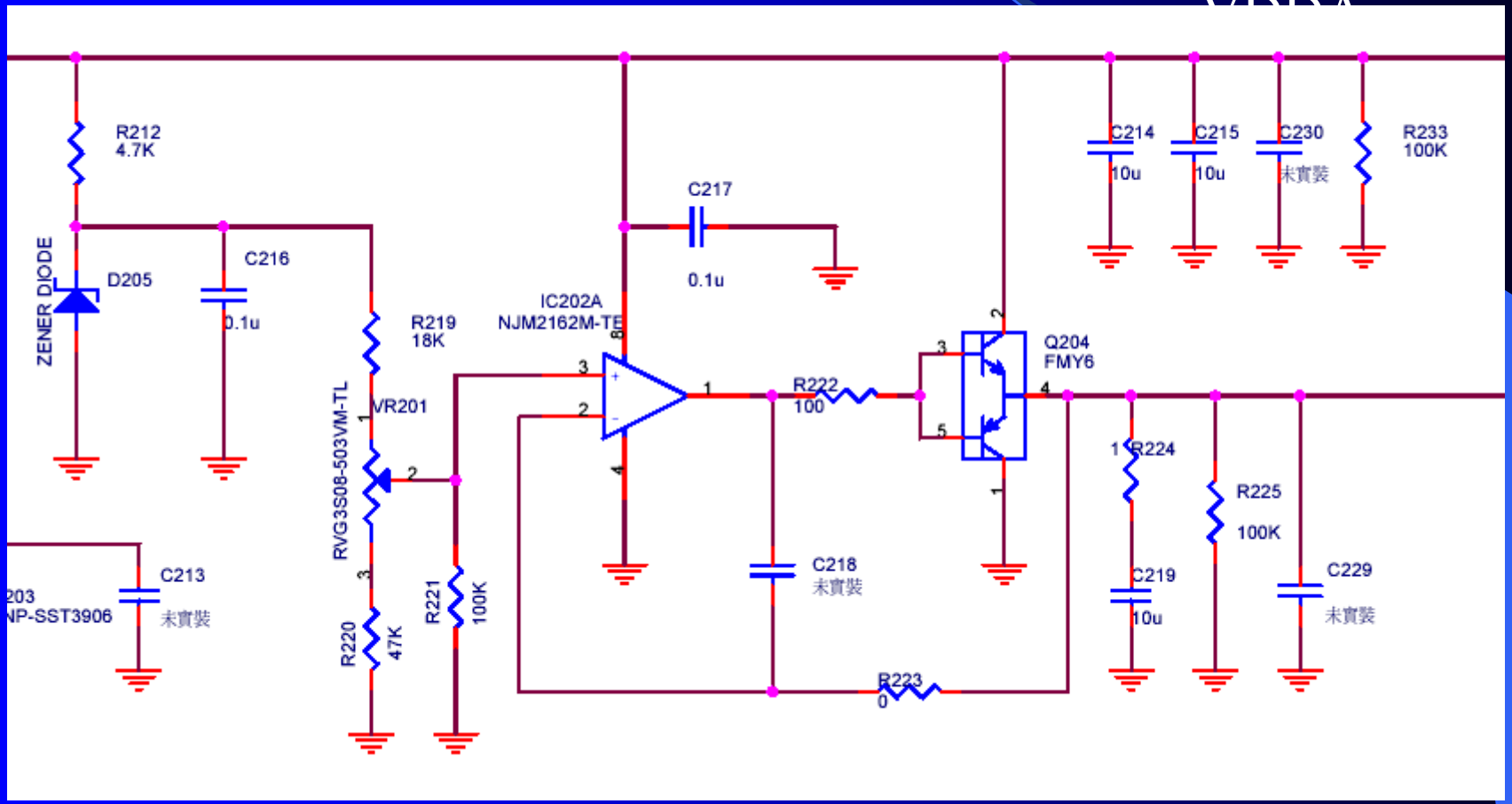
VDDG


27.6
18.4V
D201
Switching DIODE *2
D202
Switching DIODE *2
R213
100
C220
0.1u
C221
0.1u
C222
0.22u
C223
0.47u
D203
ZENER DIODE(24V)
C224
1u

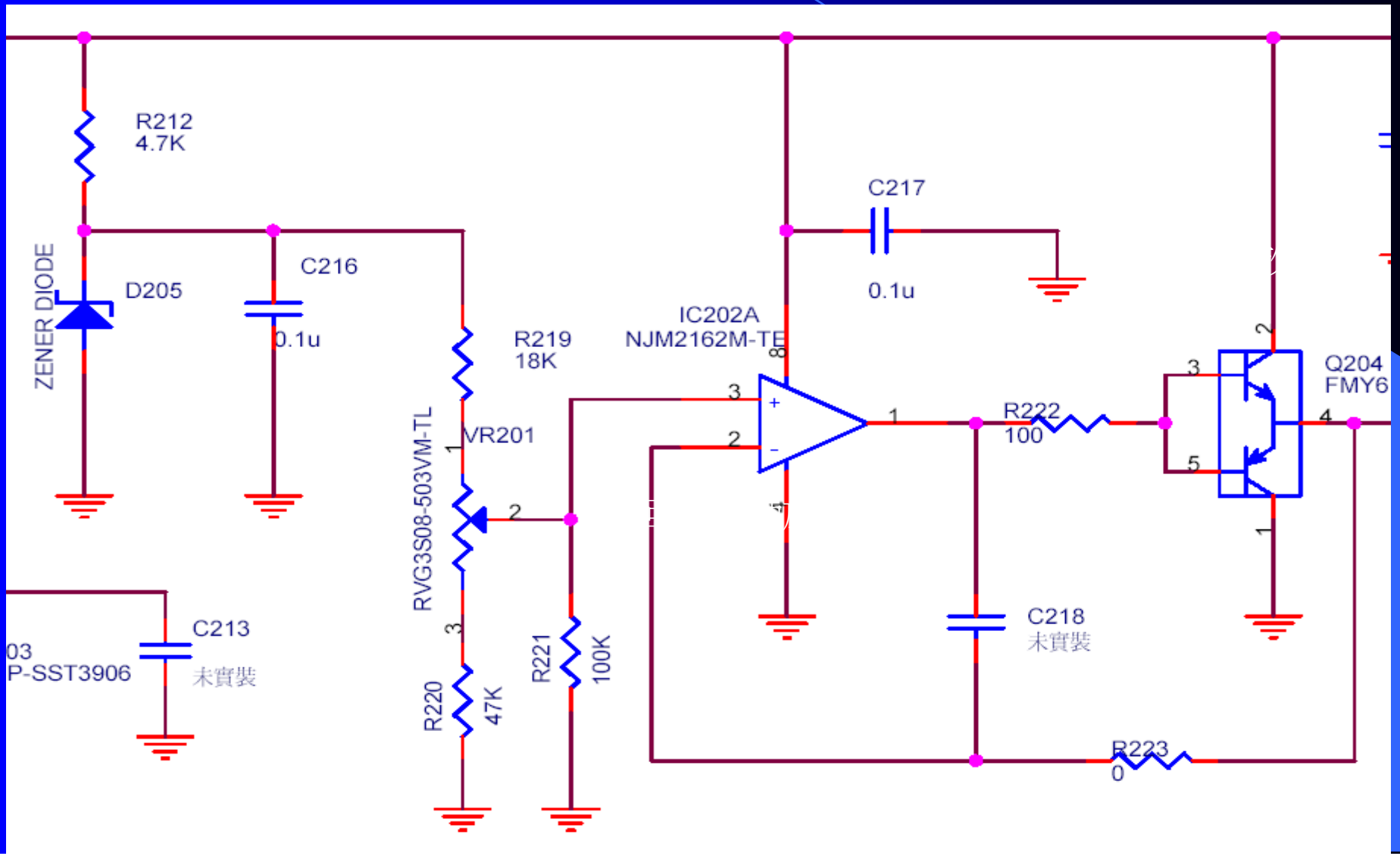
VDDG-D202


Ax
D202-3
C222-2
Ay
C222-1
Bx
← T
H
500 ns/div
0.0 s
0
T
6.87 V
Markers
Scales
X
Y
A——(3) = -1.8273 µs
9.75 V
B---(2) = -1.6727 µs
25.60 V
Δ = 154.5 ns
15.84 V
1/ΔX = 6.47073650 Hz

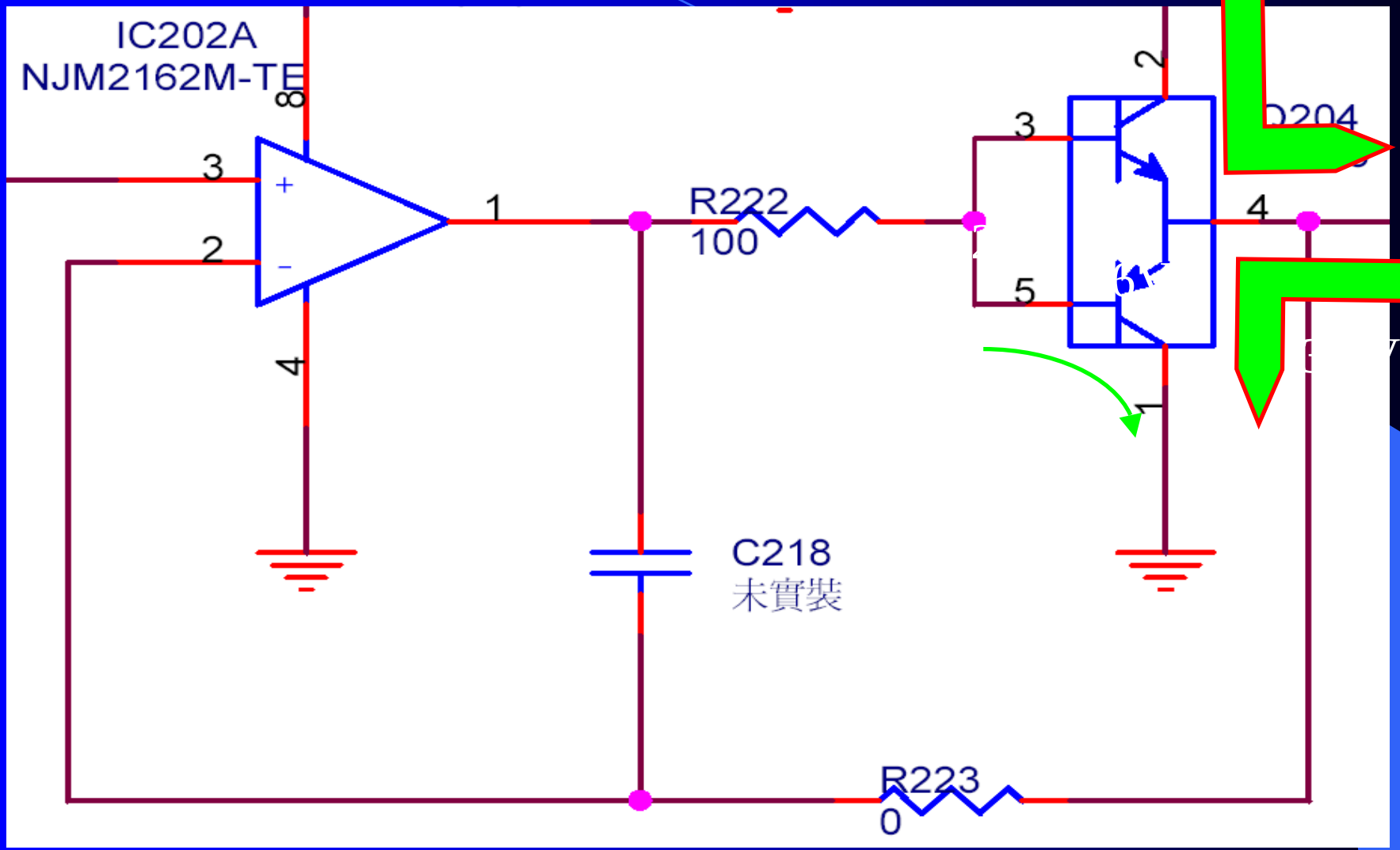
Vcom


VDDA
R212
4.7K
ZENER DIODE
D205
C216
0.1u
C217
0.1u
IC202A
NJM2162M-TE
R219
18K
VR201
RVG3S08-503VM-TL
R220
47K
R221
100K
R222
100
Q204
FMY6
C214
10u
C215
10u
C230
未實裝
R233
100K
R224
R225
100K
C218
未實裝
C219
10u
C229
未實裝
R223
0
C213
未實裝
203
NP-SST3906

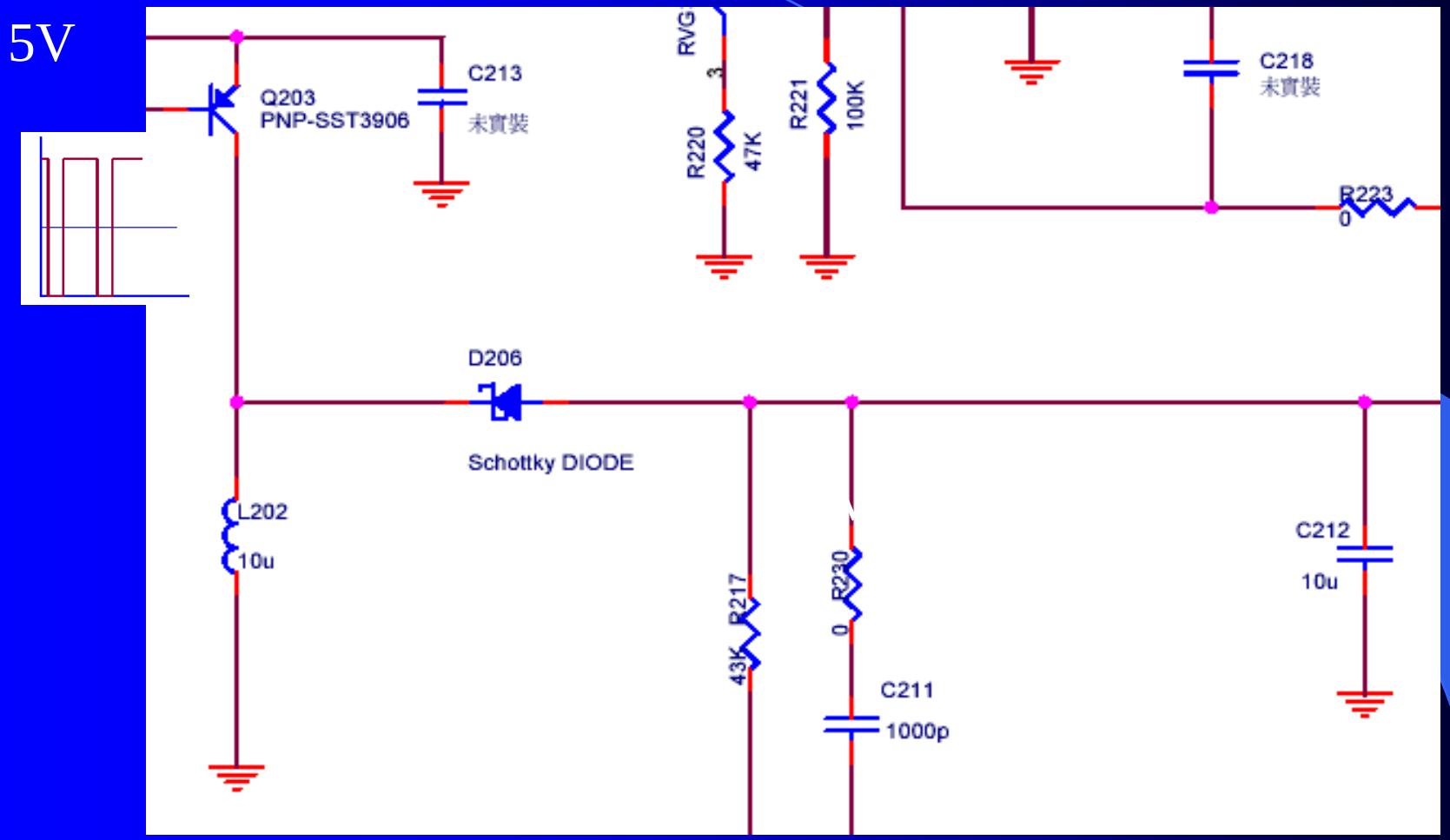
Vcom


R212
4.7K
ZENER DIODE
D205
C216
0.1u
C213
未實裝
03
P-SST3906
R219
18K
VR201
RVG3S08-503VM-TL
R220
47K
R221
100K
C217
0.1u
IC202A
NJM2162M-TE
R222
100
C218
未實裝
R223
0
Q204
FMY6

Vcom



VEEG


5V
Q203
PNP-SST3906
C213
未實裝
RVG
3
R220
47K
R221
100K
C218
未實裝
R223
0
D206
Schottky DIODE
L202
10u
R217
43K
R230
0
C211
1000p
C212
10u


~The End~