NAT-MCH
µTCA Telecom MCH Module
Technical Reference Manual V 1.2
M4 BASE-Module
HW Revision 1.1 to 1.2

The NAT-MCH has been designed by:

N.A.T. GmbH
Konrad-Zuse-Platz 9
D-53227 Bonn

Phone: +49 / 228 /965 864 - 0
Fax: +49 / 228 /965 864 - 10

Internet: http://www.nateurope.com

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.

Table 1 gives a list of the abbreviations used in this document:

Table 1: List of used Abbreviations

Abbreviation	Description
AMC	Advanced Mezzanine Card
b	bit, binary
B	Byte
ColdFire	MCF54452
CPU	Central Processing Unit
CU	Cooling Unit
FLASH	Programmable ROM
FRU	Field Replaceable Unit
K	kilo (factor 400 in hex, factor 1024 in decimal)
M	mega (factor 10,0000 in hex, factor 1,048,576 in decimal)
MCH	µTCA Carrier Hub
MHz	1,000,000 Herz
µTCA	Micro Telecommunications Computing Architecture
PCIe	PCI Express
PCI	Peripheral Component Interconnect
PM	Power Module
RAM	Random Access Memory
ROM	Read Only Memory
SDRAM	Synchronous Dynamic RAM
SSC	Spread Spectrum Clock
RTM	Rear Transition Module

1 Introduction

The **NAT-MCH-M4** consists of a **BASE-Module**, which can be expanded with additional Sub-Modules. The **BASE-Module** satisfies the basic requirements of the MicroTCA Specification for a MicroTCA Carrier Hub. The main capabilities of the **BASE-Module** are:

- management of up to 13 AMCs, two cooling units (CUs) and up to four power modules (PMs)
- Gigabit Ethernet Hub Function for Fabric A (up to 12 AMCs) and for the Update Fabric A to a second (redundant) MCH

To meet also the optional requirements of the MicroTCA specification, a **CLK-Module** and different **HUB-Modules** are available. With the **CLK-Module** the following functions can be enabled:

- generation and distribution of synchronized clock signals for up to 12 AMCs

By extending the **NAT-MCH** with a **HUB-Module**, hub functions for fabric D to G can be enabled. With the different versions the customers have the opportunity to choose a **HUB-Module** that fits best to their application. The versions differ in:

- max. number of supported AMCs (up to 6 / up to 12)
- supported protocols:
  - PCI Express (GenI or GenIII)
  - Serial Rapid IO (GenI or GenII)
  - 10Gigabit Ethernet (XAUI)

The **NAT-MCH-M4** is targeting especially MicroTCA.4 systems or applications. Therefore it complies with the full-height double-width form factor, whereas the "standard" **NAT-MCH** conforms to the full-height single-width form factor. In addition to the different form factor the **NAT-MCH-M4** is featuring the Zone3 connectors defined by the MTCA.4 that are needed to support MTCA.4 **RTMs** (Rear transition Modules).

The additional gained board space is used to support up to two SATA devices for an attached **NAT-RTM**.

The NAT-MCH-M4 provides the following main features at the zone 3 (RTM) connector.

- RTM detection and power switching/ramping
- Management via IPMI
- Two SATA connections
- One PCIe x4 interface, up to GenIII (only supported with **PCIe-HUB-**Module)
- Gigabit Ethernet connectivity to fabric A Ethernet switch

The features of the individual extension modules or RTMs are described in more detail in the corresponding Technical Reference Manuals.

2 Overview

2.1 Major Features

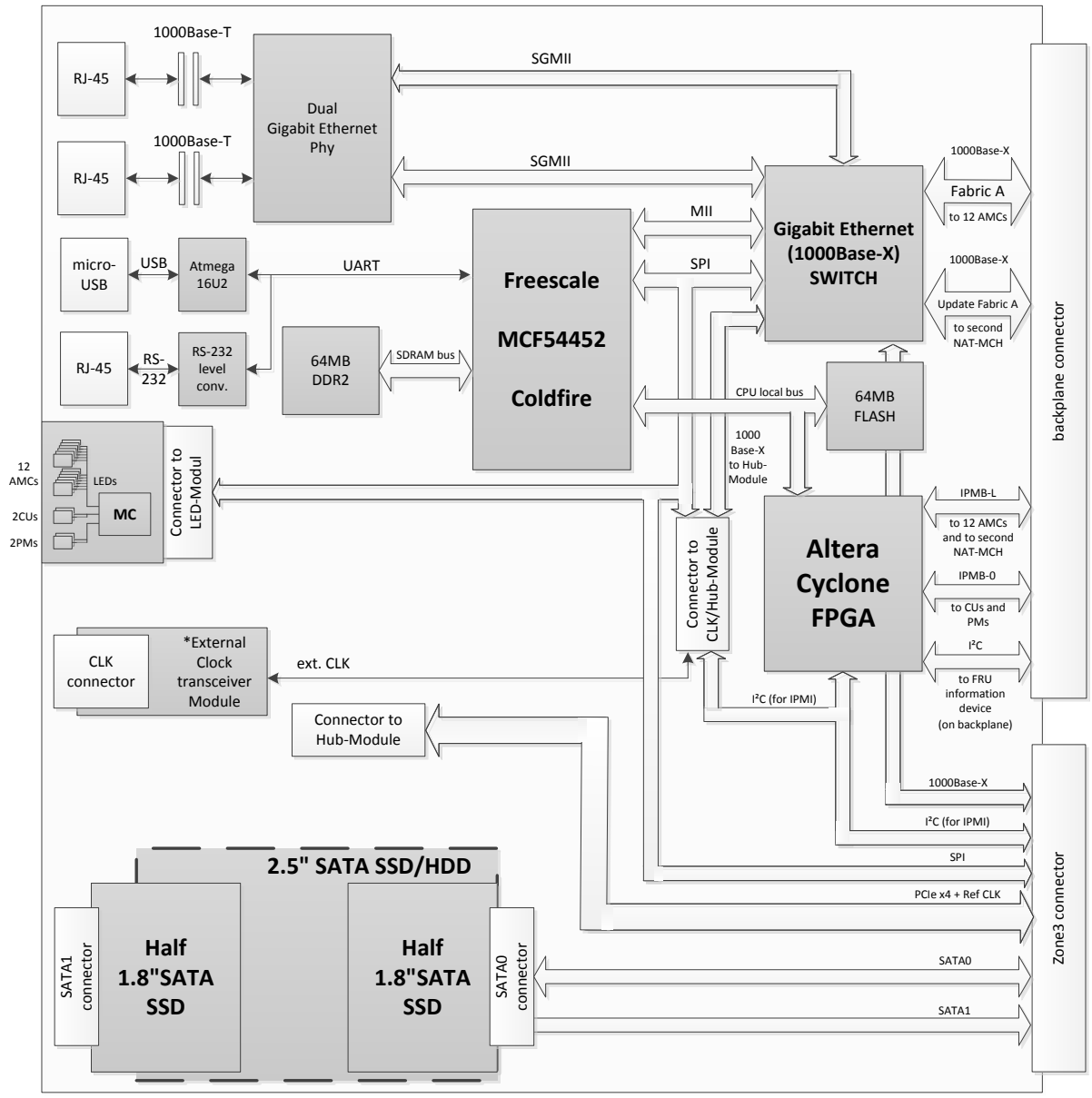
- ColdFire MCF54452 32-bit CPU
- up to 64 MB main Memory (SDRAM)
- up to 64 MB FLASH
- real time clock
- USB debug port on faceplate
- RS-232 debug port on faceplate via RJ45
- 100Mbit Ethernet interface between CPU and Ethernet switch for:
  - communication with external Shelf or System Manager
  - software update
- 12 x IPMB-L interface for AMCs
  - IPMB-L interface for a second NAT-MCH
  - IPMB-L interface for a NAT-MCH-RTM
  - IPMB-0 interface for CUs and PMs
- I²C interface to FRU information device
- Gigabit Ethernet Hub function for fabric A
  - 1000BaseX over Backplane
    - up to 12 AMCs
    - second MCH
  - NAT-MCH-RTM 1000BaseX via zone 3 connector
  - two 1000BaseT channel on front panel
- 2 interfaces for external clock signals (only with CLK-Module)
- Two half-sized 1.8” or one standard-sized 2.5” SATA devices accessible via zone 3 connector
- PCIe x4 connectivity zone 3 connector (only with PCIe-Hub-Module)
- Various status LEDs
  - 12 bicolour LEDs for AMC status information
  - 2 bicolour LEDs for CU status information
  - 2 bicolour LEDs for PM status information
  - 1 bicolour LED for RTM status information

For detailed description see the following chapter.

2.2 Block Diagram

The following figure shows a block diagram of the **NAT-MCH-M4 BASE-Module** and optional available extension modules. If the extension module is added, customized I/O functionality is available.

Figure 1: NAT-MCH-M4 BASE-Module – Block Diagram incl. LED Module



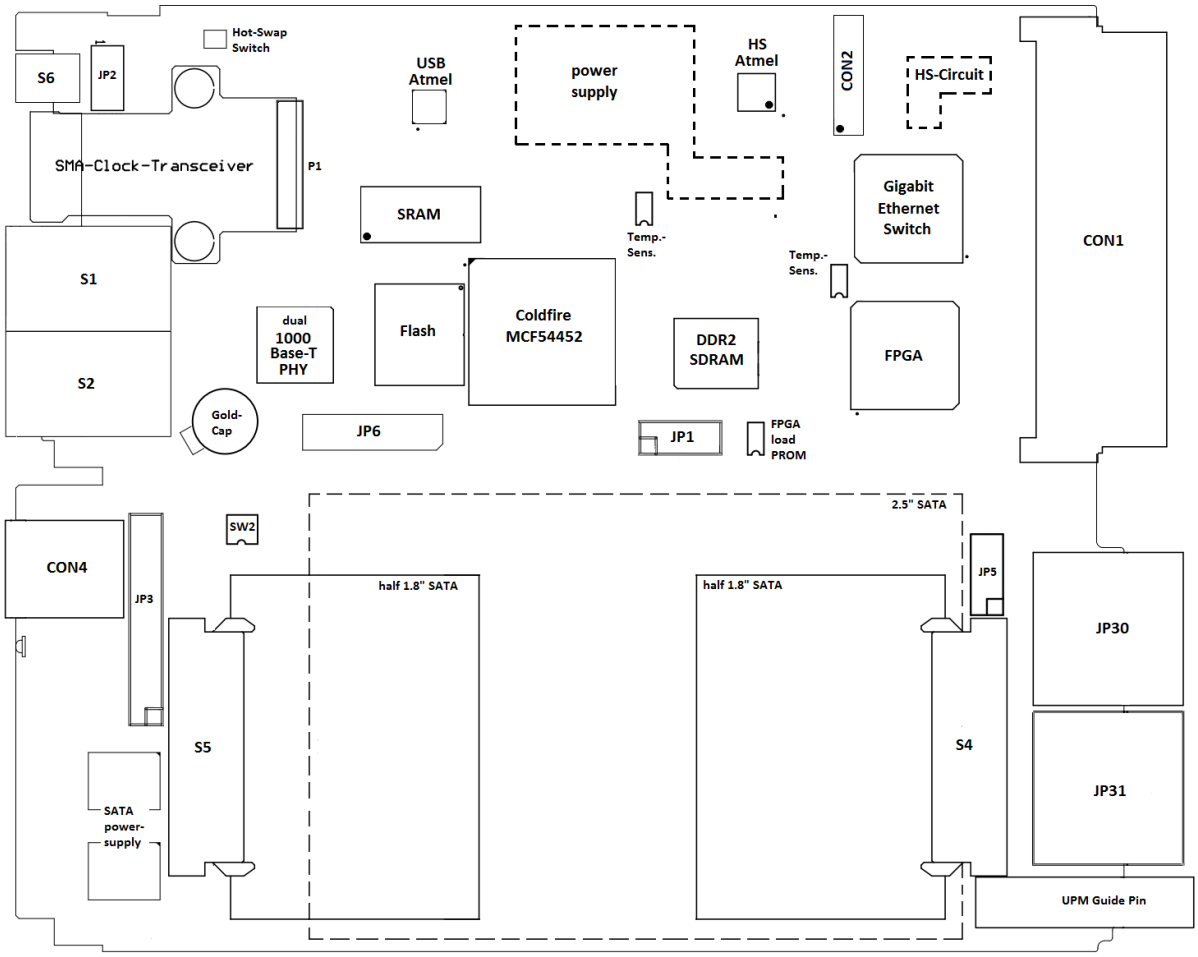
* There are different external clock transceiver modules available. Please refer to the **NAT-MCH CLK-Module** technical reference manual for a more detailed description.

As shown in Figure 1: a LED-Module is mounted on the front panel of the **NAT-MCH-M4 BASE-Module**.

2.3 Location Diagram

The position of important components is shown in the following location overview. Depending on the board type it may be that the board does not include all components named in the location diagram.

Figure 2: NAT-MCH-M4 BASE-Module – Location Diagram – top view



3 Board Features

The **NAT-MCH-M4 BASE-Module** can be divided into a number of functional blocks, which are described in the following paragraphs.

3.1 CPU

The **NAT-MCH-M4 BASE-Module** features a 32-bit CPU ColdFire MCF54452 (Freescale) which is based on the V4e ColdFire core. The MCF54452 includes a memory management unit (MMU), a dual precision floating-point unit (FPU) and an enhanced multiply-accumulate unit (EMAC), delivering 308 (Drystone 2.1) MIPS at 266 MHz.
The processor has integrated a 32 KB I-Cache, a 32 KB D-Cache and 32 KB on-chip system SRAM. The MCF54452 is equipped with a 32-bit DDR2 266 controller at 133 MHz clock rate.

The MFC5470 ColdFire integrates the following interfaces:

- two 10/100 Ethernet Controllers (FECs)
- DSPI – SPI with DMA capability
- a I²C interface
- a 16-channel DMA controller
- USB Interface

3.2 Memory

3.2.1 DDR2SDRAM

The onboard DDR2SDRAM memory is 16 bit wide and provides 32 or 64 MB (assembly option). The interface to the SDRAM is implemented in the ColdFire MCF54452 CPU. By programming several registers, the SDRAM controller can be adapted to different RAM architectures.

3.2.2 FLASH

FLASH memory is connected to the demultiplexed upper 16 data bits D0 – 15 of the local bus and to the latched address lines. Its size (16, 32, or 64 MB) depends on the assembly option. The FLASH memory on the **NAT-MCH-M4 Base-Module** can be programmed by the CPU (by appropriate software) or via the BDM port.

3.3 Backplane Interfaces

3.3.1.1 IPMB

The **NAT-MCH-M4 BASE-Module** implements IPMB interfaces which conform to the MicroTCA specification.
IPMB-L interfaces are available for communication with up to 12 AMCs and a second **NAT-MCH**.
An additional IPMB-L interface is available for communication with the **NAT-RTM**.
An IPMB-0 interface is available for communication with CUs and PMs.

3.3.1.2 I²C

The **NAT-MCH-M4 BASE-Module** provides an I²C interface to access the dedicated FRU information device (resided on the backplane).

3.3.1.3 Ethernet

The **NAT-MCH-M4 BASE-Module** provides 1000BaseX interfaces for fabric A of 12 AMCs and the Update channel of fabric A. Furthermore one 1000BaseX interface connects to the **NAT-RTM**. These interfaces are connected to a Broadcom BCM5396 Gigabit Ethernet Switch.

3.4 Front Panel Interfaces

The **NAT-MCH BASE-Module** is equipped with various interfaces at the front panel, described in the following sections.

3.4.1 Ethernet Uplink Ports

Two ports of the BCM5396 Gigabit Ethernet Switch are wired to connector GbE1 and GbE2 via a Broadcom BCM5482 1000BaseT physical layer chip. By this external device the user may access fabric A also from the front panel.

GbE1: The switch interfaces the network to fabric A and to the ColdFire CPU. Therefore this port can be used to update the ColdFire Software and to permit communication with external shelf or system managers.

GbE2: Together with GbE1 this port can be used to increase the bandwidth of the uplink. Instead of the second GbE-Interface the **NAT-MCH BASE-Module** can be equipped with a RJ45 clock interface (see chapter 3.4.4.2 for details).

Configuration settings of the BCM5482 are done by CPU ports. The BCM5461 PHY has to be set up in GBIC mode (1000BaseT to 1000BaseX translation). Like all other I/O devices, the BCM5461 PHY is resettable by software by programming an FPGA register.

3.4.2 USB Debug Port

The front panel micro USB connector available on the **NAT-MCH-M4 BASE-Module** is connected to the USB capable Atmel Atmega16U2 microcontroller.

This Microcontroller implements a serial interface device. The serial interface of the microcontroller is connected to the ColdFire MCF54452 UART interface. It provides a console interface for configuration, monitoring and debugging. The microcontroller USB interface is running in USB Device Mode. The microcontroller is powered by the USB power, independent of the board power supply. This has the advantage that a terminal connection will not get lost after reboot or power-cycle.

3.4.3 RJ45 RS232 Debug Port

The ColdFire MCF54452 UART interface is connected to the RJ45 debug port via a RS232 level shifter. The level shifter is disabled by the USB voltage. That means that the ColdFire MCF54452 will not receive any inputs via the RJ45 debug port if a USB host is connected!

3.4.4 Clock Interface

The **NAT-MCH BASE-Module** can be equipped with various External Reference Clock Transceiver Modules. The available transceiver modules differ in the number of supported clock signals, in the supported electrical standard (e.g. LVDS, TTL, CMOS) and the supported connector.

The external clock interfaces are routed from the transceiver module to the **CLK-Module**. Therefore the external clock interfaces can only be used in collaboration with the **NAT-MCH CLK-Module**.

At the moment the following External clock transceiver modules are available:

3.4.4.1 Coax-IO

The Coax-IO transceiver module supports two SMA connectors at the face plate. Each connector is connected to its independent amplifier circuit. Each amplifier circuit can be configured as receiver or transmitter.

Configured as transmitter the output signal coming from the **CLK-Module** FPGA is transmitted via a simple CMOS driver. This driver is connected to the SMA connector via AC-coupling.

The amplifier circuit first comes really into operation if configured as receiver. The receiver part is designed to be able to work with a wide range of input voltages, as well as signal forms (e.g. sine wave, rectangle).

To be independent of any DC-offset the receiver part is also connected via AC-coupling.

The main part of the amplifier is a comparator that transfers the input signal from the SMA connector into a rectangle signal with a peak to peak voltage of 3.3V. Refer to 0for the electrical characteristics.

The signal mapping for the Coax-IO module can be found below:

Table 2: NAT-MCH-M4 BASE-Module – Coax-IO signal mapping

Schematic Name	Script Name	Function Coax-IO
Extref1_p	EXT single ended 1	SMA_1 Rx
Extref1_n	EXT single ended 2	SMA_1 Tx
Extref2_p	EXT single ended 3	SMA_2 Rx
Extref2_n	EXT single ended 4	SMA_2 Tx

Table 3: NAT-MCH-M4 BASE-Module – Coax-IO electrical characteristics

Parameter	Min.	Typ.	Max.	Unit
Input Voltage peak to peak	0.3		5	V
Output Voltage peak to peak (with 50 Ohm sink termination)		1		V
Input Frequency	1		50M	Hz
Output Frequency	250		125M	Hz
Termination Resistance		50		Ω

3.4.4.2 RJ45-Clock-Interface

Instead of the second GbE-Port the **NAT-MCH BASE-Module** can be assembled with a second RJ45 connector usable as RJ45-Clock-Interface.

CAUTION:

The second GbE-Interface is not available with this assembly option! The pin assignment of the RJ45-Clock-Interface differs from the GbE-Interface! For detailed information please regard chapter 4.2.11.

The signals are directly connected to LVDS compliant IOs of the clock module FPGA. To cause no destruction no signals should be applied to this interface that do not comply with the LVDS signal standard.

Other External Reference Clock Transceiver Modules

Please contact N.A.T. GmbH if the available Clock transceiver modules or any parameter does not satisfy the needs for your application.

3.5 Interface to Extension Modules

3.5.1 NAT-MCH CKL-Module / NAT-MCH CLK-PHYS-Module

The **NAT-MCH CLK-Module** / **NAT-MCH CLK-PHYS-Module** can be accessed by the ColdFire MCF54452 via I²C bus.

To interface the **NAT-MCH HUB-Module**, a SPI interface is also available. The SPI interface of the ColdFire is used for this purpose.

3.5.2 NAT-MCH HUB-Module

The **NAT-MCH HUB-Module** is connected to the **NAT-MCH-M4 BASE-Module** over the same connector that connects the **NAT-MCH CLK-Module** / **NAT-MCH CLK-PHYS-Module**. The **NAT-MCH HUB-Module** can also be accessed by the ColdFire via I²C bus.

To interface the **NAT-MCH HUB-Module**, a SPI interface is also available. The SPI interface of the ColdFire is used for this purpose. Depending on the **HUB-Module** the SPI interface is only used for update purposes or as an additional communication path.

3.6 Interface to NAT-RTM-Module (via Zone3 connector):

3.6.1 Power supply

The **NAT-MCH-M4** supplies the **NAT-RTM** with a locally generated 3.3V management power and with a switched version of the MCH 12V payload power. Both supplies are ramped and over-current controlled to support hot-swap.

3.6.2 Management

The **NAT-MCH-M4** supports an IPMB-L interface to the **NAT-RTM**.

3.6.3 Ethernet

The **NAT-MCH-M4** supports one 1000Base-X Ethernet interface that connects between the Fabric-A Gigabit Ethernet switch on the **NAT-MCH-M4 BASE-Module** and the RTM.

3.6.4 SATA

The **NAT-MCH-M4** supports two SATA interfaces that allow a **NAT-RTM** to access the SATA devices located on the **NAT-MCH-M4 BASE-Module**

3.6.5 PCI Express

The **NAT-MCH-M4** supports a PCIe (GenIII) x4 connection between the **NAT-MCH PCIe-HUB-Module** and the **NAT-RTM**.

3.7 I^2C Devices

There are three I^2C Devices on the **NAT-MCH-M4 BASE-Module**, which are connected to the MCF54452 via I^2C bus

- An EEPROM (24C08) used for storage of board-specific information (address 0x50)
- Two temperature sensors (LM75), which sense the board temperature near CPU and near FPGA (addresses 0x9C and 0x9E)

3.8 Ethernet Switch

The Broadcom BCM5396 Gigabit Ethernet Switch provides a layer 2, non-blocking, low-latency Gigabit Ethernet switch, supporting VPN as well as a port based rate control. The BCM5396 supports Fabric A switching according to MicroTCA.0 R1.0 and PICMG SFP.1 R1.0, serving up to 12 AMCs as well as the update channel from the second NAT-MCH in redundant environments. Also supported are two uplink ports at the front panel of the **NAT-MCH BASE-Module** in order to interconnect to other carriers, shelves or systems. Refer to section 3.4.1 for the Uplink ports.

The configuration register of the BMC5396 can be accessed through the MCF54452's PHY message channel interface.
For frame management the BMC5396 is connected to the MCF54452's TSEC0 through the MII interface.

3.9 SATA Devices

The **NAT-MCH-M4** supports two SATA connectors including power supply and mounting holes for standard 2.5” and half-sized 1.8” SATA devices. Because of the limited board space the **NAT-MCH-M4** can only be equipped with one 2.5” SATA device.
The SATA connections are directly routed to the zone 3 RTM Connector.

4 Hardware

4.1 Front Panel and LEDs

The following figure shows the front panel of the **NAT-MCH-M4 BASE-Module**. It is equipped with various LEDs.

Figure 3: NAT-MCH-M4 BASE-Module – Front Panel

4.1.1 MCH Basic-LEDs

- The *Status-LED* indicates the operation status of the **NAT-MCH BASE-Module**. If the LED is *green*, the **NAT-MCH BASE-Module** operates as *primary* MCH in the MicroTCA-system, if the LED shines *orange*, it is operating as *secondary* MCH
- The *Fault-LED* indicates a malfunction of the **NAT-MCH BASE-Module**
- The *Hot-Swap-LED* indicates the Hot-Swap-Status of the **NAT-MCH BASE-Module**

4.1.2 RJ45-LEDs

Two *RJ45-LEDs* are integrated in each RJ45-connector to indicate GbE-Status.

4.1.3 AMC/CU/PM Status LEDs

Various *Status-LEDs* residing on the front panel (mounted on the LED-Module) indicate the status of 12 AMCs, 2 CUs and 2 PMs.

4.1.4 PCIe-Link LEDs

The *PCIe-Link-LEDS* indicate the Link-Status of an optionally mountable **NAT-MCH PCIe-HUB-Module.**

Slow blink: PCIe-GEN1-Link established
Fast Flash: PCIe-GEN2-Link established
Solid On: PCIe-GEN3-Link established

PCIE-Link-LEDs 1-11 are green; *PCIe-Link-LED 12* is bi-coloured, as it owns a special status:

- if the PCIe switch port is connected to *AMC12* via multiplexer, the LED is shining *green*
- if the multiplexer connects to the ***NAT-RTM*** instead, the LED is lightened *orange*

4.1.5 RTM-Status-LED

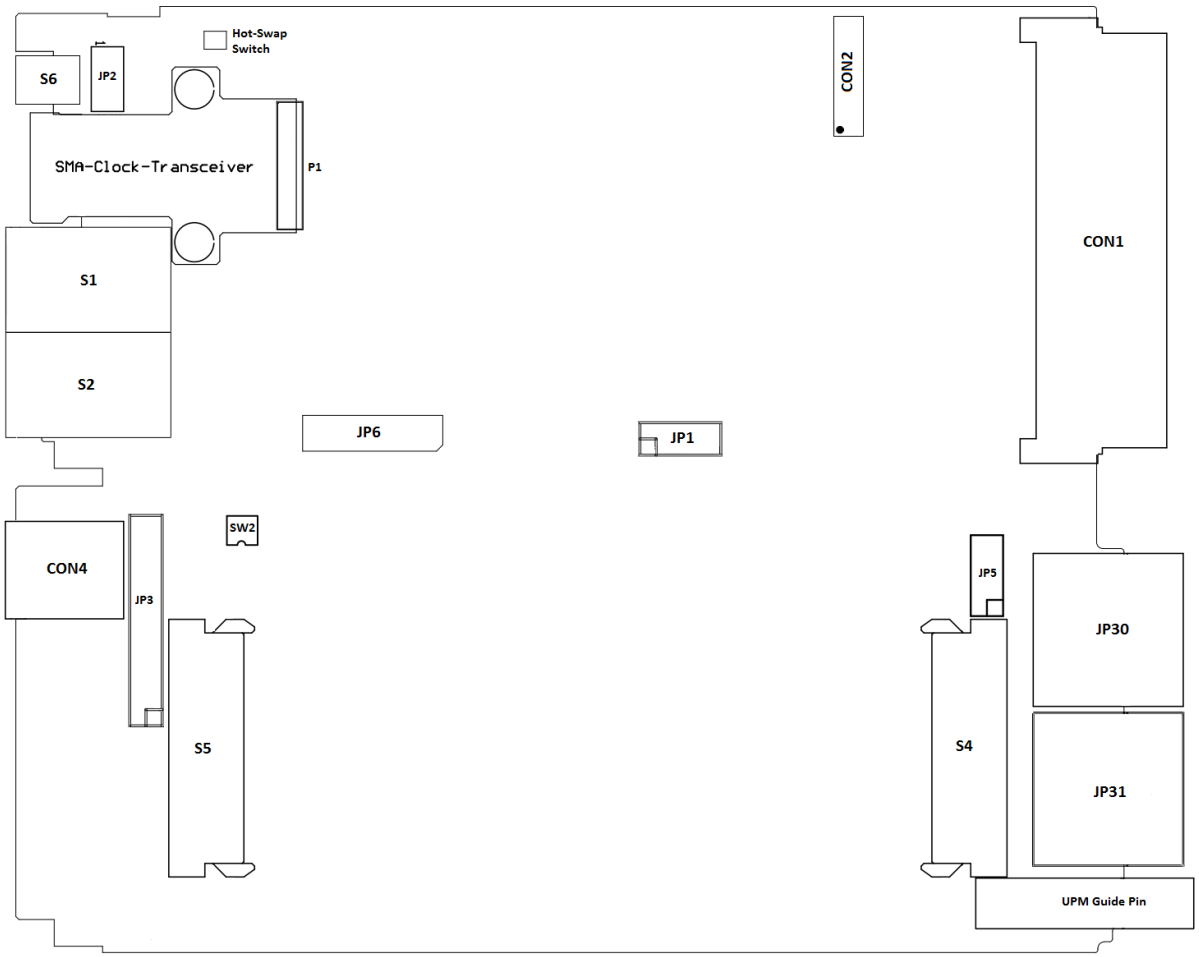
The bi-coloured *RTM-Status-LED* indicates the status of an optionally mountable **NAT-RTM.**

Off:	no **NAT-RTM** present
Green Blink:	Link established, no Payload Power
Solid Green On:	Link established, Payload Power on
Solid Red On:	no Link established / unknown RTM

Please refer to Chapter 4.2 for details on front panel connectors.

4.2 Connectors and Switches

Figure 4: NAT-MCH-M4 BASE-Module – Connectors – Overview



Please refer to the following tables to look up the pin assignment of the **NAT-MCH-M4 BASE-Module**.

4.2.1 CON1: MCH Connector

Table 4: CON1: MCH Connector – Pin-Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	GND	PWR_ON	170
2	PWR	NC	169
3	/PS1	NC	168
4	MP	NC	167
5	GA0	NC	166
6	RESVD	NC	165
7	GND	GND	164
8	RESVD	TxFA-1+	163
9	PWR	TxFA-1-	162
10	GND	GND	161
11	TxFUA+	RxFA-1+	160
12	TxFUA-	RxFA-1-	159
13	GND	GND	158
14	RxFUA+	TxFA-2+	157
15	RxFUA-	TxFA-2-	156
16	GND	GND	155
17	GA1	RxFA-2+	154
18	PWR	RxFA-2-	153
19	GND	GND	152
20	TxFA-3+	TxFA-4+	151
21	TxFA-3-	TxFA-4-	150
22	GND	GND	149
23	RxFA-3+	RxFA-4+	148
24	RxFA-3-	RxFA-4-	147
25	GND	GND	146
26	GA2	TxFA-6+	145
27	PWR	TxFA-6-	144
28	GND	GND	143
29	TxFA-5+	RxFA-6+	142
30	TxFA-5-	RxFA-6-	141
31	GND	GND	140
32	RxFA-5+	TxFA-8+	139
33	RxFA-5-	TxFA-8-	138
34	GND	GND	137
35	TxFA-7+	RxFA-8+	136
36	TxFA-7-	RxFA-8-	135
37	GND	GND	134
38	RxFA-7+	/TMREQ	133
39	RxFA-7-	RSVD	132
40	GND	GND	131
41	/ENABLE	I2C_SCL	130
42	PWR	I2C_SDA	129
43	GND	GND	128
44	TxFA-9+	IPMB0-SCL-A	127
45	TxFA-9-	IPMB0-SDA-A	126
46	GND	GND	125

Pin #	AMC-Signal	AMC-Signal	Pin #
47	RxFA-9+	IPMB0-SCL-B	124
48	RxFA-9-	IPMB0-SDA-B	123
49	GND	GND	122
50	TxFA-10+	IPMBL-SCL-1	121
51	TxFA-10-	IPMBL-SDA-1	120
52	GND	GND	119
53	RxFA-10+	IPMBL-SCL-2	118
54	RxFA-10-	IPMBL-SDA-2	117
55	GND	GND	116
56	SCL_L	IPMBL-SCL-3	115
57	PWR	IPMBL-SDA-3	114
58	GND	GND	113
59	TxFA-11+	IPMBL-SCL-4	112
60	TxFA-11-	IPMBL-SDA-4	111
61	GND	GND	110
62	RxFA-11+	IPMBL-SCL-5	109
63	RxFA-11-	IPMBL-SDA-5	108
64	GND	GND	107
65	TxFA-12+	IPMBL-SCL-6	106
66	TxFA-12-	IPMBL-SDA-6	105
67	GND	GND	104
68	RxFA-12+	IPMBL-SCL-7	103
69	RxFA-12-	IPMBL-SDA-7	102
70	GND	GND	101
71	SDA_L	IPMBL-SCL-8	100
72	PWR	IPMBL-SDA-8	99
73	GND	GND	98
74	XOVER0+	IPMBL-SCL-9	97
75	XOVER0-	IPMBL-SDA-9	96
76	GND	GND	95
77	XOVER1+	IPMBL-SCL-10	94
78	XOVER1-	IPMBL-SDA-10	93
79	GND	GND	92
80	XOVER2+	IPMBL-SCL-11	91
81	XOVER2-	IPMBL-SDA-11	90
82	GND	GND	89
83	/PS0	IPMBL-SCL-12	88
84	PWR	IPMBL-SDA-12	87
85	GND	GND	86

4.2.2 CON2: Extension Module Connector

Connector CON2 connects the **NAT-MCH-M4 BASE-Module** with the **NAT-MCH CLK-Module** and/or the **NAT-MCH HUB-Module**.

Table 5: CON2: Extension Module Connector – Pin Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	/SPISEL_CLKPCB	/INT_HUB	2
3	GND	GND	4
5	NC	NC	6
7	NC	NC	8
9	+12V	+12V	10
11	+12V	+12V	12
13	EXTREF_1_P	+3.3V MP	14
15	EXTREF_1_N	SPICLK	16
17	EXTREF_2_N	EXTREF_2_P	18
19	MOSI	MISO	20
21	GND	/SPISEL_Hub-Module	22
23	SCL	/Reset_CLK-Module	24
25	SDA	/Reset_Hub-Module	26
27	GND	GND	28

The I^2C- and SPI- interfaces of Connector CON2 are connected to the respective interfaces of the local Coldfire CPU.

4.2.3 CON3: RJ45 Front Panel Serial Console Connector

Connector CON3 is connected to the MCF54452 UART via a RS232 level converter.

Table 6: CON3: RJ45 Front Panel Serial Console Connector (RS232) – Pin Assignment

Pin #	Signal	Signal	Pin #.
1	NC	NC	2
3	NC	GND	4
5	RS232-TD	RS232-RD	6
7	NC	NC	8

Please note: If the USB interface is connected to an USB host (e.g. a PC) the RS232 receive path will be disabled. That means if the serial console is connected to a terminal program the debug outputs of the MCH firmware will still show up but it will not be possible to interact.

4.2.4 JP1: Altera FPGA Programming Port

Connector JP1 connects the JTAG- or programming-port of the Altera FPGA device.

Table 7: JP1: Altera FPGA Programming Port – Pin Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	DCLK	GND	2
3	CONF_DONE	+3.3V	4
5	/CONFIG	/CECONF	6
7	DATAO	/CSO	8
9	ASDI	GND	10

4.2.5 JP2. LED-Module Connector

Connector JP2 connects the LED-Module via a ribbon cable

Table 8: JP2: LED-Module Connector – Pin Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	GND	nRESET_LED	2
3	+3.3V	MOSI	4
5	nSPISEL_LED	MISO	6
7	GND	SPICLK	8

4.2.6 JP3: Development Connector

The BDM port (also called COP header) can be used for debugging. It is supported by major debug tool manufacturers.

Table 9: JP3: Development Connector – Pin Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	/CPU_RSTOUT	/BKPT	2
3	GND	/DSCLK	4
5	GND	SLV_TCK	6
7	/HRESET	SLV_TDI	8
9	+3.3V	CPU_TDO	10
11	GND	PST_D7	12
13	PST_D6	PST_D5	14
15	PST_D4	PST_D3	16
17	PST_D2	PST_D1	18
19	PST_D0	JTAG_EN	20
21	NC	NC	22
23	GND	PST_CLK	24
25	TMREQ	/TA	26

4.2.7 JP5: RTM JTAG Connector

Connector JP5 connects directly to the JTAG signals coming from the RTM Connector JP30.

Table 10: JP5: RTM JTAG Connector – Pin Assignment

Pin #	Signal	Signal	Pin No.
1	+3.3V	RTM_TDO	2
3	RTM_TDI	NC	4
5	NC	RTM_TMS	6
7	GND	RTM_TCK	8
9	NC	NC	10

4.2.8 JP30/JP31: Zone 3 RTM Connectors

JP30 and JP31 are the Zone3 connectors as defined by the MicroTCA.4 specification. These connectors can be used to connect to a **NAT-MCH-RTM Module**.

Table 11: JP30: Zone3 RTM Connector – Pin Assignment

Col→ Row↓	GND	F	E	GND	D	C	GND	B	A
10	GND	RTM_PCIe 3-Rx_N	RTM_PCIe 3-Rx_P	GND	RTM_Rx_ CLK_N	RTM_Rx_ CLK_P	GND	RTM_Tx_ CLK_P	RTM_Tx_ CLK_N
9	GND	RTM_PCIe 3-Tx_N	RTM_PCIe 3-Tx_P	GND	SATA1_D SS	SATA0_D SS	GND	NC	NC
8	GND	RTM_PCIe 2-Rx_N	RTM_PCIe 2-Rx_P	GND	RTM_SAT A1-Rx_N	RTM_SAT A1-Rx_P	GND	NC	NC
7	GND	RTM_PCIe 2-Tx_N	RTM_PCIe 2-Tx_P	GND	RTM_SAT A1-Tx_N	RTM_SAT A1-Tx_P	GND	RTM_SPISE L2n	RTM_SPIS EL1n
6	GND	RTM_PCIe 1-Rx_N	RTM_PCIe 1-Rx_P	GND	RTM_SAT A0-Rx_N	RTM_SAT A0-Rx_P	GND	RTM_MOSI	RTM_MISO
5	GND	RTM_PCIe 1-Tx_N	RTM_PCIe 1-Tx_P	GND	RTM_SAT A0-Tx_N	RTM_SAT A0-Tx_P	GND	RTM_SPICL K	RTM_ENn
4	GND	RTM_PCIe 0-Rx_N	RTM_PCIe 0-Rx_P	GND	RTM_ET H0-Rx_N	RTM_ETH 0-Rx_P	GND	NC	NC
3	GND	RTM_PCIe 0-Tx_N	RTM_PCIe 0-Tx_P	GND	RTM_ET H0-Tx_N	RTM_ETH 0-Tx_P	GND	NC	NC
2	GND	RTM_TDI	RTM_TMS	GND	RTM_SCL	RTM_MP	GND	RTM_PWR	RTM_PWR
1	GND	RTM_TDO	RTM_TCK	GND	RTM_SD A	RTM_PS#	GND	RTM_PWR	RTM_PWR

Table 12: JP31: Zone3 RTM Connector – Pin Assignment

Col→ Row↓	GND	F	E	GND	D	C	GND	B	A
10	GND	NC	NC	GND	NC	NC	GND	NC	NC
9	GND	NC	NC	GND	NC	NC	GND	NC	NC
8	GND	NC	NC	GND	NC	NC	GND	NC	NC
7	GND	NC	NC	GND	NC	NC	GND	NC	NC
6	GND	NC	NC	GND	NC	NC	GND	NC	NC
5	GND	NC	NC	GND	NC	NC	GND	NC	NC
4	GND	NC	NC	GND	NC	NC	GND	NC	NC
3	GND	NC	NC	GND	NC	NC	GND	NC	NC
2	GND	NC	NC	GND	NC	NC	GND	NC	NC
1	GND	NC	NC	GND	NC	NC	GND	NC	NC

Please note: by default JP31 is not assembled!

4.2.9 P3: External Clock Transceiver Module Connector

Connector P3 is used to connect the external clock transceiver module to the **NAT-MCH-M4 Base-Module.**

Table 13: P3: External Clock Transceiver Module Connector – Pin Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	SGND	+3.3V	2
3	EXTREF_C_P	EXTREF_CONF1	4
5	EXTREF_C_N	EXTREF_CONF2	6
7	EXTREF_A_P	EXTREF1_P	8
9	EXTREF_A_N	EXTREF1_N	10
11	EXTREF_B_P	EXTREF2_P	12
13	EXTREF_B_N	EXTREF2_N	14
15	EXTREF_D_P	EXTREF_CONF3	16
17	EXTREF_D_P	SGND	18
19	EXTREF_CONF4	GND	20

4.2.10S1: Front Panel Ethernet Connector

Connector S1 carries the 1000BaseT signals of the front panel Ethernet interface of the Gigabit Ethernet Switch.

Table 14: S1: Front Panel Ethernet Connector – Pin Assignment

Pin #	Signal	Signal	Pin#
1	MDI1_0+	MDI1_0-	2
3	MDI1_1+	MDI1_2+	4
5	MDI1_2-	MDI1_1-	6
7	MDI1_3+	MDI1_3-	8

4.2.11S2: Front Panel Ethernet Connector

Connector S2 carries the 1000BaseT signals of the front panel Ethernet interface of the Gigabit Ethernet Switch.

Table 15: S2: Front Panel Ethernet Connector – Pin Assignment

Pin #	Signal	Signal	Pin#
1	MDI2_0+	MDI2_0-	2
3	MDI2_1+	MDI2_2+	4
5	MDI2_2-	MDI2_1-	6
7	MDI2_3+	MDI2_3-	8

If chosen as assembly option the second RJ45 connector can be used as RJ45-Clock-Interface. The deviating pin assignment can be found in the following table.

Table 16: S2: RJ45 Connector/ RJ45-Clock-Interface – Pin-Assignment

Pin #	Signal	Signal	Pin #
1	nc	nc	2
3	Extref2_p	Extref1_p	4
5	Extref1_n	Extref2_n	6
7	nc	nc	8

4.2.12S4/S5: SATA Connectors

Connectors S4 and S5 are standard SATA connectors. The power pins are assigned to local DC/DC converters which are only responsible for these SATA devices. All other connections are directly routed to the zone 3 (RTM-) connector. JP30 is therefore only usable by an MCH-RTM.
S4 connects to SATA device 0. This connector can be equipped with a standard-sized 2.5" SATA device (HDD or SSD) or with a half-sized 1.8" SATA device (only available as SSD).

Table 17: S4: SATA Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
S1	GND	+3.3V	P1
S2	RTM_SATA0-Rx_P	+3.3V	P2
S3	RTM_SATA0-Rx_N	+3.3V	P3
S4	GND	GND	P4
S5	RTM_SATA0-Tx_N	GND	P5
S6	RTM_SATA0-Tx_P	GND	P6
S7	GND	+5V	P7
		+5V	P8
		+5V	P9
		GND	P10
		SATA0_DSS	P11
		GND	P12

S5 connects to SATA device 1. This connector can only be equipped with half-sized 1.8" SATA devices. The limited board space will not allow plugging 2.5" devices into this connector.
Please note: SATA device 1 can**not** be used if SATA device 0 is equipped with a 2.5" SATA device.

Table 18: S5: SATA Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
S1	GND	+3.3V	P1
S2	RTM_SATA1-Rx_P	+3.3V	P2
S3	RTM_SATA1-Rx_N	+3.3V	P3
S4	GND	GND	P4
S5	RTM_SATA1-Tx_N	GND	P5
S6	RTM_SATA1-Tx_P	GND	P6
S7	GND	+5V	P7
		+5V	P8
		+5V	P9
		GND	P10
		SATA1_DSS	P11
		GND	P12

4.2.13S6: Front Panel Micro USB Connector

Front panel connector S6 is connected to the USB interface of the Atmel Atmega 16U2 that converts the serial console interface of the MCF54452 into a standard USB CDC interface.

Table 19: S6: Front Panel Micro USB Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	VBUS	USB_DM	2
3	USB_DP	NC	4
5	GND		

4.2.14SW1: Hot Swap Switch

Switch SW1 is used to support hot swapping of the module. It conforms to the PICMG AMC.0 specification.

4.2.15DIL SW2: SATA Present

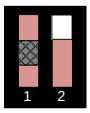
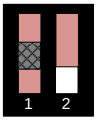
Switch DIL SW2 is used to inform the **NAT-MCH** which SATA device is present or not. There is no other (auto-) detecting mechanism that allows the **NAT-MCH** to detect the presence of a SATA device. Basically the MCMC will request more power if a SATA device is present.

The tables below give an overview of the operating parameters configurable via DIL SW2.

Table 20: DIL SW2: Switch 1 – SATA Present

DIL SW2 – Switch 1	Function
	SATA device 0 present
	SATA device 0 **not** present

Table 21: DIL SW2: Switch 2 – SATA Present

DIL SW2 – Switch 2	Function
	SATA device 1 present
	SATA device 1 **not** present

5 NAT-MCH-M4 BASE-Module Programming Notes

Please refer to the **NAT-MCH** User's Manual for programming notes.

6 Board Specification

Table 22: NAT-MCH-M4 BASE-Module – Features

Processor	ColdFire MCF54452 (266 MHz)
MCH-Module	standard MicroTCA MCH-Module, double width, full-size height
Front-I/O	3 RJ45 connectors, 1 Micro-USB connector and up to 2 clock in/output connectors, depending on the chosen external clock transceiver module.
Main Memory	32/64 MByte DDR2RAM
Flash PROM	16/32/64 MByte Flash PROM, on board programmable
Firmware	OK1, Carrier Manager, Shelf Manager
Power Consumption	12V / 700mA typ. (only **NAT-MCH-M4 BASE-Module,** equipped SATA devices will increase power consumption!)
Operating Temperature	0°C – +55°C with forced cooling
Storage Temperature	-40°C - +85°C
Humidity	10% – 90% rh non-condensing
Standards compliance	PICMG AMC.0 Rev. 2.0 PICMG AMC.2 Rev. 1.0 PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format) IPMI Specification V1.5 Rev. 1.0 PICMG µTCA.0 Rev. 1.0 PICMG MicroTCA.4 Rev. 1.0

7 Installation

7.1 Safety Note

To ensure proper functioning of the **NAT-MCH-M4 BASE-Module** during its usual life-time take the following precautions before handling the board.

CAUTION
Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime.

- Before installing or uninstalling the **NAT-MCH-M4 BASE-Module** read this installation section
- Before installing or uninstalling the **NAT-MCH-M4 BASE-Module** read the Installation Guide and the User's Manual of the MicroTCA system the board will be plugged into.
- Before installing or uninstalling the **NAT-MCH-M4 BASE-Module** on a backplane:
  - **-** Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - - Take those steps.
  - - Finally turn on or off the power if necessary.
  - - Make sure the part to be installed / removed is hot swap capable, if you do not switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NAT-MCH-M4 BASE-Module** is connected to the MicroTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

7.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up check this section for installation prerequisites and requirements

7.2.1 Requirements

The installation requires only

- an µTCA backplane for connecting the **NAT-MCH-M4 BASE-Module**
- power supply
- cooling devices

7.2.2 Power Supply

The power supply for the **NAT-MCH-M4 BASE-Module** must meet the following specifications:

- required for the module: +12 V / 700mA typ. (only **NAT-MCH-M4 BASE-Module**)

7.2.3 Automatic Power Up

In the following situations the **NAT-MCH-M4 BASE-Module** will automatically be reset and proceed with a normal power up.

- The voltage sensor generates a reset when +12 V voltage level drops below 8 V

7.3 Statement on Environmental Protection

7.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

7.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

7.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

7.3.4 Product Safety

The board complies with EN60950 and UL1950.

7.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

8 Known Bugs / Restrictions

ERR001: Hardware version 1.1 does not have the mounting holes for half-sized 1.8” SATA devices at the correct position.

Appendix A: Reference Documentation

[1] Freescale, MCF54452 ColdFire® CF4e Core Users Manual, 06/2001, Rev. 0
[2] Altera, Cyclone Device Handbook, 02/2005
[5] Broadcom, BCM5461S 10/100/1000Base-T Gigabit Ethernet Transceiver, 12/2005

Appendix B: Document's History

Revision	Date	Description	Author
1.0	08.05.2013	initial revision	ks
1.1	20.05.2013	Phone and fax updated, words updated Updated Pinout of RJ45-Console connector	Fh Ks
1.2	06.02.2014	Adaption to new Layout Minor changes in wording etc. Updates: pin assignments, LED status	se
	30.06.2014	Update chapter 7.3 RoHS-Directive / REACH	SE