NAT-MCH
µTCA Telecom MCH Module
Technical Reference Manual V 1.0
HUB-Module PCIe-x80
HW Revision 1.0

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by 0x.
The following table gives a list of the abbreviations used in this document:

Table 1: **List of used Abbreviations**

Abbreviation	Description
AMC	Advanced Mezzanine Card
CPU	Central Processing Unit
CU	Cooling Unit
EEPROM	Electrically Erasable PROM
FPGA	Field Programmable Gate Array
I²C	Inter-Integrated Circuit
IPMI	Intelligent Platform Management Interface
LED	Light Emitting Diode
µC	Microcontroller
µTCA/MTCA	Micro Telecommunications Computing Architecture
MCH	µTCA/MTCA Carrier Hub
(P)ROM	(Programmable) Read Only Memory
PCB	Printed Circuit Board
PCI(e)	Peripheral Component Interconnect (Express)
PM	Power Module
QoS	Quality of Service
RTM	Rear Transition Module
SRIO	Serial Rapid I/O
SPI (FLASH)	Serial Peripheral Interface (FLASH)
XAUI	10 GbE (via 4x 3.125 GB/s)

1 Introduction

The **NAT-MCH-M4** consists of a **BASE-Module**, which can be expanded with additional PCBs. The **BASE-Module** satisfies the basic requirements of the MicroTCA Specification for a MicroTCA Carrier Hub. The main capabilities of the **BASE-Module** are:

- management of up to 13 AMCs, two cooling units (CUs) and up to four power modules (PMs)
- Gigabit Ethernet Hub Function for Fabric A (up to 12 AMCs) and for the Update Fabric A to a second (redundant) **NAT-MCH**

Please note: The **NAT-MCH** supports either up to 13 AMCs ***OR*** up to 12 AMCs ***AND*** a second (redundant) **NAT-MCH**.

To meet also the optional requirements of the MicroTCA specification, a **CLK-Module** and different **HUB-Modules** are available. With the **CLK-Module** the following functions can be enabled:

- generation and distribution of synchronized clock signals for up to 12 AMCs

The **NAT-MCH-M4** is targeting especially MicroTCA.4 systems or applications. Therefore it complies with the full-height double-width form factor, whereas the "standard" **NAT-MCH** conforms to the full-height single-width form factor. In addition to the different form factor the **NAT-MCH-M4** is featuring the Zone3 connectors defined by the MTCA.4 that are needed to support MTCA.4 **RTMs** (Rear Transition Modules).

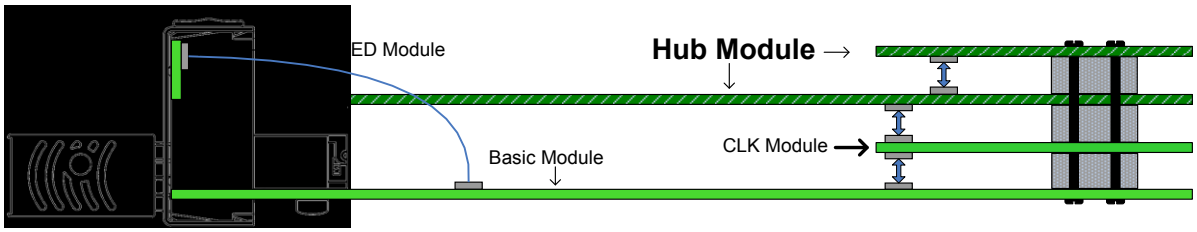
Through the extension of the **NAT-MCH-M4** with a **HUB-Module**, hub functions for fabric D to G can be enabled. With the different versions the customers have the opportunity to choose a **HUB-Module** that fits best to their applications. The versions differ in the supported protocols:

- PCI Express (GenI or GenIII)
- Serial Rapid IO (GenI or GenII)
- 10Gigabit Ethernet (XAUI)

The features of the individual modules are described in more detail in the corresponding Technical Reference Manuals.

A general arrangement of the different modules of a **NAT-MCH-M4** is shown in the following figure

Figure 1: **Arrangement of different NAT-MCH-M4 Modules**



This Technical Reference Manual describes the **NAT-MCH HUB-Module PCIe-x80**. In addition to the **CLK-Module** it can be mounted on the **NAT-MCH-M4 BASE-Module**. With the **NAT-MCH HUB-Module PCIe-x80** the 3rd tongue and 4th tongue of the **NAT-MCH** connector to the MicroTCA backplane is installed.

2 Overview

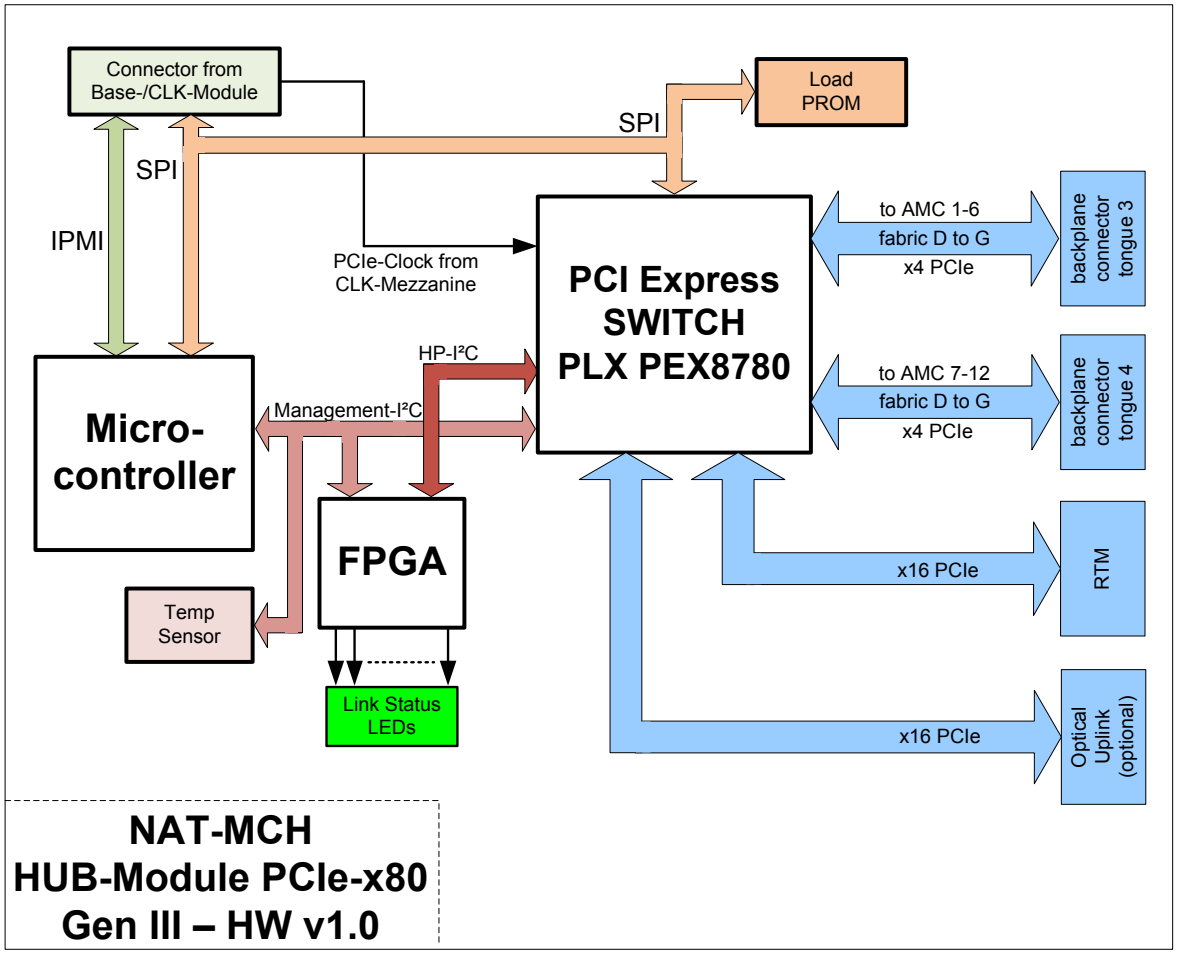
2.1 Major Features

- PLX PEX8780 PCI Express switch
  - 80 lanes
  - non-blocking switching at full line rate
  - Quality of Service (QoS)
  - 2 virtual cannels and 8 traffic classes per port supported
  - Configuration of every port as upstream port
  - Clustering support – up to four clusters can be operated individually, each having its own Root Complex
- Lattice MachXO2 FPGA
- PCIe x1, x4, x8 and x16 switching function
- PCIe compliant Spread Spectrum Clocking (optional)

2.2 Block Diagram

The following figure shows a block diagram of the **NAT-MCH HUB-Module PCIe-x80**.

Figure 2: **NAT-MCH HUB-Module PCIe-x80 – Block Diagram**



2.3 Location Diagram

The following location diagram of the **NAT-MCH HUB-Module PCIe-x80** shows the position of important components.

Figure 3: **NAT-MCH HUB-Module PCIe-x80 – Location Diagram (top)**

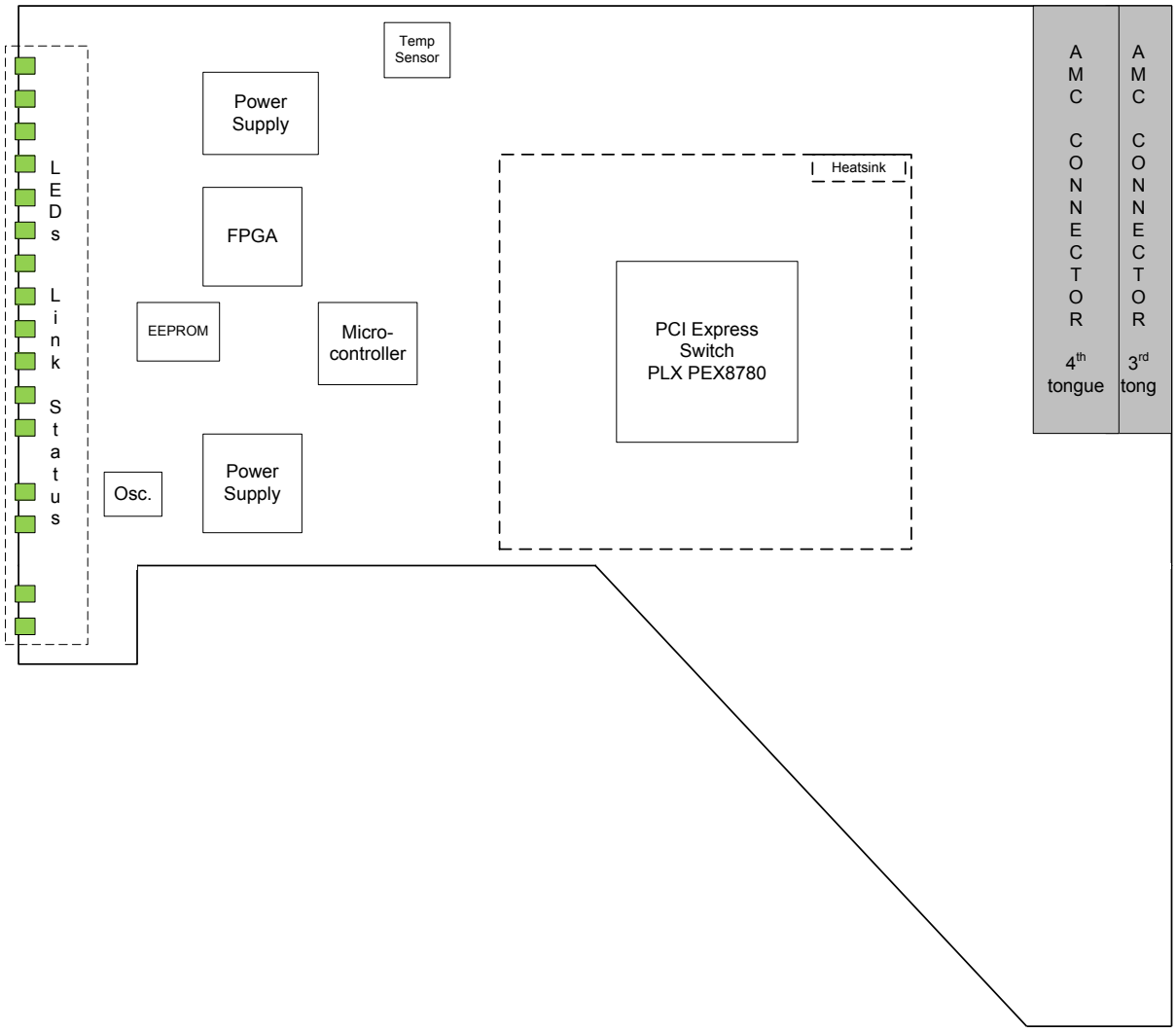
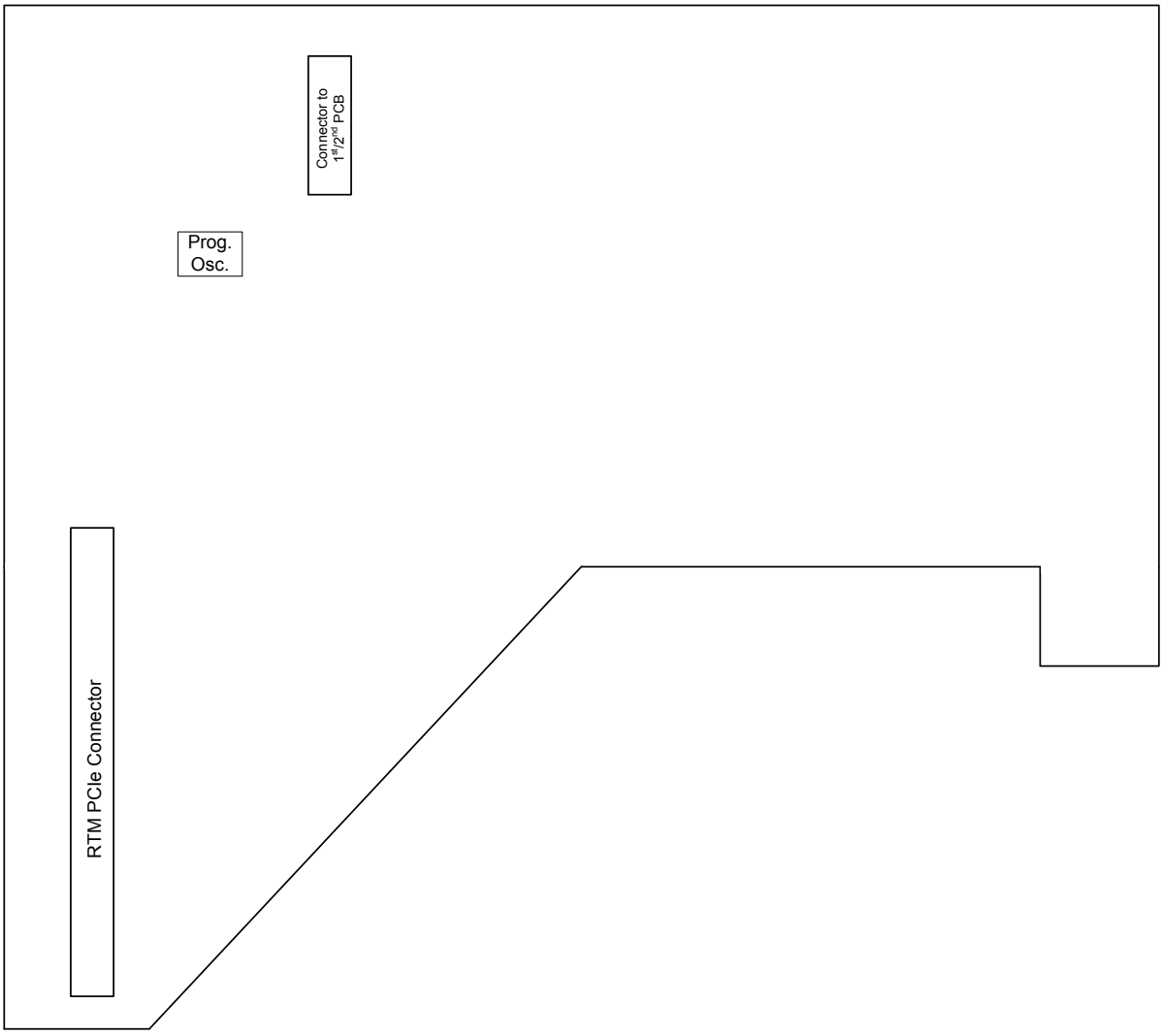


Figure 4: **NAT-MCH HUB-Module PCIe-x80 – Location Diagram (bottom)**



3 Board Features

The **NAT-MCH HUB-Module PCIe-x80** is divided into a number of functional blocks, which are described in the following paragraphs.

3.1 PCI Express Switch PLX PEX8780

The **NAT-MCH HUB-Module PCIe-x80** is equipped with a PLX PEX8780 PCI Express switch, which provides non-blocking switching at full line rate. Quality of Service (QoS) is provided by the PEX8780, supporting 2 virtual cannels and 8 traffic classes per port. Every switch port can be configured as upstream port.

The PLX PEX8780 supports up to 20 ports (depending on configuration), per default with 4 lanes (PCIe x4) towards the AMC slots and 16 lanes (PCIe x16) towards the RTM and the optional Uplink port (assembly option). As shown in Table 2: a certain switch port is not constrained to the according AMC port or MCH fabric.

The PCI Express Switch PEX8780 can be configured by strapping pins, by loading an EEPROM or by PCI Express messages from a host. A standard configuration is done by the microprocessor and resistors by setting the strapping pins. The values of the strapping signals that are connected to the microcontroller can be controlled by programming a register in the microcontroller.
These standard settings can be changed by reading the EEPROM after a reset or by receiving PCI Express messages from a host.
The EEPROM contains basic configuration information for the PCIe switch as well as user settings, e.g. upstream port settings. The user settings can be changed by the CPU on the **NAT-MCH BASE-Module**.

The /PERST pin is also connected to the microcontroller. The value of this pin can also be controlled by programming a register in the microcontroller.

Table 2: **PCIe Switch Lane to MCH Fabric / AMC Port Mapping**

Switch Lanes	Switch Port	MCH Fabric	AMC Slot # / Uplink
0	0	G-10	10
1		F-10	
2		E-10	
3		D-10	
4	1	G-4	4
5		F-4	
6		E-4	
7		D-4	
8	2	G-9	9
9		F-9	
10		E-9	
11		D-9	
12	3	G-3	3
13		F-3	
14		E-3	
15		D-3	
16	4	G-12	12
17		F-12	
18		E-12	
19		D-12	
20	5	G-6	6
21		F-6	
22		E-6	
23		D-6	
24	6	G-11	11
25		F-11	
26		E-11	
27		D-11	
28	7	G-5	5
29		F-5	
30		E-5	
31		D-5	
32	8	G-8	8
33		F-8	
34		E-8	
35		D-8	
36	9	G-2	2
37		F-2	
38		E-2	
39		D-2	
40	10	G-7	7
41		F-7	
42		E-7	
43		D-7	

Switch Lanes	Switch Port		MCH Fabric	AMC Slot # / Uplink	
44	11		G-1	1	
45			F-1		
46			E-1		
47			D-1		
48	12		RTM-15	Uplink via RTM	
49			RTM-14		
50			RTM-13		
51			RTM-12		
52			RTM-11		
53			RTM-10		
54			RTM-9		
55			RTM-8		
56			RTM-7		
57			RTM-6		
58			RTM-5		
59			RTM-4		
60			RTM-3		
61			RTM-2		
62			RTM-1		
63			RTM-0		
64	16	16	UpLNK1-0	Front Uplink1	Front Uplink1
65			UpLNK1-1		
66			UpLNK1-2		
67			UpLNK1-3		
68			UpLNK1-4		
69			UpLNK1-5		
70			UpLNK1-6		
71			UpLNK1-7		
72		17	UpLNK1-8 / UpLNK2-0		Front Uplink2
73			UpLNK1-9 / UpLNK2-1		
74			UpLNK1-10 / UpLNK2-2		
75			UpLNK1-11 / UpLNK2-3		
76			UpLNK1-12 / UpLNK2-4		
77			UpLNK1-13 / UpLNK2-5		
78			UpLNK1-14 / UpLNK2-6		
79			UpLNK1-15 / UpLNK2-7		

This table shows the standard configuration:
Switch ports to AMC slots: PCIe x4-Link
Switch ports Uplink ports: PCIe x16-Link

3.2 Microcontroller

For configuration of the PCIe switch and for providing hot-swap functionality, an 8-bit Atmel microcontroller resides on the **NAT-MCH HUB-Module PCIe-x80**. The microcontroller can be updated by the CPU on the **NAT-MCH BASE-Module** via SPI interface. Normal communication between the CPU and the microcontroller is done by IPMI messages over the I²C interface.

The strapping options and the reset signal of the switch can be controlled by programming registers in the microcontroller. Also the PCIe Hot-Plug signals can be served by the microcontroller.

Furthermore, three temperature sensors are connected to a second I²C bus of the microcontroller. The microcontroller makes these sensors accessible to the CPU on the **NAT-MCH BASE-Module** via IPMI.

3.3 FPGA

The Lattice MachXO2 FPGA is used to emulate a set of I^2C port expanders that the PLX switch normally uses to extend its pins for PCIe Hotplug support on all ports. The FPGA implements an I^2C interface towards the PLX switch and behaves as if there were 12 I^2C port expenders connected.
Further it implements a second interface towards the Atmel µC, so that the Hotplug signals finally can be exchanged with the MCH main firmware.

3.4 PCIe Interfaces

The **NAT-MCH HUB-Module PCIe-x80** implements interfaces to connect fabrics D to G of up to 12 AMCs (PCIe x4), an **RTM-Module** (PCIe x16) and an optional Optical Uplink (PCIe x16).

3.5 Interface to NAT-MCH BASE-Module

The Microcontroller on the **NAT-MCH HUB-Module PCIe-x80** can be updated by the CPU on the **NAT-MCH BASE-Module** via SPI interface. Normal communication between Microprocessor and CPU is done by IPMI messages via I²C interface.
A configuration EEPROM for the PCIe Switch resides on the **NAT-MCH HUB-Module PCIe-x80**. This EEPROM can be programmed / updated by the CPU of the **NAT-MCH BASE-Module** via SPI interface.

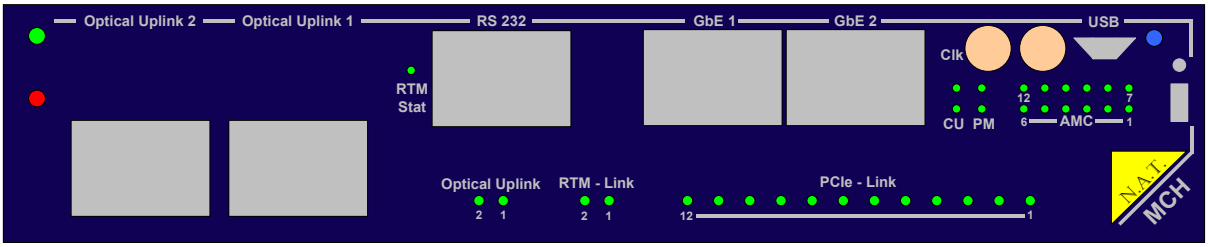
3.6 Interface to NAT-MCH CLK-Module

The **NAT-MCH CLK-Module** can provide the 100 MHz PCI Express compliant clock signal to the **NAT-MCH HUB-Module PCIe-x80**.

4 Hardware

4.1 LEDs

Figure 5: **NAT-MCH with HUB-Module PCIe-x80 – Front Plate**



The **NAT-MCH HUB-Module PCIe-x80** features several green LEDs which reflect the PCIe-Link Status.

PCIe-Link 1-12: PCIe-Link Status of AMC 1-12.
RTM-Link 1: PCIe-Link Status of RTM
RTM-Link 2: tbd
Optical Uplink 1: PCIe-Link Status of Optical Uplink 1*
Optical Uplink 2: PCIe-Link Status of Optical Uplink 2**

Please note:
* Optical Uplink 1/2 is available as assembly option.
** This LED is used only, if the Upstream Port is set up as two x8-Links. If configured as one x16-Link, the second LED is not used.

The behaviour is common to all PCIe-Link-LEDs, they can take the following states:

Table 3: **LED State – Link Status**

LED State	Link Status
OFF	No PCIe link established
SLOW BLINK (1 blink/second)	PCIe GEN1 Link (2.5 GBaud)
FAST BLINK (2 blinks/second)	PCIe GEN2 Link (5 GBaud)
SOLID ON	PCIe GEN3 (8 GBaud)

4.2 Connectors

Figure 6: **NAT-MCH HUB-Module PCIe-x80 – Connectors (top)**

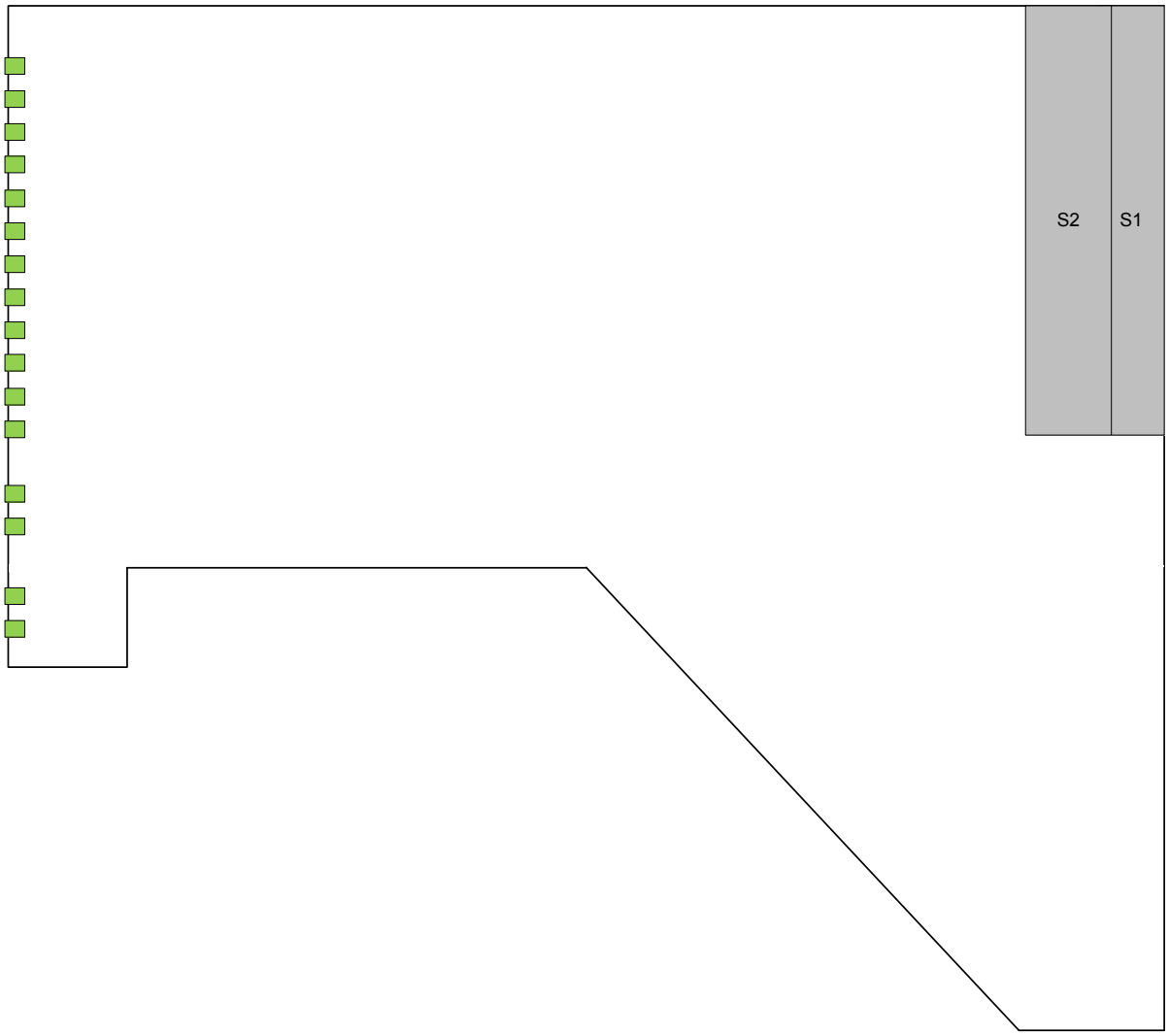
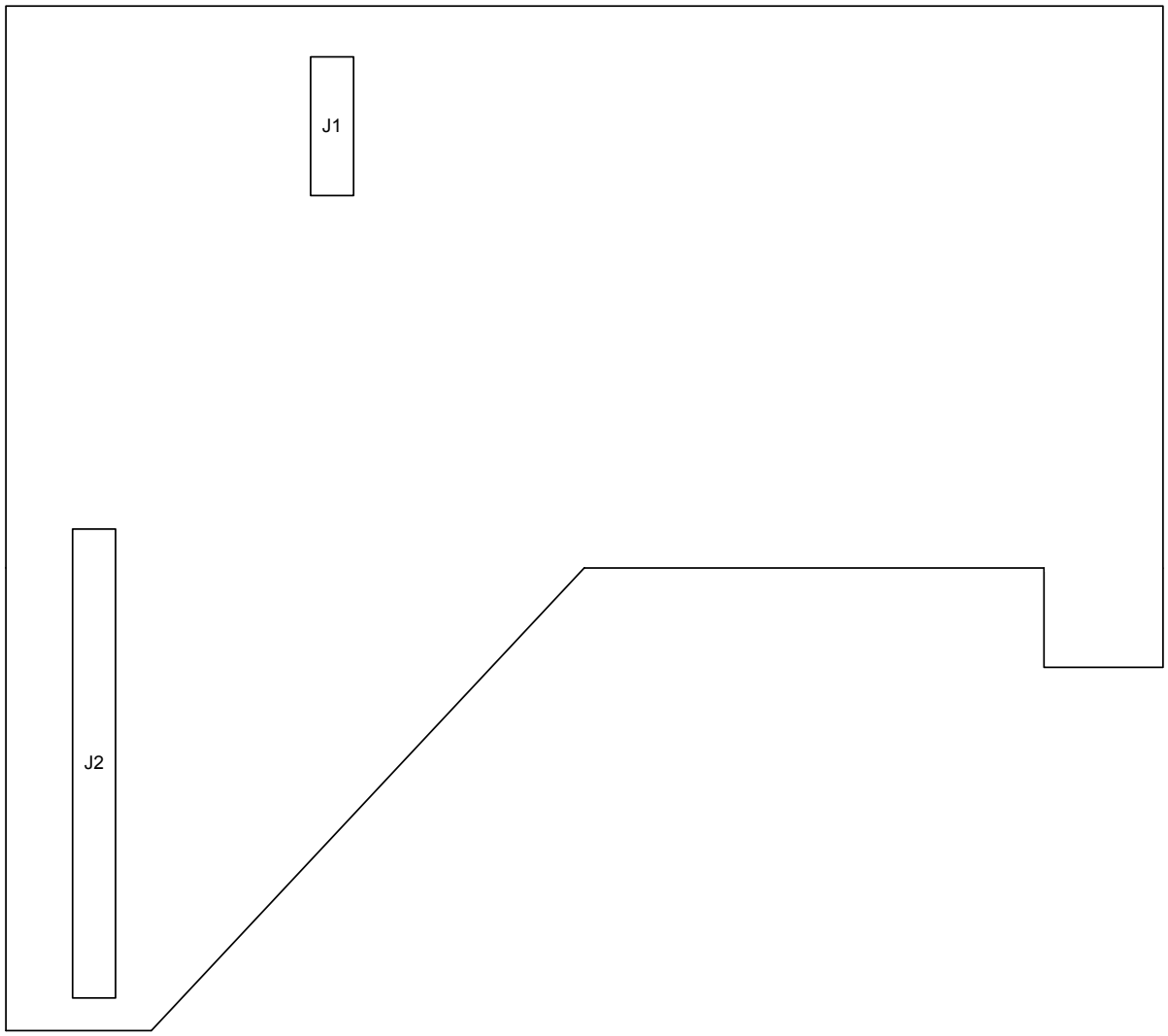


Figure 7: **NAT-MCH HUB-Module PCIe – Connectors (bottom)**



Please refer to the following tables to look up the pin assignment of the **NAT-MCH HUB-Module PCIe-x80**.

4.2.1 S1: MCH Connector to 3rd tongue

Table 4: **S1: MCH Connector to 3rd tongue – Pin Assignment**

Pin #	MCH-Signal	MCH-Signal	Pin #
1	GND	GND	170
2	RSVD	RSVD	169
3	RSVD	RSVD	168
4	GND	GND	167
5	RSVD	RSVD	166
6	RSVD	RSVD	165
7	GND	GND	164
8	NC	NC	163
9	NC	NC-	162
10	GND	GND	161
11	NC	NC	160
12	NC	NC	159
13	GND	GND	158
14	TxFD1+	RxFD1+	157
15	TxFD1-	RxFD1-	156
16	GND	GND	155
17	TxFE1+	RxFE1+	154
18	TxFE1-	RxFE1-	153
19	GND	GND	152
20	TxFF1+	RxFF1+	151
21	TxFF1-	RxFF1-	150
22	GND	GND	149
23	TxFG1+	RxFG1+	148
24	TxFG1-	RxFG1-	147
25	GND	GND	146
26	TxFD2+	RxFD2+	145
27	TxFD2-	RxFD2-	144
28	GND	GND	143
29	TxFE2+	RxFE2+	142
30	TxFE2-	RxFE2-	141
31	GND	GND	140
32	TxFF2+	RxFF2+	139
33	TxFF2-	RxFF2-	138
34	GND	GND	137
35	TxFG2+	RxFG2+	136
36	TxFG2-	RxFG2-	135
37	GND	GND	134
38	TxFD3+	RxFD3+	133
39	TxFD3-	RxFD3-	132
40	GND	GND	131
41	TxFE3+	RxFE3+	130
42	TxFE3-	RxFE3-	129
43	GND	GND	128
44	TxFF3+	RxFF3+	127
45	TxFF3-	RxFF3-	126

Pin #	MCH-Signal	MCH-Signal	Pin #
46	GND	GND	125
47	TxFG3+	RxFG3+	124
48	TxFG3+	RxFG3-	123
49	GND	GND	122
50	TxFD4+	RxFD4+	121
51	TxFD4-	RxFD4-	120
52	GND	GND	119
53	TxFE4+	RxFE4+	118
54	TxFE4-	RxFE4-	117
55	GND	GND	116
56	TxFF4+	RxFF4+	115
57	TxFF4-	RxFF4-	114
58	GND	GND	113
59	TxFG4+	RxFG4+	112
60	TxFG4-	RxFG4-	111
61	GND	GND	110
62	TxFD5+	RxFD5+	109
63	TxFD5-	RxFD5-	108
64	GND	GND	107
65	TxFE5+	RxFE5+	106
66	TxFE5-	RxFE5-	105
67	GND	GND	104
68	TxFF5+	RxFF5+	103
69	TxFF5-	RxFF5-	102
70	GND	GND	101
71	TxFG5+	RxFG5+	100
72	TxFG5-	RxFG5-	99
73	GND	GND	98
74	TxFD6+	RxFD6+	97
75	TxFD6-	RxFD6-	96
76	GND	GND	95
77	TxFE6+	RxFE6+	94
78	TxFE6-	RxFE6-	93
79	GND	GND	92
80	TxFF6+	RxFF6+	91
81	TxFF6+	RxFF6-	90
82	GND	GND	89
83	TxFG6+	RxFG6+	88
84	TxFG6-	RxFG6-	87
85	GND	GND	86

4.2.2 S2: MCH Connector to 4th tongue

Table 5: **S2: MCH Connector to 4th tongue – Pin Assignment**

Pin #	MCH-Signal	MCH-Signal	Pin #
1	GND	GND	170
2	RSVD	RSVD	169
3	RSVD	RSVD	168
4	GND	GND	167
5	RSVD	RSVD	166
6	RSVD	RSVD	165
7	GND	GND	164
8	NC	NC	163
9	NC	NC-	162
10	GND	GND	161
11	NC	NC	160
12	NC	NC	159
13	GND	GND	158
14	TxFD7+	RxFD7+	157
15	TxFD7-	RxFD7-	156
16	GND	GND	155
17	TxFE7+	RxFE7+	154
18	TxFE7-	RxFE7-	153
19	GND	GND	152
20	TxFF7+	RxFF7+	151
21	TxFF7-	RxFF7-	150
22	GND	GND	149
23	TxFG7+	RxFG7+	148
24	TxFG7-	RxFG7-	147
25	GND	GND	146
26	TxFD8+	RxFD8+	145
27	TxFD8-	RxFD8-	144
28	GND	GND	143
29	TxFE8+	RxFE8+	142
30	TxFE8-	RxFE8-	141
31	GND	GND	140
32	TxFF8+	RxFF8+	139
33	TxFF8-	RxFF8-	138
34	GND	GND	137
35	TxFG8+	RxFG8+	136
36	TxFG8-	RxFG8-	135
37	GND	GND	134
38	TxFD9+	RxFD9+	133
39	TxFD9-	RxFD9-	132
40	GND	GND	131
41	TxFE9+	RxFE9+	130
42	TxFE9-	RxFE9-	129
43	GND	GND	128
44	TxFF9+	RxFF9+	127
45	TxFF9-	RxFF9-	126

Pin #	MCH-Signal	MCH-Signal	Pin #
46	GND	GND	125
47	TxFG9+	RxFG9+	124
48	TxFG9+	RxFG9-	123
49	GND	GND	122
50	TxFD10+	RxFD10+	121
51	TxFD10-	RxFD10-	120
52	GND	GND	119
53	TxFE10+	RxFE10+	118
54	TxFE10-	RxFE10-	117
55	GND	GND	116
56	TxFF10+	RxFF10+	115
57	TxFF10-	RxFF10-	114
58	GND	GND	113
59	TxFG10+	RxFG10+	112
60	TxFG10-	RxFG10-	111
61	GND	GND	110
62	TxFD11+	RxFD5+	109
63	TxFD11-	RxFD5-	108
64	GND	GND	107
65	TxFE11+	RxFE5+	106
66	TxFE11-	RxFE5-	105
67	GND	GND	104
68	TxFF11+	RxFF11+	103
69	TxFF11-	RxFF11-	102
70	GND	GND	101
71	TxFG11+	RxFG11+	100
72	TxFG11-	RxFG11-	99
73	GND	GND	98
74	TxFD12+	RxFD12+	97
75	TxFD12-	RxFD12-	96
76	GND	GND	95
77	TxFE12+	RxFE12+	94
78	TxFE12-	RxFE12-	93
79	GND	GND	92
80	TxFF12+	RxFF12+	91
81	TxFF12+	RxFF12-	90
82	GND	GND	89
83	TxFG12+	RxFG12+	88
84	TxFG12-	RxFG12-	87
85	GND	GND	86

4.2.3 J1: Connector to NAT-MCH CLK/BASE-Module

Table 6: **J1: Connector to NAT-MCH CLK/BASE-Module – Pin Assignment**

Pin #	Signal	Signal	Pin #
1	INT1	INT2	2
3	GND	GND	4
5	BASE_TA_N	BASE_RA_N	6
7	BASE_TA_P	BASE_RA_N	8
9	+12V	+12V	10
11	+12V	+12V	12
13	PCIeCLK_HUB_P	NC	14
15	PCIeCLK_HUB_N	SPICLK	16
17	GND	NC	18
19	MOSI	MISO	20
21	GND	/SPISEL_HUBPCB	22
23	SCL	NC	24
25	SDA	/RESET_HUBPCB	26
27	GND	GND	28

J1 connects to the **NAT-MCH CLK-Module**; on the **CLK-Module** these signals are routed via another connector to the **NAT-MCH-M4 BASE-Module**.

4.2.4 J2: RTM-PCIe-Connector

Connector J2 connects to the **NAT-MCH-M4 BASE-Module** which routes the PCIe-Lanes towards the **RTM-Module**.

Table 7: **J2: RTM-PCIe-Connector – Pin Assignment**

Pin #	Signal	Signal	Pin #
1	GND	GND	2
3	UpLNK_ETH0-Tx_P	UpLNK_ETH0-Rx_P	4
5	UpLNK_ETH0-Tx_N	UpLNK_ETH0-Rx_N	6
7	GND	GND	8
9	UpLNK_ETH1-Tx_P	UpLNK_ETH1-Rx_P	10
11	UpLNK_ETH1-Tx_N	UpLNK_ETH1-Rx_N	12
13	GND	GND	14
15	RTM_CONo	RTM_CON1	16
17	GND	GND	18
19	RTM_CLK1_P	RTM_CLK0_P	20
21	RTM_CLK1_N	RTM_CLK0_N	22
23	GND	GND	24
25	RTM_PCIe00-Tx_P	RTM_PCIe00-Rx_P	26
27	RTM_PCIe00-Tx_N	RTM_PCIe00-Rx_N	28
29	GND	GND	30
31	RTM_PCIe01-Tx_P	RTM_PCIe01-Rx_P	32
33	RTM_PCIe01-Tx_N	RTM_PCIe01-Rx_N	34
35	GND	GND	36
37	RTM_PCIe02-Tx_P	RTM_PCIe02-Rx_P	38

Pin #	Signal	Signal	Pin #
39	RTM_PCIe02-Tx_N	RTM_PCIe02-Rx_N	40
41	GND	GND	42
43	RTM_PCIe03-Tx_P	RTM_PCIe05-Rx_P	44
45	RTM_PCIe03-Tx_N	RTM_PCIe05-Rx_N	46
47	GND	GND	48
49	RTM_PCIe03-Rx_P	RTM_PCIe06-Rx_P	50
51	RTM_PCIe03-Rx_N	RTM_PCIe06-Rx_N	52
53	GND	GND	54
55	RTM_PCIe04-Rx_P	RTM_PCIe07-Rx_P	56
57	RTM_PCIe04-Rx_N	RTM_PCIe07-Rx_N	58
59	GND	GND	60
61	RTM_PCIe04-Tx_P	RTM_PCIe06-Tx_P	62
63	RTM_PCIe04-Tx_N	RTM_PCIe06-Tx_N	64
65	GND	GND	66
67	RTM_PCIe05-Tx_P	RTM_PCIe07-Tx_P	68
69	RTM_PCIe05-Tx_N	RTM_PCIe07-Tx_N	70
71	GND	GND	72
73	RTM_PCIe08-Rx_P	RTM_PCIe09-Rx_P	74
75	RTM_PCIe08-Rx_N	RTM_PCIe09-Rx_N	76
77	GND	GND	78
79	RTM_PCIe10-Rx_P	RTM_PCIe11-Rx_P	80
81	RTM_PCIe10-Rx_N	RTM_PCIe11-Rx_N	82
83	GND	GND	84
85	RTM_PCIe08-Tx_P	RTM_PCIe12-Rx_P	86
87	RTM_PCIe08-Tx_N	RTM_PCIe12-Rx_N	88
89	GND	GND	90
91	RTM_PCIe09-Tx_P	RTM_PCIe13-Rx_P	92
93	RTM_PCIe09-Tx_N	RTM_PCIe13-Rx_N	94
95	GND	GND	96
97	RTM_PCIe10-Tx_P	RTM_PCIe14-Rx_P	98
99	RTM_PCIe10-Tx_N	RTM_PCIe14-Rx_N	100
101	GND	GND	102
103	RTM_PCIe11-Tx_P	RTM_PCIe15-Rx_P	104
105	RTM_PCIe11-Tx_N	RTM_PCIe15-Rx_N	106
107	GND	GND	108
109	RTM_PCIe12-Tx_P	RTM_PCIe14-Tx_P	110
111	RTM_PCIe12-Tx_N	RTM_PCIe14-Tx_N	112
113	GND	GND	114
115	RTM_PCIe13-Tx_P	RTM_PCIe15-Tx_P	116
117	RTM_PCIe13-Tx_N	RTM_PCIe15-Tx_N	118
119	GND	GND	120

5 Programming Notes

5.1 SPI Interface

The SPI interface on the **NAT-MCH HUB-Module PCIe-x80** can be connected in two different ways.

5.1.1 SPI-Interface – Default mode

In Default mode the SPI interface establishes a connection between the CPU on the **BASE-Module** and the Atmel microcontroller for maintenance purposes, e.g. microcontroller firmware update.
At the same time the PCIe Switch PEX8780 is connected to the load PROM.

5.1.2 SPI-Interface – Update mode

In Update mode the SPI Bus connects the CPU on the **BASE-Module** with the load PROM. In this case data is read from or written to the PROM.

5.2 I²C Interface

The I²C interface is the main communication interface between the microcontroller and the CPU of the **NAT-MCH BASE-Module**. All communication is based on IPMI messages.

5.3 Register

A register interface is implemented in the Atmel microcontroller. With the help of this interface different functions can be controlled and various identification values can be read.

5.3.1 Board Identifier Register

The Board Identifier Register contains the Board ID that identifies the board as **NAT-MCH HUB-Module PCIe-x80**.

Table 8: **Board Identifier Register**

Board Identifier - Address 0x00								
Default value 0xbc								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	**BOARD_ID**							

5.3.2 PCB Revision Register

The PCB Revision Register contains the revision code of the **NAT-MCH HUB-Module PCIe-x80**.

Table 9: **PCB Revision Register**

PCB Revision - Address 0x01								
Default value 0x10								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	**PCB_REV**							

5.3.3 Atmel Version

The Atmel Version Register contains the revision of the firmware, which is running on the Atmel on the **NAT-MCH HUB-Module PCIe-x80**.

Table 10: **Atmel Revision Register**

Atmel Version - Address 0x02								
Default value 0x10								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	**Atmel_vers**							

6 Board Specification

Table 11: **NAT-MCH HUB-Module PCIe-x80 Features**

Power Consumption	12V/4.3A max. - 12V/1.5A typ. (only **NAT-MCH HUB-Module PCIe-x80**)
Operating Temperature	0°C – +50°C with forced cooling
Storage Temperature	-40°C - +85°C
Humidity	10% – 90% rh non-condensing
Standards compliance	PCI Express Base Specification Rev. 1.1 PICMG µTCA.0 Rev. 1.0 PICMG AMC.0 Rev. 2.0 PICMG AMC.1 Rev. 1.0 PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format) IPMI Specification v2.0 Rev. 1.0

7 Installation

7.1 Safety Note

To ensure proper functioning of the **NAT-MCH HUB-Module PCIe-x80** during its usual lifetime take refer to the safety note section of the **NAT-MCH-M4 BASE-Module** Technical Reference Manual before handling the board.

7.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up check this section for installation prerequisites and requirements!

7.2.1 Requirements

The installation requires a **NAT-MCH-M4 BASE-Module** and a **NAT-MCH CLK-Module** where the **NAT-MCH HUB-Module PCIe-x80** can be mechanically fixed on to. The **NAT-MCH HUB-Module PCIe-x80** must be completely connected and joined to the complete PCB stack (**BASE-Module** and **CLK-Module**), before the **NAT-MCH** can be stacked into a MicroTCA backplane (as one device). For further requirements refer to the requirements section of the **NAT-MCH-M4 BASE-Module** Technical Reference Manual.

7.2.2 Power supply

The power supply for the **NAT-MCH HUB-Module PCIe-x80** must meet the following specifications:

- +12 V / 4.3 A max. (**NAT-MCH HUB-Module PCIe-x80** only – in addition to other PCBs of the **NAT-MCH**).

7.2.3 Automatic Power Up

Power ramping/monitoring and power up reset generation is done by the **NAT-MCH BASE-Module**

In the following situations the **NAT-MCH BASE-Module** will automatically be reset and proceed with a normal power up.

- The voltage sensor generates a reset, when +12 V voltage level drops below 8V.

7.3 Statement on Environmental Protection

7.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

7.3.2 Compliance to WEEE Directive

Directive 2012/19/EU of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2011/65/EU of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2012/19/EU of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

7.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

7.3.4 Product Safety

The board complies with EN60950 and UL1950.

7.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

8 Known Bugs / Restrictions

none

Appendix A: Reference Documentation

[1] PLX PEX8780 80-Lane, 20-Port PCI Express Gen 3 (8 GT/s) Switch, Data Book V1.0 05/2013

Appendix B: Document's History

Revision	Date	Description	Author
0.9	16.09.2014	initial release	SE
1.0	01.04.2016	Minor corrections	KS