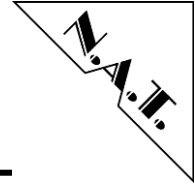


The NAT-MCH has been designed by:

**N.A.T. GmbH
Konrad-Zuse-Platz 9
D-53227 Bonn-Oberkassel**

**Phone: +49 / 228 / 965 864 - 0
Fax: +49 / 228 / 965 864 - 10**

Internet: <http://www.nateurope.com>



Disclaimer

The following documentation, compiled by N.A.T. GmbH (henceforth called N.A.T.), represents the current status of the product's development. The documentation is updated on a regular basis. Any changes which might ensue, including those necessitated by updated specifications, are considered in the latest version of this documentation. N.A.T. is under no obligation to notify any person, organization, or institution of such changes or to make these changes public in any other way.

We must caution you, that this publication could include technical inaccuracies or typographical errors.

N.A.T. offers no warranty, either expressed or implied, for the contents of this documentation or for the product described therein, including but not limited to the warranties of merchantability or the fitness of the product for any specific purpose.

In no event will N.A.T. be liable for any loss of data or for errors in data utilization or processing resulting from the use of this product or the documentation. In particular, N.A.T. will not be responsible for any direct or indirect damages (including lost profits, lost savings, delays or interruptions in the flow of business activities, including but not limited to, special, incidental, consequential, or other similar damages) arising out of the use of or inability to use this product or the associated documentation, even if N.A.T. or any authorized N.A.T. representative has been advised of the possibility of such damages.

The use of registered names, trademarks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations (patent laws, trade mark laws, etc.) and therefore free for general use. In no case does N.A.T. guarantee that the information given in this documentation is free of such third-party rights.

Neither this documentation nor any part thereof may be copied, translated, or reduced to any electronic medium or machine form without the prior written consent from N.A.T. GmbH.

This product (and the associated documentation) is governed by the N.A.T. General Conditions and Terms of Delivery and Payment.

Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

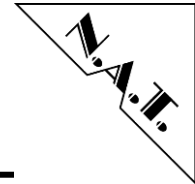
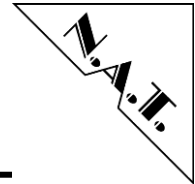
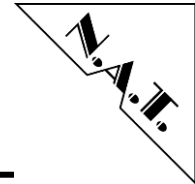


Table of Contents

TABLE OF CONTENTS	4
LIST OF TABLES	6
LIST OF FIGURES	6
CONVENTIONS	7
1 INTRODUCTION	8
2 OVERVIEW	9
2.1 MAJOR FEATURES	9
2.2 BLOCK DIAGRAM	10
2.3 LOCATION DIAGRAM	11
3 BOARD FEATURES	12
3.1 CPU	12
3.2 MEMORY	12
3.2.1 <i>DDR2SDRAM</i>	12
3.2.2 <i>FLASH</i>	12
3.3 BACKPLANE INTERFACES	13
3.3.1 <i>IPMB</i>	13
3.3.2 <i>I²C</i>	13
3.3.3 <i>Ethernet</i>	13
3.4 FRONT PANEL INTERFACES	13
3.4.1 <i>Ethernet Uplink Ports</i>	13
3.4.2 <i>USB Debug Port</i>	14
3.4.3 <i>Clock Interface</i>	14
3.4.3.1 <i>Coax-IO</i>	14
3.4.3.2 <i>RJ45-Clock-Interface</i>	15
3.5 INTERFACE TO EXTENSION MODULES	15
3.5.1 <i>NAT-MCH CKL-Module / NAT-MCH CLK-PHYS-Module</i>	15
3.5.2 <i>NAT-MCH HUB-Module</i>	15
3.6 <i>I²C</i> DEVICES	16
3.7 ETHERNET SWITCH	16
4 HARDWARE	17
4.1 FRONT PANEL AND LEDs	17
4.1.1 <i>MCH Basic-LEDs</i>	17
4.1.2 <i>RJ45-LEDs</i>	17
4.1.3 <i>Status LEDs</i>	17
4.2 CONNECTORS AND SWITCHES	18
4.2.1 <i>CON1: MCH Connector</i>	19
4.2.2 <i>CON2: Extension Module Connector</i>	21
4.2.3 <i>JP1: Altera FPGA Programming Port</i>	21
4.2.4 <i>JP2: LED-Module Connector</i>	21
4.2.5 <i>JP3: Development Connector</i>	22
4.2.6 <i>P3: External Clock Transceiver Module Connector</i>	22
4.2.7 <i>SW1: Hot Swap Switch</i>	22
4.2.8 <i>SW2: General Purpose DIL Switch</i>	22
4.2.9 <i>S1: Micro USB Connector</i>	23



4.2.10	<i>S100: RJ45 Connector</i>	23
4.2.11	<i>S101: RJ45 Connector</i>	23
5	PROGRAMMING NOTES	24
6	BOARD SPECIFICATION	25
7	INSTALLATION	26
7.1	SAFETY NOTE	26
7.2	INSTALLATION PREREQUISITES AND REQUIREMENTS	27
7.2.1	<i>Requirements</i>	27
7.2.2	<i>Power Supply</i>	27
7.2.3	<i>Automatic Power Up</i>	27
7.3	STATEMENT ON ENVIRONMENTAL PROTECTION	28
7.3.1	<i>Compliance to RoHS Directive</i>	28
7.3.2	<i>Compliance to WEEE Directive</i>	28
7.3.3	<i>Compliance to CE Directive</i>	29
7.3.4	<i>Product Safety</i>	29
8	KNOWN BUGS / RESTRICTIONS	30
APPENDIX A: REFERENCE DOCUMENTATION		31
APPENDIX B: DOCUMENT'S HISTORY		32

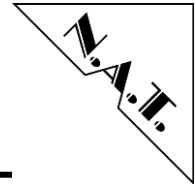


List of Tables

Table 1:	List of used Abbreviations	7
Table 2:	NAT-MCH BASE-Module – Coax-IO signal mapping	15
Table 3:	NAT-MCH BASE-Module – Coax-IO Electrical characteristics	15
Table 4:	CON1: MCH Connector – Pin-Assignment	19
Table 5:	CON2: Extension Module Connector – Pin Assignment	21
Table 6:	JP1: Altera FPGA Programming Port – Pin Assignment	21
Table 7:	JP2: LED-Module Connector – Pin Assignment	21
Table 8:	JP3: Development Connector – Pin Assignment	22
Table 9:	P3: External Clock Transceiver Module Connector – Pin Assignment	22
Table 10:	S1: Micro USB Connector – Pin Assignment.....	23
Table 11:	S100: RJ45 Connector – Pin-Assignment	23
Table 12:	S101: RJ45 Connector – Pin-Assignment – GbE-Interface	23
Table 13:	S101: RJ45 Connector – Pin-Assignment – RJ45-Clock-Interface	23
Table 14:	NAT-MCH BASE-Module – Features	25

List of Figures

Figure 1:	NAT-MCH BASE-Module – Block Diagram incl. LED Module	10
Figure 2:	NAT-MCH BASE-Module – Location Diagram – top-view	11
Figure 3:	NAT-MCH BASE-Module – Front Panel.....	17
Figure 4:	NAT-MCH BASE-Module – Connectors – Overview	18



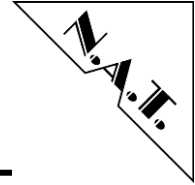
Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.

The following table gives a list of the abbreviations used in this document:

Table 1: List of used Abbreviations

Abbreviation	Description
AMC	Advanced Mezzanine Card
b	bit, binary
B	Byte
ColdFire	MCF54452
CPU	Central Processing Unit
CU	Cooling Unit
DMA	Direct Memory Access
E1	2.048 Mbit G.703 Interface
FLASH	Programmable ROM
FRU	Field Replaceable Unit
J1	1,544 Mbit G.703 Interface (Japan)
K	kilo (factor 400 in hex, factor 1024 in decimal)
LIU	Line Interface Unit
M	mega (factor 10,000 in hex, factor 1,048,576 in decimal)
MCH	μTCA Carrier Hub
MHz	1,000,000 Herz
μTCA	Micro Telecommunications Computing Architecture
PCIe	PCI Express
PCI	Peripheral Component Interconnect
PM	Power Manager
RAM	Random Access Memory
ROM	Read Only Memory
SDRAM	Synchronous Dynamic RAM
SSC	Spread Spectrum Clock
T1	1,544 Mbit G.703 Interface (USA)



1 Introduction

The **NAT-MCH BASE-Module** satisfies the basic requirements of the MicroTCA Specification for a MicroTCA Carrier Hub. The main capabilities of the **BASE-MODULE** are:

- management of up to 12 AMCs, two cooling units (CUs) and up to four power modules (PMs)
- Gigabit Ethernet Hub Function for Fabric A (up to 12 AMCs) and for the Update Fabric A to a second (redundant) **NAT-MCH**

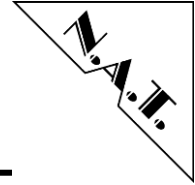
The **NAT-MCH** consists of a **BASE-MODULE**, which can be expanded with additional extension PCBs. To meet also the optional requirements of the MicroTCA specification, a **CLK-MODULE** and different **HUB-MODULEs** are available. With the **CLK-MODULE** the following functions can be enabled:

- generation and distribution of synchronized clock signals for up to 12 AMCs

By extending the **NAT-MCH** with a **HUB-MODULE**, hub functions for fabric D to G can be enabled. With the different versions the customers have the opportunity to choose a **HUB-MODULE** that fits best to their application. The versions differ in:

- max. number of supported AMCs (up to 6 / up to 12)
- supported protocols:
 - PCI Express
 - Serial Rapid IO
 - 10Gigabit Ethernet (XAUI)

The features of the individual extension PCBs are described in more detail in the corresponding Technical Reference Manuals.

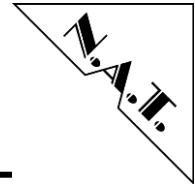


2 Overview

2.1 Major Features

- ColdFire MCF54452 32-bit CPU @266MHz
- up to 64 MB main Memory (SDRAM) - 32 bit wide
- up to 64 MB FLASH – 16 bit wide
- 12 x IPMB-L interface for AMCs
 - IPMB-L interface for a second NAT-MCH
 - IPMB-0 interface for CUs and PMs
- I²C interface on backplane to access FRU information device
- Gigabit Ethernet Hub function for fabric A
 - 1000BaseX over Backplane
 - up to 12 AMCs
 - second MCH
 - two 1000BaseT channel on front panel
 - 1000BaseX channel to MCH Hub-Module (not supported by all Hub Modules)
- USB debug port on faceplate
- RJ45-Clock-Interface
- Interface to extension PCBs (extension PCBs are optional)
 - **NAT-MCH CLK-Module**
 - **NAT-MCH CLK-PHYS-Module**
 - Various **NAT-MCH HUB-Modules** (e.g. PCIe, SRIO, XAUI)
 - Access to all extension modules via I²C and SPI; 1000BaseX for XAUI only!
- 100Mbit Ethernet interface between CPU and Ethernet switch for:
 - communication with external Shelf or System Manager
 - software update
- Various status LEDs
 - 12 bicolour LEDs for AMC status information
 - 2 bicolour LEDs for CU status information
 - 2 bicolour LEDs for PM status information

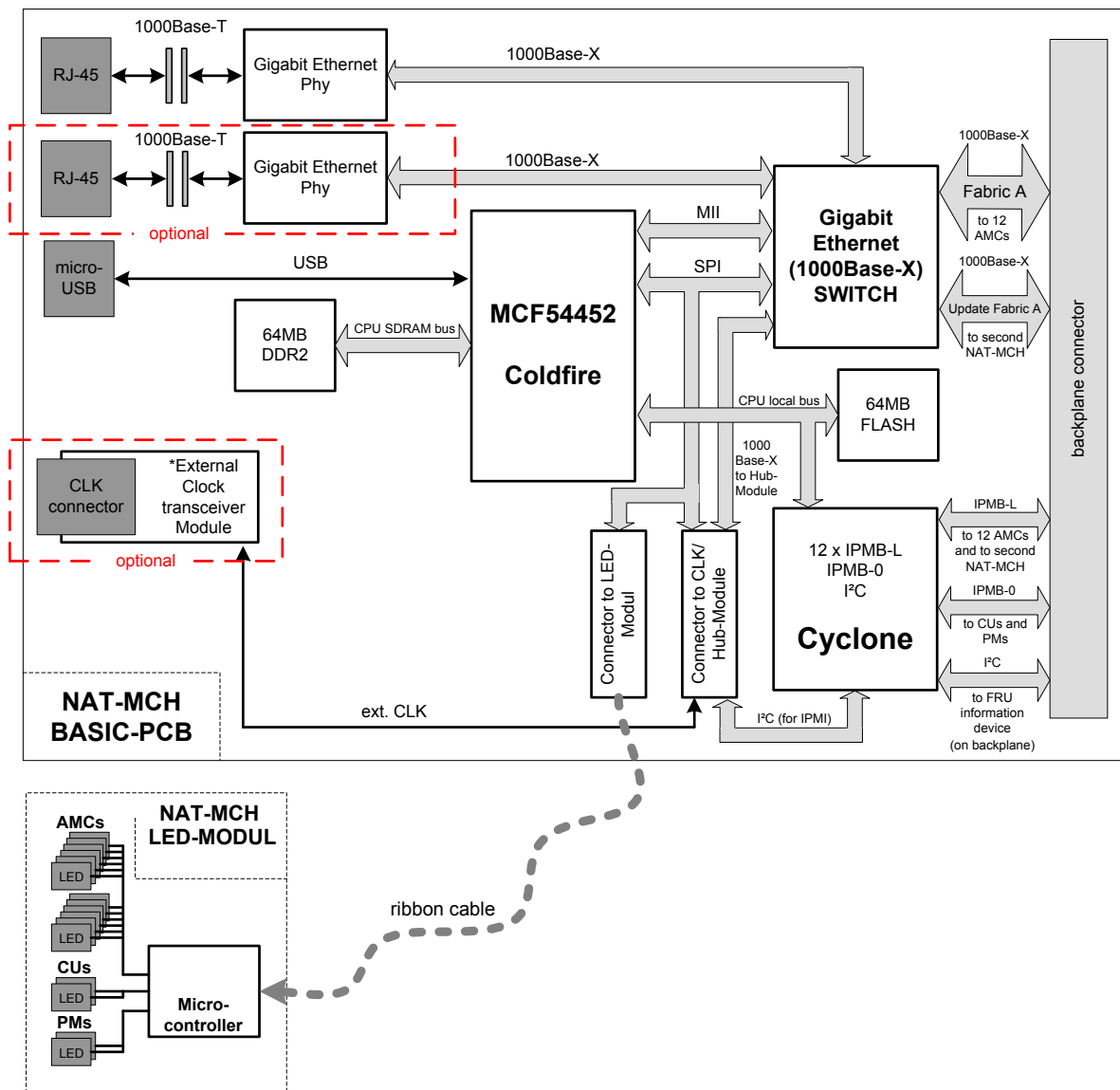
For detailed description see the following chapter.



2.2 Block Diagram

The following figure shows a block diagram of the **NAT-MCH BASE-Module** and optional available extension modules. If the extension module is added, customized I/O functionality is available.

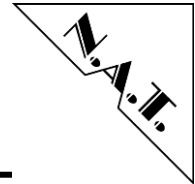
Figure 1: **NAT-MCH BASE-Module – Block Diagram incl. LED Module**



* There are different external clock transceiver modules available. Please refer to the **NAT-MCH CLK-Module** technical reference manual for a more detailed description.

As it can be seen in Figure 1:, a LED-Module belongs to the **NAT-MCH BASE-Module**; it is mounted on the front panel.

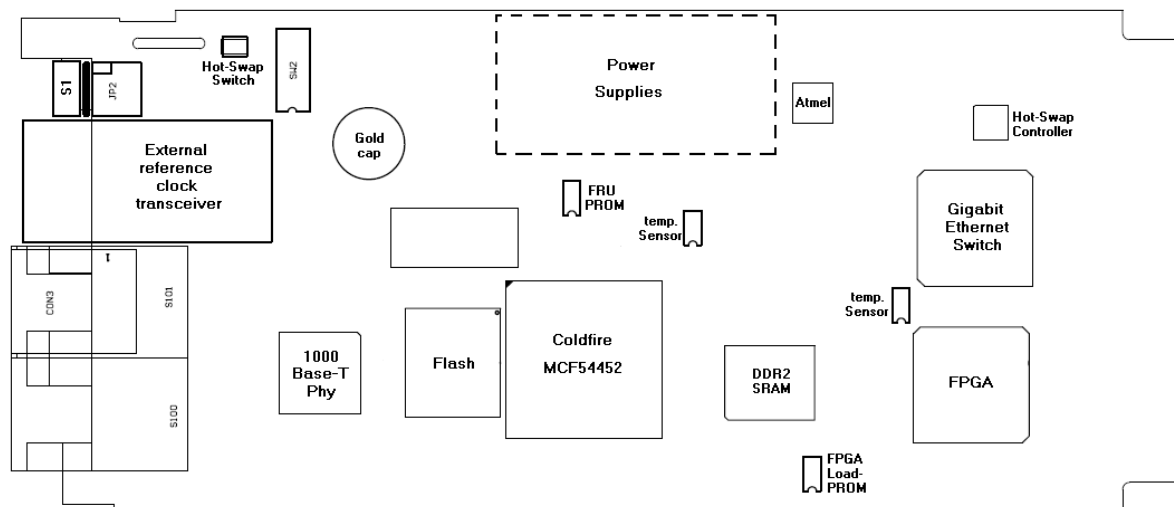
Please note: the LED-Module, the second optional RJ45 and the external clock transceiver module are not available for the LC (Low Cost) version!

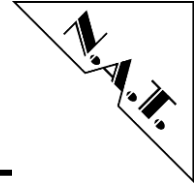


2.3 Location Diagram

The position of important components is shown in the following location overview. Depending on the board type it may be that the board does not include all components named in the location diagram.

Figure 2: **NAT-MCH BASE-Module – Location Diagram – top-view**





3 Board Features

The **NAT-MCH BASE-Module** can be divided into a number of functional blocks, which are described in the following paragraphs.

3.1 CPU

The **NAT-MCH BASE-Module** features a 32-bit CPU ColdFire MCF54452 (Freescale) which is based on the V4e ColdFire core. The MCF54452 includes a memory management unit (MMU), a dual precision floating-point unit (FPU) and an enhanced multiply-accumulate unit (EMAC), delivering 308 (Drystone 2.1) MIPS at 266 MHz.

The processor has integrated a 32 KB I-Cache, a 32 KB D-Cache and 32 KB on-chip system SRAM. The MCF54452 is equipped with a 32-bit DDR2 266 controller at 133 MHz clock rate.

The MCF5470 ColdFire integrates the following interfaces:

- two 10/100 Ethernet Controllers (FECs)
- DSPI – SPI with DMA capability
- a I²C interface
- a 16-channel DMA controller
- USB Interface

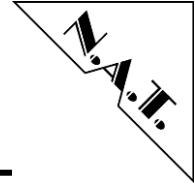
3.2 Memory

3.2.1 DDR2SDRAM

The onboard DDR2SDRAM memory is 16 bit wide; its size is 32 or 64 MB (assembly option). The interface to the SDRAM is implemented in the ColdFire MCF54452. By programming several registers, the SDRAM controller can be adapted to different RAM architectures.

3.2.2 FLASH

FLASH memory is connected to the demultiplexed upper 16 data bits D0 – 15 of the local bus and to the latched address lines. Its size is 16, 32 or 64 MB (assembly option). The FLASH on the **NAT-MCH BASE-MODULE** can be programmed by the CPU (by appropriate software) or through the BDM port.



3.3 Backplane Interfaces

The **NAT-MCH BASE-Module** is equipped with various backplane interfaces, described in the following sections.

3.3.1 IPMB

The **NAT-MCH BASE-Module** implements IPMB interfaces which conform to the MicroTCA specification.

IPMB-L interfaces are available for communication with up to 12 AMCs and a second **NAT-MCH**. An IPMB-0 interface is available for communication with CUs and PMs.

3.3.2 I²C

The **NAT-MCH BASE-Module** provides an I²C interface to access the dedicated FRU information device (resided on the backplane).

3.3.3 Ethernet

The **NAT-MCH BASE-Module** provides 1000BaseX interfaces for fabric A of 12 AMCs and the Update channel of fabric A. These interfaces are connected to a Broadcom BCM5396 Gigabit Ethernet Switch.

3.4 Front Panel Interfaces

The **NAT-MCH BASE-Module** is equipped with various interfaces at the front panel, described in the following sections.

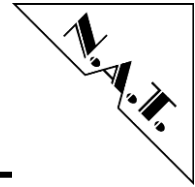
3.4.1 Ethernet Uplink Ports

Two ports of the BCM5396 Gigabit Ethernet Switch are wired to connector GbE1 and GbE2 via a Broadcom BCM5482 1000BaseT physical layer chip. By this external device the user may access fabric A also from the front panel.

GbE1: The switch interfaces the network to fabric A and to the ColdFire CPU. Therefore this port can be used to update the ColdFire Software and to permit communication with external shelf or system managers.

GbE2: Together with GbE1 this port can be used to increase the bandwidth of the uplink. Instead of the second GbE-Interface the **NAT-MCH BASE-Module** can be equipped with a RJ45 clock interface (see chapter 3.4.3.2 for details).

Configuration settings of the BCM5482 are done by CPU ports. It has to be set up in GBIC mode (1000BaseT to 1000BaseX translation). Like all other I/O devices, the PHY is resettable via software by programming an FPGA register.



3.4.2 USB Debug Port

The front panel micro USB connector available on the **NAT-MCH BASE-Module** is connected to the USB interface of the ColdFire MCF54452. It provides a console interface for configuration and monitoring. The USB interface is running in USB Device Mode. Hardware version 3.4 or higher supports also USB Host Mode (not for LC version!).

A special USB-to-RS232 adapter cable can be ordered from N.A.T. GmbH. Connecting this cable to the **NAT-MCH** USB port (configured to Host Mode) has the advantage that a terminal connection will not get lost after a “reboot” or power-cycle.

3.4.3 Clock Interface

The **NAT-MCH BASE-Module** can be equipped with various External Reference Clock Transceiver Modules. The available transceiver modules differ in the number of supported clock signals, in the supported electrical standard (e.g. LVDS, TTL, CMOS) and the supported connector.

The external clock interfaces are routed from the transceiver module to the **CLK-Module**. Therefore the external clock interfaces can only be used in collaboration with the **NAT-MCH CLK-Module**.

At the moment the following External Clock Transceiver Modules are available:

3.4.3.1 Coax-IO

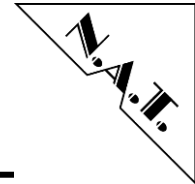
The Coax-IO transceiver module supports two SMA connectors at the face plate. Each connector is connected to its independent amplifier circuit. Each amplifier circuit can be configured as receiver or transmitter.

Configured as transmitter the output signal coming from the Clock Module FPGA is transmitted via a simple CMOS driver. This driver is connected to the SMA connector via AC-coupling.

The amplifier circuit first comes really into operation if configured as receiver. The receiver part is designed to be able to work with a wide range of input voltages, as well as signal forms (e.g. sine wave, rectangle).

To be independent of any DC-offset the receiver part is also connected via AC-coupling.

The main part of the amplifier is a comparator that transfers the input signal from the SMA connector into a rectangle signal with a peak to peak voltage of 3.3V. Refer to Table 3: for the electrical characteristics.



The signal mapping for the Coax-IO module can be found below:

Table 2: NAT-MCH BASE-Module – Coax-IO signal mapping

Schematic Name	Script Name	Function Coax-IO
Extref1_p	EXT single ended 1	SMA_1 Rx
Extref1_n	EXT single ended 2	SMA_1 Tx
Extref2_p	EXT single ended 3	SMA_2 Rx
Extref2_n	EXT single ended 4	SMA_2 Tx

Table 3: NAT-MCH BASE-Module – Coax-IO Electrical characteristics

Parameter	Min.	Typ.	Max.	Unit
Input Voltage peak to peak	0.3		5	V
Output Voltage peak to peak (with 50 Ohm sink termination)		1		V
Input Frequency	1		50M	Hz
Output Frequency	250		125M	Hz
Termination Resistance		50		Ω

3.4.3.2 RJ45-Clock-Interface

Instead of the second GbE-Port the **NAT-MCH BASE-Module** can be assembled with a second RJ45 connector usable as RJ45-Clock-Interface.

CAUTION:

The second GbE-Interface is not available with this assembly option! The pin assignment of the RJ45-Clock-Interface differs from the GbE-Interface! For detailed information please refer to chapter 4.2.11.

The signals are directly connected to LVDS compliant I/Os of the clock module FPGA. To prevent the unit from damage, only signals complying with the LVDS signal standard may be applied to this interface!

Other External Reference Clock Transceiver Modules

Please contact N.A.T. GmbH if the available Clock transceiver modules or any parameter does not satisfy the needs for your application.

3.5 Interface to Extension Modules

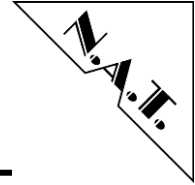
3.5.1 NAT-MCH CKL-Module / NAT-MCH CLK-PHYS-Module

The **NAT-MCH CLK-Module** / **NAT-MCH CLK-PHYS-Module** can be accessed by the ColdFire MCF54452 via I²C bus.

To interface the **NAT-MCH HUB-Module**, a SPI interface is also available. The SPI interface of the ColdFire is used for this purpose.

3.5.2 NAT-MCH HUB-Module

The **NAT-MCH HUB-Module** is connected to the **NAT-MCH BASE-Module** over the same connector that connects the **NAT-MCH CLK-Module** / **NAT-MCH CLK-**



PHYS-Module. The **NAT-MCH HUB-Module** can also be accessed by the ColdFire via I²C bus.

To interface the **NAT-MCH HUB-Module**, a SPI interface is also available. The SPI interface of the ColdFire is used for this purpose.

To have a high-speed interface to the **NAT-MCH HUB-Module** a 1000Base-X interface is connected used. At the moment this interface is only supported by the **NAT-MCH XAUI-Module**.

3.6 I²C Devices

There are three I²C Devices on the **NAT-MCH BASE-Module**, which are connected to the MCF54452 via I²C bus

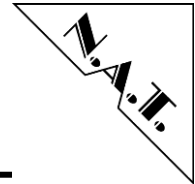
- An EEPROM (24C08) used for storage of board-specific information (address 0x50)
- Two temperature sensors (LM75), which sense the board temperature near CPU and near FPGA (addresses 0x9C and 0x9E)

3.7 Ethernet Switch

The Broadcom BCM5396 Gigabit Ethernet Switch provides a layer 2, non-blocking, low-latency Gigabit Ethernet switch, supporting VPN as well as a port based rate control. The BCM5396 supports Fabric A switching according to MicroTCA.0 R1.0 and PICMG SFP.1 R1.0, serving up to 12 AMCs as well as the update channel from the second **NAT-MCH** in redundant environments. Also supported are two uplink ports at the front panel of the **NAT-MCH BASE-Module** in order to interconnect to other carriers, shelves or systems. Refer to section 3.4.1 for the Uplink ports.

The configuration register of the BMC5396 can be accessed through the MCF54452's PHY message channel interface.

For frame management the BMC5396 is connected to the MCF54452's TSEC0 through the MII interface.

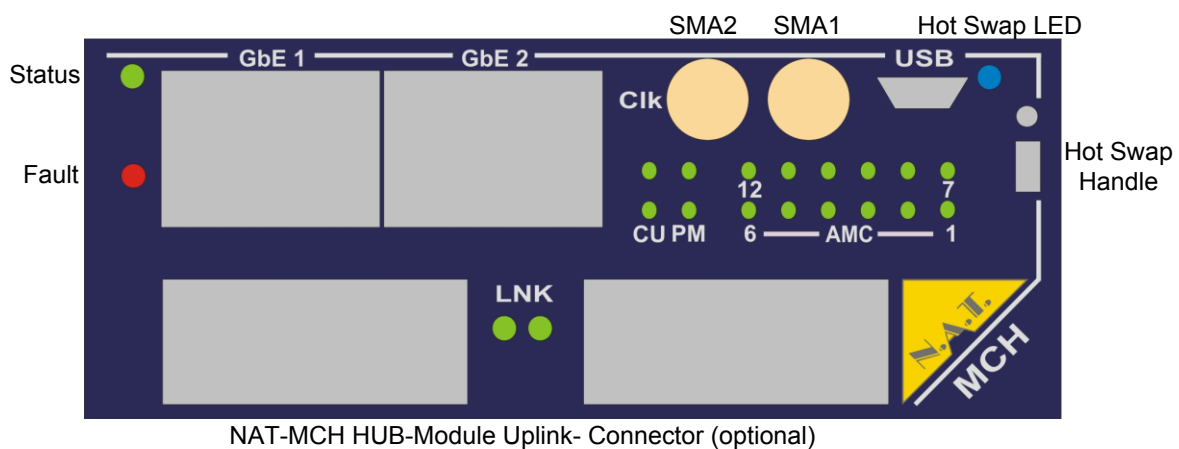


4 Hardware

4.1 Front Panel and LEDs

The following figure shows the front panel of the **NAT-MCH BASE-Module**. It is equipped with various LEDs.

Figure 3: **NAT-MCH BASE-Module – Front Panel**



4.1.1 MCH Basic-LEDs

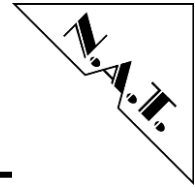
- The *Status-LED* indicates the operation status of the **NAT-MCH BASE-Module**. If the LED is green, the **NAT-MCH BASE-Module** operates as primary MCH in the MicroTCA-system, if the LED shines orange, it is operating as secondary MCH
- The *Fault-LED* indicates a malfunction of the **NAT-MCH BASE-Module**
- The *Hot-Swap-LED* indicates the Hot-Swap-Status of the **NAT-MCH BASE-Module**

4.1.2 RJ45-LEDs

Two *RJ45-LEDs* are integrated in each RJ45-connector to indicate GbE-Status.

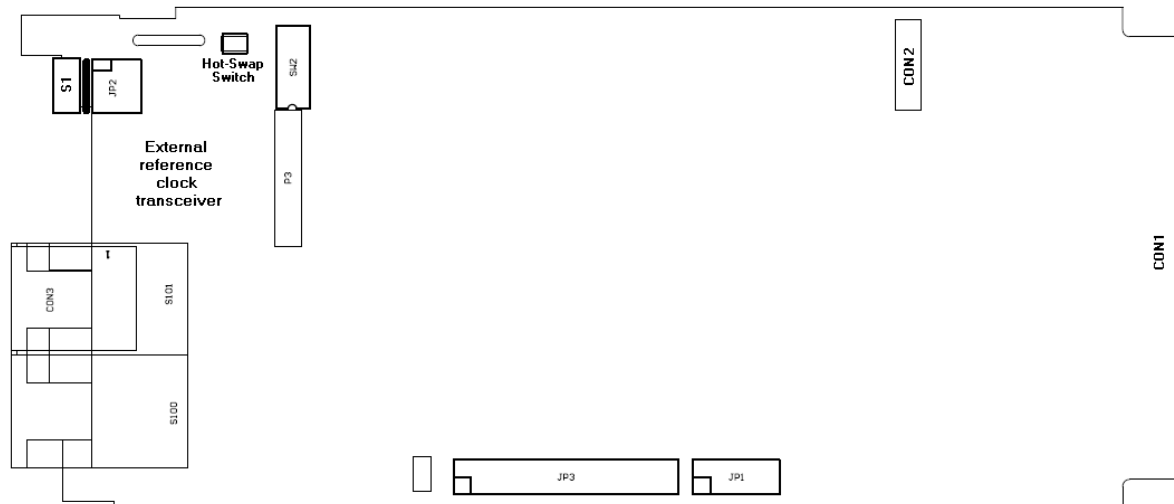
4.1.3 Status LEDs

- Various *Status-LEDs* residing on the front panel (mounted on the LED-Module) indicate the status of 12 AMCs, 2 CUs and 2 PMs
- The *LNK-LEDs* indicate the Link-Status of an optionally mountable **NAT-MCH HUB-Module**

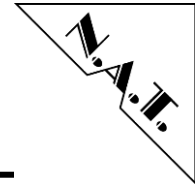


4.2 Connectors and Switches

Figure 4: NAT-MCH BASE-Module – Connectors – Overview



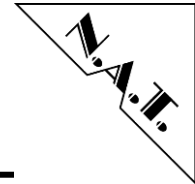
Please refer to the following tables to look up the connector and switch pin assignment of the **NAT-MCH BASE-Module**.



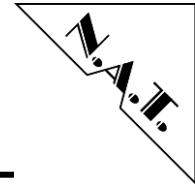
4.2.1 CON1: MCH Connector

Table 4: CON1: MCH Connector – Pin-Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	GND	PWR_ON	170
2	PWR	NC	169
3	/PS1	NC	168
4	MP	NC	167
5	GA0	NC	166
6	RESVD	NC	165
7	GND	GND	164
8	RESVD	TxFA-1+	163
9	PWR	TxFA-1-	162
10	GND	GND	161
11	TxFUA+	RxFA-1+	160
12	TxFUA-	RxFA-1-	159
13	GND	GND	158
14	RxFUA+	TxFA-2+	157
15	RxFUA-	TxFA-2-	156
16	GND	GND	155
17	GA1	RxFA-2+	154
18	PWR	RxFA-2-	153
19	GND	GND	152
20	TxFA-3+	TxFA-4+	151
21	TxFA-3-	TxFA-4-	150
22	GND	GND	149
23	RxFA-3+	RxFA-4+	148
24	RxFA-3-	RxFA-4-	147
25	GND	GND	146
26	GA2	TxFA-6+	145
27	PWR	TxFA-6-	144
28	GND	GND	143
29	TxFA-5+	RxFA-6+	142
30	TxFA-5-	RxFA-6-	141
31	GND	GND	140
32	RxFA-5+	TxFA-8+	139
33	RxFA-5-	TxFA-8-	138
34	GND	GND	137
35	TxFA-7+	RxFA-8+	136
36	TxFA-7-	RxFA-8-	135
37	GND	GND	134
38	RxFA-7+	/TMREQ	133
39	RxFA-7-	RSVD	132
40	GND	GND	131
41	/ENABLE	I2C_SCL	130
42	PWR	I2C_SDA	129
43	GND	GND	128
44	TxFA-9+	IPMB0-SCL-A	127



Pin #	AMC-Signal	AMC-Signal	Pin #
45	TxFA-9-	IPMB0-SDA-A	126
46	GND	GND	125
47	RxFA-9+	IPMB0-SCL-B	124
48	RxFA-9-	IPMB0-SDA-B	123
49	GND	GND	122
50	TxFA-10+	IPMBL-SCL-1	121
51	TxFA-10-	IPMBL-SDA-1	120
52	GND	GND	119
53	RxFA-10+	IPMBL-SCL-2	118
54	RxFA-10-	IPMBL-SDA-2	117
55	GND	GND	116
56	SCL_L	IPMBL-SCL-3	115
57	PWR	IPMBL-SDA-3	114
58	GND	GND	113
59	TxFA-11+	IPMBL-SCL-4	112
60	TxFA-11-	IPMBL-SDA-4	111
61	GND	GND	110
62	RxFA-11+	IPMBL-SCL-5	109
63	RxFA-11-	IPMBL-SDA-5	108
64	GND	GND	107
65	TxFA-12+	IPMBL-SCL-6	106
66	TxFA-12-	IPMBL-SDA-6	105
67	GND	GND	104
68	RxFA-12+	IPMBL-SCL-7	103
69	RxFA-12-	IPMBL-SDA-7	102
70	GND	GND	101
71	SDA_L	IPMBL-SCL-8	100
72	PWR	IPMBL-SDA-8	99
73	GND	GND	98
74	XOVER0+	IPMBL-SCL-9	97
75	XOVER0-	IPMBL-SDA-9	96
76	GND	GND	95
77	XOVER1+	IPMBL-SCL-10	94
78	XOVER1-	IPMBL-SDA-10	93
79	GND	GND	92
80	XOVER2+	IPMBL-SCL-11	91
81	XOVER2-	IPMBL-SDA-11	90
82	GND	GND	89
83	/PS0	IPMBL-SCL-12	88
84	PWR	IPMBL-SDA-12	87
85	GND	GND	86



4.2.2 CON2: Extension Module Connector

Connector CON2 connects the **NAT-MCH BASE-Module** with the **NAT-MCH CLK-Module** and/or the **NAT-MCH HUB-Module**.

Table 5: CON2: Extension Module Connector – Pin Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	/SPISEL_CLKPCB	/INT_HUB	2
3	GND	GND	4
5	NC	NC	6
7	NC	NC	8
9	+12V	+12V	10
11	+12V	+12V	12
13	EXTREF_1_P	+3.3V MP	14
15	EXTREF_1_N	SPICLK	16
17	EXTREF_2_N	EXTREF_2_P	18
19	MOSI	MISO	20
21	GND	/SPISEL_Hub-Module	22
23	SCL	/Reset_CLK-Module	24
25	SDA	/Reset_Hub-Module	26
27	GND	GND	28

The I²C- and SPI- interfaces of Connector CON2 are connected to the respective interfaces of the local Coldfire CPU.

4.2.3 JP1: Altera FPGA Programming Port

Connector JP1 connects the JTAG- or programming-port of the Altera FPGA device.

Table 6: JP1: Altera FPGA Programming Port – Pin Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	DCLK	GND	2
3	CONF_DONE	+3.3V	4
5	/CONFIG	/CECONF	6
7	DATA0	/CS0	8
9	ASDI	GND	10

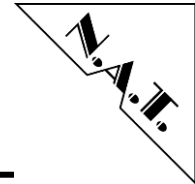
4.2.4 JP2: LED-Module Connector

Connector JP2 connects the LED-Module via a ribbon cable.

Table 7: JP2: LED-Module Connector – Pin Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	GND	nRESET_LED	2
3	+3.3V	MOSI	4
5	nSPISEL_LED	MISO	6
7	GND/PDI-DATA*	SPICLK	8

* Hardware version v3.5 reuses GND pin7 as programming pin to support incircuit programming of the latest LED module version



4.2.5 JP3: Development Connector

The BDM/JTAG-Port (also called COP header) can be used for debugging. It is supported by major debug tool manufacturers.

Table 8: JP3: Development Connector – Pin Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	/CPU_RSTOUT	/BKPT	2
3	GND	/DSCLK	4
5	GND	SLV_TCK	6
7	/HRESET	SLV_TDI	8
9	+3.3V	CPU_TDO	10
11	GND	PST_D7	12
13	PST_D6	PST_D5	14
15	PST_D4	PST_D3	16
17	PST_D2	PST_D1	18
19	PST_D0	JTAG_EN	20
21	NC	NC	22
23	GND	PST_CLK	24
25	TMREQ	/TA	26

4.2.6 P3: External Clock Transceiver Module Connector

Connector P3 is used to connect the external clock transceiver module to the **NAT-MCH BASE-Module**.

Table 9: P3: External Clock Transceiver Module Connector – Pin Assignment

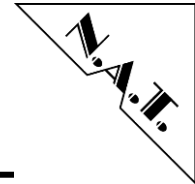
Pin #	AMC-Signal	AMC-Signal	Pin #
1	SGND	+3.3V	2
3	EXTREF_C_P	EXTREF_CONF1	4
5	EXTREF_C_N	EXTREF_CONF2	6
7	EXTREF_A_P	EXTREF1_P	8
9	EXTREF_A_N	EXTREF1_N	10
11	EXTREF_B_P	EXTREF2_P	12
13	EXTREF_B_N	EXTREF2_N	14
15	EXTREF_D_P	EXTREF_CONF3	16
17	EXTREF_D_P	SGND	18
19	EXTREF_CONF4	GND	20

4.2.7 SW1: Hot Swap Switch

Switch SW1 is used to support hot swapping of the module. It conforms to the PICMG AMC.0 specification.

4.2.8 SW2: General Purpose DIL Switch

Switch SW2 is used for general purpose settings. It is an octal DIL switch and was implemented for future use. SW2 is connected to the FPGA, by which its status can be read.



4.2.9 S1: Micro USB Connector

The USB connector S1 is connected to the USB interface of the MCF54452.

Table 10: S1: Micro USB Connector – Pin Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	VBUS	USB_DM	2
3	USB_DP	NC	4
5	GND		

4.2.10 S100: RJ45 Connector

The RJ45 connector S100 connects a 1000BaseT Ethernet network (over a PHY chip) to the Gigabit Ethernet switch.

Table 11: S100: RJ45 Connector – Pin-Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	MDI1_0+	MDI1_0-	2
3	MDI1_1+	MDI1_2+	4
5	MDI1_2-	MDI1_1-	6
7	MDI1_3+	MDI1_3-	8

4.2.11 S101: RJ45 Connector

The RJ45 connector S101 connects a 1000BaseT Ethernet network (over a PHY chip) to the Gigabit Ethernet switch.

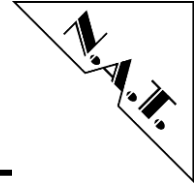
Table 12: S101: RJ45 Connector – Pin-Assignment – GbE-Interface

Pin #	AMC-Signal	AMC-Signal	Pin #
1	MDI2_0+	MDI2_0-	2
3	MDI2_1+	MDI2_2+	4
5	MDI2_2-	MDI2_1-	6
7	MDI2_3+	MDI2_3-	8

If chosen as assembly option the second RJ45 connector can be used as RJ45-Clock-Interface. The deviating pin assignment can be found in the following table.

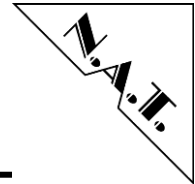
Table 13: S101: RJ45 Connector – Pin-Assignment – RJ45-Clock-Interface

Pin #	Signal	Signal	Pin #
1	N.C.	N.C.	2
3	Extref2_p	Extref1_p	4
5	Extref1_n	Extref2_n	6
7	N.C.	N.C.	8



5 Programming Notes

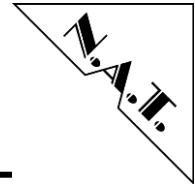
Please refer to the **NAT-MCH BASE-Module** User's Manual for programming notes.



6 Board Specification

Table 14: NAT-MCH BASE-Module – Features

Processor	ColdFire MCF54452 (266 MHz)
MCH-Module	standard MicroTCA MCH-Module, single width, full or midsize height (depending on configuration)
Front-I/O	2 RJ45 connectors, 1 Micro-USB connector and one or more clock in/output connector(s), depending on the chosen external clock transceiver module.
Main Memory	32/64 MByte DDR2RAM
Flash PROM	16/32/64 MByte Flash PROM, on board programmable
Firmware	OK1, Carrier Manager, Shelf Manager
Power Consumption	12V / 700mA typ. (only NAT-MCH BASE-Module)
Operating Temperature	0°C – +55°C with forced cooling
Storage Temperature	-40°C - +85°C
Humidity	10% – 90% rh non-condensing
Standards compliance	PICMG AMC.0 Rev. 2.0 PICMG AMC.2 Rev. 1.0 PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format) IPMI Specification V1.5 Rev. 1.0 PICMG µTCA.0 Rev. 1.0



7 Installation

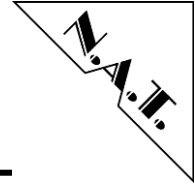
7.1 Safety Note

To ensure proper functioning of the **NAT-MCH BASE-Module** during its usual lifetime take the following precautions before handling the board.

CAUTION

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime.

- Before installing or uninstalling the **NAT-MCH BASE-Module** read this installation section
- Before installing or uninstalling the **NAT-MCH BASE-Module**, read the Installation Guide and the User's Manual of the MicroTCA system the board will be plugged into.
- Before installing or uninstalling the **NAT-MCH BASE-Module** on a backplane:
 - Check all installed boards and modules for steps that you have to take before turning on or off the power
 - Take those steps
 - Finally turn on or off the power if necessary
 - Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NAT-MCH BASE-Module** is connected to the MicroTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
 - is bolted the front panel or rack
 - and shielded by closed housing



7.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up check this section for installation prerequisites and requirements

7.2.1 Requirements

The installation requires only

- an μ TCA backplane for connecting the **NAT-MCH BASE-Module**
- power supply
- cooling devices

7.2.2 Power Supply

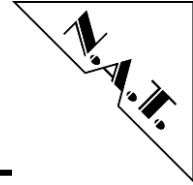
The power supply for the **NAT-MCH BASE-Module** must meet the following specifications:

- required for the module: +12 V / 700mA typ. (only **NAT-MCH BASE-Module**)

7.2.3 Automatic Power Up

In the following situations the **NAT-MCH BASE-Module** will automatically be reset and proceed with a normal power up:

- The Voltage sensor generates a reset when +12 V voltage level drops below 8 V



7.3 Statement on Environmental Protection

7.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

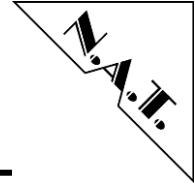
Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

7.3.2 Compliance to WEEE Directive

Directive 2012/19/EU of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronic equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2011/65/EU of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronic products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.



If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2012/19/EU of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

7.3.3 Compliance to CE Directive

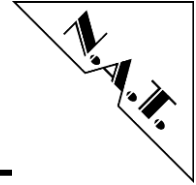
Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

7.3.4 Product Safety

The board complies with EN60950 and UL1950.

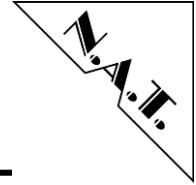
7.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.



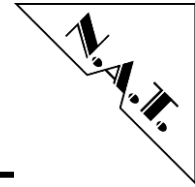
8 Known Bugs / Restrictions

none



Appendix A: Reference Documentation

- [1] Freescale, MCF54452 ColdFire® CF4e Core Users Manual, 06/2001, Rev. 0
- [2] Altera, Cyclone Device Handbook, 02/2005
- [3] Broadcom, BCM5396 SerDes Gigabit Switch, DS110, 02/2008
- [4] Broadcom, BCM5482 Gigabit Ethernet Transceiver, DS11, 02/2012



Appendix B: Document's History

Revision	Date	Description	Author
1.0	08.12.2006	initial revision	ks, ga
1.1	16.01.2007	reworked, adapted to HW Rev. 1.1	ga
1.2	20.03.2007	reworked, adapted to CLK-MODULE Rev. 1.2 and HUB-PCB Rev. 1.1	ks
2.0	04.05.2007	adapted to Basic-PCB Rev. 2.0, description reduced to Basic-PCB	ga
2.1	12.08.2008	added specification of the external clock input circuit	ks
2.2	31.03.2009	reworked, adapted to HW Rev.3.1	ks
2.4	16.02.2010	Added description of USB Host Mode support	ks
2.5	11.11.2010	Added detailed description of external clock transceiver modules (section 3.4.3)	ks
2.6	29.11.2010	Added signal mapping of external clock transceiver module	te
2.7	18.05.2013 03.07.2013	Contact data updated, typo correction Updated to new layout, reworked	fh se
2.8	24.09.2013 11.02.2014 09.04.2014	Minor changes in formatting Pin Assignment CON2/P3 updated Link updates	se
2.9	19.02.2015	Added support for hardware version v3.5	ks
2.10	23.04.2015	Updated document to the latest RoHS and WEEE Directive	ks