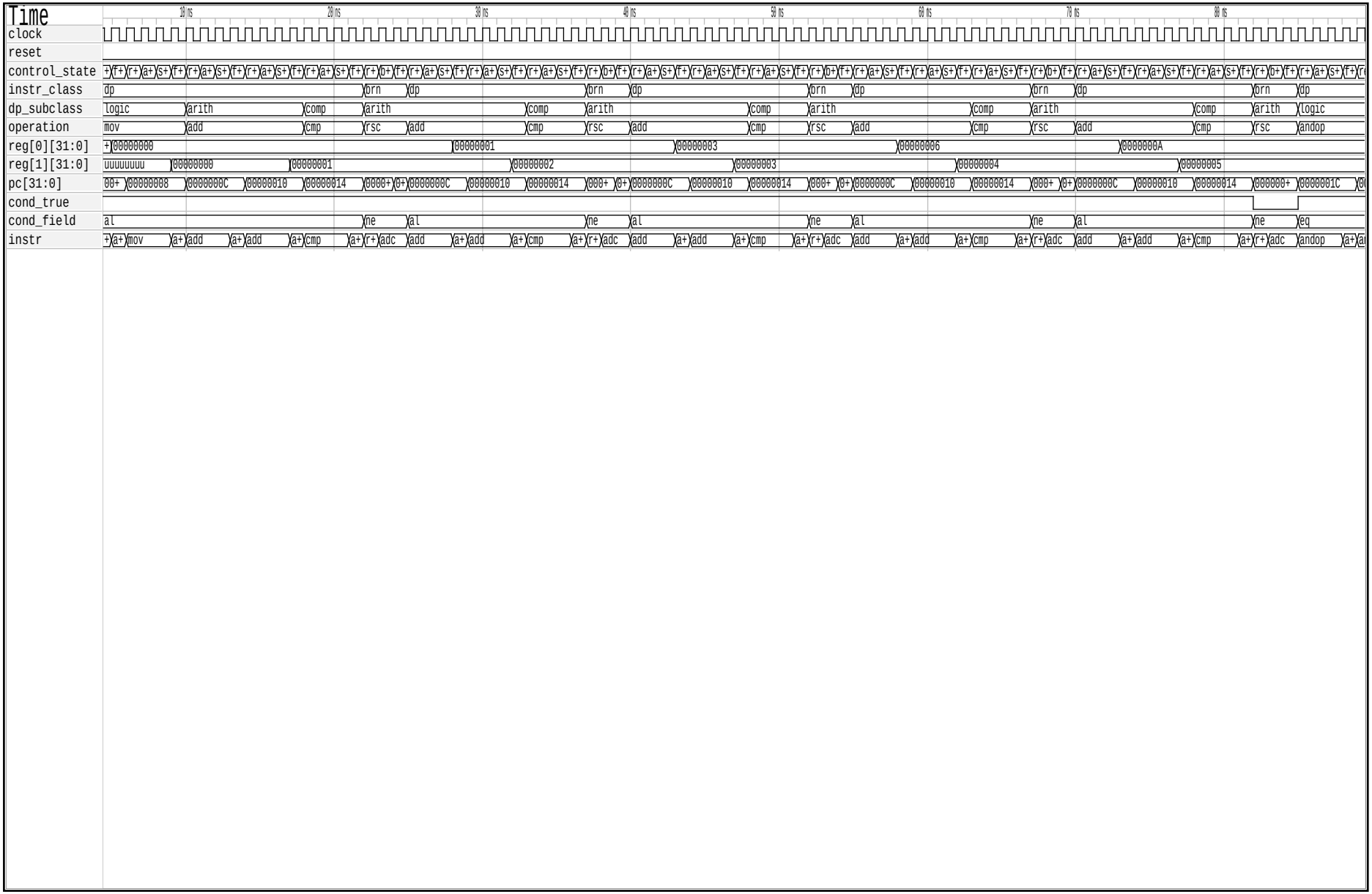
Time
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80 ns
clock
reset
control_state
instr_class
dp
brn
dp
brn
dp
brn
dp
brn
dp
brn
dp
dp_subclass
logic
arith
comp
arith
comp
arith
comp
arith
comp
arith
comp
arith
logic
operation
mov
add
cmp
rsc
add
cmp
rsc
add
cmp
rsc
add
cmp
rsc
add
cmp
rsc
andop
reg[0][31:0]
00000000
00000001
00000003
00000006
0000000A
reg[1][31:0]
uuuuuuuu
00000000
00000001
00000002
00000003
00000004
00000005
pc[31:0]
00000008
0000000C
00000010
00000014
0000001C
cond_true
cond_field
al
ne
al
ne
al
ne
al
ne
al
ne
eq
instr
mov
add
add
cmp
adc
add
add
cmp
adc
add
add
cmp
adc
add
add
cmp
adc
add
add
cmp
adc
andop