Time		10 ns		20 ns	1 1 1	30 hs			40 ts		50 hs			60 tis			70 ts		80 n		
clock				T		T			ппл		m			шш							
reset	V=V-V-V	VEVVV	Ve V V Ve V	V-V-V-V-V-	Ve V	V V= V V	VV-V-V	V-V-V-V-V			VEVV	V=V-V-V	/VV	VEVV			- V V 1	V-V-V			
control_state	dp	s+ <u>XI+Xr+Xa+X</u> s+	+ <u>XI+XI+Xa+XS+XI+XI+</u>	/xa+xs+x1+xr+x0 /brn		XS+XI+XI+X	a+,ks+,ki+,kr+,ka+	<u>Xs+XI+Xr+Xb+X</u> X brn	(<u>i+)(r+)(a+)</u> (dp	<u>(S+, XI+, XI+, Xa+, X</u>	s+XI+XI+Xa+Xs	8+ <u>XI+Xr+X0+X</u> (brn	<u> </u>	s+ <u>XI+Xr+Xa+</u> X	S+XI+XI+Xa+X	<u>x+,x1+,x1+,x0+,x</u> X brn	<u>1+,r+,ta+)</u> (dp	<u>XS+XI+XI+Xa+</u>	<u>(s+, x+, x+, xa+)</u>	(<u>s+,(i+,(r+,(o+</u> , (brn	<u>(I+,Xr+,Xa+,Xs+,XI+,XI</u>
dp_subclass	logic	X arith	You	omp Xarit			Xcomp	Xarith			Xcomp	Xarith			Xcomp	Xarith	∧up		Xcomp		Xlogic
operation	mov	Xadd		np Xrsc			Xcmp	\rsc \rsc	add		Xcmp	\rsc \rsc	X add		Xcmp	Xrsc	Xadd		Xcmp	Yrsc	Xandop
reg[0][31:0]	+100000000					(0000000				X 00000003	7 -			X 00000006	^-	^		X 0000000A			
reg[1][31:0]	uuuuuuu	(00000000	(0000)	0001			X 00000002				X 00000003				X 00000004				X 00000005		
pc[31:0]	00+ X 0000000	0000000)	C X 00000010 X 00	0000014 X 0000	+ X 0+ X 00000	00C X 000	00010 X 000000	014 (000+)	(0+) (000000	000000 X	10 X 0000001	14 X 000+ X	(0+) (000000	oc X 000000)10 X 000000	14 X000+ X	0+ X 000000	000 X 00000	010 X 000000	14 X 00000)+ X 0000001C X
cond_true																					
cond_field	al							\(ne	(al			/ne				Xne Xne	X al			X ne	X eq
instr	+ X a+ X mov	Xa+Xadd	Xa+Xadd Xa+Xcm	np Xa+Xr+Xa	dc X add	Xa+Xadd	Xa+Xcmp	Xa+Xr+Xado	add	Xa+Xadd	Xa+Xcmp	Xa+Xr+Xado	: Xadd	Xa+Xadd	Xa+Xcmp	Xa+Xr+Xadc	add	Xa+Xadd	Xa+Xcmp	Xa+Xr+Xado	z Xandop Xa+X