```
architecture behavioral of MyDesign is
        -- declaration of local signals and component declarations
        . . . .
begin
        -- component instances
        . . . .
        -- concurrent assignments for extracting instruction fields
        . . . .
        -- control signals and multiplexers
        process (control_state, IR, operation, A, B, Flags_out, PC_out )
        begin
                -- default values
                PCwrite <= '0'; Flags_write <= '0';
                ALUop <= operation; operand1 <= A;
                operand2 <= B; Carry_in <= Flags_out (1);
                rd_AdrB <= Rm;
                . . . .
                -- state dependent values
                case control_state is
                        when fetch => PCwrite <= '1';
                                ALUop <= adc; operand1 <= "00" & PC_out (31 downto 2);
                                operand2 <= X"00000000"; Carry_in <= '1';
                        when read_AB => if (instr_class = DT) then rd_adrB <= Rd end; if;
                        when arith => Flags_write <= '1';
                                if (DP_operand_src = imm) then
                                        operand2 <= X"000000" & Imm8;
                                end if;
                        . . . .
                end case;
        end process;
-- control FSM
        process (clock, reset)
        begin
                if reset ='1' then control_state <= fetch;
                elsif rising_edge(clock) then
                        case control_state is
                                when fetch => IR <= Mem_out; control_state <= read_AB;
                                when read_AB => A <= data_outA; B <= data_outB;
                                        case instr_class is
                                                when DP => control_state <= arith;
                                                . . . .
                                        end case;
                                when arith => RES <= result; control_state <= res2RF;
                                . . . .
                        end case;
                end if;
        end process;
end behavioral;
```

In the above design style, The following signals are assigned in the clocked process - control_state, A, B, IR, DR, RES.

Other signals that are going to various components (for example, operands and operation code of ALU, memory address, write enable signals for register file, memory, flags, program counter, etc.) are assigned in a process that is modeling a combinational circuit. Alternatively, instead of this process, these signals could also have been assigned in concurrent assignments.

Several alternatives are possible. For example, Some or all of {A, B, IR, DR, RES} can be assigned (under appropriate conditions) in individual clocked processes or in separate components. PC need not be a separate component. It can be a local signal and assigned in the clocked process of control FSM.