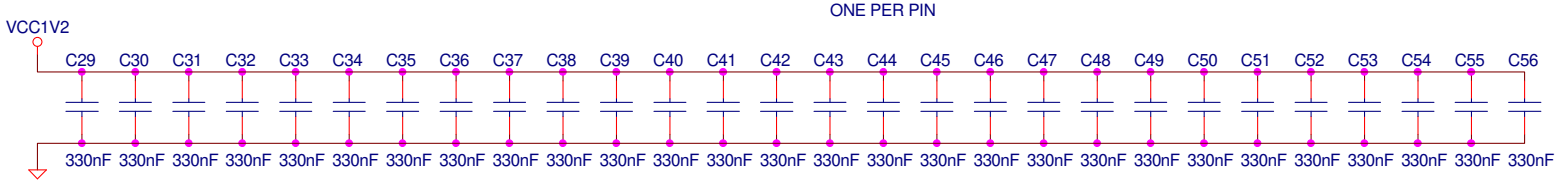
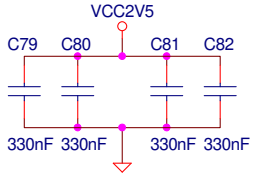
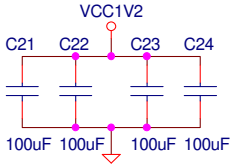
DECOUPLING CAPS FOR VCCINT
ONE PER PIN

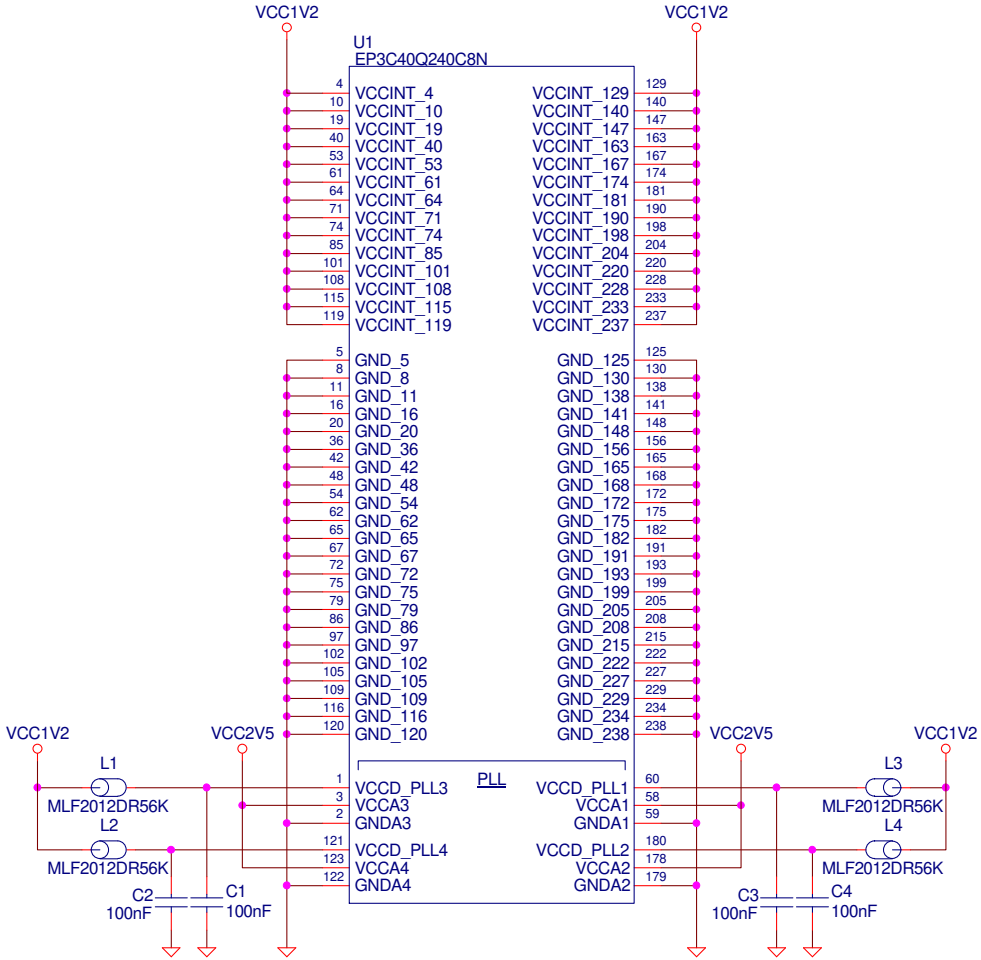


DECOUPLING CAPS FOR VCCA
ONE PER PIN



DECOUPLING CAPS FOR VCCINT
ON THE CORNERS OF THE CHIP





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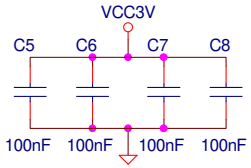
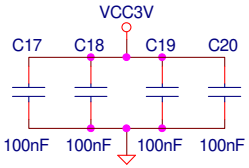
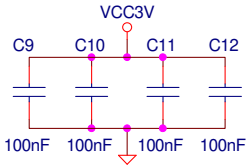
DECOUPLING CAPS FOR VCCIO BANKS 1/2



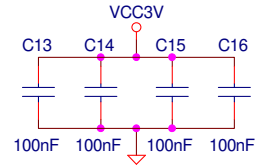
DECOUPLING CAPS FOR VCCIO BANKS 3/4



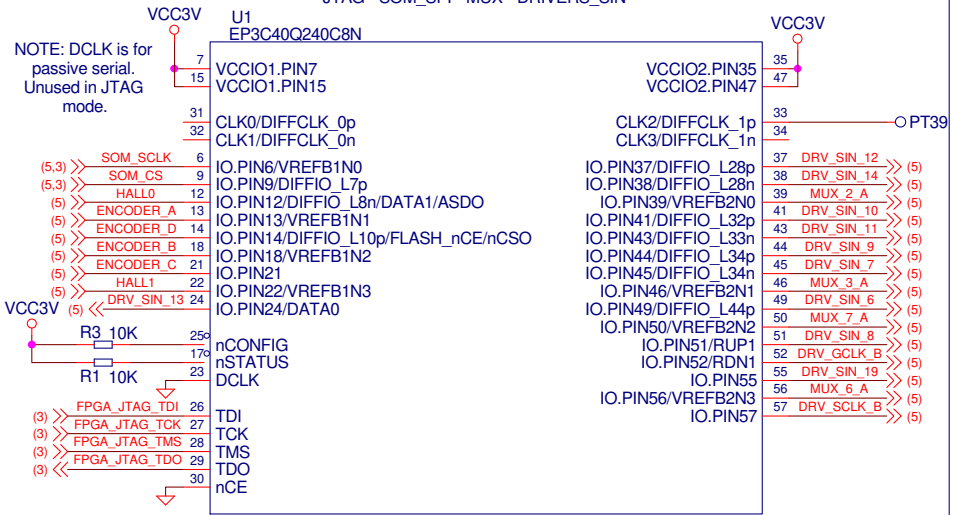
DECOUPLING CAPS FOR VCCIO BANKS 5/6



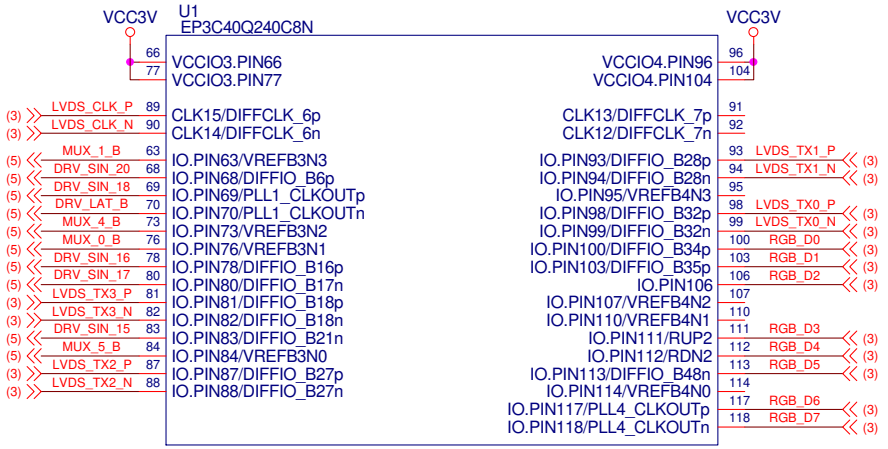
DECOUPLING CAPS FOR VCCIO BANKS 7/8



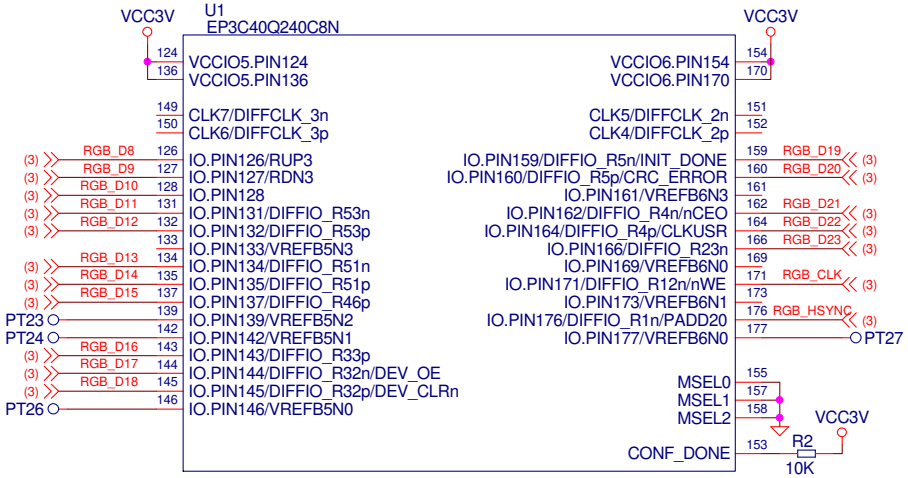
FPGA BANKS 1/2
JTAG - SOM_SPI - MUX - DRIVERS_SIN



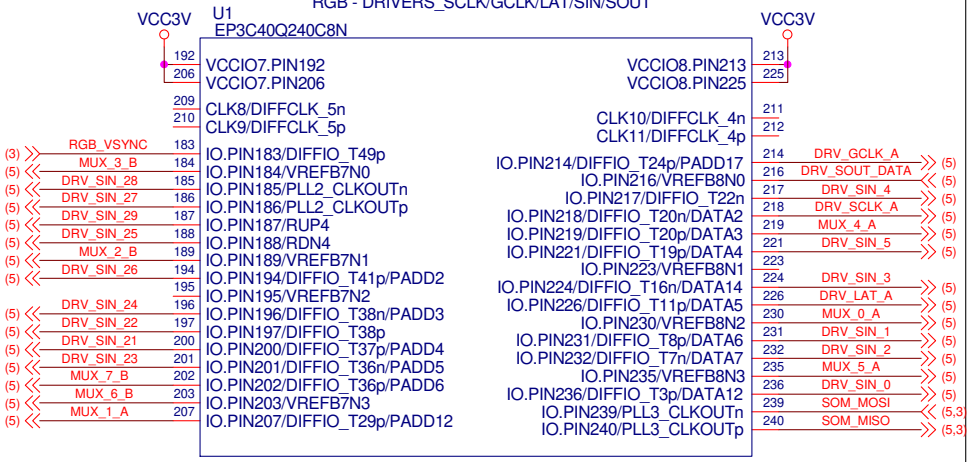
FPGA BANKS 3/4
LVDS - MUX - RGB



FPGA BANKS 5/6
RGB



FPGA BANKS 7/8
RGB - DRIVERS_SCLK/GCLK/LAT/SIN/SOUT



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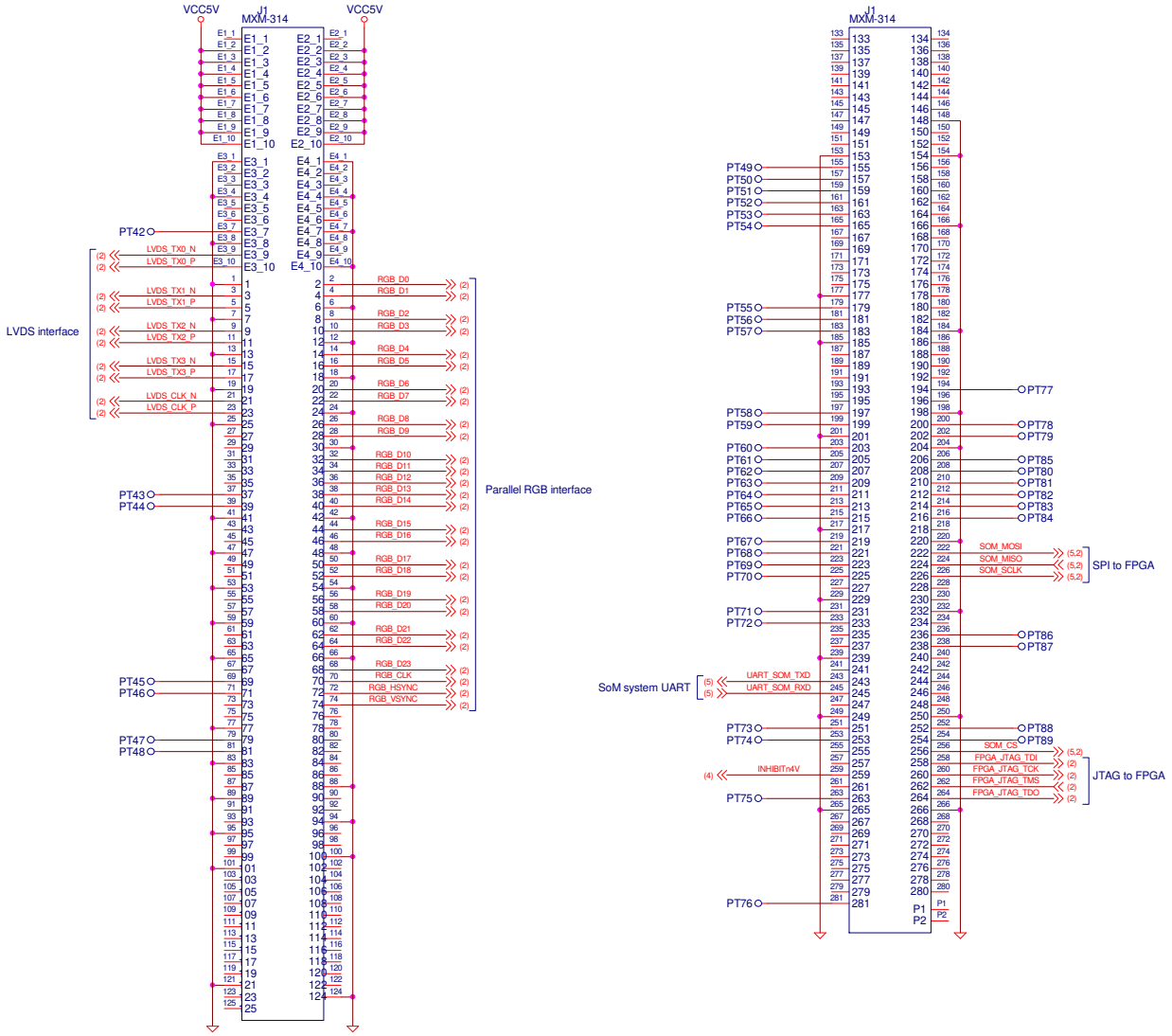

Rotative_base		
Size B	SBC	Rev 1.0
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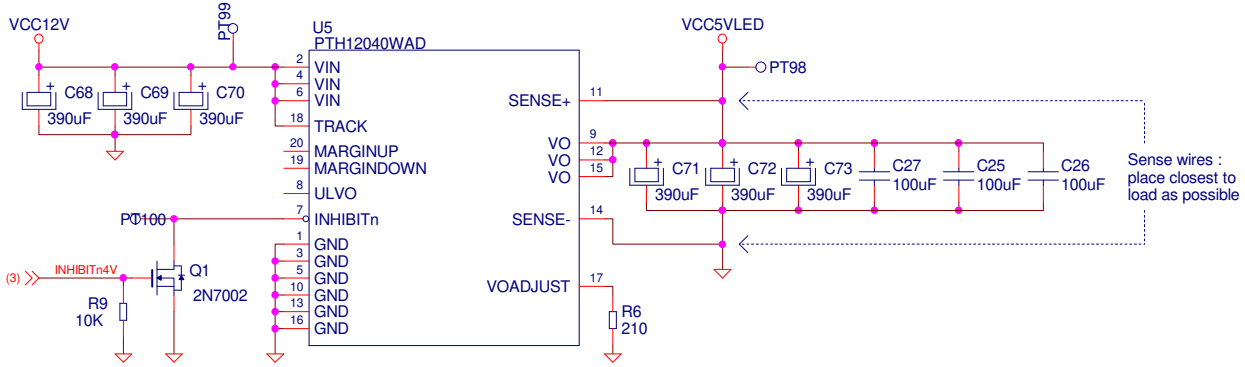
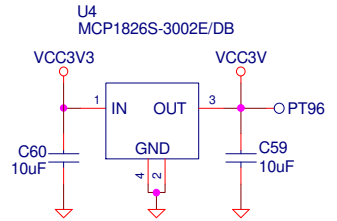
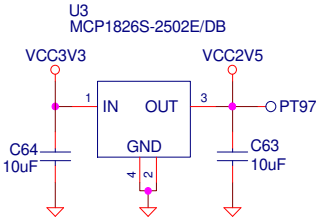


LED PSU: 5V
50A max, ~44A used

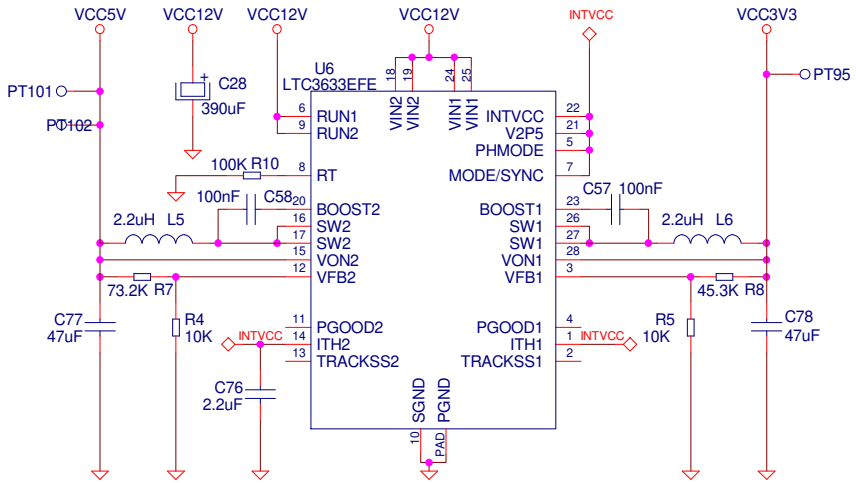


FPGA IO PSU: 3V
1A max, ~0.01A used



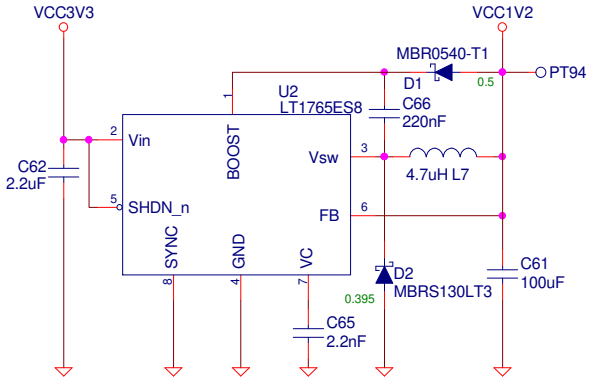
FPGA IO PSU: 2V5
1A max, ~0.05A used

Note: INTVCC signal is local to this page only.
It is used to pull high configuration pins of
the LTC3633 using its internal LDO.



SoM PSU: 5V
3A max, ~2A used

FPGA & glue logic PSU: 3V3
3A max, ~1.5A used



FPGA core PSU: 1V2
1A max, ~0.5A used

NOTE: The absence of a resistor network for the output voltage is not an oversight. The feedback voltage reference is 1.2V for the adjustable model, so no need for a resistor network as we want 1.2V.

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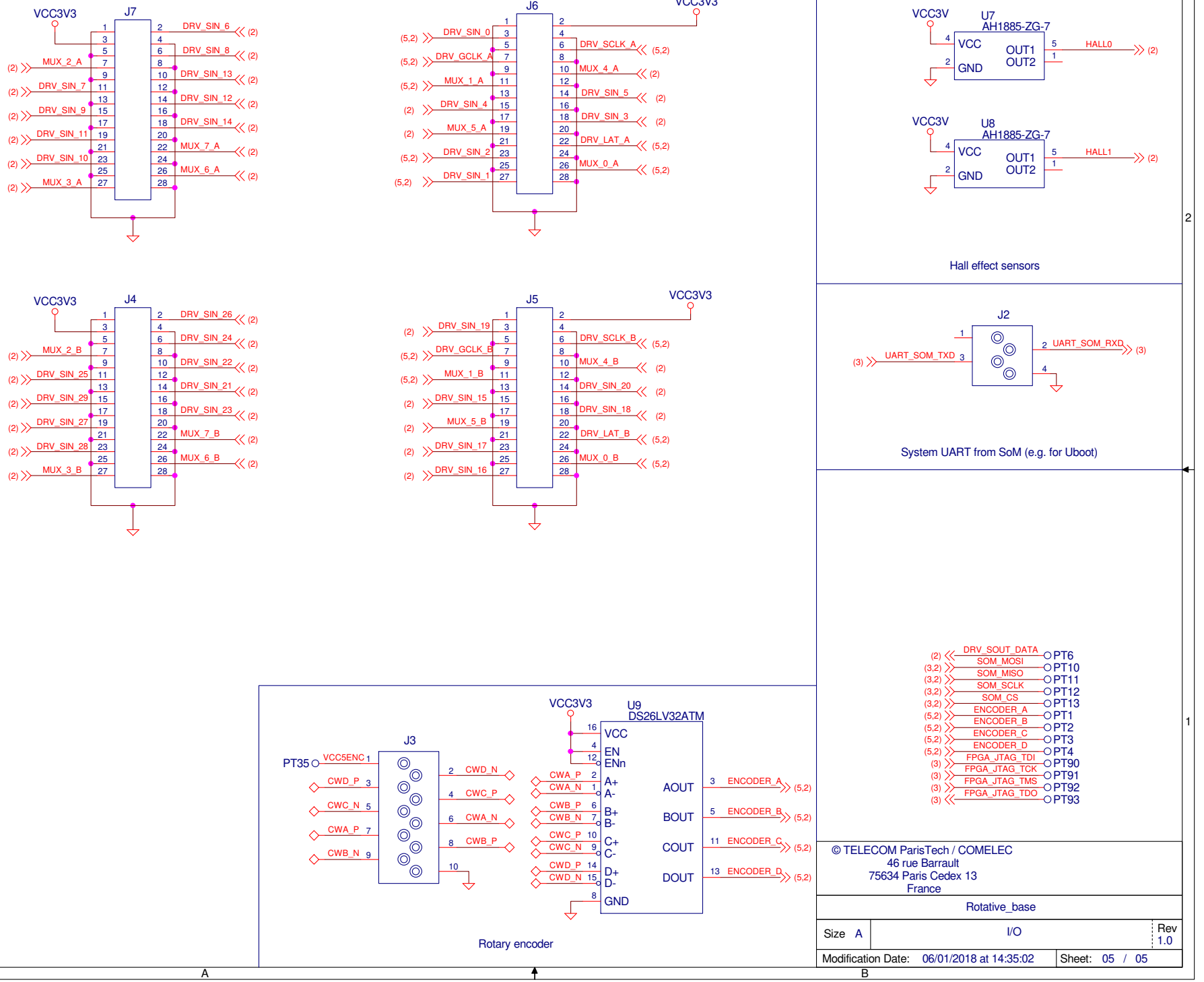

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