Exercise 1

For the following values of A and B, how many clock cycles are needed to execute your first program from Lab 7 on your baseline MIPS processor, before adding optimizations of Lab 9? Assuming that we run the MIPS processor at 20 MHz, how much time (in seconds) would that take? (You can assume that the loading of the numbers requires only one instruction)

Value of A	Value of B	Number of cycles	Time in seconds
0	8	48	$2.4 \cdot 10^{-6}$
6	8	18	$9 \cdot 10^{-7}$
0	250'000'000	1'250'000'008	62.5000004
249'999'996	250'000'002	38	$1.9 \cdot 10^{-6}$

Exercise 2

Fill in the new values for the Table in Exercise 1 when using the modified MIPS architecture running the optimized code, as discussed in the manual for Lab 9. (You can assume that the loading of the numbers requires only one inctruction)

Value of A	Value of B	Number of cycles	Time in seconds
0	8	11	5.5 × 10^-7
6	8	11	5.5 × 10^-7
0	250'000'000	11	5.5 × 10^-7
249'999'996	250'000'002	11	5.5 × 10^-7

Exercise 3

Compare the size/device utilization of the two implementations (before and after the modifications in Lab manual 9). What differences do you see? Briefly comment on them. *Hint: Look into the synthesis report.*

We can see that our original implementation from lab 8) requires a total of 285 LUT, while our new and improved version of lab 9) utilizes a whopping 608 LUT. From this we can see that adding support for new operations cost us a fair bit of size/devices, and a considerable amount at that, more than doubling the size of our

processor. We thus simplified the programming and sped up our calculation, but at the cost of device utilization. When implementing new features such as adding new instructions to our processor, one needs to weigh the benefits gained in user simplicity and performance against the size increase of our hardware to decide whether the tradeoff is worth it in a given situation.